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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details	
Product Status	Obsolete
Number of LABs/CLBs	28750
Number of Logic Elements/Cells	115000
Total RAM Bits	7987200
Number of I/O	942
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1704-BCBGA, FCBGA
Supplier Device Package	1704-CFCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga115ep1-5fcn1704c

Figure 2-3. Slice Diagram
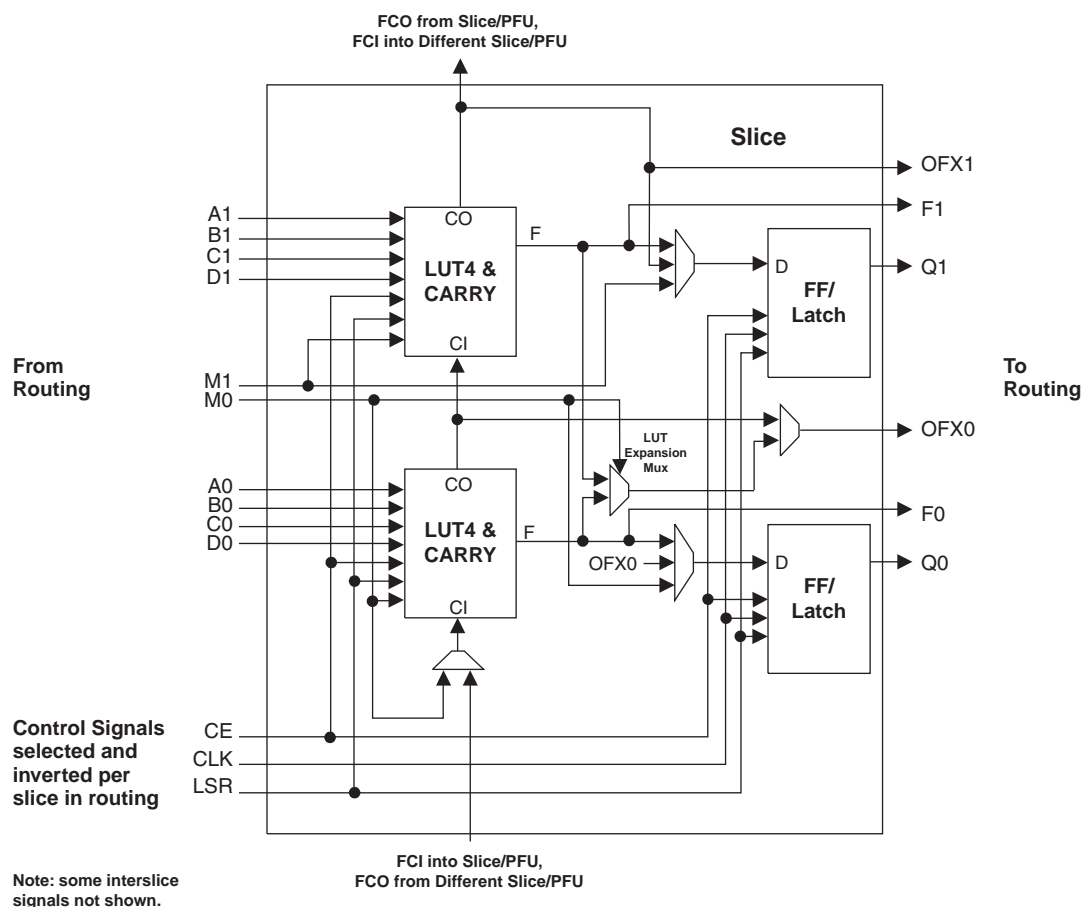
Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry In[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output[2]

1. See Figure 2-2 for connection details.
2. Requires two PFUs.

toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-9 illustrates the DCS Block diagram.

Figure 2-9. DCS Block Diagram
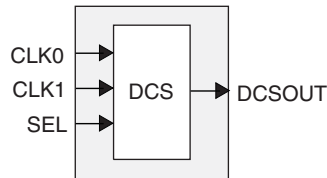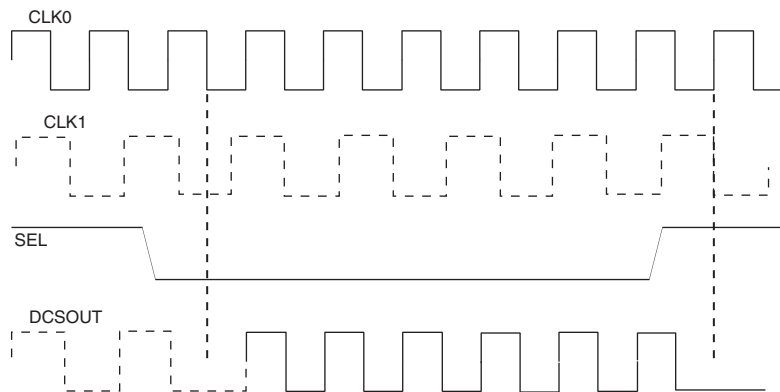
```
CLK0 →
CLK1 → DCS → DCSOUT
SEL →
```

Figure 2-10 shows timing waveforms for one of the DCS operating modes. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

Figure 2-10. DCS Waveforms

Clock Boosting

There are programmable delays available in the clock signal paths in the PFU, PIC and EBR blocks. These allow setup and clock-to-output times to be traded to meet critical timing without slowing the system clock. If this feature is enabled then the design tool automatically uses these delays to improve timing performance.
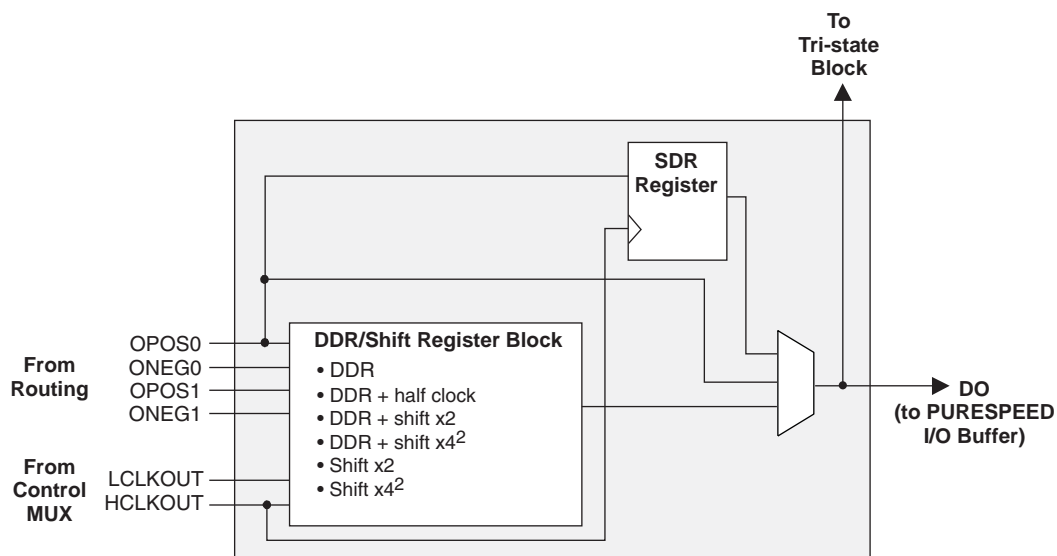
Global Set/Reset

There is a global set/reset (GSR) network on the device that is distributed to all FFs, PLLs, DLLs and other blocks on the device. This GSR network can operate in two modes:

a) asynchronous - no clock is required to get into or out of the reset state.

b) synchronous - The global GSR net is synchronized to a user selected clock. In this mode it continues to be asynchronous to get into the reset state, but is synchronous to get out of the reset state. This allows all registers on the device to become operational in the same clock period. The synchronous GSR goes out of reset in two cycles from the clock edge where the setup time of the FF was met (not from the GSR being released).

sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider and two clock output dividers. The input divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal.

Figure 2-22. Output Register Block[1]

To
Tri-state
Block

SDR
Register

OPOS0
ONEG0   **From**
Routing
OPOS1
ONEG1

DDR/Shift Register Block
• DDR
• DDR + half clock
• DDR + shift x2
• DDR + shift x4[2]
• Shift x2
• Shift x4[2]

From
Control
MUX
LCLKOUT
HCLKOUT

DO
(to PURESPEED
I/O Buffer)

Notes:
1. CE, Update, Set and Reset not shown for clarity.
2. By four shift modes utilizes DDR/Shift register block from paired PIO.
3. DDR/Shift register block shared with tristate block.

Figure 2-23. Output/Tristate DDR/Shift Register Block

Bypass Used for
DDR/DDRX Modes

From paired PIO
(x4 shift modes)

To paired PIO
(x4 shift modes)

OPOS0
(Can act as OPOS2
when paired)

Shift x2 / x4
Output

OPOS1
(Can act as OPOS3
when paired)

LCLKOUT
HCLKOUT
POS Update
NEG Update

TSDDR/DDRX

ODDR/DDR/
X2/X4

Bypass Used for
DDR/DDRX Modes

From paired PIO
(x4 shift modes)

To paired PIO
(x4 shift modes)

ONEG0
(Can act as ONEG2
when paired)

ONEG1
(Can act as ONEG3
when paired)

Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the PURESPEED I/O buffers. The block contains a register for SDR operation and a group of three registers for DDR and shift register operation. The output signal tri-state control signal (TO) can be derived directly from one of the inputs (bypass mode), the SDR shift register, the DDR registers or the data associated with the buffer (for open drain emulation). Figure 2-24 shows the diagram of the Tristate Register Block.

Tristate SDR Register/Latch Block

The SDR register operates on the positive edge of the high-speed clock. In it has a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR and Global Set Reset GSR enable or disable. The register LSR input is driven from LSRO, which is generated from the PIO control MUX. The GSR input is driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

Tristate DDR/Shift Register Block

The DDR/Shift block is shared with the output block allowing DDR support using the high-speed clock and the associated transfer from the low-speed clock domain. It functions as a gearbox allowing low–speed parallel data from the FPGA fabric to provide a high-speed tri-state control stream.

There is a special mode for DDR-II memory interfaces where the termination is controlled by the output tristate signal. During WRITE cycle when the FPGA is driving the lines, the parallel terminations are turned off. During READ cycle when the FPGA is receiving data, the parallel terminations are turned on.

Figure 2-24. Tristate Register Block[1]

Notes:
1. CE, Update, Set and Reset not shown for clarity.
2. DDR/Shift Register Block shared with output register block.
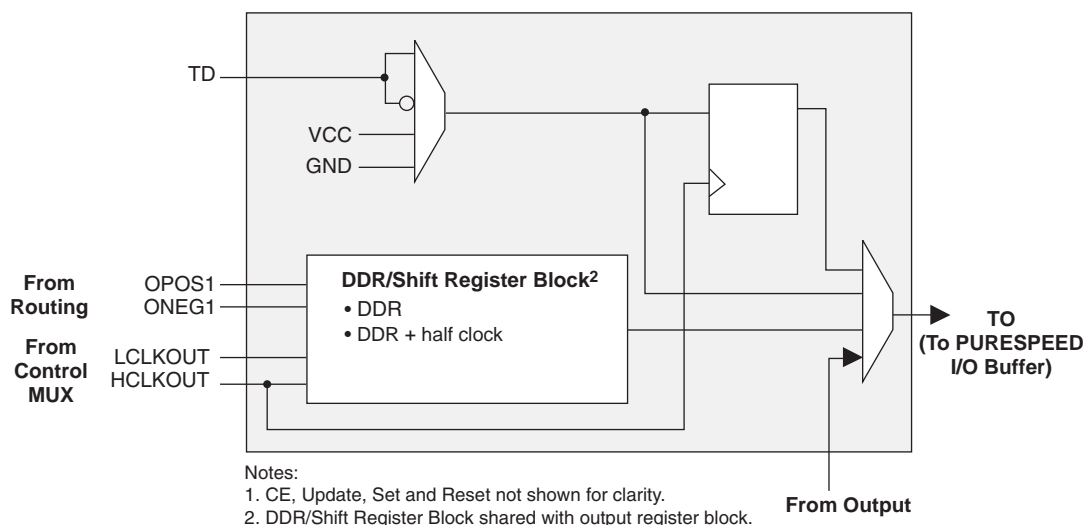
I/O Architecture Rules

Table 2-6 shows the PIO usage for x1, x2, x4 gearing. The checkmarks in the columns show the specific PIOs that are used for each gearing mode. When using x2 or x4 gearing, any PIO which is not used for gearing can still be used as an output.

Power Supply Ramp Rates

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
t_{RAMP}	Power supply ramp rates for all power supplies	Over process, voltage, temperature	3.45	—	—	mV/µs
			—	—	75	ms

1. See the Power-up and Power-Down requirements section for more details on power sequencing.
2. From 0.5V to minimum operating voltage.

Hot Socketing Specifications[1]

Symbol	Parameter	Condition	Min.	Typ.	Max	Units
I_{DK}	Programmable and dedicated Input or I/O leakage current[2, 3, 4, 5, 6]	$0 <= V_{IN} <= V_{IH}$ (MAX)	—	—	±1500	µA
I_{HDIN}	SERDES average input current when device powered down and inputs driven[7]		—	—	4	mA

1. See Hot Socket power up/down information in Chapter 2 of this document.
2. Assumes monotonic rise/fall rates for all power supplies.
3. Sensitive to power supply sequencing as described in hot socketing section.
4. Assumes power supplies are between 0 and maximum recommended operations conditions.
5. IDK is additive to I_{PU}, I_{PD} or I_{BH}.
6. Represents DC conditions. For the first 20ns after hot insertion, current specification is 8 mA.
7. Assumes that the device is powered down with all supplies grounded, both P and N inputs driven by a CML driver with maximum allowed VDDOB of 1.575V, 8b/10b data and internal AC coupling.

DC Electrical Characteristics[5]

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.[3]	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Low leakage	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	10	µA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	-30	—	-210	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	210	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7V_{CCIO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	210	µA
I_{BHLH}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	-210	µA
I_{CL}	PCI Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$	—	—	mA
I_{CH}	PCI High Clamp Current	$V_{CC} + 4 > V_{IN} \ge V_{CC} + 1$	$25 + (V_{IN} - V_{CC} -1)/0.015$	—	—	mA
V_{BHT}	Bus Hold trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{CCIP2} = 1.2V, V_{CCAUX} = 2.5, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C3[2]	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{CCIP2} = 1.2V, V_{CCAUX} = 2.5, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz
3. $I_{PU,}$ I_{PD}, I_{BHLS} and I_{BHHS} have minimum values of 15 or -15µA if V_{CCIO} is set to 1.2V nominal.
4. This table does not apply to SERDES pins.
5. For programmable I/Os.

LVPECL

The LatticeSC devices support differential LVPECL standard. This standard is emulated using controlled imped-
ance complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The
scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL
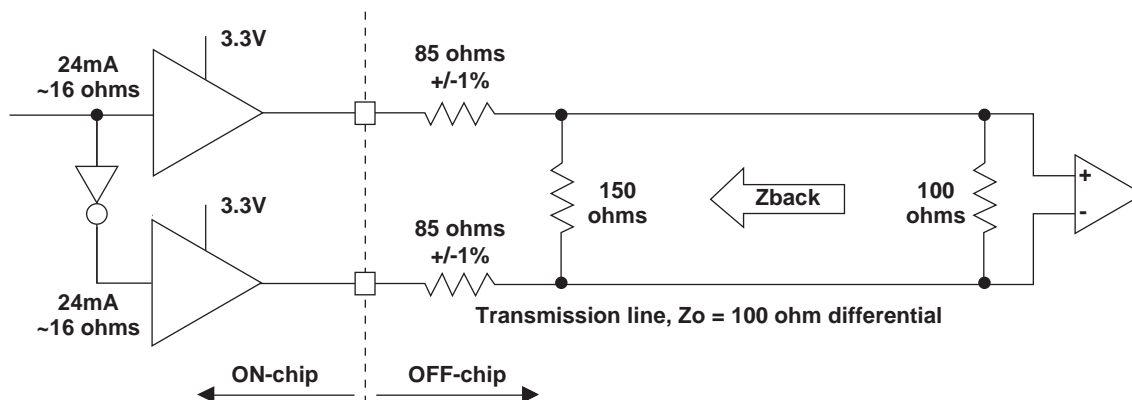
Table 3-3. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	16	ohm
R_S	Driver series resistor	85	ohm
R_P	Driver parallel resistor	150	ohm
R_T	Receiver termination	100	ohm
V_{OH}	Output high voltage	2.03	V
V_{OL}	Output low voltage	1.27	V
V_{OD}	Output differential voltage	0.76	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	86	ohm
I_{DC}	DC output current	12.6	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS, MLVDS and other differential interfaces please see details of additional
technical documentation at the end of this data sheet.

On-die Differential Common Mode Termination

Symbol	Description	Min.	Typ.	Max.	Units
C_{CMT}	Capacitance V_{CMT} to GND	—	40	—	pF

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		2	—	1000	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)		1.5625	—	1000	MHz
f_{VCO}	PLL VCO Frequency		100	—	1000	MHz
f_{PFD}	Phase Detector Input Frequency		2	—	700	MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected (at 50% levels)	45	—	55	%
t_{OPJIT}[1]	Output Clock Period Jitter	$2\ MHz \leq f_{PFD} \leq 10\ MHz$	—	—	200	ps
		$f_{PFD} > 10\ MHz$	—	—	100	ps
t_{CPJIT}[1]	Output Clock Cycle-to-Cycle Jitter		—	—	100	ps
t_{SKEW}	Output Clock-to-Clock Skew (Between Two Outputs with the Same Phase Setting)		—	—	20	ps
t_{LOCK}	PLL Lock-in Time		—	—	1	ms
t_{IPJIT}	Input Clock Period Jitter		—	—	±250	ps
t_{HI}	Input Clock High Time	At 80% level	350	—	—	ps
t_{LO}	Input Clock Low Time	At 20% level	350	—	—	ps
t_{RSWA}	Analog Reset Signal Pulse Width		100	—	—	ns
t_{RSWD}	Digital Reset Signal Pulse Width		3	—	—	ns
t_{DEL}	Timeshift Delay Step Size		40	80	120	ps
t_{RANGE}	Timeshift Delay Range		—	+/- 560	—	ps
f_{SS}	Spread Spectrum Modulation Frequency		30	—	500	KHz
% Spread	Percentage Downspread for SS Mode		0.5	—	1.5	%
	VCO Clock Phase Adjustment Accuracy		-5	—	5	°

1. Values are measured with FPGA logic active, no additional I/Os toggling and REFCLK total jitter = 30 ps

Signal Descriptions (Cont.)

Signal Name	I/O	Description
PROBE_GND	—	GND signal - Connected to internal VSS node. Can be used for feedback to control an external board power converter. Can be unconnected if not used.
PLL and Clock Functions (Used as user-programmable I/O pins when not in use for PLL, DLL or clock pins.)		
[LOC]_PLL[T, C]_FB_[A/B]	I	PLL feedback input. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the PLL is located in: ULC (upper left), URC (upper right), LLC (lower left) and LRC (lower right). [T, C] indicates whether input is true or complement. [A, B] indicates PLL reference within the corner.
[LOC]_DLL[T, C]_FB_[C, D, E, F]	I	DLL feedback input. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the DLL is located in: ULC (upper left), URC (upper right), LLC (lower left) and LRC (lower right). [T/C] indicates whether input is true or complement. [C, D, E, F] indicates DLL reference within a corner. Note: E and F are only available on the lower corners.
[LOC]_PLL[T, C]_IN[A/B]	I	PLL reference clock input. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the PLL is located in: ULC (upper left corner), URC (upper right corner), LLC (lower left corner) and LRC (lower right corner). [T, C] indicates whether input is true or complement.[A, B] indicates PLL reference within the corner.
[LOC]_DLL[T, C]_IN[C, D, E, F]	I	DLL reference clock inputs. Pull-ups are enabled on input pins during configuration. [LOC] indicates the corner the DLL is located in: ULC (upper left corner), URC (upper right corner), LLC (lower left corner) and LRC (lower right corner). [T/C] indicates whether input is true or complement. [C, D, E, F] indicates DLL reference within a corner. Note: E and F are only available on the lower corners. PCKLxy_[0:3] can drive primary clocks, edge clocks, and CLKDIVs. PCLKxy_[4:7] can only drive edge clocks.
PCLKxy_z		General clock inputs. x indicates whether T (true) or C (complement). y indicates the I/O bank the clock is associated with. z indicates the clock number within a bank.
Test and Programming (Dedicated pins. Pull-up is enabled on input pins during configuration.)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data in pin, used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence).
TDO	O	Output pin -Test Data out pin used to shift data out of device using 1149.1.
Configuration Pads (Dedicated pins. Used during sysCONFIG.)		
M[3:0]	I	Mode pins used to specify configuration modes values latched on rising edge of INITN.
INITN	I/O	Open Drain pin - Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled that will pull the I/O above 1.5V.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up.
DONE	I/O	Open Drain pin - Indicates that the configuration sequence is complete, and the startup sequence is in progress.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
N3	PL27A	6		PL30A	6	
P3	PL27B	6		PL30B	6	
P4	PL27C	6	PCLKT6_3	PL30C	6	PCLKT6_3
P2	PL28A	6		PL31A	6	
R2	PL28B	6		PL31B	6	
T3	PL28C	6	PCLKT6_2	PL31C	6	PCLKT6_2
R3	PL28D	6	PCLKC6_2	PL31D	6	PCLKC6_2
P1	PL31A	6		PL34A	6	
R1	PL31B	6		PL34B	6	
R5	PL31C	6	VREF1_6	PL34C	6	VREF1_6
R4	PL31D	6		PL34D	6	
T2	PL32A	6		PL35A	6	
U2	PL32B	6		PL35B	6	
T1	PL33A	6		PL38A	6	
U1	PL33B	6		PL38B	6	
V1	PL35A	6		PL42A	6	
W1	PL35B	6		PL42B	6	
V6	PL35D	6	DIFFR_6	PL42D	6	DIFFR_6
V2	PL36A	6		PL43A	6	
W2	PL36B	6		PL43B	6	
Y1	PL37A	6		PL44A	6	
AA1	PL37B	6		PL44B	6	
AB1	PL39A	6		PL48A	6	
AC1	PL39B	6		PL48B	6	
Y5	PL40A	6		PL49A	6	
Y6	PL40B	6		PL49B	6	
AD2	PL41A	6		PL51A	6	
AE2	PL41B	6		PL51B	6	
AB5	PL41D	6	VREF2_6	PL51D	6	VREF2_6
AC3	PL43A	6		PL52A	6	
AD3	PL43B	6		PL52B	6	
AF1	PL44A	6		PL55A	6	
AG1	PL44B	6		PL55B	6	
AB6	PL44C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL55C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AC5	PL44D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL55D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AF2	PL45A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL57A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AG2	PL45B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL57B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AC6	PL45C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL57C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AC7	PL45D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL57D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AE4	XRES	-		XRES	-	
AG4	VCC12	-		VCC12	-	
AD5	TEMP	6		TEMP	6	
AF5	VCC12	-		VCC12	-	
AH1	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AJ1	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB10	VCC	-		VCC	-	
AB21	VCC	-		VCC	-	
J10	VCC	-		VCC	-	
J21	VCC	-		VCC	-	
K10	VCC	-		VCC	-	
K11	VCC	-		VCC	-	
K12	VCC	-		VCC	-	
K13	VCC	-		VCC	-	
K14	VCC	-		VCC	-	
K17	VCC	-		VCC	-	
K18	VCC	-		VCC	-	
K19	VCC	-		VCC	-	
K20	VCC	-		VCC	-	
K21	VCC	-		VCC	-	
K22	VCC	-		VCC	-	
K9	VCC	-		VCC	-	
L10	VCC	-		VCC	-	
L21	VCC	-		VCC	-	
M10	VCC	-		VCC	-	
M21	VCC	-		VCC	-	
N10	VCC	-		VCC	-	
N21	VCC	-		VCC	-	
P10	VCC	-		VCC	-	
P21	VCC	-		VCC	-	
U10	VCC	-		VCC	-	
U21	VCC	-		VCC	-	
V10	VCC	-		VCC	-	
V21	VCC	-		VCC	-	
W10	VCC	-		VCC	-	
W21	VCC	-		VCC	-	
Y10	VCC	-		VCC	-	
Y21	VCC	-		VCC	-	
H11	VCCAUX	-		VCCAUX	-	
H12	VCCAUX	-		VCCAUX	-	
H19	VCCAUX	-		VCCAUX	-	
H20	VCCAUX	-		VCCAUX	-	
M23	VCCAUX	-		VCCAUX	-	
M24	VCCAUX	-		VCCAUX	-	
N23	VCCAUX	-		VCCAUX	-	
N24	VCCAUX	-		VCCAUX	-	
U23	VCCAUX	-		VCCAUX	-	
U24	VCCAUX	-		VCCAUX	-	
V23	VCCAUX	-		VCCAUX	-	
V24	VCCAUX	-		VCCAUX	-	
W23	VCCAUX	-		VCCAUX	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
N17	GND	-		GND	-	
N18	GND	-		GND	-	
N19	GND	-		GND	-	
N20	GND	-		GND	-	
P11	GND	-		GND	-	
P12	GND	-		GND	-	
P13	GND	-		GND	-	
P14	GND	-		GND	-	
P15	GND	-		GND	-	
P16	GND	-		GND	-	
P17	GND	-		GND	-	
P18	GND	-		GND	-	
P19	GND	-		GND	-	
P20	GND	-		GND	-	
R10	GND	-		GND	-	
R11	GND	-		GND	-	
R12	GND	-		GND	-	
R13	GND	-		GND	-	
R14	GND	-		GND	-	
R15	GND	-		GND	-	
R16	GND	-		GND	-	
R17	GND	-		GND	-	
R18	GND	-		GND	-	
R19	GND	-		GND	-	
R20	GND	-		GND	-	
R21	GND	-		GND	-	
T10	GND	-		GND	-	
T11	GND	-		GND	-	
T12	GND	-		GND	-	
T13	GND	-		GND	-	
T14	GND	-		GND	-	
T15	GND	-		GND	-	
T16	GND	-		GND	-	
T17	GND	-		GND	-	
T18	GND	-		GND	-	
T19	GND	-		GND	-	
T20	GND	-		GND	-	
T21	GND	-		GND	-	
U11	GND	-		GND	-	
U12	GND	-		GND	-	
U13	GND	-		GND	-	
U14	GND	-		GND	-	
U15	GND	-		GND	-	
U16	GND	-		GND	-	
U17	GND	-		GND	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	**VCCIO Bank**	**Dual Function**	**Ball Function**	**VCCIO Bank**	**Dual Function**
B1	GND	-		GND	-	
B32	GND	-		GND	-	
C11	GND	-		GND	-	
C12	GND	-		GND	-	
C16	GND	-		GND	-	
C21	GND	-		GND	-	
C22	GND	-		GND	-	
C24	GND	-		GND	-	
C25	GND	-		GND	-	
C26	GND	-		GND	-	
C27	GND	-		GND	-	
C29	GND	-		GND	-	
C3	GND	-		GND	-	
C30	GND	-		GND	-	
C4	GND	-		GND	-	
C6	GND	-		GND	-	
C7	GND	-		GND	-	
C8	GND	-		GND	-	
C9	GND	-		GND	-	
D17	GND	-		GND	-	
F18	GND	-		GND	-	
F3	GND	-		GND	-	
F30	GND	-		GND	-	
F9	GND	-		GND	-	
G15	GND	-		GND	-	
G24	GND	-		GND	-	
G29	GND	-		GND	-	
G3	GND	-		GND	-	
J14	GND	-		GND	-	
J22	GND	-		GND	-	
J26	GND	-		GND	-	
J6	GND	-		GND	-	
K11	GND	-		GND	-	
K19	GND	-		GND	-	
K30	GND	-		GND	-	
K4	GND	-		GND	-	
L23	GND	-		GND	-	
L9	GND	-		GND	-	
M13	GND	-		GND	-	
M15	GND	-		GND	-	
M18	GND	-		GND	-	
M20	GND	-		GND	-	
M27	GND	-		GND	-	
M7	GND	-		GND	-	
N12	GND	-		GND	-	
N14	GND	-		GND	-	
N19	GND	-		GND	-	
N21	GND	-		GND	-	
N29	GND	-		GND	-	
N3	GND	-		GND	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
U12	VCC12	-		VCC12	-	
U21	VCC12	-		VCC12	-	
AA16	VCC12	-		VCC12	-	
AA17	VCC12	-		VCC12	-	
M14	VCC12	-		VCC12	-	
P12	VCC12	-		VCC12	-	
W12	VCC12	-		VCC12	-	
AA14	VCC12	-		VCC12	-	
AA19	VCC12	-		VCC12	-	
W21	VCC12	-		VCC12	-	
P21	VCC12	-		VCC12	-	
M19	VCC12	-		VCC12	-	
A2	GND	-		GND	-	
A10	GND	-		GND	-	
E28	NC	-		NC	-	
E5	NC	-		NC	-	
F10	NC	-		NC	-	
E10	NC	-		NC	-	
E23	NC	-		NC	-	
F23	NC	-		NC	-	

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M25 and LatticeSC/M40 in a 1020-pin package support a 16-bit MPI interface.

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	**VCCIO Bank**	**Dual Function**
N27	PL47C	7	
P27	PL47D	7	
K33	PL49A	7	
L33	PL49B	7	
M30	PL49C	7	
N30	PL49D	7	
M31	PL51A	7	
N31	PL51B	7	
P24	PL51C	7	
R24	PL51D	7	
M33	PL56A	7	
N33	PL56B	7	
U25	PL56C	7	
T25	PL56D	7	
L34	PL57A	7	
M34	PL57B	7	
P29	PL57C	7	
R29	PL57D	7	
N34	PL60A	7	
P34	PL60B	7	
R27	PL60C	7	
T27	PL60D	7	
R32	PL61A	7	PCLKT7_1
R31	PL61B	7	PCLKC7_1
U24	PL61C	7	PCLKT7_3
T24	PL61D	7	PCLKC7_3
P33	PL62A	7	PCLKT7_0
R33	PL62B	7	PCLKC7_0
T26	PL62C	7	PCLKT7_2
U26	PL62D	7	PCLKC7_2
T32	PL64A	6	PCLKT6_0
T31	PL64B	6	PCLKC6_0
U29	PL64C	6	PCLKT6_1
V29	PL64D	6	PCLKC6_1
T30	PL65A	6	
U30	PL65B	6	
U27	PL65C	6	PCLKT6_3
V27	PL65D	6	PCLKC6_3
R34	PL66A	6	
T34	PL66B	6	
U28	PL66C	6	PCLKT6_2
V28	PL66D	6	PCLKC6_2
V30	PL69A	6	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AL5	GND	-	
AM14	GND	-	
AM18	GND	-	
AM24	GND	-	
AM30	GND	-	
AM8	GND	-	
AN1	GND	-	
AN34	GND	-	
AP2	GND	-	
AP33	GND	-	
B1	GND	-	
B34	GND	-	
C11	GND	-	
C12	GND	-	
C13	GND	-	
C14	GND	-	
C17	GND	-	
C21	GND	-	
C22	GND	-	
C23	GND	-	
C24	GND	-	
C26	GND	-	
C27	GND	-	
C30	GND	-	
C31	GND	-	
C4	GND	-	
C5	GND	-	
C8	GND	-	
C9	GND	-	
D18	GND	-	
E32	GND	-	
E4	GND	-	
F19	GND	-	
G16	GND	-	
G29	GND	-	
G7	GND	-	
H3	GND	-	
H31	GND	-	
J10	GND	-	
J15	GND	-	
J26	GND	-	
K20	GND	-	
K23	GND	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
Y18	VCC	-	
Y20	VCC	-	
AB15	VCC12	-	
AB20	VCC12	-	
N15	VCC12	-	
N20	VCC12	-	
R13	VCC12	-	
R22	VCC12	-	
Y13	VCC12	-	
Y22	VCC12	-	
AA12	VCCAUX	-	
AA23	VCCAUX	-	
AB12	VCCAUX	-	
AB16	VCCAUX	-	
AB17	VCCAUX	-	
AB18	VCCAUX	-	
AB19	VCCAUX	-	
AB23	VCCAUX	-	
AC12	VCCAUX	-	
AC13	VCCAUX	-	
Y19	GND	-	
AC14	VCCAUX	-	
AC17	VCCAUX	-	
AC21	VCCAUX	-	
AC22	VCCAUX	-	
AC23	VCCAUX	-	
M13	VCCAUX	-	
M14	VCCAUX	-	
M18	VCCAUX	-	
M21	VCCAUX	-	
M22	VCCAUX	-	
N12	VCCAUX	-	
N16	VCCAUX	-	
N17	VCCAUX	-	
N18	VCCAUX	-	
N19	VCCAUX	-	
N23	VCCAUX	-	
P12	VCCAUX	-	
P23	VCCAUX	-	
T13	VCCAUX	-	
T22	VCCAUX	-	
U12	VCCAUX	-	
U13	VCCAUX	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
R12	VTT_2	2	
T12	VTT_2	2	
AB11	VTT_3	3	
W12	VTT_3	3	
Y12	VTT_3	3	
AC15	VTT_4	4	
AC16	VTT_4	4	
AD13	VTT_4	4	
AC19	VTT_5	5	
AC20	VTT_5	5	
AD22	VTT_5	5	
AB24	VTT_6	6	
W23	VTT_6	6	
Y23	VTT_6	6	
N24	VTT_7	7	
R23	VTT_7	7	
T23	VTT_7	7	
M12	VDDAX25_R	-	
M23	VDDAX25_L	-	
Y16	GND	-	
Y14	GND	-	
N21	VCC12	-	
P22	VCC12	-	
AA22	VCC12	-	
AB21	VCC12	-	
AB14	VCC12	-	
AA13	VCC12	-	
P13	VCC12	-	
N14	VCC12	-	
G26	NC	-	
G9	NC	-	
J12	NC	-	
H12	NC	-	
H23	NC	-	
J23	NC	-	

1. Differential pair grouping within a PCI is A (True) and B (complement) and C (True) and D (Complement).
2. The LatticeSC/M115 in an 1152-pin package supports a 32-bit MPI interface.

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2]

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G34	A_REFCLKP_L	-		A_REFCLKP_L	-	
H34	A_REFCLKN_L	-		A_REFCLKN_L	-	
N30	VCC12	-		VCC12	-	
H33	RESP_ULC	-		RESP_ULC	-	
P25	RESETN	1		RESETN	1	
P26	TSALLN	1		TSALLN	1	
P31	DONE	1		DONE	1	
P23	INITN	1		INITN	1	
P30	M0	1		M0	1	
P22	M1	1		M1	1	
P24	M2	1		M2	1	
R22	M3	1		M3	1	
J37	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
J38	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
P32	PL16C	7		PL15C	7	
R32	PL16D	7		PL15D	7	
G40	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
H40	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N33	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P33	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
G41	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
H41	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
T29	PL18C	7		PL18C	7	
U29	PL18D	7	VREF2_7	PL18D	7	VREF2_7
G42	PL20A	7		PL19A	7	
H42	PL20B	7		PL19B	7	
M34	PL20C	7		PL19C	7	
M35	PL20D	7		PL19D	7	
K37	PL21A	7		PL26A	7	
L37	PL21B	7		PL26B	7	
N34	PL21C	7		PL26C	7	
P34	PL21D	7		PL26D	7	
K38	PL22A	7		PL30A	7	
L38	PL22B	7		PL30B	7	
T33	PL22C	7		PL30C	7	
R33	PL22D	7		PL30D	7	
J41	PL24A	7		PL34A	7	
K41	PL24B	7		PL34B	7	
U31	PL24C	7		PL34C	7	
V31	PL24D	7		PL34D	7	
K42	PL25A	7		PL38A	7	
J42	PL25B	7		PL38B	7	
J36	PL25C	7		PL38C	7	
K36	PL25D	7		PL38D	7	
N38	PL26A	7		PL40A	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
T16	GND	-		GND	-	
T19	GND	-		GND	-	
T24	GND	-		GND	-	
T27	GND	-		GND	-	
T32	GND	-		GND	-	
U18	GND	-		GND	-	
U20	GND	-		GND	-	
U23	GND	-		GND	-	
U25	GND	-		GND	-	
U36	GND	-		GND	-	
U7	GND	-		GND	-	
G36	GND	-		GND	-	
G7	GND	-		GND	-	
V17	GND	-		GND	-	
V19	GND	-		GND	-	
V24	GND	-		GND	-	
V26	GND	-		GND	-	
V4	GND	-		GND	-	
V40	GND	-		GND	-	
W12	GND	-		GND	-	
W16	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W23	GND	-		GND	-	
W25	GND	-		GND	-	
W27	GND	-		GND	-	
W31	GND	-		GND	-	
Y17	GND	-		GND	-	
Y19	GND	-		GND	-	
Y21	GND	-		GND	-	
Y22	GND	-		GND	-	
AA17	VCC	-		VCC	-	
AA18	VCC	-		VCC	-	
AA19	VCC	-		VCC	-	
AA21	VCC	-		VCC	-	
AA22	VCC	-		VCC	-	
AA24	VCC	-		VCC	-	
AA25	VCC	-		VCC	-	
AA26	VCC	-		VCC	-	
AB17	VCC	-		VCC	-	
AB18	VCC	-		VCC	-	
AB19	VCC	-		VCC	-	
AB21	VCC	-		VCC	-	
AB22	VCC	-		VCC	-	
AB24	VCC	-		VCC	-	

Date	Version	Section	Change Summary
August 2006 (cont.)	01.3 (cont.)	DC and Switching Characteristics (cont.)	Updated LatticeSC Family Timing Adders with ispLEVER 6.0 SP1 results
			Updated PLL Timing Parameters based on PDE testing results
			Removed RDDATA parameter from sysCONFIG readback timing table
		Multiple	Changed TDO/RDDATA to TDO
		Pinout Information	Removed all MPI signals from SC15 256 pin package Dual Function Column
			Added note to SC15, SC25 900 pin package that the package supports a 16 bit MPI
			Added note that pin D3 in an SC15 and SC25 900 pin package should not be used for single-ended outputs
			Added note that pin D28 in an SC15 and SC25 900 pin package should not be used for single-ended outputs
			Added note to SC25 1020 pin package that the package supports a 16 bit MPI
			Added note to SC80 1152 pin package that the package supports a 32 bit MPI
			Added note to SC80 1704 pin package that the package supports a 32 bit MPI
		Ordering Information	Changed "fcBGA" for the 1020 packages to "ffBGA"
November 2006	01.4	Introduction	LatticeSC Family Selection Guide table – I/O count for SC80 device, 1704 fcBGA package changed to 904/32. I/O count for SC115 device, 1704 fcBGA package changed to 942/32.
		DC and Switching Characteristics	DC Electrical Characteristics table – Updated the initialization and standby supply current values.
			DC Electrical Characteristics table – Updated the sysCONFIG Master Parallel mode RCLK low and RCLK high time specifications.
			DC Electrical Characteristics table – Updated VCCIO values for LVPECL33 I/Os.
		Pin Information	Pin Information Summary table - Changed number of single ended user I/Os from 906 to 904 for 1704 fcBGA.
			Removed the single-ended only output restriction on pins D3 and D28 in an SC15 and SC25 900 pin package.
		Ordering Information	Ordering Information tables - Changed number of I/Os from 906 to 904 for 1704 fcBGA.
			Added ordering part numbers for LatticeSC/SCM 40K and 115K LUT devices.
			Added lead-free ordering part numbers.
		Multiple	Changed number of available SC80 I/O from 906 to 904.
			Changed number of available SC115 I/O from 944 to 942.
January 2007	01.4a	Architecture	Added EBR Asynchronous Reset section.
February 2007	01.4b	Architecture	Updated EBR Asynchronous Reset section.
March 2007	01.5	Architecture	Added EBR asynchronous reset clarification
			Clarified that differential drivers are not supported in banks 1, 4 and 5
		DC and Switching Characteristics	Added clarification for the description of the junction temperature specification in the Absolute Maximum Ratings section.
			Updated Initialization and Standby Current table.
			Updated LatticeSC External Switching Characteristics with ispLEVER 6.1 SP1 results.