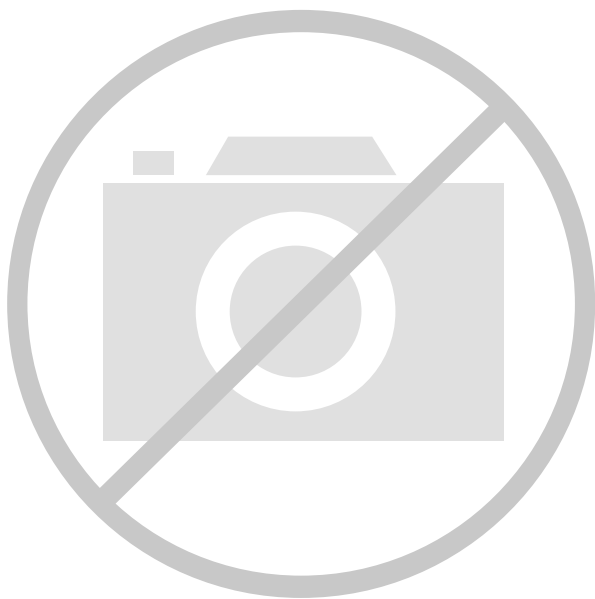




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	28750
Number of Logic Elements/Cells	115000
Total RAM Bits	7987200
Number of I/O	942
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1704-BCBGA, FCBGA
Supplier Device Package	1704-CFCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga115ep1-6fc1704i

Architecture Overview

The LatticeSC architecture contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR). The upper left and upper right corners of the devices contain SERDES blocks and their associated PCS blocks, as shown in Figure 2-1.

Top left and top right corner of the device contain blocks of SERDES. Each block of SERDES contains four channels (quad). Each channel contains a single serializer and de-serializer, synchronization and word alignment logic. The SERDES quad connects with the Physical Coding Sub-layer (PCS) blocks that contain logic to simultaneously perform alignment, coding, de-coding and other functions. The SERDES quad block has separate supply, ground and reference voltage pins.

The PICs contain logic to facilitate the conditioning of signals to and from the I/O before they leave or enter the FPGA fabric. The block provides DDR and shift register capabilities that act as a gearbox between high speed I/O and the FPGA fabric. The blocks also contain programmable Adaptive Input Logic that adjusts the delay applied to signals as they enter the device to optimize setup and hold times and ensure robust performance.

sysMEM EBRs are large dedicated fast memory blocks. They can be configured as RAM, ROM or FIFO. These blocks have dedicated logic to simplify the implementation of FIFOs.

The PFU, PIC and EBR blocks are arranged in a two-dimensional grid with rows and columns as shown in Figure 2-1. These blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

The corners contain the sysCLOCK Analog Phase Locked Loop (PLL) and Delay Locked Loop (DLL) Blocks. The PLLs have multiply, divide and phase shifting capability; they are used to manage the phase relationship of the clocks. The LatticeSC architecture provides eight analog PLLs per device and 12 DLLs. The DLLs provide a simple delay capability and can also be used to calibrate other delays within the device.

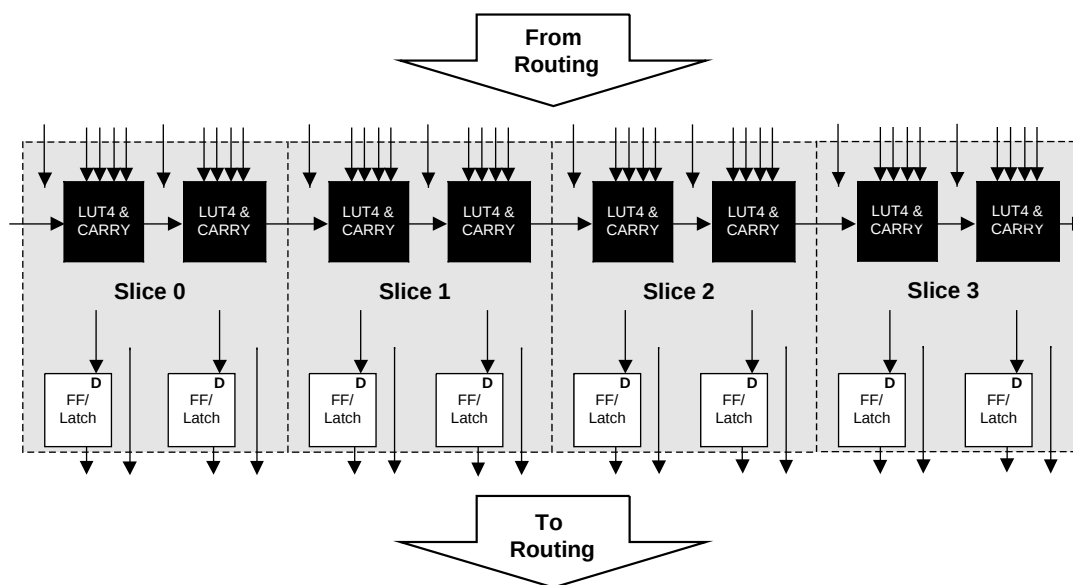
Every device in the family has a JTAG Port with internal Logic Analyzer (ispTRACY) capability. The sysCONFIG™ port which allows for serial or parallel device configuration. The system bus simplifies the connections of the external microprocessor to the device for tasks such as SERDES and PCS configuration or interface to the general FPGA logic. The LatticeSC devices use 1.2V as their core voltage operation with 1.0V operation also possible.

PFU Blocks

The core of the LatticeSC devices consists of PFU blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-2. PFU Diagram



Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to implement 5, 6, 7 and 8 Input LUTs (LUT5, LUT6, LUT7 and LUT8). There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

Figure 2-3. Slice Diagram

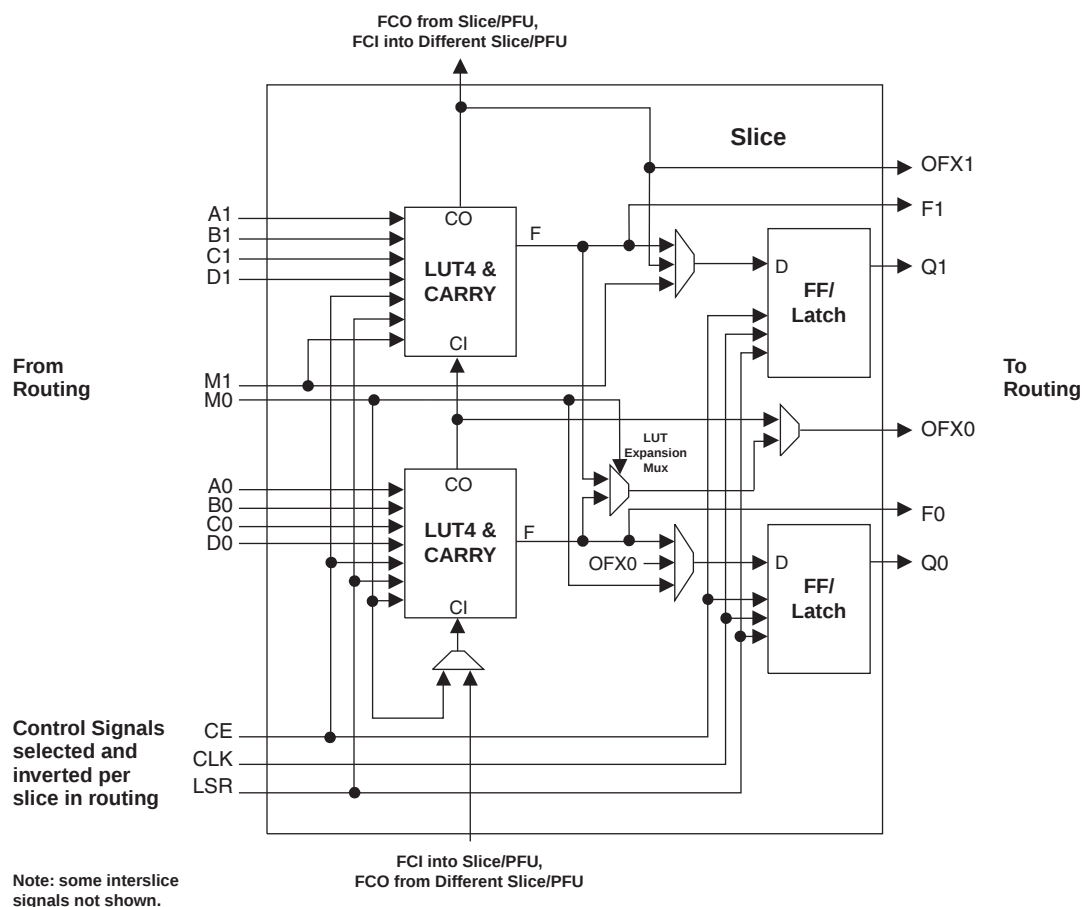


Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry In ¹
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output ²

1. See Figure 2-2 for connection details.

2. Requires two PFUs.

PCI Specification, Revision 2.2 requires the use of clamping diodes for 3.3V operation. For more information on the PCI interface, please refer to the PCI Specification, Revision 2.2.

Programmable Slew Rate Control

All output and bidirectional buffers have an optional programmable output slew rate control that can be configured for either low noise or high-speed performance. Each I/O pin has an individual slew rate control. This allows designers to specify slew rate control on a pin-by-pin basis. This slew rate control affects both the rising and falling edges.

Programmable Termination

Many of the I/O standards supported by the LatticeSC devices require termination at the transmitter, receiver or both. The SC devices provide the capability to implement many kinds of termination on-chip, minimizing stub lengths and hence improving performance. Utilizing this feature also has the benefit of reducing the number of discrete components required on the circuit board. The termination schemes can be split into two categories single-ended and differential.

Single Ended Termination

Single Ended Outputs: The SC devices support a number of different terminations for single ended outputs:

- Series
- Parallel to V_{CCIO} or GND
- Parallel to $V_{CCIO}/2$
- Parallel to $V_{CCIO}/2$ combined with series

Figure 2-27 shows the single ended output schemes that are supported. The nominal values of the termination resistors are shown in Table 2-10.

Initialization and Standby Supply Current

The table below indicates initialization and standby supply current while operating at 85°C junction temperature (T_J), which is the high end of the commercial temperature range, and 105°C, which is the high end of the industrial temperature range. This data assumes all outputs are tri-stated and all inputs are configured as LVCMOS and held at V_{CCIO} or GND. The remaining SERDES supply current for V_{DDIB} and V_{DDOB} is detailed in the SERDES section of this data sheet. For power at your design temperature, it is recommended to use the Power Calculator tool which is accessible in ispLEVER or can be used as a standalone tool. For more information on supply current, see the reference to additional technical documentation available at the end of this data sheet.

Over Recommended Operating Conditions

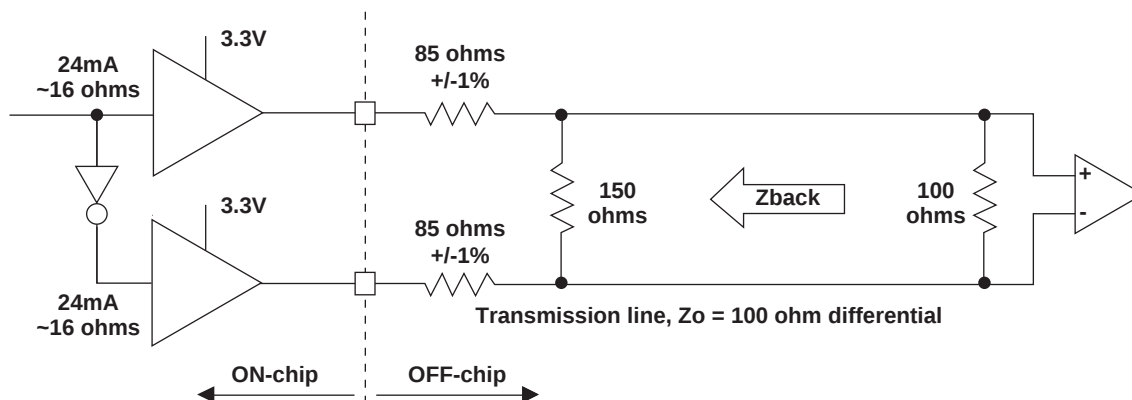
Symbol	Condition	Parameter	Device	25°C Typ. ¹	85°C Max. ²		105°C Max. ²	Units
				All	-5, -6	-7	-5, -6	
I_{CC}	(VCC = 1.2V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	65	449	678	755	mA
			LFSC/M25	113	798	1255	1343	mA
			LFSC/M40	159	1178	2006	1981	mA
			LFSC/M80	276	2122	3827	3569	mA
			LFSC/M115	454	3376	—	5679	mA
	(VCC = 1.0V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	45	312	471	524	mA
			LFSC/M25	79	554	872	933	mA
			LFSC/M40	110	818	1393	1375	mA
			LFSC/M80	191	1473	2658	2478	mA
			LFSC/M115	315	2344	—	3943	mA
I_{CC12}		1.2V Power Supply Current for Configuration Logic, FPGA PLL, SERDES PLL and SERDES Analog Supplies	LFSC/M15	23	39	59	35	mA
			LFSC/M25	25	50	78	56	mA
			LFSC/M40	31	78	133	89	mA
			LFSC/M80	50	108	195	123	mA
			LFSC/M115	65	131	—	154	mA
I_{CCAUX}		Auxiliary Operating Power Supply Current	LFSC/M15	7	12	19	14	mA
			LFSC/M25	9	16	25	18	mA
			LFSC/M40	12	23	39	25	mA
			LFSC/M80	13	25	45	23	mA
			LFSC/M115	16	27	—	26	mA
I_{CCIO} and I_{CCJ}		Bank Power Supply Current (per bank)	LFSC/M15	0.1	0.2	0.3	0.2	mA
			LFSC/M25	0.3	0.6	1.0	0.7	mA
			LFSC/M40	0.4	0.9	1.5	1.0	mA
			LFSC/M80	0.5	1.1	2.1	1.3	mA
			LFSC/M115	0.7	1.5	—	1.8	mA

1. I_{CC} is specified at $T_J = 25^\circ\text{C}$ and typical V_{CC} .

2. I_{CC} is specified at the respective commercial and industrial maximum T_J and V_{CC} limits.

LVPECL

The LatticeSC devices support differential LVPECL standard. This standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL**Table 3-3. LVPECL DC Conditions¹****Over Recommended Operating Conditions**

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	16	ohm
R_S	Driver series resistor	85	ohm
R_P	Driver parallel resistor	150	ohm
R_T	Receiver termination	100	ohm
V_{OH}	Output high voltage	2.03	V
V_{OL}	Output low voltage	1.27	V
V_{OD}	Output differential voltage	0.76	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	86	ohm
I_{DC}	DC output current	12.6	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS, MLVDS and other differential interfaces please see details of additional technical documentation at the end of this data sheet.

On-die Differential Common Mode Termination

Symbol	Description	Min.	Typ.	Max.	Units
C_{CMT}	Capacitance V_{CMT} to GND	—	40	—	pF

LatticeSC/M Internal Timing Parameters¹ (Continued)

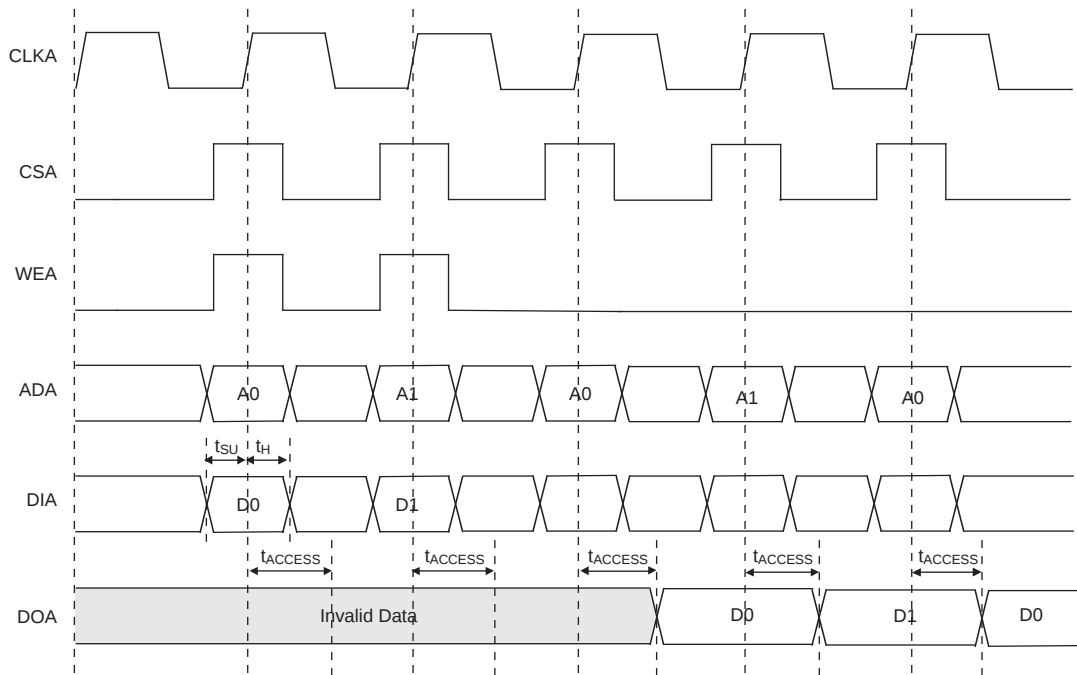
Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

Parameter	Symbol	Description	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
EBR Timing									
t _{CO_EBR}	CK_Q_DEL	Clock (Read) to output from Address or Data	—	1.900	—	2.116	—	2.335	ns
t _{COO_EBR}	CK_Q_DEL	Clock (Write) to output from EBR output Register	0.390	—	0.444	—	0.498	—	ns
t _{SUDATA_EBR}	D_CK_SET	Setup Data to EBR Memory (Write clk)	-0.173	—	-0.192	—	-0.210	—	ns
t _{HDATA_EBR}	D_CK_HLD	Hold Data to EBR Memory (Write clk)	0.276	—	0.305	—	0.335	—	ns
t _{SUADDR_EBR}	A_CK_SET	Setup Address to EBR Memory (Write clk)	-0.165	—	-0.182	—	-0.200	—	ns
t _{HADDR_EBR}	A_CK_HLD	Hold Address to EBR Memory (Write clk)	0.269	—	0.298	—	0.327	—	ns
t _{SUWREN_EBR}	CE_CK_SET	Setup Write/Read Enable to EBR Memory (Write/Read clk)	0.225	—	0.226	—	0.226	—	ns
t _{HWREN_EBR}	CE_CK_HLD	Hold Write/Read Enable to EBR Memory (write/read clk)	0.073	—	0.095	—	0.116	—	ns
t _{SUCE_EBR}	CS_CK_SET	Clock Enable Setup Time to EBR Output Register (Read clk)	0.261	—	0.269	—	0.276	—	ns
t _{HCE_EBR}	CS_CK_HLD	Clock Enable Hold Time to EBR Out-put Register (Read clk)	0.023	—	0.039	—	0.055	—	ns
t _{RSTO_EBR}	RESET_Q_DEL	Reset To Output Delay Time from EBR Output Register (asynchronous)	—	0.589	—	0.673	—	0.757	ns
Cycle Boosting Timing									
t _{DEL1}	DEL1	Cycle boosting delay 1 applies to PIO, PFU, EBR	—	0.480	—	0.524	—	0.570	ns
t _{DEL2}	DEL2	Cycle boosting delay 2 applies to PIO, PFU, EBR	—	0.922	—	1.005	—	1.090	ns
t _{DEL3}	DEL3	Cycle boosting delay 3 applies to PIO, PFU, EBR	—	1.366	—	1.488	—	1.612	ns

1. Complete timing parameters for a user design will be incorporated when running ispLEVER. This is a sampling of the key timing parameters.

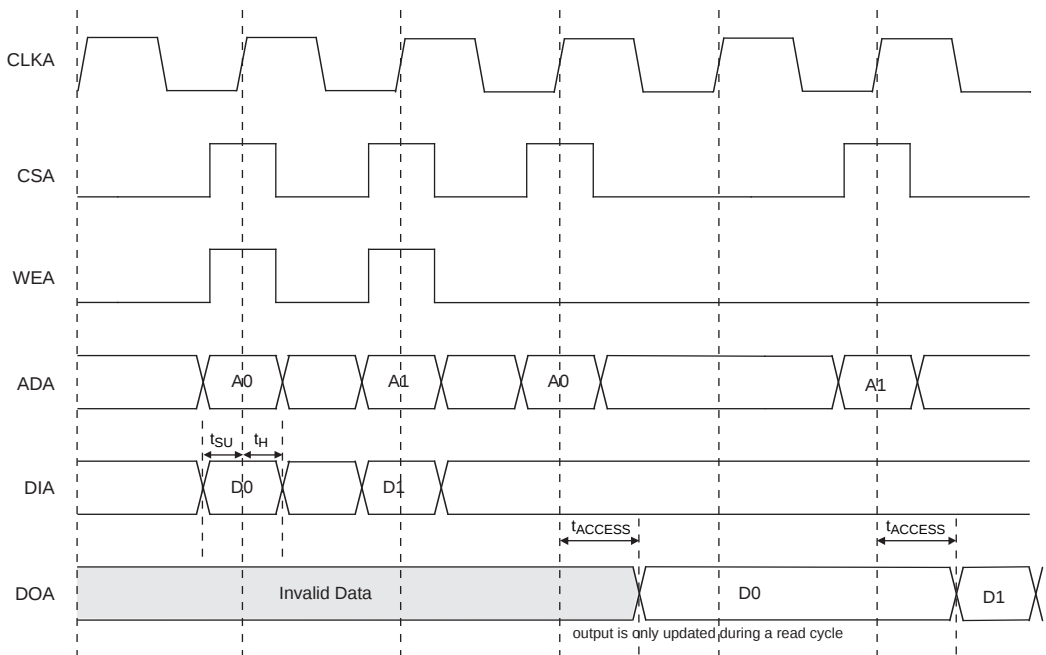
EBR Memory Timing Diagrams

Figure 3-6. Read Mode



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

Figure 3-7. Read Mode with Input Registers Only



LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH20	NC	-		PB51D	4	
AK27	NC	-		NC	-	
AJ24	NC	-		NC	-	
AF17	NC	-		PB42C	4	
AH27	NC	-		PB61B	4	
AD23	NC	-		PB57A	4	
AE23	NC	-		PB57B	4	
AH24	NC	-		PB59A	4	
AH25	NC	-		PB59B	4	
AH26	NC	-		PB61A	4	
AF24	NC	-		PB63A	4	
AG24	NC	-		PB63B	4	
AG25	NC	-		PB64A	4	
AF25	NC	-		PB64B	4	
AG26	NC	-		PB65A	4	
AF27	NC	-		PB65B	4	
AD28	NC	-		PR56B	3	
AC27	NC	-		PR56A	3	
AE29	NC	-		PR53B	3	
AD29	NC	-		PR53A	3	
AB30	NC	-		NC	-	
AA28	NC	-		NC	-	
Y27	NC	-		PR47C	3	
W27	NC	-		PR47D	3	
V30	NC	-		PR47A	3	
W30	NC	-		PR47B	3	
W26	NC	-		PR43D	3	
V26	NC	-		PR43C	3	
U25	NC	-		PR42C	3	
T27	NC	-		PR40B	3	
R27	NC	-		PR40A	3	
V27	NC	-		PR39B	3	
U27	NC	-		PR39A	3	
U29	NC	-		PR36B	3	
T29	NC	-		PR36A	3	
T24	NC	-		PR35C	3	
Y25	NC	-		PR48C	3	
P24	NC	-		NC	-	
K28	NC	-		NC	-	
P23	NC	-		NC	-	
L28	NC	-		NC	-	
M27	NC	-		PR21B	2	
L27	NC	-		PR21A	2	
H27	NC	-		PR20B	2	
G27	NC	-		PR20A	2	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB3	NC	-		PR58B	3	
AB4	NC	-		PR58A	3	
AG4	NC	-		PR57D	3	
AG3	NC	-		PR57C	3	
AA2	NC	-		PR57B	3	
AB2	NC	-		PR57A	3	
AA3	NC	-		PR56B	3	
AA4	NC	-		PR56A	3	
L5	NC	-		PR22D	2	
L6	NC	-		PR22C	2	
M2	NC	-		PR34B	2	
L2	NC	-		PR34A	2	
L3	NC	-		PR31B	2	
M3	NC	-		PR31A	2	
L4	NC	-		PR30B	2	
M4	NC	-		PR30A	2	
P7	NC	-		PR29D	2	
P8	NC	-		PR29C	2	
K1	NC	-		PR29B	2	
K2	NC	-		PR29A	2	
N6	NC	-		PR27D	2	
N7	NC	-		PR27C	2	
J2	NC	-		PR27B	2	
J1	NC	-		PR27A	2	
N5	NC	-		PR26D	2	
M5	NC	-		PR26C	2	
H3	NC	-		PR26B	2	
J3	NC	-		PR26A	2	
A5	VDDAX25_R	-		VDDAX25_R	-	
A28	VDDAX25_L	-		VDDAX25_L	-	
AJ25	NC	-		PB21A	5	
AK25	NC	-		PB21B	5	
AF20	NC	-		PB27C	5	
AG6	NC	-		PB62C	4	
AM7	NC	-		PB66A	4	
AL7	NC	-		PB66B	4	
AD13	NC	-		PB66C	4	
AC13	NC	-		PB66D	4	
AC20	NC	-		PB22C	5	
AD20	NC	-		PB22D	5	
AM9	NC	-		PB61A	4	
AM8	NC	-		PB61B	4	
AF13	NC	-		PB61C	4	
AE13	NC	-		PB61D	4	
E30	VCC12	-		VCC12	-	
E29	VCC12	-		VCC12	-	
E27	VCC12	-		VCC12	-	
E26	VCC12	-		VCC12	-	
E25	VCC12	-		VCC12	-	
E24	VCC12	-		VCC12	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L33	PL27B	7		PL35B	7	
M30	PL27C	7		PL35C	7	
N30	PL27D	7		PL35D	7	
M31	PL29A	7		PL37A	7	
N31	PL29B	7		PL37B	7	
P24	PL29C	7		PL37C	7	
R24	PL29D	7		PL37D	7	
M33	PL30A	7		PL42A	7	
N33	PL30B	7		PL42B	7	
U25	PL30C	7		PL42C	7	
T25	PL30D	7		PL42D	7	
L34	PL31A	7		PL43A	7	
M34	PL31B	7		PL43B	7	
P29	PL31C	7		PL43C	7	
R29	PL31D	7		PL43D	7	
N34	PL34A	7		PL46A	7	
P34	PL34B	7		PL46B	7	
R27	PL34C	7		PL46C	7	
T27	PL34D	7		PL46D	7	
R32	PL35A	7	PCLKT7_1	PL47A	7	PCLKT7_1
R31	PL35B	7	PCLKC7_1	PL47B	7	PCLKC7_1
U24	PL35C	7	PCLKT7_3	PL47C	7	PCLKT7_3
T24	PL35D	7	PCLKC7_3	PL47D	7	PCLKC7_3
P33	PL36A	7	PCLKT7_0	PL48A	7	PCLKT7_0
R33	PL36B	7	PCLKC7_0	PL48B	7	PCLKC7_0
T26	PL36C	7	PCLKT7_2	PL48C	7	PCLKT7_2
U26	PL36D	7	PCLKC7_2	PL48D	7	PCLKC7_2
T32	PL38A	6	PCLKT6_0	PL50A	6	PCLKT6_0
T31	PL38B	6	PCLKC6_0	PL50B	6	PCLKC6_0
U29	PL38C	6	PCLKT6_1	PL50C	6	PCLKT6_1
V29	PL38D	6	PCLKC6_1	PL50D	6	PCLKC6_1
T30	PL39A	6		PL51A	6	
U30	PL39B	6		PL51B	6	
U27	PL39C	6	PCLKT6_3	PL51C	6	PCLKT6_3
V27	PL39D	6	PCLKC6_3	PL51D	6	PCLKC6_3
R34	PL40A	6		PL52A	6	
T34	PL40B	6		PL52B	6	
U28	PL40C	6	PCLKT6_2	PL52C	6	PCLKT6_2
V28	PL40D	6	PCLKC6_2	PL52D	6	PCLKC6_2
V30	PL43A	6		PL55A	6	
W30	PL43B	6		PL55B	6	
W27	PL43C	6	VREF1_6	PL55C	6	VREF1_6
Y27	PL43D	6		PL55D	6	
T33	PL44A	6		PL56A	6	
U33	PL44B	6		PL56B	6	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD29	PL60D	6		PL84D	6	
AE31	PL61A	6		PL85A	6	
AF31	PL61B	6		PL85B	6	
AF30	PL61C	6		PL85C	6	
AF29	PL61D	6		PL85D	6	
AH33	PL62A	6		PL86A	6	
AJ33	PL62B	6		PL86B	6	
AC28	PL62C	6		PL86C	6	
AD28	PL62D	6		PL86D	6	
AH32	PL65A	6		PL89A	6	
AJ32	PL65B	6		PL89B	6	
AD27	PL65C	6		PL89C	6	
AE27	PL65D	6	VREF2_6	PL89D	6	VREF2_6
AG34	PL66A	6		PL90A	6	
AH34	PL66B	6		PL90B	6	
AC26	PL66C	6		PL90C	6	
AB26	PL66D	6		PL90D	6	
AK33	PL67A	6		PL91A	6	
AL33	PL67B	6		PL91B	6	
AG30	PL67C	6		PL91C	6	
AH30	PL67D	6		PL91D	6	
AL34	PL69A	6		PL93A	6	
AM34	PL69B	6		PL93B	6	
AJ30	PL69C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL93C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AK30	PL69D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL93D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AJ31	PL70A	6		PL94A	6	
AH31	PL70B	6		PL94B	6	
AD26	PL70C	6		PL94C	6	
AD25	PL70D	6		PL94D	6	
AL32	PL71A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL95A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AL31	PL71B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL95B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AG29	PL71C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL95C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AG28	PL71D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL95D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AF28	XRES	-		XRES	-	
AF27	TEMP	6		TEMP	6	
AM33	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AN33	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
AH29	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AJ29	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AM32	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AM31	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AG27	PB4C	5		PB4C	5	
AG26	PB4D	5		PB4D	5	
AL29	PB5A	5		PB5A	5	
AL28	PB5B	5		PB5B	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
K20	GND	-		GND	-	
K23	GND	-		GND	-	
K26	GND	-		GND	-	
K28	GND	-		GND	-	
K6	GND	-		GND	-	
K9	GND	-		GND	-	
L12	GND	-		GND	-	
L32	GND	-		GND	-	
L4	GND	-		GND	-	
M10	GND	-		GND	-	
M17	GND	-		GND	-	
M24	GND	-		GND	-	
N29	GND	-		GND	-	
N7	GND	-		GND	-	
P15	GND	-		GND	-	
P20	GND	-		GND	-	
P3	GND	-		GND	-	
P31	GND	-		GND	-	
R10	GND	-		GND	-	
R14	GND	-		GND	-	
R16	GND	-		GND	-	
R19	GND	-		GND	-	
R21	GND	-		GND	-	
R26	GND	-		GND	-	
T15	GND	-		GND	-	
T17	GND	-		GND	-	
T18	GND	-		GND	-	
T20	GND	-		GND	-	
T28	GND	-		GND	-	
T6	GND	-		GND	-	
U16	GND	-		GND	-	
U19	GND	-		GND	-	
U23	GND	-		GND	-	
U32	GND	-		GND	-	
U4	GND	-		GND	-	
V12	GND	-		GND	-	
V16	GND	-		GND	-	
V19	GND	-		GND	-	
V3	GND	-		GND	-	
V31	GND	-		GND	-	
W15	GND	-		GND	-	
W17	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W29	GND	-		GND	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AJ34	PL98A	6	
AK34	PL98B	6	
AB27	PL98C	6	
AC27	PL98D	6	
AF33	PL99A	6	
AG33	PL99B	6	
AC29	PL99C	6	
AD29	PL99D	6	
AE31	PL103A	6	
AF31	PL103B	6	
AF30	PL103C	6	
AF29	PL103D	6	
AH33	PL104A	6	
AJ33	PL104B	6	
AC28	PL104C	6	
AD28	PL104D	6	
AH32	PL107A	6	
AJ32	PL107B	6	
AD27	PL107C	6	
AE27	PL107D	6	VREF2_6
AG34	PL109A	6	
AH34	PL109B	6	
AC26	PL109C	6	
AB26	PL109D	6	
AK33	PL112A	6	
AL33	PL112B	6	
AG30	PL112C	6	
AH30	PL112D	6	
AL34	PL115A	6	
AM34	PL115B	6	
AJ30	PL115C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AK30	PL115D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AJ31	PL116A	6	
AH31	PL116B	6	
AD26	PL116C	6	
AD25	PL116D	6	
AL32	PL117A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AL31	PL117B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AG29	PL117C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AG28	PL117D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AF28	XRES	-	
AF27	TEMP	6	
AM33	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AL5	GND	-	
AM14	GND	-	
AM18	GND	-	
AM24	GND	-	
AM30	GND	-	
AM8	GND	-	
AN1	GND	-	
AN34	GND	-	
AP2	GND	-	
AP33	GND	-	
B1	GND	-	
B34	GND	-	
C11	GND	-	
C12	GND	-	
C13	GND	-	
C14	GND	-	
C17	GND	-	
C21	GND	-	
C22	GND	-	
C23	GND	-	
C24	GND	-	
C26	GND	-	
C27	GND	-	
C30	GND	-	
C31	GND	-	
C4	GND	-	
C5	GND	-	
C8	GND	-	
C9	GND	-	
D18	GND	-	
E32	GND	-	
E4	GND	-	
F19	GND	-	
G16	GND	-	
G29	GND	-	
G7	GND	-	
H3	GND	-	
H31	GND	-	
J10	GND	-	
J15	GND	-	
J26	GND	-	
K20	GND	-	
K23	GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W33	PL42C	7		PL56C	7	
Y33	PL42D	7		PL56D	7	
W37	PL43A	7		PL57A	7	
Y37	PL43B	7		PL57B	7	
Y32	PL43C	7		PL57C	7	
AA32	PL43D	7		PL57D	7	
U38	PL46A	7		PL60A	7	
V38	PL46B	7		PL60B	7	
W34	PL46C	7		PL60C	7	
Y34	PL46D	7		PL60D	7	
T40	PL47A	7	PCLKT7_1	PL61A	7	PCLKT7_1
U40	PL47B	7	PCLKC7_1	PL61B	7	PCLKC7_1
AA33	PL47C	7	PCLKT7_3	PL61C	7	PCLKT7_3
AB33	PL47D	7	PCLKC7_3	PL61D	7	PCLKC7_3
R42	PL48A	7	PCLKT7_0	PL62A	7	PCLKT7_0
T42	PL48B	7	PCLKC7_0	PL62B	7	PCLKC7_0
AA34	PL48C	7	PCLKT7_2	PL62C	7	PCLKT7_2
AB34	PL48D	7	PCLKC7_2	PL62D	7	PCLKC7_2
U41	PL50A	6	PCLKT6_0	PL64A	6	PCLKT6_0
V41	PL50B	6	PCLKC6_0	PL64B	6	PCLKC6_0
V36	PL50C	6	PCLKT6_1	PL64C	6	PCLKT6_1
W36	PL50D	6	PCLKC6_1	PL64D	6	PCLKC6_1
U42	PL51A	6		PL65A	6	
V42	PL51B	6		PL65B	6	
AB31	PL51C	6	PCLKT6_3	PL65C	6	PCLKT6_3
AC31	PL51D	6	PCLKC6_3	PL65D	6	PCLKC6_3
W38	PL52A	6		PL66A	6	
Y38	PL52B	6		PL66B	6	
AA35	PL52C	6	PCLKT6_2	PL66C	6	PCLKT6_2
AB35	PL52D	6	PCLKC6_2	PL66D	6	PCLKC6_2
W39	PL55A	6		PL69A	6	
Y39	PL55B	6		PL69B	6	
AB32	PL55C	6	VREF1_6	PL69C	6	VREF1_6
AC32	PL55D	6		PL69D	6	
W40	PL56A	6		PL70A	6	
Y40	PL56B	6		PL70B	6	
AA36	PL56C	6		PL70C	6	
AB36	PL56D	6		PL70D	6	
W41	PL57A	6		PL71A	6	
Y41	PL57B	6		PL71B	6	
AA37	PL57C	6		PL71C	6	
AB37	PL57D	6		PL71D	6	
W42	PL59A	6		PL73A	6	
Y42	PL59B	6		PL73B	6	
AC33	PL59C	6		PL73C	6	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB6	PR57D	3		PR71D	3	
AA6	PR57C	3		PR71C	3	
Y2	PR57B	3		PR71B	3	
W2	PR57A	3		PR71A	3	
AB7	PR56D	3		PR70D	3	
AA7	PR56C	3		PR70C	3	
Y3	PR56B	3		PR70B	3	
W3	PR56A	3		PR70A	3	
AC11	PR55D	3		PR69D	3	
AB11	PR55C	3	VREF1_3	PR69C	3	VREF1_3
Y4	PR55B	3		PR69B	3	
W4	PR55A	3		PR69A	3	
AB8	PR52D	3	PCLKC3_2	PR66D	3	PCLKC3_2
AA8	PR52C	3	PCLKT3_2	PR66C	3	PCLKT3_2
Y5	PR52B	3		PR66B	3	
W5	PR52A	3		PR66A	3	
AC12	PR51D	3	PCLKC3_3	PR65D	3	PCLKC3_3
AB12	PR51C	3	PCLKT3_3	PR65C	3	PCLKT3_3
V1	PR51B	3		PR65B	3	
U1	PR51A	3		PR65A	3	
W7	PR50D	3	PCLKC3_1	PR64D	3	PCLKC3_1
V7	PR50C	3	PCLKT3_1	PR64C	3	PCLKT3_1
V2	PR50B	3	PCLKC3_0	PR64B	3	PCLKC3_0
U2	PR50A	3	PCLKT3_0	PR64A	3	PCLKT3_0
AB9	PR48D	2	PCLKC2_2	PR62D	2	PCLKC2_2
AA9	PR48C	2	PCLKT2_2	PR62C	2	PCLKT2_2
T1	PR48B	2	PCLKC2_0	PR62B	2	PCLKC2_0
R1	PR48A	2	PCLKT2_0	PR62A	2	PCLKT2_0
AB10	PR47D	2	PCLKC2_3	PR61D	2	PCLKC2_3
AA10	PR47C	2	PCLKT2_3	PR61C	2	PCLKT2_3
U3	PR47B	2	PCLKC2_1	PR61B	2	PCLKC2_1
T3	PR47A	2	PCLKT2_1	PR61A	2	PCLKT2_1
Y9	PR46D	2		PR60D	2	
W9	PR46C	2		PR60C	2	
V5	PR46B	2		PR60B	2	
U5	PR46A	2		PR60A	2	
AA11	PR43D	2		PR57D	2	
Y11	PR43C	2		PR57C	2	
Y6	PR43B	2		PR57B	2	
W6	PR43A	2		PR57A	2	
Y10	PR42D	2		PR56D	2	
W10	PR42C	2		PR56C	2	
T2	PR42B	2		PR56B	2	
R2	PR42A	2		PR56A	2	
W8	PR41D	2		PR55D	2	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AC24	GND	-		GND	-	
AC26	GND	-		GND	-	
AC35	GND	-		GND	-	
AC8	GND	-		GND	-	
AD12	GND	-		GND	-	
AD16	GND	-		GND	-	
AD18	GND	-		GND	-	
AD20	GND	-		GND	-	
AD23	GND	-		GND	-	
AD25	GND	-		GND	-	
AD27	GND	-		GND	-	
AD31	GND	-		GND	-	
AE17	GND	-		GND	-	
AE19	GND	-		GND	-	
AE24	GND	-		GND	-	
AE26	GND	-		GND	-	
AE3	GND	-		GND	-	
AE39	GND	-		GND	-	
AF18	GND	-		GND	-	
AF20	GND	-		GND	-	
AF23	GND	-		GND	-	
AF25	GND	-		GND	-	
AF36	GND	-		GND	-	
AF7	GND	-		GND	-	
AG11	GND	-		GND	-	
AG16	GND	-		GND	-	
AG19	GND	-		GND	-	
AG24	GND	-		GND	-	
AG27	GND	-		GND	-	
AG32	GND	-		GND	-	
AH15	GND	-		GND	-	
AH28	GND	-		GND	-	
AH4	GND	-		GND	-	
AH40	GND	-		GND	-	
AJ35	GND	-		GND	-	
AJ8	GND	-		GND	-	
AK12	GND	-		GND	-	
AK31	GND	-		GND	-	
AL13	GND	-		GND	-	
AL19	GND	-		GND	-	
AL24	GND	-		GND	-	
AL3	GND	-		GND	-	
AL30	GND	-		GND	-	
AL39	GND	-		GND	-	
AM16	GND	-		GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AW25	VCCIO5	-		VCCIO5	-	
AW31	VCCIO5	-		VCCIO5	-	
AW37	VCCIO5	-		VCCIO5	-	
AY22	VCCIO5	-		VCCIO5	-	
AY28	VCCIO5	-		VCCIO5	-	
AY34	VCCIO5	-		VCCIO5	-	
AB39	VCCIO6	-		VCCIO6	-	
AC36	VCCIO6	-		VCCIO6	-	
AD32	VCCIO6	-		VCCIO6	-	
AE40	VCCIO6	-		VCCIO6	-	
AF35	VCCIO6	-		VCCIO6	-	
AG31	VCCIO6	-		VCCIO6	-	
AH39	VCCIO6	-		VCCIO6	-	
AJ36	VCCIO6	-		VCCIO6	-	
AK32	VCCIO6	-		VCCIO6	-	
AL40	VCCIO6	-		VCCIO6	-	
AM35	VCCIO6	-		VCCIO6	-	
AP39	VCCIO6	-		VCCIO6	-	
AR36	VCCIO6	-		VCCIO6	-	
AU40	VCCIO6	-		VCCIO6	-	
AA40	VCCIO7	-		VCCIO7	-	
H36	VCCIO7	-		VCCIO7	-	
J40	VCCIO7	-		VCCIO7	-	
L35	VCCIO7	-		VCCIO7	-	
M39	VCCIO7	-		VCCIO7	-	
P36	VCCIO7	-		VCCIO7	-	
R40	VCCIO7	-		VCCIO7	-	
T31	VCCIO7	-		VCCIO7	-	
U35	VCCIO7	-		VCCIO7	-	
V39	VCCIO7	-		VCCIO7	-	
W32	VCCIO7	-		VCCIO7	-	
Y36	VCCIO7	-		VCCIO7	-	
AA14	VTT_2	2		VTT_2	2	
AA15	VTT_2	2		VTT_2	2	
R12	VTT_2	2		VTT_2	2	
V14	VTT_2	2		VTT_2	2	
AB14	VTT_3	3		VTT_3	3	
AB15	VTT_3	3		VTT_3	3	
AE14	VTT_3	3		VTT_3	3	
AJ13	VTT_3	3		VTT_3	3	
AH21	VTT_4	4		VTT_4	4	
AJ18	VTT_4	4		VTT_4	4	
AJ19	VTT_4	4		VTT_4	4	
AJ20	VTT_4	4		VTT_4	4	
AJ21	VTT_4	4		VTT_4	4	

Conventional Packaging**Commercial**

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-7F256C	-7	fpBGA	256	COM	15.2
LFSC3GA15E-6F256C	-6	fpBGA	256	COM	15.2
LFSC3GA15E-5F256C	-5	fpBGA	256	COM	15.2
LFSC3GA15E-7F900C	-7	fpBGA	900	COM	15.2
LFSC3GA15E-6F900C	-6	fpBGA	900	COM	15.2
LFSC3GA15E-5F900C	-5	fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-7F256C	-7	fpBGA	256	COM	15.2
LFSCM3GA15EP1-6F256C	-6	fpBGA	256	COM	15.2
LFSCM3GA15EP1-5F256C	-5	fpBGA	256	COM	15.2
LFSCM3GA15EP1-7F900C	-7	fpBGA	900	COM	15.2
LFSCM3GA15EP1-6F900C	-6	fpBGA	900	COM	15.2
LFSCM3GA15EP1-5F900C	-5	fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-7F900C	-7	fpBGA	900	COM	25.4
LFSC3GA25E-6F900C	-6	fpBGA	900	COM	25.4
LFSC3GA25E-5F900C	-5	fpBGA	900	COM	25.4
LFSC3GA25E-7FF1020C ¹	-7	Organic fcBGA	1020	COM	25.4
LFSC3GA25E-6FF1020C ¹	-6	Organic fcBGA	1020	COM	25.4
LFSC3GA25E-5FF1020C ¹	-5	Organic fcBGA	1020	COM	25.4
LFSC3GA25E-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-7F900C	-7	fpBGA	900	COM	25.4
LFSCM3GA25EP1-6F900C	-6	fpBGA	900	COM	25.4
LFSCM3GA25EP1-5F900C	-5	fpBGA	900	COM	25.4
LFSCM3GA25EP1-7FF1020C ¹	-7	Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-6FF1020C ¹	-6	Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-5FF1020C ¹	-5	Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).