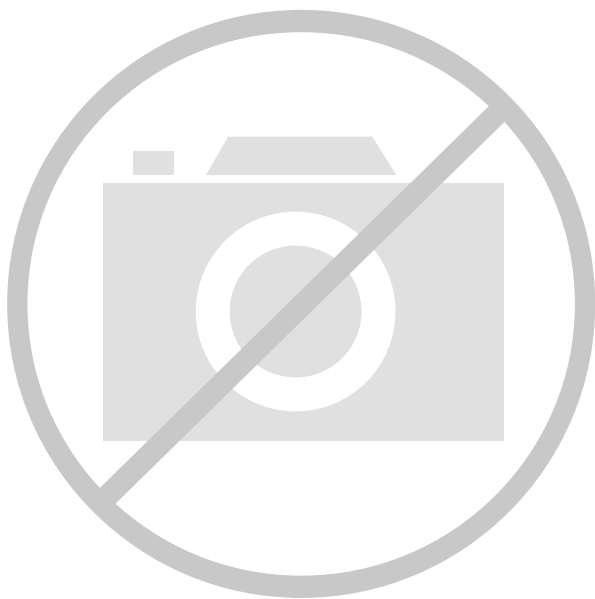




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	28750
Number of Logic Elements/Cells	115000
Total RAM Bits	7987200
Number of I/O	942
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1704-BCBGA, FCBGA
Supplier Device Package	1704-CFCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga115ep1-6fcn1704c

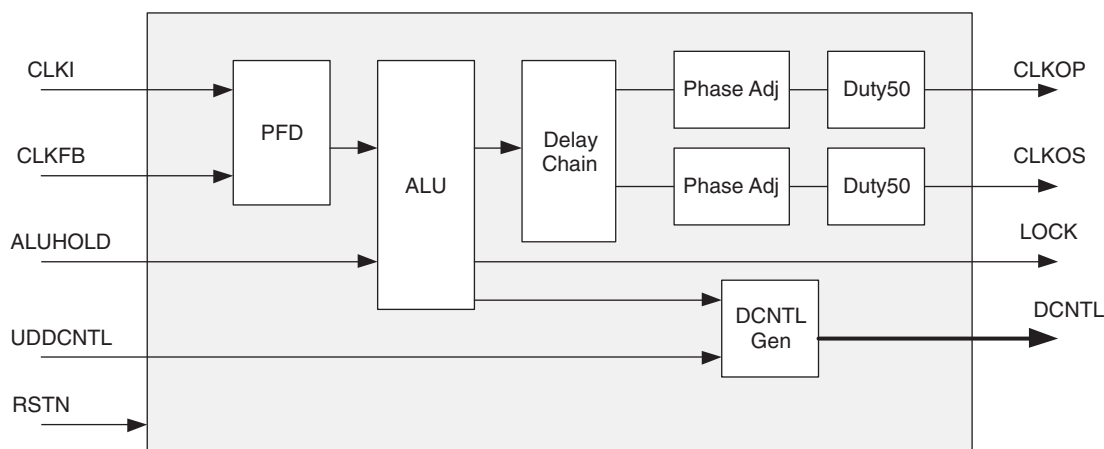
There is a Digital Control (DCNTL) bus available from the DLL block. This Digital Control bus is available to the delay lines in the PIC blocks in the adjacent banks. The UDDCNTL signal allows the user to latch the current value on the digital control bus.

Figure 2-12 shows the DLL block diagram of the DLL inputs and outputs. The output of the phase frequency detector controls an arithmetic logic unit (ALU) to add or subtract one delay tap. The digital output of this ALU is used to control the delay value of the delay chain and this digital code is transmitted via the DCNTL bus.

The sysCLOCK DLL can be configured at power-up, then, if desired, reconfigured dynamically through the Serial Memory Interface bus which interfaces with the on-chip Microprocessor Interface (MPI) bus. In addition, users can drive the SMI interface from routing if desired.

The user can configure the DLL for many common functions such as clock injection match and single delay cell. Lattice provides primitives in its design for time reference delay (DDR memory) and clock injection delay removal.

Figure 2-12. DLL Diagram



PLL/DLL Cascading

The LatticeSC devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are as follows:

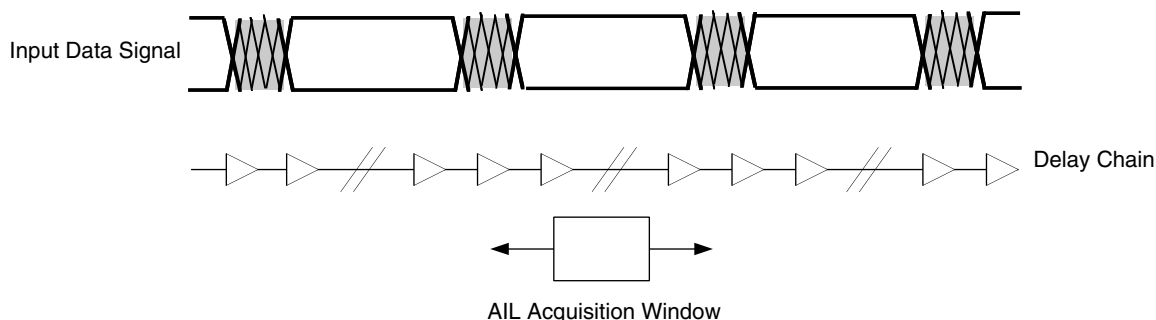
- PLL to PLL
- PLL to DLL
- DLL to DLL
- DLL to PLL

DLLs are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLL and PLLs.

When cascading the DLL to the PLL, the DLL can be used to drive the PLL to create fine phase shifts of an input clock signal. Figure 2-13 shows a shift of all outputs for CLKOP and CLKOS out in time.

Adaptive Input Logic (AIL) Overview

The Adaptive Input Logic (AIL) provides the ability of the input logic to dynamically find a solution by monitoring multiple samples of the input data. The input data signal from the input buffer is run through a delay chain. Data, transitions, jitter, noise are all contained inside of the delay chain. The AIL will then search the delay chain for a clean sampling point for data. Once found the AIL will monitor and walk with the data dynamically. This novel approach of using a delay chain to create multiple copies of the data provides a lower power solution than oversampling data with a higher speed clock. Figure 2-19 provides a high level view of the AIL methodology.

Figure 2-19. LatticeSC AIL Delay of Input Data Waveform

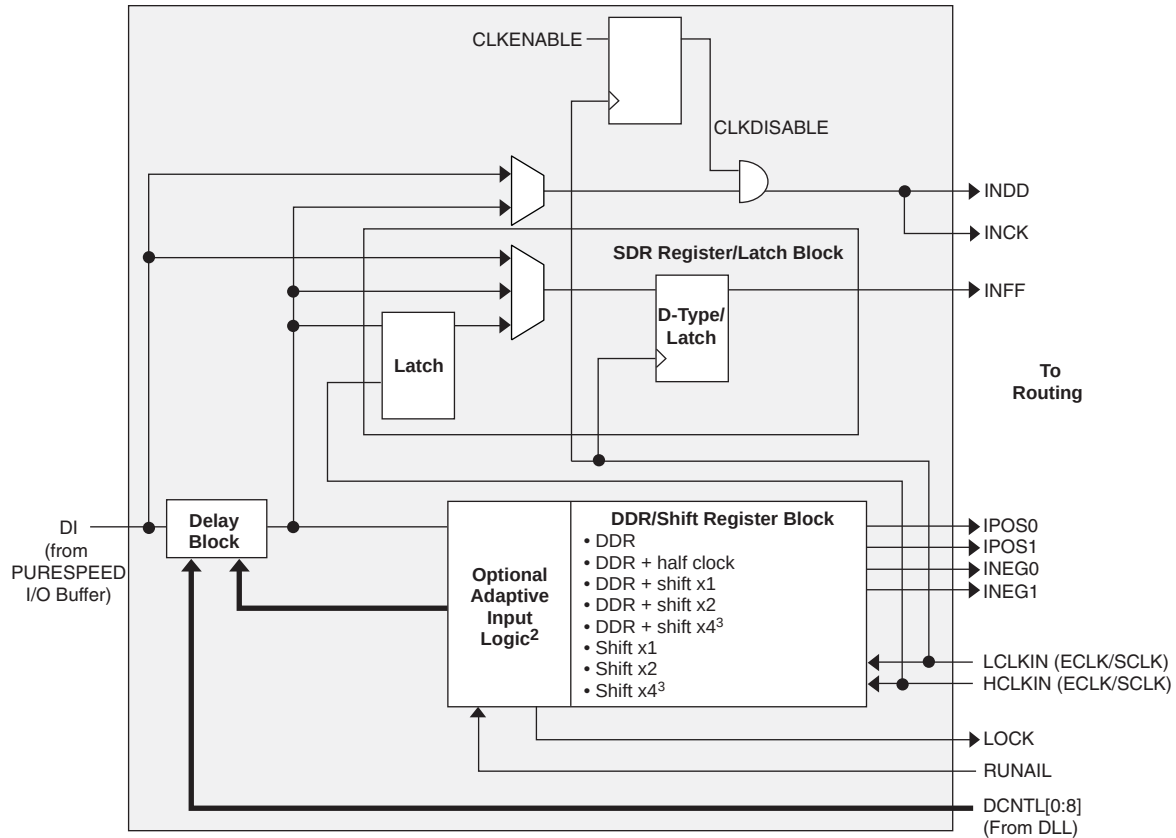
The AIL slides the acquisition window through the delay chain searching for stable data based solely on data transitions. A specific training pattern is not required to perform this bit alignment, simply data transitions. The size of the acquisition window is user-selectable allowing the AIL to operate over the full range of the PURESPEED I/O range. Based on dynamic user control the AIL can either continuously adjust the window location based on data edge detection or it can be locked to a specific delay.

The AIL operates on single data and double data rate interfaces and is available on most FPGA input pins on the LatticeSC device and all buffer types. The AIL block is low power using only 0.003 mW/MHz typical (6 mW @ 2 Gbps) for PRBS 2^7 data. Multiple AIL inputs can be used to create a bus with a FPGA circuit to realign the bus to a common clock cycle. The FPGA circuit to realign the bus is required and is provided by Lattice as a reference design.

For more information on the LatticeSC AIL please refer to TN1158 [LatticeSC PURESPEED I/O Adaptive Input Logic User's Guide](#).

Input DDR/Shift Block

The DDR/Shift block contains registers and associated logic that support DDR and shift register functions using the high-speed clock and the associated transfer to the low-speed clock domain. It functions as a gearbox allowing high-speed incoming data to be passed into the FPGA fabric. Each PIO supports DDR and x2 shift functions. If desired PIOs A and B or C and D can be combined to form x4 shift functions. The PIOs A and C on the left, right and bottom of the device also contain an optional Adaptive Input Logic (AIL) element. This logic automatically aligns incoming data with the clock allowing for easy design of high-speed interfaces. Figure 2-21 shows a simplified block diagram of the shift register block. The shift block in conjunction with the update and clock divider blocks automatically handles the hand off between the low-speed and high-speed clock domains.

Figure 2-20. Input Register Block¹

1. UPDATE, Set and Reset not shown for clarity
2. Adaptive input logic is only available in selected PIO
3. By four shift modes utilize DDR/shift register block from paired PIO.
4. CLKDISABLE is used to block the transitions on the DQS pin during post-amble. Its main use is to disable DQS (typically found in DDR memory interfaces) or other clock signals. It can also be used to disable any/all input signals to save power.

this allows for easy integration with the rest of the system. These capabilities make the LatticeSC ideal for many multiple power supply and hot-swap applications. The maximum current during hot socketing is 4mA. See Hot Socketing Specifications in Chapter 3 of this data sheet.

Power-Up Requirements

To prevent high power supply and input pin currents, each VCC, VCC12, VCCAUX, VCCIO and VCCJ power supplies must have a monotonic ramp up time of 75 ms or less to reach its minimum operating voltage. Apart from VCC and VCC12, which have an additional requirement, and VCCIO and VCCAUX, which also have an additional requirement, the VCC, VCC12, VCCAUX, VCCIO and VCCJ power supplies can ramp up in any order, with no restriction on the time between them. However, the ramp time for each must be 75 ms or less. Configuration of the device will not proceed until the last power supply has reached its minimum operating voltage.

Additional Requirement for VCC and VCC12:

VCC12 must always be higher than VCC. This condition must be maintained at ALL times, including during power-up and power-down. Note that for 1.2V only operation, it is advisable to source both of these supplies from the same power supply.

Additional Requirement for VCCIO and VCCAUX:

If any VCCIOs are 1.2/1.5/1.8V, then VCCAUX MUST be applied before them. If any VCCIO is 1.2/1.5/1.8V and is powered up before VCCAUX, then when VCCAUX is powered up, it may drag VCCIO up with it as it crosses through the VCCIO value. (Note: If the VCCIO supply is capable of sinking current, as well as the more usual sourcing capability, this behavior is eliminated. However, the amount of current that the supply needs to sink is unknown and is likely to be in the hundreds of milliamps range).

Power-Down Requirements

To prevent high power supply and input pin currents, power must be removed monotonically from either VCC or VCCAUX (and must reach the power-down trip point of 0.5V for VCC, 0.95V for VCCAUX) before power is removed monotonically from VCC12, any of the VCCIOs, or VCCJ. Note that VCC12 can be removed at the same time as VCC, but it cannot be removed earlier. In many applications, VCC and VCC12 will be sourced from the same power supply and so will be removed together. For systems where disturbance of the user pins is a don't care condition, the power supplies can be removed in any order as long as they power down monotonically within 200ms of each other.

Additionally, if any banks have VCCIO=3.3V nominal (potentially banks 1, 4, 5) then VCCIO for those banks must not be lower than VCCAUX during power-down. The normal variation in ramp-up times of power supplies and voltage regulators is not a concern here.

Note: The SERDES power supplies are NOT included in these requirements and have no specific sequencing requirements. However, when using the SERDES with VDDIB or VDDOB that is greater than 1.2V (1.5V nominal for example), the SERDES should not be left in a steady state condition with the 1.5V power applied and the 1.2V power not applied. Both the 1.2V and 1.5V power should be applied to the SERDES at nominally the same time. The normal variation in the ramp-up times of power supplies and voltage regulators is not a concern here.

SERDES Power Supply Sequencing Requirements

When using the SERDES with 1.5V VDDIB or VDDOB supplies, the SERDES should not be left in a steady state condition with the 1.5V power applied and the 1.2V power not applied. Both the 1.2V and the 1.5V power should be applied to the SERDES at nominally the same time. The normal variation in ramp-up times of power supplies and voltage regulators is not a concern.

Additional Requirement for SERDES Power Supply

All VCC12 pins need to be connected on all devices independent of functionality used on the device. This analog supply is used by both the RX and TX portions of the SERDES and is used to control the core SERDES logic regardless of the SERDES being used in the design. VDDIB and VDDOB are used as supplies for the terminations on the CML input and output buffers. If a particular channel is not used, these can be UNCONNECTED (floating).

PURESPEED I/O Recommended Operating Conditions

Standard	V _{CCIO} (V)			V _{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVC MOS 33	3.135	3.3	3.465	—	—	—
LVC MOS 25	2.375	2.5	2.625	—	—	—
LVC MOS 18	1.71	1.8	1.89	—	—	—
LVC MOS 15	1.425	1.5	1.575	—	—	—
LVC MOS 12	1.14	1.2	1.26	—	—	—
LV TTL	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
PCIX33	3.135	3.3	3.465	—	—	—
PCIX15	1.425	1.5	1.575	0.49V _{CCIO}	0.5V _{CCIO}	0.51V _{CCIO}
AGP1X33	3.135	3.3	3.465	—	—	—
AGP2X33	3.135	3.3	3.465	0.39V _{CCIO}	0.4V _{CCIO}	0.41V _{CCIO}
SSTL18_I, II ³	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II ³	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II ³	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I, II ³	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15_III ^{1,3} and IV ^{1,3}	1.425	1.5	1.575	0.68	0.9	0.9
HSTL 18_I ³ , II ³	1.71	1.8	1.89	0.816	0.9	1.08
HSTL 18_III ^{1,3} , IV ^{1,3}	1.71	1.8	1.89	0.816	1.08	1.08
GTL12 ^{1,3} , GTLPLUS15 ^{1,3}	—	—	—	0.882	1.0	1.122
LVDS	—	—	—	—	—	—
Mini-LVDS	—	—	—	—	—	—
RSDS	—	—	—	—	—	—
LVPECL33 (outputs) ²	3.135	3.3	3.465	—	—	—
LVPECL33 (inputs) ^{2,4}	—	≤ 2.5	—	—	—	—
BLVDS25 ^{2,3}	2.375	2.5	2.625	—	—	—
MLVDS25 ^{2,3}	2.375	2.5	2.625	—	—	—
SSTL18D_I ³ , II ³	1.71	1.8	1.89	—	—	—
SSTL25D_I ³ , II ³	2.375	2.5	2.625	—	—	—
SSTL33D_I ³ , II ³	3.135	3.3	3.465	—	—	—
HSTL15D_I ³ , II ³	1.425	1.5	1.575	—	—	—
HSTL18D_I ³ , II ³	1.71	1.8	1.89	—	—	—

1. Input only.

2. Inputs on chip. Outputs are implemented with the addition of external resistors.

3. Input for this standard does not depend on the value of V_{CCIO}.

4. Inputs for this standard cannot be in 3.3V VCCIO banks (≤ 2.5V only).

LFSC/M15 Logic Signal Connections: 256 fpBGA^{1,2}

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
E4	A_VDDAX25_L	-	
B1	A_REFCLKP_L	-	
C1	A_REFCLKN_L	-	
D2	RESP_ULC	-	
F5	RESETN	1	
D1	DONE	1	
E1	INITN	1	
E2	M0	1	
E3	M1	1	
E5	M2	1	
E6	M3	1	
F2	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
F1	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
F3	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
G1	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
G4	PL18D	7	VREF2_7
H3	PL22A	7	
H2	PL22B	7	
H5	PL22C	7	VREF1_7
G5	PL22D	7	DIFFR_7
H1	PL23A	7	PCLKT7_1
J1	PL23B	7	PCLKC7_1
J2	PL24A	7	PCLKT7_0
J3	PL24B	7	PCLKC7_0
H4	PL24C	7	PCLKT7_2
H6	PL24D	7	PCLKC7_2
J4	PL26A	6	PCLKT6_0
K5	PL26B	6	PCLKC6_0
J5	PL26C	6	PCLKT6_1
J6	PL26D	6	PCLKC6_1
K1	PL28A	6	
L1	PL28B	6	
L4	PL28C	6	PCLKT6_2
K4	PL28D	6	PCLKC6_2
L2	PL31C	6	VREF1_6
L3	PL35A	6	
M3	PL35B	6	
M2	PL35D	6	DIFFR_6
M1	PL37A	6	
N1	PL37B	6	
P2	PL41D	6	VREF2_6
M5	PL43A	6	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AK14	PB25A	5		PB35A	5	
AK15	PB25B	5		PB35B	5	
AK16	PB27A	4		PB37A	4	
AK17	PB27B	4		PB37B	4	
AJ16	PB28A	4		PB38A	4	
AJ17	PB28B	4		PB38B	4	
AE16	PB28C	4		PB38C	4	
AH16	PB29A	4		PB39A	4	
AG16	PB29B	4		PB39B	4	
AK18	PB31A	4		PB41A	4	
AK19	PB31B	4		PB41B	4	
AH17	PB32A	4		PB42A	4	
AH18	PB32B	4		PB42B	4	
AG17	PB32D	4		PB42D	4	
AJ18	PB33A	4		PB43A	4	
AJ19	PB33B	4		PB43B	4	
AK20	PB35A	4	PCLKT4_2	PB46A	4	PCLKT4_2
AK21	PB35B	4	PCLKC4_2	PB46B	4	PCLKC4_2
AF18	PB36A	4	PCLKT4_1	PB47A	4	PCLKT4_1
AG18	PB36B	4	PCLKC4_1	PB47B	4	PCLKC4_1
AJ20	PB37A	4	PCLKT4_0	PB49A	4	PCLKT4_0
AJ21	PB37B	4	PCLKC4_0	PB49B	4	PCLKC4_0
AG19	PB37C	4	VREF2_4	PB49C	4	VREF2_4
AK22	PB39A	4	PCLKT4_5	PB51A	4	PCLKT4_5
AK23	PB39B	4	PCLKC4_5	PB51B	4	PCLKC4_5
AH19	PB39C	4		PB51C	4	
AK24	PB40A	4	PCLKT4_3	PB52A	4	PCLKT4_3
AK25	PB40B	4	PCLKC4_3	PB52B	4	PCLKC4_3
AE19	PB40C	4	PCLKT4_4	PB52C	4	PCLKT4_4
AE20	PB40D	4	PCLKC4_4	PB52D	4	PCLKC4_4
AE21	PB41A	4		PB53A	4	
AF21	PB41B	4		PB53B	4	
AG21	PB43A	4		PB55A	4	
AG22	PB43B	4		PB55B	4	
AH22	PB44A	4		PB56A	4	
AH23	PB44B	4		PB56B	4	
AH21	PB44C	4		PB56C	4	
AK28	PB45A	4		PB60A	4	
AK29	PB45B	4		PB60B	4	
AE22	PB45C	4		PB60C	4	
AJ28	PB47A	4		PB67A	4	
AH28	PB47B	4		PB67B	4	
AE24	PB47C	4	VREF1_4	PB67C	4	VREF1_4
AE25	PB47D	4		PB67D	4	
AJ29	PB48A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB68A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P22	VCCIO2	-		VCCIO2	-	
R22	VCCIO2	-		VCCIO2	-	
AA23	VCCIO3	-		VCCIO3	-	
AA24	VCCIO3	-		VCCIO3	-	
AB23	VCCIO3	-		VCCIO3	-	
AB24	VCCIO3	-		VCCIO3	-	
T22	VCCIO3	-		VCCIO3	-	
U22	VCCIO3	-		VCCIO3	-	
V22	VCCIO3	-		VCCIO3	-	
W22	VCCIO3	-		VCCIO3	-	
Y22	VCCIO3	-		VCCIO3	-	
Y23	VCCIO3	-		VCCIO3	-	
Y24	VCCIO3	-		VCCIO3	-	
AB16	VCCIO4	-		VCCIO4	-	
AB17	VCCIO4	-		VCCIO4	-	
AB18	VCCIO4	-		VCCIO4	-	
AB19	VCCIO4	-		VCCIO4	-	
AB20	VCCIO4	-		VCCIO4	-	
AC20	VCCIO4	-		VCCIO4	-	
AC21	VCCIO4	-		VCCIO4	-	
AC22	VCCIO4	-		VCCIO4	-	
AD20	VCCIO4	-		VCCIO4	-	
AD21	VCCIO4	-		VCCIO4	-	
AD22	VCCIO4	-		VCCIO4	-	
AB11	VCCIO5	-		VCCIO5	-	
AB12	VCCIO5	-		VCCIO5	-	
AB13	VCCIO5	-		VCCIO5	-	
AB14	VCCIO5	-		VCCIO5	-	
AB15	VCCIO5	-		VCCIO5	-	
AC10	VCCIO5	-		VCCIO5	-	
AC11	VCCIO5	-		VCCIO5	-	
AC9	VCCIO5	-		VCCIO5	-	
AD10	VCCIO5	-		VCCIO5	-	
AD11	VCCIO5	-		VCCIO5	-	
AD9	VCCIO5	-		VCCIO5	-	
AA7	VCCIO6	-		VCCIO6	-	
AA8	VCCIO6	-		VCCIO6	-	
AB7	VCCIO6	-		VCCIO6	-	
AB8	VCCIO6	-		VCCIO6	-	
T9	VCCIO6	-		VCCIO6	-	
U9	VCCIO6	-		VCCIO6	-	
V9	VCCIO6	-		VCCIO6	-	
W9	VCCIO6	-		VCCIO6	-	
Y7	VCCIO6	-		VCCIO6	-	
Y8	VCCIO6	-		VCCIO6	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
H1	PR25B	2		PR23B	2	
H2	PR25A	2		PR23A	2	
N8	PR22D	2		PR25D	2	
M8	PR22C	2		PR25C	2	
H4	PR22B	2		PR25B	2	
J4	PR22A	2		PR25A	2	
G1	PR21B	2		PR22B	2	
G2	PR21A	2		PR22A	2	
L7	PR20D	2		PR21D	2	
L8	PR20C	2		PR21C	2	
F2	PR20B	2		PR21B	2	
F1	PR20A	2		PR21A	2	
K5	PR18D	2	VREF2_2	PR18D	2	VREF2_2
J5	PR18C	2		PR18C	2	
E2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
E1	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
N10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
M10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
D2	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
D1	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
K6	PR16D	2		PR16D	2	
K7	PR16C	2		PR16C	2	
J8	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
K8	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
J10	VCCJ	-		VCCJ	-	
J9	TDO	-	TDO	TDO	-	TDO
K9	TMS	-		TMS	-	
J12	TCK	-		TCK	-	
J13	TDI	-		TDI	-	
K12	PROGRAMN	1		PROGRAMN	1	
K13	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
K10	CCLK	1		CCLK	1	
F5	RESP_URC	-		RESP_URC	-	
B5	VCC12	-		VCC12	-	
D5	A_REFCLKN_R	-		A_REFCLKN_R	-	
C5	A_REFCLKP_R	-		A_REFCLKP_R	-	
B2	A_VDDIB0_R	-		A_VDDIB0_R	-	
C1	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P
C2	A_HDINN0_R	-	PCS 3E0 CH 0 IN N	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
A3	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P
D3	A_VDDOB0_R	-		A_VDDOB0_R	-	
B3	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N
D4	A_VDDOB1_R	-		A_VDDOB1_R	-	
B4	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N
A4	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P
H5	A_HDINN1_R	-	PCS 3E0 CH 1 IN N	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
G5	A_HDINP1_R	-	PCS 3E0 CH 1 IN P	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
F4	A_VDDIB1_R	-		A_VDDIB1_R	-	
H6	A_VDDIB2_R	-		A_VDDIB2_R	-	
F6	A_HDINP2_R	-	PCS 3E0 CH 2 IN P	A_HDINP2_R	-	PCS 3E0 CH 2 IN P

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
E22	VCC12	-		VCC12	-	
E21	VCC12	-		VCC12	-	
E3	VCC12	-		VCC12	-	
E4	VCC12	-		VCC12	-	
E6	VCC12	-		VCC12	-	
E7	VCC12	-		VCC12	-	
E8	VCC12	-		VCC12	-	
E9	VCC12	-		VCC12	-	
E11	VCC12	-		VCC12	-	
E12	VCC12	-		VCC12	-	
A23	GND	-		GND	-	
A31	GND	-		GND	-	
AA13	GND	-		GND	-	
AA15	GND	-		GND	-	
AA18	GND	-		GND	-	
AA20	GND	-		GND	-	
AA26	GND	-		GND	-	
AA6	GND	-		GND	-	
AB10	GND	-		GND	-	
AB24	GND	-		GND	-	
AC14	GND	-		GND	-	
AC22	GND	-		GND	-	
AC29	GND	-		GND	-	
AC3	GND	-		GND	-	
AD11	GND	-		GND	-	
AD19	GND	-		GND	-	
AD27	GND	-		GND	-	
AD7	GND	-		GND	-	
AF12	GND	-		GND	-	
AF18	GND	-		GND	-	
AF24	GND	-		GND	-	
AF30	GND	-		GND	-	
AF4	GND	-		GND	-	
AG15	GND	-		GND	-	
AG21	GND	-		GND	-	
AG9	GND	-		GND	-	
AJ10	GND	-		GND	-	
AJ16	GND	-		GND	-	
AJ20	GND	-		GND	-	
AJ26	GND	-		GND	-	
AJ29	GND	-		GND	-	
AJ4	GND	-		GND	-	
AK13	GND	-		GND	-	
AK17	GND	-		GND	-	
AK23	GND	-		GND	-	
AK7	GND	-		GND	-	
AL1	GND	-		GND	-	
AL32	GND	-		GND	-	
AM2	GND	-		GND	-	
AM31	GND	-		GND	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P17	VCC	-		VCC	-	
P19	VCC	-		VCC	-	
R13	VCC	-		VCC	-	
R15	VCC	-		VCC	-	
R18	VCC	-		VCC	-	
R20	VCC	-		VCC	-	
T13	VCC	-		VCC	-	
T14	VCC	-		VCC	-	
T16	VCC	-		VCC	-	
T17	VCC	-		VCC	-	
T19	VCC	-		VCC	-	
T20	VCC	-		VCC	-	
U13	VCC	-		VCC	-	
U14	VCC	-		VCC	-	
U16	VCC	-		VCC	-	
U17	VCC	-		VCC	-	
U19	VCC	-		VCC	-	
U20	VCC	-		VCC	-	
V13	VCC	-		VCC	-	
V15	VCC	-		VCC	-	
V18	VCC	-		VCC	-	
V20	VCC	-		VCC	-	
W14	VCC	-		VCC	-	
W16	VCC	-		VCC	-	
W17	VCC	-		VCC	-	
W19	VCC	-		VCC	-	
Y13	VCC	-		VCC	-	
Y15	VCC	-		VCC	-	
Y16	VCC	-		VCC	-	
Y17	VCC	-		VCC	-	
Y18	VCC	-		VCC	-	
Y20	VCC	-		VCC	-	
C17	VCCIO1	-		VCCIO1	-	
D16	VCCIO1	-		VCCIO1	-	
F15	VCCIO1	-		VCCIO1	-	
F24	VCCIO1	-		VCCIO1	-	
G18	VCCIO1	-		VCCIO1	-	
G9	VCCIO1	-		VCCIO1	-	
J11	VCCIO1	-		VCCIO1	-	
J19	VCCIO1	-		VCCIO1	-	
K14	VCCIO1	-		VCCIO1	-	
K22	VCCIO1	-		VCCIO1	-	
G4	VCCIO2	-		VCCIO2	-	
J7	VCCIO2	-		VCCIO2	-	
K3	VCCIO2	-		VCCIO2	-	
L10	VCCIO2	-		VCCIO2	-	
M6	VCCIO2	-		VCCIO2	-	
N4	VCCIO2	-		VCCIO2	-	
P9	VCCIO2	-		VCCIO2	-	
R7	VCCIO2	-		VCCIO2	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AL11	GND	-		GND	-	
AL17	GND	-		GND	-	
AL21	GND	-		GND	-	
AL27	GND	-		GND	-	
AL5	GND	-		GND	-	
AM14	GND	-		GND	-	
AM18	GND	-		GND	-	
AM24	GND	-		GND	-	
AM30	GND	-		GND	-	
AM8	GND	-		GND	-	
AN1	GND	-		GND	-	
AN34	GND	-		GND	-	
AP2	GND	-		GND	-	
AP33	GND	-		GND	-	
B1	GND	-		GND	-	
B34	GND	-		GND	-	
C11	GND	-		GND	-	
C12	GND	-		GND	-	
C13	GND	-		GND	-	
C14	GND	-		GND	-	
C17	GND	-		GND	-	
C21	GND	-		GND	-	
C22	GND	-		GND	-	
C23	GND	-		GND	-	
C24	GND	-		GND	-	
C26	GND	-		GND	-	
C27	GND	-		GND	-	
C30	GND	-		GND	-	
C31	GND	-		GND	-	
C4	GND	-		GND	-	
C5	GND	-		GND	-	
C8	GND	-		GND	-	
C9	GND	-		GND	-	
D18	GND	-		GND	-	
E32	GND	-		GND	-	
E4	GND	-		GND	-	
F19	GND	-		GND	-	
G16	GND	-		GND	-	
G29	GND	-		GND	-	
G7	GND	-		GND	-	
H3	GND	-		GND	-	
H31	GND	-		GND	-	
J10	GND	-		GND	-	
J15	GND	-		GND	-	
J26	GND	-		GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2}

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G34	A_REFCLKP_L	-		A_REFCLKP_L	-	
H34	A_REFCLKN_L	-		A_REFCLKN_L	-	
N30	VCC12	-		VCC12	-	
H33	RESP_ULC	-		RESP_ULC	-	
P25	RESETN	1		RESETN	1	
P26	TSALLN	1		TSALLN	1	
P31	DONE	1		DONE	1	
P23	INITN	1		INITN	1	
P30	M0	1		M0	1	
P22	M1	1		M1	1	
P24	M2	1		M2	1	
R22	M3	1		M3	1	
J37	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
J38	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
P32	PL16C	7		PL15C	7	
R32	PL16D	7		PL15D	7	
G40	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
H40	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N33	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P33	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
G41	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
H41	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
T29	PL18C	7		PL18C	7	
U29	PL18D	7	VREF2_7	PL18D	7	VREF2_7
G42	PL20A	7		PL19A	7	
H42	PL20B	7		PL19B	7	
M34	PL20C	7		PL19C	7	
M35	PL20D	7		PL19D	7	
K37	PL21A	7		PL26A	7	
L37	PL21B	7		PL26B	7	
N34	PL21C	7		PL26C	7	
P34	PL21D	7		PL26D	7	
K38	PL22A	7		PL30A	7	
L38	PL22B	7		PL30B	7	
T33	PL22C	7		PL30C	7	
R33	PL22D	7		PL30D	7	
J41	PL24A	7		PL34A	7	
K41	PL24B	7		PL34B	7	
U31	PL24C	7		PL34C	7	
V31	PL24D	7		PL34D	7	
K42	PL25A	7		PL38A	7	
J42	PL25B	7		PL38B	7	
J36	PL25C	7		PL38C	7	
K36	PL25D	7		PL38D	7	
N38	PL26A	7		PL40A	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
BA19	PB73A	4		PB87A	4	
BA18	PB73B	4		PB87B	4	
AU19	PB73C	4		PB87C	4	
AU18	PB73D	4		PB87D	4	
AV19	PB74A	4	PCLKT4_2	PB89A	4	PCLKT4_2
AV18	PB74B	4	PCLKC4_2	PB89B	4	PCLKC4_2
AN19	PB74C	4	PCLKT4_7	PB89C	4	PCLKT4_7
AP19	PB74D	4	PCLKC4_7	PB89D	4	PCLKC4_7
BB17	PB75A	4	PCLKT4_1	PB90A	4	PCLKT4_1
BB16	PB75B	4	PCLKC4_1	PB90B	4	PCLKC4_1
AT19	PB75C	4	PCLKT4_6	PB90C	4	PCLKT4_6
AT18	PB75D	4	PCLKC4_6	PB90D	4	PCLKC4_6
BA17	PB77A	4	PCLKT4_0	PB91A	4	PCLKT4_0
BA16	PB77B	4	PCLKC4_0	PB91B	4	PCLKC4_0
AR19	PB77C	4	VREF2_4	PB91C	4	VREF2_4
AR18	PB77D	4		PB91D	4	
AY17	PB79A	4	PCLKT4_5	PB93A	4	PCLKT4_5
AY16	PB79B	4	PCLKC4_5	PB93B	4	PCLKC4_5
AN18	PB79C	4		PB93C	4	
AP18	PB79D	4		PB93D	4	
AW17	PB80A	4	PCLKT4_3	PB94A	4	PCLKT4_3
AW16	PB80B	4	PCLKC4_3	PB94B	4	PCLKC4_3
AU17	PB80C	4	PCLKT4_4	PB94C	4	PCLKT4_4
AU16	PB80D	4	PCLKC4_4	PB94D	4	PCLKC4_4
AV17	PB81A	4		PB95A	4	
AV16	PB81B	4		PB95B	4	
AL18	PB81C	4		PB95C	4	
AM18	PB81D	4		PB95D	4	
BB15	PB83A	4		PB97A	4	
BB14	PB83B	4		PB97B	4	
AP17	PB83C	4		PB97C	4	
AN17	PB83D	4		PB97D	4	
BA15	PB84A	4		PB98A	4	
BA14	PB84B	4		PB98B	4	
AT16	PB84C	4		PB98C	4	
AT15	PB84D	4		PB98D	4	
AV15	PB85A	4		PB99A	4	
AV14	PB85B	4		PB99B	4	
AR16	PB85C	4		PB99C	4	
AR15	PB85D	4		PB99D	4	
AY14	PB87A	4		PB101A	4	
AY13	PB87B	4		PB101B	4	
AU15	PB87C	4		PB101C	4	
AU14	PB87D	4		PB101D	4	
BB13	PB88A	4		PB102A	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AU9	PB103C	4		PB117C	4	
AU8	PB103D	4		PB117D	4	
AY8	PB104A	4		PB118A	4	
AY7	PB104B	4		PB118B	4	
AU7	PB104C	4		PB118C	4	
AU6	PB104D	4		PB118D	4	
BA7	PB105A	4		PB119A	4	
BA6	PB105B	4		PB119B	4	
AN13	PB105C	4		PB119C	4	
AN12	PB105D	4		PB119D	4	
AV9	PB107A	4		PB121A	4	
AV8	PB107B	4		PB121B	4	
AT10	PB107C	4		PB121C	4	
AT9	PB107D	4		PB121D	4	
AW8	PB108A	4		PB122A	4	
AW7	PB108B	4		PB122B	4	
AP11	PB108C	4		PB122C	4	
AP10	PB108D	4		PB122D	4	
BB5	PB109A	4		PB123A	4	
BB4	PB109B	4		PB123B	4	
AR10	PB109C	4		PB123C	4	
AR9	PB109D	4		PB123D	4	
BA5	PB111A	4		PB125A	4	
BA4	PB111B	4		PB125B	4	
AT7	PB111C	4		PB125C	4	
AT6	PB111D	4		PB125D	4	
BB3	PB112A	4		PB126A	4	
BA3	PB112B	4		PB126B	4	
AM14	PB112C	4		PB126C	4	
AL14	PB112D	4		PB126D	4	
AY5	PB113A	4		PB127A	4	
AY4	PB113B	4		PB127B	4	
AN11	PB113C	4		PB127C	4	
AN10	PB113D	4		PB127D	4	
AV7	PB115A	4		PB129A	4	
AV6	PB115B	4		PB129B	4	
AM12	PB115C	4		PB129C	4	
AM11	PB115D	4		PB129D	4	
AW5	PB116A	4		PB130A	4	
AW4	PB116B	4		PB130B	4	
AT5	PB116C	4		PB130C	4	
AT4	PB116D	4		PB130D	4	
AY2	PB117A	4		PB131A	4	
BA2	PB117B	4		PB131B	4	
AP9	PB117C	4		PB131C	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C3	GND	-		GND	-	
C30	GND	-		GND	-	
C33	GND	-		GND	-	
C35	GND	-		GND	-	
C36	GND	-		GND	-	
C39	GND	-		GND	-	
C4	GND	-		GND	-	
C40	GND	-		GND	-	
C7	GND	-		GND	-	
C8	GND	-		GND	-	
D15	GND	-		GND	-	
D21	GND	-		GND	-	
D25	GND	-		GND	-	
D31	GND	-		GND	-	
F4	GND	-		GND	-	
F40	GND	-		GND	-	
G11	GND	-		GND	-	
G17	GND	-		GND	-	
G26	GND	-		GND	-	
G32	GND	-		GND	-	
H14	GND	-		GND	-	
H20	GND	-		GND	-	
H23	GND	-		GND	-	
H29	GND	-		GND	-	
H35	GND	-		GND	-	
H8	GND	-		GND	-	
J3	GND	-		GND	-	
J39	GND	-		GND	-	
L16	GND	-		GND	-	
L27	GND	-		GND	-	
L36	GND	-		GND	-	
L7	GND	-		GND	-	
M19	GND	-		GND	-	
M24	GND	-		GND	-	
M4	GND	-		GND	-	
M40	GND	-		GND	-	
N12	GND	-		GND	-	
N31	GND	-		GND	-	
P35	GND	-		GND	-	
P8	GND	-		GND	-	
R15	GND	-		GND	-	
R28	GND	-		GND	-	
R3	GND	-		GND	-	
R39	GND	-		GND	-	
T11	GND	-		GND	-	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-7FCN1152C ¹	-7	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-6FCN1152C ¹	-6	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-5FCN1152C ¹	-5	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-7FFN1152C	-7	Lead-Free Organic fcBGA	1152	COM	80.1
LFSC3GA80E-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	80.1
LFSC3GA80E-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	80.1
LFSC3GA80E-7FCN1704C ¹	-7	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-6FCN1704C ¹	-6	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-5FCN1704C ¹	-5	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-7FFN1704C	-7	Lead-Free Organic fcBGA	1704	COM	80.1
LFSC3GA80E-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	80.1
LFSC3GA80E-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-7FCN1152C ¹	-7	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FCN1152C ¹	-6	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FCN1152C ¹	-5	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FFN1152C	-7	Lead-Free Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FCN1704C ¹	-7	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FCN1704C ¹	-6	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FCN1704C ¹	-5	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-7FFN1704C	-7	Lead-Free Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FCN1152C ¹	-6	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-5FCN1152C ¹	-5	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	115.2
LFSC3GA115E-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	115.2
LFSC3GA115E-6FCN1704C ¹	-6	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-5FCN1704C ¹	-5	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	115.2
LFSC3GA115E-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FCN1152C ¹	-6	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FCN1152C ¹	-5	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FCN1704C ¹	-6	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FCN1704C ¹	-5	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Industrial

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-6FN256I	-6	Lead-Free fpBGA	256	IND	15.2
LFSC3GA15E-5FN256I	-5	Lead-Free fpBGA	256	IND	15.2
LFSC3GA15E-6FN900I	-6	Lead-Free fpBGA	900	IND	15.2
LFSC3GA15E-5FN900I	-5	Lead-Free fpBGA	900	IND	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-6FN256I	-6	Lead-Free fpBGA	256	IND	15.2
LFSCM3GA15EP1-5FN256I	-5	Lead-Free fpBGA	256	IND	15.2
LFSCM3GA15EP1-6FN900I	-6	Lead-Free fpBGA	900	IND	15.2
LFSCM3GA15EP1-5FN900I	-5	Lead-Free fpBGA	900	IND	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-6FN900I	-6	Lead-Free fpBGA	900	IND	25.4
LFSC3GA25E-5FN900I	-5	Lead-Free fpBGA	900	IND	25.4
LFSC3GA25E-6FFN1020I ¹	-6	Lead-Free Organic fcBGA	1020	IND	25.4
LFSC3GA25E-5FFN1020I ¹	-5	Lead-Free Organic fcBGA	1020	IND	25.4
LFSC3GA25E-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4
LFSC3GA25E-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-6FN900I	-6	Lead-Free fpBGA	900	IND	25.4
LFSCM3GA25EP1-5FN900I	-5	Lead-Free fpBGA	900	IND	25.4
LFSCM3GA25EP1-6FFN1020I ¹	-6	Lead-Free Organic fcBGA	1020	IND	25.4
LFSCM3GA25EP1-5FFN1020I ¹	-5	Lead-Free Organic fcBGA	1020	IND	25.4
LFSCM3GA25EP1-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4
LFSCM3GA25EP1-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA40E-6FFN1020I ¹	-6	Lead-Free Organic fcBGA	1020	IND	40.4
LFSC3GA40E-5FFN1020I ¹	-5	Lead-Free Organic fcBGA	1020	IND	40.4
LFSC3GA40E-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSC3GA40E-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSC3GA40E-6FCN1152I ²	-6	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSC3GA40E-5FCN1152I ²	-5	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSC3GA40E-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	40.4
LFSC3GA40E-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

2. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Date	Version	Section	Change Summary
February 2006	01.0	—	Initial release.
March 2006	01.1	Introduction	SC25 1020 I/O count changed to 476.
		Architecture	Changed ROM 16X4 to ROM 16X2.
			Changed “X2 or X4” to “DIV2 or DIV4”.
			Added Global Set/Reset Section.
		DC and Switching Characteristics	Added notes 5 and 6 to Recommended Operating Conditions table.
			Added Power Supply Ramp Rates table.
			Removed -5 and -6 speed grades from Typical Building Block Performance table.
			Added Input Delay Timing table.
			Added Synchronous GSR Timing table.
		Pinout Information	Expanded PROBE_VCC and PROBE_GND description.
			Removed A-RXREFCLKP_[L/R] from Signal Description table.
			Added RESP_[ULC/URC] to Signal Description table.
			Added notes 1 and 2 to Signal Description table.
			Changed number of NCs to 28.
			Changed number of SERDES (signal + power supply) to 74.
			Removed RESP balls from NC list (B2, C2, B29, C29).
			Added note to VTT table.
			Changed RxRefclk (B2 and C2) to NC.
			Added RESP_ULC.
			Added RESP_URC.
			Changed RxRefclk (B29 and C29) to NC.
June 2006	01.2	Introduction	Changed SERDES min bandwidth from 622 Mbps to 600 Mbps.
			Changed max SERDES bandwidth from 3.4 Gbps to 3.8 Gbps.
			Corrected number of package I/Os for the SC80 and SC115 1704 pin packages.
			Updated speed performance for typical functions with ispLEVER 6.0 values.
		Architecture	Changed “When these pins are not used they should be left unconnected.” with “Unused VTT pins should be connected to GND if the internal or external VCMT function is not used in the bank. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.”
			Added “SERDES Power Supply Sequencing Requirements” section.
			Changed total bandwidth per quad from 13.6 Gbps to 15.2 Gbps.
			Added the accuracy of the temperature-sensing diode to be typically +/- 10 °C. Also referred to a temperature-sensing diode application note for more information.
		DC and Switching Characteristics	Changed “CTAP” to “internal or external VCMT”.
			Changed VCC12 parameter to include VDDP, VDDTX and VDDRFX.
			Changed typical values to match ispLEVER 6.0 Power Calculator.