Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	28750
Number of Logic Elements/Cells	115000
Total RAM Bits	7987200
Number of I/O	660
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga115ep1-6ff1152i

DLLs and dynamic glitch free clock MUXs which are required in today's high end system designs. High-speed, high-bandwidth I/O make this family ideal for high-throughput systems.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeSC family of FPGA devices. Synthesis library support for LatticeSC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeSC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeSC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Innovative high-performance FPGA architecture, high-speed SERDES with PCS support, sysMEM embedded memory and high performance I/O are combined in the LatticeSC to provide excellent performance for today's leading edge systems designs. Table 1-3 details the performance of several common functions implemented within the LatticeSC.

Table1-3. Speed Performance for Typical Functions[1]

Functions	Performance (MHz)[2]
32-bit Address Decoder	539
64-bit Address Decoder	517
32:1 Multiplexer	779
64-bit Adder (ripple)	353
32x8 Distributed Single Port (SP) RAM	768
64-bit Counter (up or down counter, non-loadable)	369
True Dual-Port 1024x18 bits	372
FIFO Port A: x36 bits, B: x9 bits	375

1. For additional information, see Typical Building BLock Function Performance table in this data sheet.
2. Advance information (-7 speed grade).

PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR 16x2 x 4 DPR 16x2 x 2	ROM 16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR 16x4 x 2 DPR 16x4 x 1	ROM 16x2 x 4
LUT 6x2 or MUX 8x1 x 2	2-bit Counter x 4	SPR 16x8 x 1	ROM 16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM 16x8 x1

Routing

There are many resources provided in the LatticeSC devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

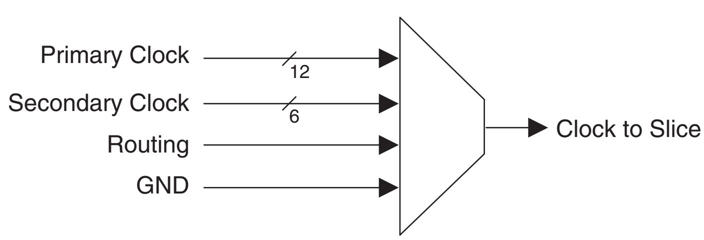
The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU) resources. The x1 and x2 connections provide fast and efficient connections in horizontal, vertical and diagonal directions. All connections are buffered to ensure high-speed operation even with long high-fanout connections.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Network

The LatticeSC devices have three distinct clock networks for use in distributing high-performance clocks within the device: primary clocks, secondary clocks and edge clocks. In addition to these dedicated clock networks, users are free to route clocks within the device using the general purpose routing. Figure 2-4 shows the clock resources available to each slice.

Figure 2-4. Slice Clock Selection



Note: GND is available to switch off the network.

Primary Clock Sources

LatticeSC devices have a wide variety of primary clock sources available. Primary clocks sources consists of the following:

- Primary clock input pins
- Edge clock input pins
- Two outputs per DLL

toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-9 illustrates the DCS Block diagram.

Figure 2-9. DCS Block Diagram

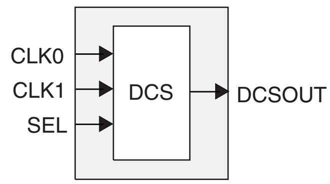
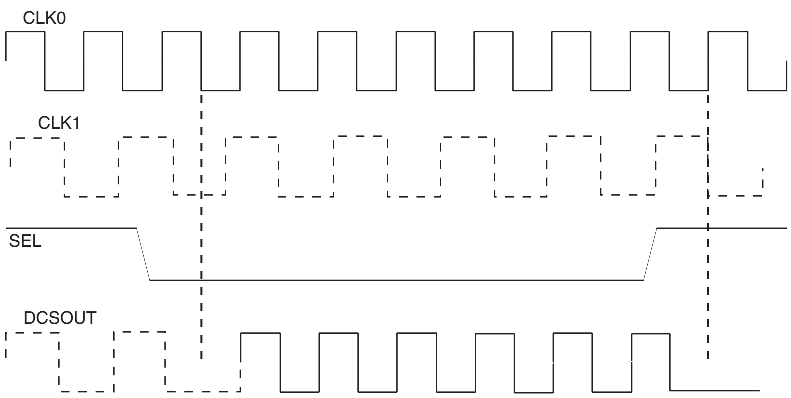


Figure 2-10 shows timing waveforms for one of the DCS operating modes. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

Figure 2-10. DCS Waveforms



Clock Boosting

There are programmable delays available in the clock signal paths in the PFU, PIC and EBR blocks. These allow setup and clock-to-output times to be traded to meet critical timing without slowing the system clock. If this feature is enabled then the design tool automatically uses these delays to improve timing performance.

Global Set/Reset

There is a global set/reset (GSR) network on the device that is distributed to all FFs, PLLs, DLLs and other blocks on the device. This GSR network can operate in two modes:

a) asynchronous - no clock is required to get into or out of the reset state.

b) synchronous - The global GSR net is synchronized to a user selected clock. In this mode it continues to be asynchronous to get into the reset state, but is synchronous to get out of the reset state. This allows all registers on the device to become operational in the same clock period. The synchronous GSR goes out of reset in two cycles from the clock edge where the setup time of the FF was met (not from the GSR being released).

sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider and two clock output dividers. The input divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal.

PCI Specification, Revision 2.2 requires the use of clamping diodes for 3.3V operation. For more information on the PCI interface, please refer to the PCI Specification, Revision 2.2.

Programmable Slew Rate Control

All output and bidirectional buffers have an optional programmable output slew rate control that can be configured for either low noise or high-speed performance. Each I/O pin has an individual slew rate control. This allows designers to specify slew rate control on a pin-by-pin basis. This slew rate control affects both the rising and falling edges.

Programmable Termination

Many of the I/O standards supported by the LatticeSC devices require termination at the transmitter, receiver or both. The SC devices provide the capability to implement many kinds of termination on-chip, minimizing stub lengths and hence improving performance. Utilizing this feature also has the benefit of reducing the number of discrete components required on the circuit board. The termination schemes can be split into two categories single-ended and differential.

Single Ended Termination

Single Ended Outputs: The SC devices support a number of different terminations for single ended outputs:

- Series
- Parallel to V_{CCIO} or GND
- Parallel to $V_{CCIO}/2$
- Parallel to $V_{CCIO}/2$ combined with series

Figure 2-27 shows the single ended output schemes that are supported. The nominal values of the termination resistors are shown in Table 2-10.

flexiPCS quads are not dedicated solely to industry standard protocols. Each quad (and each channel within a quad) can be programmed for many user defined data manipulation modes. For example, modes governing user-defined word alignment and multi-channel alignment can be programmed for non-standard protocol applications.

For more information on the functions and use of the flexiPCS, refer to the LatticeSC/M Family flexiPCS Data Sheet.

System Bus

Each LatticeSC device connects the FPGA elements with a standardized bus framework referred to as a System Bus. Multiple bus masters optimize system performance by sharing resources between different bus masters such as the MPI and configuration logic. The wide data bus configuration of 32 bits with 4-bit parity supports high-bandwidth, data intensive applications.

There are two types of interfaces on the System Bus, master and slave. A master interface has the ability to perform actions on the bus, such as writes and reads to and from a specific address. A slave interface responds to the actions of a master by accepting data and address on a write and providing data on a read. The System Bus has a memory map which describes each of the slave peripherals that is connected on the bus. Using the addresses listed in the memory map, a master interface can access each of the slave peripherals on the System Bus. Any and all peripherals on the System Bus can be used at the same time. Table 2-12 list all of the available user peripherals on the System Bus after device power-up.

Table 2-12. System Bus User Peripherals

Peripheral	Name	Interface Type
Micro Processor Interface	MPI	Master
User Master Interface	UMI	Master
User Slave Interface	USI	Slave
Serial Management Interface (PLL, DLL, User Logic)	SMI	Slave
Physical Coding Sublayer	PCS	Slave
Direct FPGA Access	DFA	Slave

The peripherals listed in Table 2-12 can be added when the System Bus module is created using Module IP/Manager (ispLEVER Module/IP Manager).

Figure 2-31 also lists the existing peripherals on the System Bus. The gray boxes are available only during configuration. Refer to Lattice technical note TN1080, LatticeSC sysCONFIG Usage Guide, for configuration options. The Status and Config box refers to internal System Bus registers. This document presents all the interfaces listed in Table 2-12 in detail to help the user utilize the desired functions of the System Bus.

LatticeSC/M Family Timing Adders (Continued)

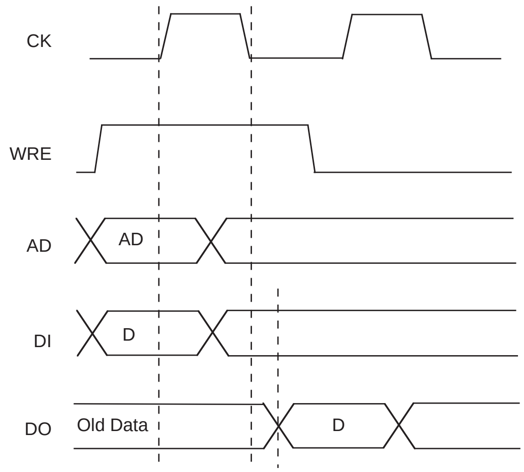
Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS18_12mA	LVCMOS 1.8 12mA drive	0.024	-0.106	0.019	-0.004	0.016	0.099	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive	0.074	-0.134	0.08	-0.022	0.088	0.089	ns
LVCMOS18_OD	LVCMOS 1.8 open drain	0.002	-0.206	0	-0.196	-0.002	-0.221	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive	-0.344	-0.164	-0.379	-0.186	-0.412	-0.209	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive	-0.125	-0.137	-0.145	-0.157	-0.164	-0.176	ns
LVCMOS15_12mA	LVCMOS 1.5 12mA drive	-0.027	-0.166	-0.043	-0.07	-0.059	0.026	ns
LVCMOS15_16mA	LVCMOS 1.5 16mA drive	0.025	-0.195	0.013	-0.089	0.003	0.017	ns
LVCMOS15_OD	LVCMOS 1.5 open drain	-0.047	-0.267	-0.067	-0.267	-0.087	-0.299	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive	-0.473	-0.293	-0.505	-0.317	-0.537	-0.34	ns
LVCMOS12_4mA	LVCMOS 1.2 4mA drive	-0.218	-0.239	-0.25	-0.271	-0.28	-0.303	ns
LVCMOS12_8mA	LVCMOS 1.2 8mA drive	-0.109	-0.269	-0.143	-0.181	-0.176	-0.093	ns
LVCMOS12_12mA	LVCMOS 1.2 12mA drive	-0.054	-0.3	-0.085	-0.203	-0.114	-0.106	ns
LVCMOS12_OD	LVCMOS 1.2 open drain	-0.126	-0.371	-0.166	-0.398	-0.204	-0.43	ns
PCI33	PCI	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX33	PCI-X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX15	PCI-X 1.5	0.208	0.227	0.233	0.312	0.259	0.398	ns
AGP1X33	AGP-1X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
AGP2X33	AGP-2X	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns

Timing Diagrams

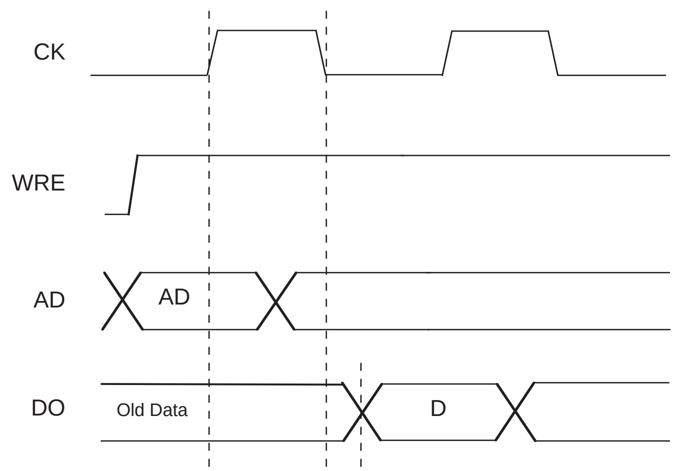
PFU Timing Diagrams

Figure 3-4. Slice Single/Dual Port Write Cycle Timing



Notes:
- Rising Edge for latching WREN, WAD and DATAIN.
- WREN must continue past falling edge clock.
- Data output occurs on negative edge.

Figure 3-5. Slice Single/Dual Port Read Cycle Timing



LatticeSC/M Family Data Sheet
Pinout Information

January 2008 **Data Sheet DS1004**

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PIC row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
VREF1_x, VREF2_x	—	The reference supply pins for I/O bank x. Any I/O pin in a bank can be assigned as a reference supply pin, but software defaults use designated pin.
NC	—	No connect. NC pins should not be connected to any active signals, VCC or GND.
Non-SERDES Power Supplies		
VCCIOx	—	VCCIO - The power supply pins for I/O bank x. Dedicated pins.
VCC12[1]	—	1.2V supply for configuration logic, PLLs and SERDES Rx, Tx and PLL. All VCC12 pins must be connected. As VCC12 supplies power for analog circuitry, VCC12 should be quiet and isolated from noisy digital board supplies.
VTT_x	—	Termination voltage for bank x. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. VCMT function is not used in the bank. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.
GND	—	GND - Ground. Dedicated pins. All grounds must be electrically connected at the board level.
VCC	—	VCC - The power supply pins for core logic. Dedicated pins (1.2V/ 1.0V).
VCCAUX	—	VCCAUX - Auxiliary power supply pin - powers all differential and referenced input buffers. Dedicated pins (2.5V).
VCCJ	—	VCCJ - The power supply pin for JTAG Test Access Port.
PROBE_VCC	—	VCC signal - Connected to internal VCC node. Can be used for feedback to control an external board power converter. Can be unconnected if not used.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
N3	PL27A	6		PL30A	6	
P3	PL27B	6		PL30B	6	
P4	PL27C	6	PCLKT6_3	PL30C	6	PCLKT6_3
P2	PL28A	6		PL31A	6	
R2	PL28B	6		PL31B	6	
T3	PL28C	6	PCLKT6_2	PL31C	6	PCLKT6_2
R3	PL28D	6	PCLKC6_2	PL31D	6	PCLKC6_2
P1	PL31A	6		PL34A	6	
R1	PL31B	6		PL34B	6	
R5	PL31C	6	VREF1_6	PL34C	6	VREF1_6
R4	PL31D	6		PL34D	6	
T2	PL32A	6		PL35A	6	
U2	PL32B	6		PL35B	6	
T1	PL33A	6		PL38A	6	
U1	PL33B	6		PL38B	6	
V1	PL35A	6		PL42A	6	
W1	PL35B	6		PL42B	6	
V6	PL35D	6	DIFFR_6	PL42D	6	DIFFR_6
V2	PL36A	6		PL43A	6	
W2	PL36B	6		PL43B	6	
Y1	PL37A	6		PL44A	6	
AA1	PL37B	6		PL44B	6	
AB1	PL39A	6		PL48A	6	
AC1	PL39B	6		PL48B	6	
Y5	PL40A	6		PL49A	6	
Y6	PL40B	6		PL49B	6	
AD2	PL41A	6		PL51A	6	
AE2	PL41B	6		PL51B	6	
AB5	PL41D	6	VREF2_6	PL51D	6	VREF2_6
AC3	PL43A	6		PL52A	6	
AD3	PL43B	6		PL52B	6	
AF1	PL44A	6		PL55A	6	
AG1	PL44B	6		PL55B	6	
AB6	PL44C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL55C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AC5	PL44D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL55D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AF2	PL45A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL57A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AG2	PL45B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL57B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AC6	PL45C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL57C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AC7	PL45D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL57D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AE4	XRES	-		XRES	-	
AG4	VCC12	-		VCC12	-	
AD5	TEMP	6		TEMP	6	
AF5	VCC12	-		VCC12	-	
AH1	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AJ1	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
R29	PR28B	3		PR31B	3	
P29	PR28A	3		PR31A	3	
P27	PR27C	3	PCLKT3_3	PR30C	3	PCLKT3_3
N29	PR27B	3		PR30B	3	
N28	PR27A	3		PR30A	3	
R25	PR26D	3	PCLKC3_1	PR29D	3	PCLKC3_1
R26	PR26C	3	PCLKT3_1	PR29C	3	PCLKT3_1
R28	PR26B	3	PCLKC3_0	PR29B	3	PCLKC3_0
P28	PR26A	3	PCLKT3_0	PR29A	3	PCLKT3_0
N27	PR24D	2	PCLKC2_2	PR27D	2	PCLKC2_2
P26	PR24C	2	PCLKT2_2	PR27C	2	PCLKT2_2
L30	PR24B	2	PCLKC2_0	PR27B	2	PCLKC2_0
K30	PR24A	2	PCLKT2_0	PR27A	2	PCLKT2_0
J30	PR23B	2	PCLKC2_1	PR26B	2	PCLKC2_1
H30	PR23A	2	PCLKT2_1	PR26A	2	PCLKT2_1
M26	PR22D	2	DIFFR_2	PR25D	2	DIFFR_2
M25	PR22C	2	VREF1_2	PR25C	2	VREF1_2
G29	PR22B	2		PR25B	2	
F29	PR22A	2		PR25A	2	
H28	PR19D	2		PR22D	2	
J28	PR19C	2		PR22C	2	
E30	PR19B	2		PR22B	2	
E29	PR19A	2		PR22A	2	
L26	PR18D	2	VREF2_2	PR18D	2	VREF2_2
L25	PR18C	2		PR18C	2	
F28	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
G28	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
K26	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
K25	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
D30	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
D29	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
G26	PR15D	2		PR16D	2	
H26	PR15C	2		PR16C	2	
E28	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
D28	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
J25	VCCJ	-		VCCJ	-	
H25	TDO	-	TDO	TDO	-	TDO
J26	TMS	-		TMS	-	
G25	TCK	-		TCK	-	
G24	TDI	-		TDI	-	
F26	PROGRAMN	1		PROGRAMN	1	
H24	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
F25	CCLK	1		CCLK	1	
D27	VCC12	-		VCC12	-	
E26	VCC12	-		VCC12	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AA21	VCCAUX	-		VCCAUX	-	
AA22	VCCAUX	-		VCCAUX	-	
AB11	VCCAUX	-		VCCAUX	-	
AB12	VCCAUX	-		VCCAUX	-	
AB15	VCCAUX	-		VCCAUX	-	
AB16	VCCAUX	-		VCCAUX	-	
AB17	VCCAUX	-		VCCAUX	-	
AB18	VCCAUX	-		VCCAUX	-	
AB21	VCCAUX	-		VCCAUX	-	
AB22	VCCAUX	-		VCCAUX	-	
L11	VCCAUX	-		VCCAUX	-	
L12	VCCAUX	-		VCCAUX	-	
L14	VCCAUX	-		VCCAUX	-	
L15	VCCAUX	-		VCCAUX	-	
L18	VCCAUX	-		VCCAUX	-	
L19	VCCAUX	-		VCCAUX	-	
L21	VCCAUX	-		VCCAUX	-	
L22	VCCAUX	-		VCCAUX	-	
M11	VCCAUX	-		VCCAUX	-	
M12	VCCAUX	-		VCCAUX	-	
M21	VCCAUX	-		VCCAUX	-	
M22	VCCAUX	-		VCCAUX	-	
P11	VCCAUX	-		VCCAUX	-	
P22	VCCAUX	-		VCCAUX	-	
R11	VCCAUX	-		VCCAUX	-	
R22	VCCAUX	-		VCCAUX	-	
V11	VCCAUX	-		VCCAUX	-	
V22	VCCAUX	-		VCCAUX	-	
W11	VCCAUX	-		VCCAUX	-	
W22	VCCAUX	-		VCCAUX	-	
N11	VTT_2	2		VTT_2	2	
R10	VTT_2	2		VTT_2	2	
T11	VTT_3	3		VTT_3	3	
U11	VTT_3	3		VTT_3	3	
Y11	VTT_3	3		VTT_3	3	
AB13	VTT_4	4		VTT_4	4	
AB14	VTT_4	4		VTT_4	4	
AC15	VTT_4	4		VTT_4	4	
AB19	VTT_5	5		VTT_5	5	
AB20	VTT_5	5		VTT_5	5	
AC18	VTT_5	5		VTT_5	5	
T22	VTT_6	6		VTT_6	6	
U22	VTT_6	6		VTT_6	6	
Y22	VTT_6	6		VTT_6	6	
N22	VTT_7	7		VTT_7	7	
R23	VTT_7	7		VTT_7	7	
M17	VCC12	-		VCC12	-	
M16	VCC12	-		VCC12	-	
T12	VCC12	-		VCC12	-	
T21	VCC12	-		VCC12	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH27	PB5C	5		PB5C	5	
AH26	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AN32	PB7A	5		PB7A	5	
AP32	PB7B	5		PB7B	5	
AF25	PB7C	5		PB7C	5	
AE25	PB7D	5		PB7D	5	
AN31	PB8A	5		PB9A	5	
AN30	PB8B	5		PB9B	5	
AK29	PB8C	5		PB9C	5	
AK28	PB8D	5		PB9D	5	
AP31	PB9A	5		PB11A	5	
AP30	PB9B	5		PB11B	5	
AD24	PB9C	5		PB11C	5	
AE24	PB9D	5		PB11D	5	
AM29	PB11A	5		PB13A	5	
AM28	PB11B	5		PB13B	5	
AJ27	PB11C	5		PB13C	5	
AJ26	PB11D	5		PB13D	5	
AP29	PB13A	5		PB15A	5	
AP28	PB13B	5		PB15B	5	
AK27	PB13C	5		PB15C	5	
AK26	PB13D	5		PB15D	5	
AN29	PB15A	5		PB17A	5	
AN28	PB15B	5		PB17B	5	
AG25	PB15C	5		PB17C	5	
AG24	PB15D	5		PB17D	5	
AL26	PB17A	5		PB19A	5	
AL25	PB17B	5		PB19B	5	
AG23	PB17C	5		PB19C	5	
AG22	PB17D	5		PB19D	5	
AN27	PB19A	5		PB21A	5	
AN26	PB19B	5		PB21B	5	
AF24	PB19C	5		PB21C	5	
AF23	PB19D	5		PB21D	5	
AP27	PB22A	5		PB24A	5	
AP26	PB22B	5		PB24B	5	
AK25	PB22C	5		PB24C	5	
AK24	PB22D	5		PB24D	5	
AN25	PB25A	5		PB27A	5	
AN24	PB25B	5		PB27B	5	
AE22	PB25C	5		PB27C	5	
AE21	PB25D	5		PB27D	5	
AM26	PB26A	5		PB29A	5	
AM25	PB26B	5		PB29B	5	
AF22	PB26C	5		PB29C	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

	LFSC/M40			LFSC/M80		
Ball Number	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AM17	VCCIO4	-		VCCIO4	-	
AM5	VCCIO4	-		VCCIO4	-	
AE20	VCCIO5	-		VCCIO5	-	
AE23	VCCIO5	-		VCCIO5	-	
AE26	VCCIO5	-		VCCIO5	-	
AH22	VCCIO5	-		VCCIO5	-	
AH28	VCCIO5	-		VCCIO5	-	
AJ19	VCCIO5	-		VCCIO5	-	
AJ25	VCCIO5	-		VCCIO5	-	
AL18	VCCIO5	-		VCCIO5	-	
AL24	VCCIO5	-		VCCIO5	-	
AL30	VCCIO5	-		VCCIO5	-	
AM21	VCCIO5	-		VCCIO5	-	
AM27	VCCIO5	-		VCCIO5	-	
AA31	VCCIO6	-		VCCIO6	-	
AB29	VCCIO6	-		VCCIO6	-	
AC24	VCCIO6	-		VCCIO6	-	
AD32	VCCIO6	-		VCCIO6	-	
AE28	VCCIO6	-		VCCIO6	-	
AG31	VCCIO6	-		VCCIO6	-	
AK32	VCCIO6	-		VCCIO6	-	
T29	VCCIO6	-		VCCIO6	-	
U31	VCCIO6	-		VCCIO6	-	
V32	VCCIO6	-		VCCIO6	-	
W28	VCCIO6	-		VCCIO6	-	
Y26	VCCIO6	-		VCCIO6	-	
E31	VCCIO7	-		VCCIO7	-	
G28	VCCIO7	-		VCCIO7	-	
H32	VCCIO7	-		VCCIO7	-	
K29	VCCIO7	-		VCCIO7	-	
L31	VCCIO7	-		VCCIO7	-	
M25	VCCIO7	-		VCCIO7	-	
N28	VCCIO7	-		VCCIO7	-	
P32	VCCIO7	-		VCCIO7	-	
R25	VCCIO7	-		VCCIO7	-	
J25	VCCIO1	-		VCCIO1	-	
N11	VTT_2	2		VTT_2	2	
R12	VTT_2	2		VTT_2	2	
T12	VTT_2	2		VTT_2	2	
AB11	VTT_3	3		VTT_3	3	
W12	VTT_3	3		VTT_3	3	
Y12	VTT_3	3		VTT_3	3	
AC15	VTT_4	4		VTT_4	4	
AC16	VTT_4	4		VTT_4	4	
AD13	VTT_4	4		VTT_4	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
F25	B_HDINN0_L	-	PCS 361 CH 0 IN N
E25	B_HDINP0_L	-	PCS 361 CH 0 IN P
D28	B_VDDIB0_L	-	
G25	VCC12	-	
D29	A_VDDIB3_L	-	
C25	VCC12	-	
A25	A_HDINP3_L	-	PCS 360 CH 3 IN P
B25	A_HDINN3_L	-	PCS 360 CH 3 IN N
A26	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
E27	VCC12	-	
B26	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
F26	A_VDDOB3_L	-	
B27	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
F27	A_VDDOB2_L	-	
A27	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
E28	VCC12	-	
B28	A_HDINN2_L	-	PCS 360 CH 2 IN N
A28	A_HDINP2_L	-	PCS 360 CH 2 IN P
D30	A_VDDIB2_L	-	
C28	VCC12	-	
D31	A_VDDIB1_L	-	
C29	VCC12	-	
A29	A_HDINP1_L	-	PCS 360 CH 1 IN P
B29	A_HDINN1_L	-	PCS 360 CH 1 IN N
A30	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
E29	VCC12	-	
B30	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
F28	A_VDDOB1_L	-	
B31	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
F29	A_VDDOB0_L	-	
A31	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
E30	VCC12	-	
B32	A_HDINN0_L	-	PCS 360 CH 0 IN N
A32	A_HDINP0_L	-	PCS 360 CH 0 IN P
D32	A_VDDIB0_L	-	
C32	VCC12	-	
E34	PL30A	7	
F34	PL30B	7	
F33	PL34A	7	
G33	PL34B	7	
K30	PL38A	7	
L30	PL38B	7	
G34	PL40A	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

	LFSC/M80			LFSC/M115		
Ball Number	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AE1	PR74A	3		PR88A	3	
AF12	PR73D	3		PR87D	3	
AE12	PR73C	3		PR87C	3	
AF2	PR73B	3		PR87B	3	
AE2	PR73A	3		PR87A	3	
AF11	PR72D	3		PR86D	3	
AE11	PR72C	3		PR86C	3	
AF5	PR72B	3		PR86B	3	
AE5	PR72A	3		PR86A	3	
AF10	PR69D	3		PR83D	3	
AE10	PR69C	3		PR83C	3	
AD1	PR69B	3		PR83B	3	
AC1	PR69A	3		PR83A	3	
AF9	PR68D	3		PR82D	3	
AE9	PR68C	3		PR82C	3	
AD2	PR68B	3		PR82B	3	
AC2	PR68A	3		PR82A	3	
AF6	PR67D	3		PR81D	3	
AE6	PR67C	3		PR81C	3	
AD3	PR67B	3		PR81B	3	
AC3	PR67A	3		PR81A	3	
AE8	PR65D	3		PR79D	3	
AD8	PR65C	3		PR79C	3	
AD4	PR65B	3		PR79B	3	
AC4	PR65A	3		PR79A	3	
AE7	PR64D	3		PR78D	3	
AD7	PR64C	3		PR78C	3	
AD5	PR64B	3		PR78B	3	
AC5	PR64A	3		PR78A	3	
AD6	PR63D	3		PR77D	3	
AC6	PR63C	3		PR77C	3	
AB1	PR63B	3		PR77B	3	
AA1	PR63A	3		PR77A	3	
AD9	PR61D	3		PR75D	3	
AC9	PR61C	3		PR75C	3	
AB2	PR61B	3		PR75B	3	
AA2	PR61A	3		PR75A	3	
AD14	PR60D	3		PR74D	3	
AC14	PR60C	3		PR74C	3	
AB5	PR60B	3		PR74B	3	
AA5	PR60A	3		PR74A	3	
AD10	PR59D	3		PR73D	3	
AC10	PR59C	3		PR73C	3	
Y1	PR59B	3		PR73B	3	
W1	PR59A	3		PR73A	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80 Ball Function	LFSC/M80 VCCIO Bank	LFSC/M80 Dual Function	LFSC/M115 Ball Function	LFSC/M115 VCCIO Bank	LFSC/M115 Dual Function
V8	PR41C	2		PR55C	2	
T4	PR41B	2		PR55B	2	
U4	PR41A	2		PR55A	2	
V9	PR39D	2		PR53D	2	
U9	PR39C	2		PR53C	2	
V6	PR39B	2		PR53B	2	
U6	PR39A	2		PR53A	2	
AA12	PR38D	2		PR52D	2	
Y12	PR38C	2		PR52C	2	
P1	PR38B	2		PR52B	2	
N1	PR38A	2		PR52A	2	
T7	PR37D	2		PR51D	2	
R7	PR37C	2		PR51C	2	
T5	PR37B	2		PR51B	2	
R5	PR37A	2		PR51A	2	
U10	PR35D	2		PR49D	2	
V10	PR35C	2		PR49C	2	
P2	PR35B	2		PR49B	2	
N2	PR35A	2		PR49A	2	
T8	PR34D	2		PR48D	2	
R8	PR34C	2		PR48C	2	
N3	PR34B	2		PR48B	2	
P3	PR34A	2		PR48A	2	
M6	PR33D	2		PR47D	2	
M7	PR33C	2		PR47C	2	
T6	PR33B	2		PR47B	2	
R6	PR33A	2		PR47A	2	
V11	PR31D	2		PR45D	2	
U11	PR31C	2		PR45C	2	
M1	PR31B	2		PR45B	2	
L1	PR31A	2		PR45A	2	
Y14	PR30D	2		PR44D	2	
W14	PR30C	2		PR44C	2	
M2	PR30B	2		PR44B	2	
L2	PR30A	2		PR44A	2	
T9	PR29D	2	DIFFR_2	PR43D	2	DIFFR_2
R9	PR29C	2	VREF1_2	PR43C	2	VREF1_2
P4	PR29B	2		PR43B	2	
N4	PR29A	2		PR43A	2	
N7	PR26D	2		PR40D	2	
N8	PR26C	2		PR40C	2	
P5	PR26B	2		PR40B	2	
N5	PR26A	2		PR40A	2	
K7	PR25D	2		PR38D	2	
J7	PR25C	2		PR38C	2	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

	LFSC/M80			LFSC/M115		
Ball Number	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
J1	PR25B	2		PR38B	2	
K1	PR25A	2		PR38A	2	
V12	PR24D	2		PR34D	2	
U12	PR24C	2		PR34C	2	
K2	PR24B	2		PR34B	2	
J2	PR24A	2		PR34A	2	
R10	PR22D	2		PR30D	2	
T10	PR22C	2		PR30C	2	
L5	PR22B	2		PR30B	2	
K5	PR22A	2		PR30A	2	
P9	PR21D	2		PR26D	2	
N9	PR21C	2		PR26C	2	
L6	PR21B	2		PR26B	2	
K6	PR21A	2		PR26A	2	
M8	PR20D	2		PR19D	2	
M9	PR20C	2		PR19C	2	
H1	PR20B	2		PR19B	2	
G1	PR20A	2		PR19A	2	
U14	PR18D	2	VREF2_2	PR18D	2	VREF2_2
T14	PR18C	2		PR18C	2	
H2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
G2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
H3	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
G3	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
R11	PR16D	2		PR15D	2	
P11	PR16C	2		PR15C	2	
J5	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
J6	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
P18	VCCJ	-		VCCJ	-	
P19	TDO	-	TDO	TDO	-	TDO
R21	TMS	-		TMS	-	
P20	TCK	-		TCK	-	
P12	TDI	-		TDI	-	
P17	PROGRAMN	1		PROGRAMN	1	
P21	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
P13	CCLK	1		CCLK	1	
H10	RESP_URC	-		RESP_URC	-	
N13	VCC12	-		VCC12	-	
H9	A_REFCLKN_R	-		A_REFCLKN_R	-	
G9	A_REFCLKP_R	-		A_REFCLKP_R	-	
F2	VCC12	-		VCC12	-	
H4	A_VDDIB0_R	-		A_VDDIB0_R	-	
C1	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

	LFSC/M80			LFSC/M115		
Ball Number	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
V21	VCC	-		VCC	-	
V22	VCC	-		VCC	-	
V23	VCC	-		VCC	-	
V25	VCC	-		VCC	-	
V27	VCC	-		VCC	-	
W17	VCC	-		VCC	-	
W19	VCC	-		VCC	-	
W21	VCC	-		VCC	-	
W22	VCC	-		VCC	-	
W24	VCC	-		VCC	-	
W26	VCC	-		VCC	-	
Y16	VCC	-		VCC	-	
Y18	VCC	-		VCC	-	
Y20	VCC	-		VCC	-	
Y23	VCC	-		VCC	-	
Y25	VCC	-		VCC	-	
Y27	VCC	-		VCC	-	
AG22	VCC12	-		VCC12	-	
AG26	VCC12	-		VCC12	-	
T17	VCC12	-		VCC12	-	
T21	VCC12	-		VCC12	-	
T22	VCC12	-		VCC12	-	
T26	VCC12	-		VCC12	-	
U16	VCC12	-		VCC12	-	
U27	VCC12	-		VCC12	-	
AC15	VCCAUX	-		VCCAUX	-	
AC28	VCCAUX	-		VCCAUX	-	
AD15	VCCAUX	-		VCCAUX	-	
AD28	VCCAUX	-		VCCAUX	-	
AE15	VCCAUX	-		VCCAUX	-	
AE28	VCCAUX	-		VCCAUX	-	
AF15	VCCAUX	-		VCCAUX	-	
AF28	VCCAUX	-		VCCAUX	-	
AG15	VCCAUX	-		VCCAUX	-	
AG28	VCCAUX	-		VCCAUX	-	
AH14	VCCAUX	-		VCCAUX	-	
AH16	VCCAUX	-		VCCAUX	-	
AH17	VCCAUX	-		VCCAUX	-	
AH18	VCCAUX	-		VCCAUX	-	
AH19	VCCAUX	-		VCCAUX	-	
AH20	VCCAUX	-		VCCAUX	-	
AH23	VCCAUX	-		VCCAUX	-	
AH24	VCCAUX	-		VCCAUX	-	
AH25	VCCAUX	-		VCCAUX	-	
AH26	VCCAUX	-		VCCAUX	-	

LatticeSC/M Family Data Sheet Ordering Information

January 2010 **Data Sheet DS1004**

Part Number Description

LF XXX XXX XX E PX – X XXXXXX X

LF = Lattice FPGA

Device Family
- LatticeSC FPGA
- LatticeSCM FPGA

SERDES Speed
- 3GA = 3.8G

Logic Capacity
- 15K LUTs
- 25K LUTs
- 40K LUTs
- 80K LUTs
- 115K LUTs

Supply Voltage
- E = 1.2V

Grade
- C = Commercial
- I = Industrial

Package[1]
- F256 = 256-ball fpBGA
- F900 = 900-ball fpBGA
- FF1020 = 1020-ball Organic fcBGA[2]
- FFA1020 = 1020-ball Organic fcBGA Revision 2
- FC1152 = 1152-ball Ceramic fcBGA[3]
- FF1152 = 1152-ball Organic fcBGA
- FC1704 = 1704-ball Ceramic fcBGA[3]
- FF1704 = 1704-ball Organic fcBGA

- FN256 = 256-ball Lead-Free fpBGA
- FN900 = 900-ball Lead-Free fpBGA
- FFN1020 = 1020-ball Lead-Free Organic fcBGA[2]
- FFAN1020 = 1020-ball Lead-Free Organic fcBGA Revision 2
- FCN1152 = 1152-ball Lead-Free Ceramic fcBGA[3]
- FFN1152 = 1152-ball Lead-Free Organic fcBGA
- FCN1704 = 1704-ball Lead-Free Ceramic fcBGA[3]
- FFN1704 = 1704-ball Lead-Free Organic fcBGA

Speed Grade
- -5 (Slowest)
- -6
- -7 (Fastest)[4]

Predefined Function (LatticeSCM Only)
- P1 = Initial MACO Option

1. fpBGA = 1.0 mm pitch BGA, fcBGA = 1.0 mm flip-chip BGA (organic and ceramic).
2. Converted to organic fcBGA per PCN #02A-10.
3. Converted to organic fcBGA per PCN #01A-10.
4. Not available in the LatticeSC115 and LatticeSCM115 devices.

Ordering Information

Depending on the speed and temperature grade, the device can either be dual marked or single marked. The commercial grade is one speed grade faster than the associated dual marked industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:

Lattice SC
LFSC3GA25E
6F900C-5I
XXXXXXXX

or

Lattice SC
LFSC3GA25E
7F900C
XXXXXXXX

Temperature Grade	Speed Grade	Single or Dual Mark?
Commercial	-7	Either OK
	-6	Dual Only
	-5	Single Only
Industrial	-6	Either OK
	-5	Dual Only

Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FC1152I[1]	-6	Ceramic fcBGA	1152	IND	115.2
LFSC3GA115E-5FC1152I[1]	-5	Ceramic fcBGA	1152	IND	115.2
LFSC3GA115E-6FF1152I	-6	Organic fcBGA	1152	IND	115.2
LFSC3GA115E-5FF1152I	-5	Organic fcBGA	1152	IND	115.2
LFSC3GA115E-6FC1704I[1]	-6	Ceramic fcBGA	1704	IND	115.2
LFSC3GA115E-5FC1704I[1]	-5	Ceramic fcBGA	1704	IND	115.2
LFSC3GA115E-6FF1704I	-6	Organic fcBGA	1704	IND	115.2
LFSC3GA115E-5FF1704I	-5	Organic fcBGA	1704	IND	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FC1152I[1]	-6	Ceramic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-5FC1152I[1]	-5	Ceramic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-6FF1152I	-6	Organic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-5FF1152I	-5	Organic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-6FC1704I[1]	-6	Ceramic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-5FC1704I[1]	-5	Ceramic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-6FF1704I	-6	Organic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-5FF1704I	-5	Organic fcBGA	1704	IND	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.