Lattice Semiconductor Corporation - LFSCM3GA115EP1-6FF1704C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	28750
Number of Logic Elements/Cells	115000
Total RAM Bits	7987200
Number of I/O	942
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1704-BBGA, FCBGA
Supplier Device Package	1704-OFCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga115ep1-6ff1704c

VDDAX25 needs to be connected independent of the use of the SERDES. This supply is used to control the SERDES CML I/O regardless of the SERDES being used in the design.

Supported Source Synchronous Interfaces

The LatticeSC devices contain a variety of hardware, such as delay elements, DDR registers and PLLs, to simplify the implementation of Source Synchronous interfaces. Table 2-11 lists Source Synchronous and DDR/QDR standards supported in the LatticeSC. For additional detail refer to technical information at the end of the data sheet.

Table 2-11. Source Synchronous Standards Table[1]

Source Synchronous Standard	Clocking	Speeds (MHz)	Data Rate (Mbps)
RapidIO	DDR	500	1000
SPI4.2 (POS-PHY4)/NPSI	DDR	500	1000
SFI4/XSBI	DDR SDR	334 667	667
XGMII	DDR	156.25	312
CSIX	SDR	250	250
QDRII/QDRII+ memory interface	DDR	300	600
DDR memory interface	DDR	240	480
DDRII memory interface	DDR	333	667
RLDRAM memory interface	DDR	400	800

1. Memory width is dependent on the system design and limited by the number of I/Os in the device.

flexiPCS™ (Physical Coding Sublayer Block)

flexiPCS Functionality

The LatticeSC family combines a high-performance FPGA fabric, high-performance I/Os and large embedded RAM in a single industry leading architecture. LatticeSC devices also feature up to 32 channels of embedded SERDES with associated Physical Coding Sublayer (PCS) logic. The flexiPCS logic can be configured to support numerous industry standard high-speed data transfer protocols.

Each channel of flexiPCS logic contains dedicated transmit and receive SERDES for high-speed, full-duplex serial data transfers at data rates up to 3.8 Gbps. The PCS logic in each channel can be configured to support an array of popular data protocols including SONET (STS-12/STS-12c, STS-48/STS-48c, and TFI-5 support of 10 Gbps or above), Gigabit Ethernet (compliant to the IEEE 1000BASE-X specification), 1.02 or 2.04 Gbps Fibre Channel, PCI-Express, and Serial RapidIO. In addition, the protocol based logic can be fully or partially bypassed in a number of configurations to allow users flexibility in designing their own high-speed data interface.

Protocols requiring data rates above 3.8 Gbps can be accommodated by dedicating either one pair or all four channels in one flexiPCS quad block to one data link. One quad can support full-duplex serial data transfers at data rates up to 15.2 Gbps. A single flexiPCS quad can be configured to support 10Gb Ethernet (with a fully compliant XAUI interface), 10Gb Fibre Channel, and x4 PCI-Express and 4x RapidIO.

The flexiPCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic which can also be geared to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic. Each SERDES pin can be DC coupled independently and can allow for both high-speed and low-speed operation down to DC rates on the same SERDES pin, as required by some Serial Digital Video applications.

The ispLEVER design tools from Lattice support all modes of the flexiPCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow a user to define their own operation. With ispLEVER, the user can define the mode for each quad in a design. Nine modes are currently supported by the ispLEVER design flow:

sysCLOCK DLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		100	—	700	MHz
f_{OUTOP}	Output Clock Frequency (CLKOP)		100	—	700	MHz
f_{OUTOS}	Output Clock Frequency (CLKOS)		25	—	700	MHz
AC Characteristics						
t_{DUTY}	Output Clock Duty Cycle	Output Clock Duty Cycle (at 50% levels, 50% duty cycle input clock, duty cycle correction turned off, time reference delay mode)	38	—	62	%
t_{DUTYRD}	Output Clock Duty Cycle	Output Clock Duty Cycle (at 50% levels, arbitrary duty cycle input clock, duty cycle correction turned on, time reference delay mode)	45	—	55	%
$t_{DUTYCIR}$	Output Clock Duty Cycle	Output Clock Duty Cycle (at 50% levels, arbitrary duty cycle input clock, duty cycle correction turned on, clock injection removal mode)	40	—	60	%
t_{OPJIT}[1]	Output Clock Period Jitter		—	—	200	ps
t_{CPJIT}[1]	Output Clock Cycle-to-Cycle Jitter		—	—	200	ps
t_{SKEW}	Output Clock to Clock Skew (Between Two Outputs with the Same Phase Setting)		—	—	100	ps
t_{LOCK}	DLL Lock-in Time		8	—	18500	cycles
t_{IDUTY}	Input Clock Duty Cycle	Applies to all operating conditions	35	—	65	%
t_{IPJIT}	Input Clock Period Jitter		—	—	+/- 250	ps
t_{HI}	Input Clock High Time	At 80% level	500	—	—	ps
t_{LO}	Input Clock Low Time	At 20% level	500	—	—	ps
t_{RSWD}	Reset Signal Pulse Width		3	—	—	ns
t_{FDEL}	Timeshift Delay Step Size		35	45	80	ps
t_{DLL}	Delay Through the DLL when No Delay Taps are Chosen but Not in Bypass Mode.		—	760	—	ps

1. Values are measured with FPGA logic active, no additional I/Os toggling and REFCLK total jitter = 30 ps.

LFSC/M15 Logic Signal Connections: 256 fpBGA[1,2] (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
J9	VCC	-	
K8	VCC	-	
F6	VCC12	-	
F11	VCC12	-	
L11	VCC12	-	
L6	VCC12	-	
K7	VCC12	-	
K10	VCC12	-	
F10	VCCAUX	-	
F7	VCCAUX	-	
T1	GND	-	
G11	VCCAUX	-	
K11	VCCAUX	-	
L10	VCCAUX	-	
L9	VCCAUX	-	
L7	VCCAUX	-	
L8	VCCAUX	-	
T16	GND	-	
G6	VCCAUX	-	
K6	VCCAUX	-	
B13	VCCIO1	-	
D11	VCCIO1	-	
D14	VCCIO1	-	
F12	VCCIO2	-	
G15	VCCIO2	-	
K14	VCCIO3	-	
N15	VCCIO3	-	
M11	VCCIO4	-	
P13	VCCIO4	-	
R10	VCCIO4	-	
N6	VCCIO5	-	
P7	VCCIO5	-	
R4	VCCIO5	-	
K2	VCCIO6	-	
N3	VCCIO6	-	
F4	VCCIO7	-	
G3	VCCIO7	-	
D4	VCC12	-	
D7	VCC12	-	
D5	VCC12	-	
D6	VCC12	-	

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M15 in a 256-pin package does not support an MPI interface.

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F19	PT24A	1	MPI_TEA	PT30A	1	MPI_TEA
J18	PT23D	1	D14/MPI_DATA14	PT28D	1	D14/MPI_DATA14
K18	PT23C	1	DP1/MPI_PAR1	PT28C	1	DP1/MPI_PAR1
E20	PT23B	1	A21/MPI_BURST	PT27B	1	A21/MPI_BURST
F20	PT23A	1	D15/MPI_DATA15	PT27A	1	D15/MPI_DATA15
C23	B_REFCLKP_L	-		B_REFCLKP_L	-	
D23	B_REFCLKN_L	-		B_REFCLKN_L	-	
B23	VCC12	-		VCC12	-	
H21	B_VDDIB3_L	-		B_VDDIB3_L	-	
F21	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
G21	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D21	B_VDDOB3_L	-		B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D22	B_VDDOB2_L	-		B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
G22	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
F22	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
H22	B_VDDIB2_L	-		B_VDDIB2_L	-	
H24	B_VDDIB1_L	-		B_VDDIB1_L	-	
G23	B_HDINP1_L	-	PCS 361 CH 1 IN P	B_HDINP1_L	-	PCS 361 CH 1 IN P
H23	B_HDINN1_L	-	PCS 361 CH 1 IN N	B_HDINN1_L	-	PCS 361 CH 1 IN N
A24	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
B24	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
D24	B_VDDOB1_L	-		B_VDDOB1_L	-	
B25	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
D25	B_VDDOB0_L	-		B_VDDOB0_L	-	
A25	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
G25	B_HDINN0_L	-	PCS 361 CH 0 IN N	B_HDINN0_L	-	PCS 361 CH 0 IN N
F25	B_HDINP0_L	-	PCS 361 CH 0 IN P	B_HDINP0_L	-	PCS 361 CH 0 IN P
H25	B_VDDIB0_L	-		B_VDDIB0_L	-	
H26	A_VDDIB3_L	-		A_VDDIB3_L	-	
F26	A_HDINP3_L	-	PCS 360 CH 3 IN P	A_HDINP3_L	-	PCS 360 CH 3 IN P
G26	A_HDINN3_L	-	PCS 360 CH 3 IN N	A_HDINN3_L	-	PCS 360 CH 3 IN N
A26	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
B26	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
D26	A_VDDOB3_L	-		A_VDDOB3_L	-	
B27	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
D27	A_VDDOB2_L	-		A_VDDOB2_L	-	
A27	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
G27	A_HDINN2_L	-	PCS 360 CH 2 IN N	A_HDINN2_L	-	PCS 360 CH 2 IN N
F27	A_HDINP2_L	-	PCS 360 CH 2 IN P	A_HDINP2_L	-	PCS 360 CH 2 IN P
H27	A_VDDIB2_L	-		A_VDDIB2_L	-	
F29	A_VDDIB1_L	-		A_VDDIB1_L	-	
G28	A_HDINP1_L	-	PCS 360 CH 1 IN P	A_HDINP1_L	-	PCS 360 CH 1 IN P
H28	A_HDINN1_L	-	PCS 360 CH 1 IN N	A_HDINN1_L	-	PCS 360 CH 1 IN N
A29	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
B29	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
D29	A_VDDOB1_L	-		A_VDDOB1_L	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
V25	PL44C	6		PL56C	6	
W25	PL44D	6		PL56D	6	
U34	PL45A	6		PL57A	6	
V34	PL45B	6		PL57B	6	
V26	PL45C	6		PL57C	6	
W26	PL45D	6		PL57D	6	
V33	PL47A	6		PL60A	6	
W33	PL47B	6		PL60B	6	
V24	PL47C	6		PL60C	6	
W24	PL47D	6		PL60D	6	
W31	PL48A	6		PL63A	6	
Y31	PL48B	6		PL63B	6	
Y29	PL48C	6		PL63C	6	
AA29	PL48D	6		PL63D	6	
Y33	PL49A	6		PL65A	6	
AA33	PL49B	6		PL65B	6	
Y28	PL49C	6		PL65C	6	
AA28	PL49D	6		PL65D	6	
AB32	PL51A	6		PL76A	6	
AC32	PL51B	6		PL76B	6	
AA26	PL51C	6		PL76C	6	
AA27	PL51D	6	DIFFR_6	PL76D	6	DIFFR_6
AB31	PL52A	6		PL77A	6	
AC31	PL52B	6		PL77B	6	
Y24	PL52C	6		PL77C	6	
AA24	PL52D	6		PL77D	6	
AE34	PL53A	6		PL78A	6	
AF34	PL53B	6		PL78B	6	
AB30	PL53C	6		PL78C	6	
AC30	PL53D	6		PL78D	6	
AD33	PL56A	6		PL80A	6	
AE33	PL56B	6		PL80B	6	
AD30	PL56C	6		PL80C	6	
AE30	PL56D	6		PL80D	6	
AE32	PL57A	6		PL81A	6	
AF32	PL57B	6		PL81B	6	
AA25	PL57C	6		PL81C	6	
AB25	PL57D	6		PL81D	6	
AJ34	PL58A	6		PL82A	6	
AK34	PL58B	6		PL82B	6	
AB27	PL58C	6		PL82C	6	
AC27	PL58D	6		PL82D	6	
AF33	PL60A	6		PL84A	6	
AG33	PL60B	6		PL84B	6	
AC29	PL60C	6		PL84C	6	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
H21	PT38D	1	D28/PCLKC1_6/MPI_DATA28	PT57D	1	D28/PCLKC1_6/MPI_DATA28
J21	PT38C	1	D29/PCLKT1_6/MPI_DATA29	PT57C	1	D29/PCLKT1_6/MPI_DATA29
A19	PT38B	1	A9/MPI_ADDR23	PT57B	1	A9/MPI_ADDR23
B19	PT38A	1	A10/MPI_ADDR24	PT57A	1	A10/MPI_ADDR24
H22	PT37D	1	D30/PCLKC1_7/MPI_DATA30	PT56D	1	D30/PCLKC1_7/MPI_DATA30
J22	PT37C	1	D31/PCLKT1_7/MPI_DATA31	PT56C	1	D31/PCLKT1_7/MPI_DATA31
F20	PT37B	1	A11/MPI_ADDR25	PT56B	1	A11/MPI_ADDR25
G20	PT37A	1	A12/MPI_ADDR26	PT56A	1	A12/MPI_ADDR26
K21	PT35D	1	D11/MPI_DATA11	PT55D	1	D11/MPI_DATA11
K22	PT35C	1	D12/MPI_DATA12	PT55C	1	D12/MPI_DATA12
A20	PT35B	1	A13/MPI_ADDR27	PT55B	1	A13/MPI_ADDR27
B20	PT35A	1	A14/MPI_ADDR28	PT55A	1	A14/MPI_ADDR28
L21	PT33D	1	A16/MPI_ADDR30	PT53D	1	A16/MPI_ADDR30
L20	PT33C	1	D13/MPI_DATA13	PT53C	1	D13/MPI_DATA13
D20	PT33B	1	A15/MPI_ADDR29	PT53B	1	A15/MPI_ADDR29
E20	PT33A	1	A17/MPI_ADDR31	PT53A	1	A17/MPI_ADDR31
L19	PT30D	1	A19/MPI_TSIZ1	PT52D	1	A19/MPI_TSIZ1
K19	PT30C	1	A20/MPI_BDIP	PT52C	1	A20/MPI_BDIP
D21	PT30B	1	A18/MPI_TSIZ0	PT52B	1	A18/MPI_TSIZ0
E21	PT30A	1	MPI_TEA	PT52A	1	MPI_TEA
M20	PT28D	1	D14/MPI_DATA14	PT51D	1	D14/MPI_DATA14
M19	PT28C	1	DP1/MPI_PAR1	PT51C	1	DP1/MPI_PAR1
F21	PT27B	1	A21/MPI_BURST	PT51B	1	A21/MPI_BURST
G21	PT27A	1	D15/MPI_DATA15	PT51A	1	D15/MPI_DATA15
H24	B_REFCLKP_L	-		B_REFCLKP_L	-	
J24	B_REFCLKN_L	-		B_REFCLKN_L	-	
L22	VCC12	-		VCC12	-	
E26	B_VDDIB3_L	-		B_VDDIB3_L	-	
G22	VCC12	-		VCC12	-	
E22	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
F22	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
L24	VCC12	-		VCC12	-	
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D22	B_VDDOB3_L	-		B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D23	B_VDDOB2_L	-		B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
K24	VCC12	-		VCC12	-	
F23	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
E23	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
D26	B_VDDIB2_L	-		B_VDDIB2_L	-	
G23	VCC12	-		VCC12	-	
D27	B_VDDIB1_L	-		B_VDDIB1_L	-	
G24	VCC12	-		VCC12	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP27	PB26A	5	
AP26	PB26B	5	
AK25	PB26C	5	
AK24	PB26D	5	
AN25	PB29A	5	
AN24	PB29B	5	
AE22	PB29C	5	
AE21	PB29D	5	
AM26	PB31A	5	
AM25	PB31B	5	
AF22	PB31C	5	
AF21	PB31D	5	
AN23	PB47A	5	
AN22	PB47B	5	
AP23	PB57A	5	
AP22	PB57B	5	
AG21	PB57C	5	
AG20	PB57D	5	
AP25	PB50A	5	PCLKT5_3
AP24	PB50B	5	PCLKC5_3
AD21	PB50C	5	PCLKT5_4
AD20	PB50D	5	PCLKC5_4
AL23	PB51A	5	PCLKT5_5
AL22	PB51B	5	PCLKC5_5
AH24	PB51C	5	
AH23	PB51D	5	
AM23	PB53A	5	PCLKT5_0
AM22	PB53B	5	PCLKC5_0
AJ24	PB53C	5	
AJ23	PB53D	5	VREF2_5
AN21	PB54A	5	PCLKT5_1
AN20	PB54B	5	PCLKC5_1
AE19	PB54C	5	PCLKT5_6
AD19	PB54D	5	PCLKC5_6
AK21	PB55A	5	PCLKT5_2
AK20	PB55B	5	PCLKC5_2
AK23	PB55C	5	PCLKT5_7
AK22	PB55D	5	PCLKC5_7
AL20	PB58A	5	
AL19	PB58B	5	
AG19	PB58C	5	
AF19	PB58D	5	
AP21	PB61A	5	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP20	PB61B	5	
AH21	PB61C	5	
AH20	PB61D	5	
AM20	PB63A	5	
AM19	PB63B	5	
AJ21	PB63C	5	
AJ20	PB63D	5	
AK19	PB66A	5	
AK18	PB66B	5	
AE18	PB66C	5	
AD18	PB66D	5	
AN19	PB69A	5	
AN18	PB69B	5	
AG18	PB69C	5	
AF18	PB69D	5	
AP19	PB71A	5	
AP18	PB71B	5	
AJ18	PB71C	5	
AH18	PB71D	5	
AP17	PB73A	4	
AP16	PB73B	4	
AJ17	PB73C	4	
AH17	PB73D	4	
AN17	PB75A	4	
AN16	PB75B	4	
AE17	PB75C	4	
AD17	PB75D	4	
AK17	PB78A	4	
AK16	PB78B	4	
AG17	PB78C	4	
AF17	PB78D	4	
AM16	PB81A	4	
AM15	PB81B	4	
AJ15	PB81C	4	
AJ14	PB81D	4	
AL16	PB83A	4	
AL15	PB83B	4	
AG16	PB83C	4	
AF16	PB83D	4	
AP15	PB86A	4	
AP14	PB86B	4	
AH15	PB86C	4	
AH14	PB86D	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AN15	PB89A	4	PCLKT4_2
AN14	PB89B	4	PCLKC4_2
AE16	PB89C	4	PCLKT4_7
AD16	PB89D	4	PCLKC4_7
AK15	PB90A	4	PCLKT4_1
AK14	PB90B	4	PCLKC4_1
AG15	PB90C	4	PCLKT4_6
AG14	PB90D	4	PCLKC4_6
AM13	PB91A	4	PCLKT4_0
AM12	PB91B	4	PCLKC4_0
AJ12	PB91C	4	VREF2_4
AJ11	PB91D	4	
AL13	PB93A	4	PCLKT4_5
AL12	PB93B	4	PCLKC4_5
AH12	PB93C	4	
AH11	PB93D	4	
AN13	PB94A	4	PCLKT4_3
AN12	PB94B	4	PCLKC4_3
AD14	PB94C	4	PCLKT4_4
AD15	PB94D	4	PCLKC4_4
AP13	PB87A	4	
AP12	PB87B	4	
AK13	PB87C	4	
AK12	PB87D	4	
AP11	PB97A	4	
AP10	PB97B	4	
AN11	PB113A	4	
AN10	PB113B	4	
AF14	PB113C	4	
AF13	PB113D	4	
AM10	PB115A	4	
AM9	PB115B	4	
AE14	PB115C	4	
AE13	PB115D	4	
AP9	PB118A	4	
AP8	PB118B	4	
AK11	PB118C	4	
AK10	PB118D	4	
AL10	PB121A	4	
AL9	PB121B	4	
AF12	PB121C	4	
AF11	PB121D	4	
AN9	PB123A	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AN8	PB123B	4	
AG11	PB123C	4	
AG10	PB123D	4	
AP7	PB125A	4	
AP6	PB125B	4	
AG13	PB125C	4	
AG12	PB125D	4	
AN7	PB127A	4	
AN6	PB127B	4	
AK9	PB127C	4	
AK8	PB127D	4	
AP5	PB129A	4	
AP4	PB129B	4	
AD11	PB129C	4	
AE11	PB129D	4	
AM7	PB131A	4	
AM6	PB131B	4	
AJ9	PB131C	4	
AJ8	PB131D	4	
AP3	PB133A	4	
AN3	PB133B	4	
AF10	PB133C	4	
AE10	PB133D	4	
AL7	PB135A	4	
AL6	PB135B	4	
AK7	PB135C	4	
AK6	PB135D	4	
AN5	PB138A	4	
AN4	PB138B	4	
AH9	PB138C	4	VREF1_4
AH8	PB138D	4	
AM3	PB139A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AM4	PB139B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AG9	PB139C	4	
AG8	PB139D	4	
AN2	PB141A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AM2	PB141B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ6	PB141C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH6	PB141D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF7	PROBE_VCC	-	
AF8	PROBE_GND	-	
AG7	PR117D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AG6	PR117C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AL4	PR117B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AL3	PR117A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD10	PR116D	3	
AD9	PR116C	3	
AH4	PR116B	3	
AJ4	PR116A	3	
AK5	PR115D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AJ5	PR115C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AM1	PR115B	3	
AL1	PR115A	3	
AH5	PR112D	3	
AG5	PR112C	3	
AL2	PR112B	3	
AK2	PR112A	3	
AB9	PR109D	3	
AC9	PR109C	3	
AH1	PR109B	3	
AG1	PR109A	3	
AE8	PR107D	3	VREF2_3
AD8	PR107C	3	
AJ3	PR107B	3	
AH3	PR107A	3	
AD7	PR104D	3	
AC7	PR104C	3	
AJ2	PR104B	3	
AH2	PR104A	3	
AF6	PR103D	3	
AF5	PR103C	3	
AF4	PR103B	3	
AE4	PR103A	3	
AD6	PR99D	3	
AC6	PR99C	3	
AG2	PR99B	3	
AF2	PR99A	3	
AC8	PR98D	3	
AB8	PR98C	3	
AK1	PR98B	3	
AJ1	PR98A	3	
AB10	PR96D	3	
AA10	PR96C	3	
AF3	PR96B	3	
AE3	PR96A	3	
AE5	PR94D	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AL5	GND	-	
AM14	GND	-	
AM18	GND	-	
AM24	GND	-	
AM30	GND	-	
AM8	GND	-	
AN1	GND	-	
AN34	GND	-	
AP2	GND	-	
AP33	GND	-	
B1	GND	-	
B34	GND	-	
C11	GND	-	
C12	GND	-	
C13	GND	-	
C14	GND	-	
C17	GND	-	
C21	GND	-	
C22	GND	-	
C23	GND	-	
C24	GND	-	
C26	GND	-	
C27	GND	-	
C30	GND	-	
C31	GND	-	
C4	GND	-	
C5	GND	-	
C8	GND	-	
C9	GND	-	
D18	GND	-	
E32	GND	-	
E4	GND	-	
F19	GND	-	
G16	GND	-	
G29	GND	-	
G7	GND	-	
H3	GND	-	
H31	GND	-	
J10	GND	-	
J15	GND	-	
J26	GND	-	
K20	GND	-	
K23	GND	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AH16	VCCIO4	-	
AJ13	VCCIO4	-	
AJ7	VCCIO4	-	
AL14	VCCIO4	-	
AL8	VCCIO4	-	
AM11	VCCIO4	-	
AM17	VCCIO4	-	
AM5	VCCIO4	-	
AE20	VCCIO5	-	
AE23	VCCIO5	-	
AE26	VCCIO5	-	
AH22	VCCIO5	-	
AH28	VCCIO5	-	
AJ19	VCCIO5	-	
AJ25	VCCIO5	-	
AL18	VCCIO5	-	
AL24	VCCIO5	-	
AL30	VCCIO5	-	
AM21	VCCIO5	-	
AM27	VCCIO5	-	
AA31	VCCIO6	-	
AB29	VCCIO6	-	
AC24	VCCIO6	-	
AD32	VCCIO6	-	
AE28	VCCIO6	-	
AG31	VCCIO6	-	
AK32	VCCIO6	-	
T29	VCCIO6	-	
U31	VCCIO6	-	
V32	VCCIO6	-	
W28	VCCIO6	-	
Y26	VCCIO6	-	
E31	VCCIO7	-	
G28	VCCIO7	-	
H32	VCCIO7	-	
K29	VCCIO7	-	
L31	VCCIO7	-	
M25	VCCIO7	-	
N28	VCCIO7	-	
P32	VCCIO7	-	
R25	VCCIO7	-	
J25	VCCIO1	-	
N11	VTT_2	2	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P38	PL26B	7		PL40B	7	
N35	PL26C	7		PL40C	7	
N36	PL26D	7		PL40D	7	
N39	PL29A	7		PL43A	7	
P39	PL29B	7		PL43B	7	
R34	PL29C	7	VREF1_7	PL43C	7	VREF1_7
T34	PL29D	7	DIFFR_7	PL43D	7	DIFFR_7
L41	PL30A	7		PL44A	7	
M41	PL30B	7		PL44B	7	
W29	PL30C	7		PL44C	7	
Y29	PL30D	7		PL44D	7	
L42	PL31A	7		PL45A	7	
M42	PL31B	7		PL45B	7	
U32	PL31C	7		PL45C	7	
V32	PL31D	7		PL45D	7	
R37	PL33A	7		PL47A	7	
T37	PL33B	7		PL47B	7	
M36	PL33C	7		PL47C	7	
M37	PL33D	7		PL47D	7	
P40	PL34A	7		PL48A	7	
N40	PL34B	7		PL48B	7	
R35	PL34C	7		PL48C	7	
T35	PL34D	7		PL48D	7	
N41	PL35A	7		PL49A	7	
P41	PL35B	7		PL49B	7	
V33	PL35C	7		PL49C	7	
U33	PL35D	7		PL49D	7	
R38	PL37A	7		PL51A	7	
T38	PL37B	7		PL51B	7	
R36	PL37C	7		PL51C	7	
T36	PL37D	7		PL51D	7	
N42	PL38A	7		PL52A	7	
P42	PL38B	7		PL52B	7	
Y31	PL38C	7		PL52C	7	
AA31	PL38D	7		PL52D	7	
U37	PL39A	7		PL53A	7	
V37	PL39B	7		PL53B	7	
U34	PL39C	7		PL53C	7	
V34	PL39D	7		PL53D	7	
U39	PL41A	7		PL55A	7	
T39	PL41B	7		PL55B	7	
V35	PL41C	7		PL55C	7	
W35	PL41D	7		PL55D	7	
R41	PL42A	7		PL56A	7	
T41	PL42B	7		PL56B	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AV32	PB27B	5		PB29B	5	
AU36	PB27C	5		PB29C	5	
AU37	PB27D	5		PB29D	5	
BA35	PB28A	5		PB30A	5	
BA34	PB28B	5		PB30B	5	
AJ26	PB28C	5		PB30C	5	
AJ27	PB28D	5		PB30D	5	
AW33	PB29A	5		PB31A	5	
AW32	PB29B	5		PB31B	5	
AU35	PB29C	5		PB31C	5	
AU34	PB29D	5		PB31D	5	
BB35	PB31A	5		PB33A	5	
BB34	PB31B	5		PB33B	5	
AN29	PB31C	5		PB33C	5	
AP29	PB31D	5		PB33D	5	
AY33	PB32A	5		PB34A	5	
AY32	PB32B	5		PB34B	5	
AR31	PB32C	5		PB34C	5	
AR30	PB32D	5		PB34D	5	
AV31	PB33A	5		PB35A	5	
AV30	PB33B	5		PB35B	5	
AN28	PB33C	5		PB35C	5	
AP28	PB33D	5		PB35D	5	
BA33	PB35A	5		PB37A	5	
BA32	PB35B	5		PB37B	5	
AT30	PB35C	5		PB37C	5	
AT31	PB35D	5		PB37D	5	
BB33	PB36A	5		PB38A	5	
BB32	PB36B	5		PB38B	5	
AM26	PB36C	5		PB38C	5	
AL26	PB36D	5		PB38D	5	
AW30	PB37A	5		PB39A	5	
AW29	PB37B	5		PB39B	5	
AP27	PB37C	5		PB39C	5	
AN27	PB37D	5		PB39D	5	
BA31	PB39A	5		PB41A	5	
BA30	PB39B	5		PB41B	5	
AU32	PB39C	5		PB41C	5	
AU33	PB39D	5		PB41D	5	
BB31	PB40A	5		PB42A	5	
BB30	PB40B	5		PB42B	5	
AR28	PB40C	5		PB42C	5	
AR27	PB40D	5		PB42D	5	
AV29	PB41A	5		PB43A	5	
AV28	PB41B	5		PB43B	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AG38	NC	-		PL95A	6	
AH38	NC	-		PL95B	6	
AJ39	NC	-		PL100A	6	
AK39	NC	-		PL100B	6	
AL41	NC	-		PL105A	6	
AM41	NC	-		PL105B	6	
AN40	NC	-		PL108A	6	
AM40	NC	-		PL108B	6	
AM39	NC	-		PL111A	6	
AN39	NC	-		PL111B	6	
AR42	NC	-		PL113A	6	
AT42	NC	-		PL113B	6	
AT1	NC	-		PR113B	3	
AR1	NC	-		PR113A	3	
AN4	NC	-		PR111B	3	
AM4	NC	-		PR111A	3	
AM3	NC	-		PR108B	3	
AN3	NC	-		PR108A	3	
AM2	NC	-		PR105B	3	
AL2	NC	-		PR105A	3	
AK4	NC	-		PR100B	3	
AJ4	NC	-		PR100A	3	
AH5	NC	-		PR95B	3	
AG5	NC	-		PR95A	3	
P6	NC	-		PR39B	2	
N6	NC	-		PR39A	2	
L3	NC	-		PR36B	2	
K3	NC	-		PR36A	2	
M5	NC	-		PR35A	2	
L4	NC	-		PR32B	2	
K4	NC	-		PR32A	2	
A2	GND	-		GND	-	
A41	GND	-		GND	-	
AA20	GND	-		GND	-	
AA23	GND	-		GND	-	
AA3	GND	-		GND	-	
AA39	GND	-		GND	-	
AB20	GND	-		GND	-	
AB23	GND	-		GND	-	
AB4	GND	-		GND	-	
AB40	GND	-		GND	-	
AC17	GND	-		GND	-	
AC19	GND	-		GND	-	
AC21	GND	-		GND	-	
AC22	GND	-		GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AM27	GND	-		GND	-	
AM36	GND	-		GND	-	
AM7	GND	-		GND	-	
AP4	GND	-		GND	-	
AP40	GND	-		GND	-	
AR14	GND	-		GND	-	
AR20	GND	-		GND	-	
AR23	GND	-		GND	-	
AR29	GND	-		GND	-	
AR35	GND	-		GND	-	
AR8	GND	-		GND	-	
AT11	GND	-		GND	-	
AT17	GND	-		GND	-	
AT26	GND	-		GND	-	
AT32	GND	-		GND	-	
AU3	GND	-		GND	-	
AU39	GND	-		GND	-	
AW12	GND	-		GND	-	
AW18	GND	-		GND	-	
AW22	GND	-		GND	-	
AW28	GND	-		GND	-	
AW34	GND	-		GND	-	
AW6	GND	-		GND	-	
AY15	GND	-		GND	-	
AY21	GND	-		GND	-	
AY25	GND	-		GND	-	
AY31	GND	-		GND	-	
AY37	GND	-		GND	-	
AY9	GND	-		GND	-	
B1	GND	-		GND	-	
B42	GND	-		GND	-	
BA1	GND	-		GND	-	
BA42	GND	-		GND	-	
BB2	GND	-		GND	-	
BB41	GND	-		GND	-	
C10	GND	-		GND	-	
C12	GND	-		GND	-	
C13	GND	-		GND	-	
C16	GND	-		GND	-	
C18	GND	-		GND	-	
C19	GND	-		GND	-	
C22	GND	-		GND	-	
C24	GND	-		GND	-	
C27	GND	-		GND	-	
C28	GND	-		GND	-	

Industrial

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-6FN256I	-6	Lead-Free fpBGA	256	IND	15.2
LFSC3GA15E-5FN256I	-5	Lead-Free fpBGA	256	IND	15.2
LFSC3GA15E-6FN900I	-6	Lead-Free fpBGA	900	IND	15.2
LFSC3GA15E-5FN900I	-5	Lead-Free fpBGA	900	IND	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-6FN256I	-6	Lead-Free fpBGA	256	IND	15.2
LFSCM3GA15EP1-5FN256I	-5	Lead-Free fpBGA	256	IND	15.2
LFSCM3GA15EP1-6FN900I	-6	Lead-Free fpBGA	900	IND	15.2
LFSCM3GA15EP1-5FN900I	-5	Lead-Free fpBGA	900	IND	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-6FN900I	-6	Lead-Free fpBGA	900	IND	25.4
LFSC3GA25E-5FN900I	-5	Lead-Free fpBGA	900	IND	25.4
LFSC3GA25E-6FFN1020I[1]	-6	Lead-Free Organic fcBGA	1020	IND	25.4
LFSC3GA25E-5FFN1020I[1]	-5	Lead-Free Organic fcBGA	1020	IND	25.4
LFSC3GA25E-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4
LFSC3GA25E-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-6FN900I	-6	Lead-Free fpBGA	900	IND	25.4
LFSCM3GA25EP1-5FN900I	-5	Lead-Free fpBGA	900	IND	25.4
LFSCM3GA25EP1-6FFN1020I[1]	-6	Lead-Free Organic fcBGA	1020	IND	25.4
LFSCM3GA25EP1-5FFN1020I[1]	-5	Lead-Free Organic fcBGA	1020	IND	25.4
LFSCM3GA25EP1-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4
LFSCM3GA25EP1-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA40E-6FFN1020I[1]	-6	Lead-Free Organic fcBGA	1020	IND	40.4
LFSC3GA40E-5FFN1020I[1]	-5	Lead-Free Organic fcBGA	1020	IND	40.4
LFSC3GA40E-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSC3GA40E-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSC3GA40E-6FCN1152I[2]	-6	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSC3GA40E-5FCN1152I[2]	-5	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSC3GA40E-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	40.4
LFSC3GA40E-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Date	Version	Section	Change Summary
June 2006 (cont.)	01.2 (cont.)	DC and Switching Characteristics (cont.)	Updated Typical Building Block Performance with ispLEVER 6.0 values.
			Updated LatticeSC External Switching Characteristics with ispLEVER 6.0 values.
			Updated Lattice SC Internal Timing Parameters with ispLEVER 6.0 values.
			Updated Lattice SC Family Timing Adders with ispLEVER 6.0 values
			Changed % spread from 1 to 0.5 min and from 3 to 1.5 max.
			Changed conditions to refer to “with multiplication” and “without multiplication”.
			Changed the formula for t_{OPJIT} with multiplication (same result, different representation).
		Pinout Information	Expanded definition of NC.
			Expanded definition of GND.
			Expanded definition of VTT_x.
			Expanded definition of VCC12.
			Added accuracy of TEMP pin.
			Added RESPN_[ULC/URC].
			Updated Pin Information Summary with additional devices and packages.
			Added additional devices and packages pinouts.
			Removed Power Supply and NC connections table
			Removed VTT table
			Removed LFSC25 Logic Signal Connections: 900-Ball ffBGA1 table
			Changed all VDDP, VDDTX and VDDRX to VCC12.
		Ordering Information	Added dual marking.
			Added lead free packaging information to part number description.
August 2006	01.3	Introduction	Added SC40 1152 information to Table 1-1.
			Updated Table 1-3 with ispLEVER 6.0 SP1 results.
		Architecture	Added SSTL18 II to Table 2-8.
			Changed Table 2-10 VCCIO column to “N/A” for LVDS, mini-LVDS, BLVDS25, MLVDS25, HYPT and RSDS.
			Changed Hypertransport performance to 700 MHz (1400 Mbps) in Table 2-11.
			Changed SPI4.2 performance to 500 MHz (1000 Mbps) in Table 2-11
			Added “On packages that include PROBE_GND, the most accurate measurements will occur between the TEMP pin and the PROBE_GND pin. On packages that do not include PROBE_GND, measurements should be made between the TEMP pin and board ground.”
			Added VCCIO of 2.5 V for LVPECL33 in table 2-9.
		DC and Switching Characteristics	Updated Typical Building Block Performance with ispLEVER 6.0 SP1 results.
			Updated Initialization and Standby Supply Current table to break out ICC and ICC12.
			Updated LatticeSC External Switching Characteristics with ispLEVER 6.0 SP1 results.
			Updated LatticeSC Internal Timing Parameters with ispLEVER 6.0 SP1 results.

Date	Version	Section	Change Summary
August 2006 (cont.)	01.3 (cont.)	DC and Switching Characteristics (cont.)	Updated LatticeSC Family Timing Adders with ispLEVER 6.0 SP1 results
			Updated PLL Timing Parameters based on PDE testing results
			Removed RDDATA parameter from sysCONFIG readback timing table
		Multiple	Changed TDO/RDDATA to TDO
		Pinout Information	Removed all MPI signals from SC15 256 pin package Dual Function Column
			Added note to SC15, SC25 900 pin package that the package supports a 16 bit MPI
			Added note that pin D3 in an SC15 and SC25 900 pin package should not be used for single-ended outputs
			Added note that pin D28 in an SC15 and SC25 900 pin package should not be used for single-ended outputs
			Added note to SC25 1020 pin package that the package supports a 16 bit MPI
			Added note to SC80 1152 pin package that the package supports a 32 bit MPI
			Added note to SC80 1704 pin package that the package supports a 32 bit MPI
		Ordering Information	Changed “fcBGA” for the 1020 packages to “ffBGA”
November 2006	01.4	Introduction	LatticeSC Family Selection Guide table – I/O count for SC80 device, 1704 fcBGA package changed to 904/32. I/O count for SC115 device, 1704 fcBGA package changed to 942/32.
		DC and Switching Characteristics	DC Electrical Characteristics table – Updated the initialization and standby supply current values.
			DC Electrical Characteristics table – Updated the sysCONFIG Master Parallel mode RCLK low and RCLK high time specifications.
			DC Electrical Characteristics table – Updated VCCIO values for LVPECL33 I/Os.
		Pin Information	Pin Information Summary table - Changed number of single ended user I/Os from 906 to 904 for 1704 fcBGA.
			Removed the single-ended only output restriction on pins D3 and D28 in an SC15 and SC25 900 pin package.
		Ordering Information	Ordering Information tables - Changed number of I/Os from 906 to 904 for 1704 fcBGA.
			Added ordering part numbers for LatticeSC/SCM 40K and 115K LUT devices.
			Added lead-free ordering part numbers.
		Multiple	Changed number of available SC80 I/O from 906 to 904.
			Changed number of available SC115 I/O from 944 to 942.
January 2007	01.4a	Architecture	Added EBR Asynchronous Reset section.
February 2007	01.4b	Architecture	Updated EBR Asynchronous Reset section.
March 2007	01.5	Architecture	Added EBR asynchronous reset clarification
			Clarified that differential drivers are not supported in banks 1, 4 and 5
		DC and Switching Characteristics	Added clarification for the description of the junction temperature specification in the Absolute Maximum Ratings section.
			Updated Initialization and Standby Current table.
			Updated LatticeSC External Switching Characteristics with ispLEVER 6.1 SP1 results.