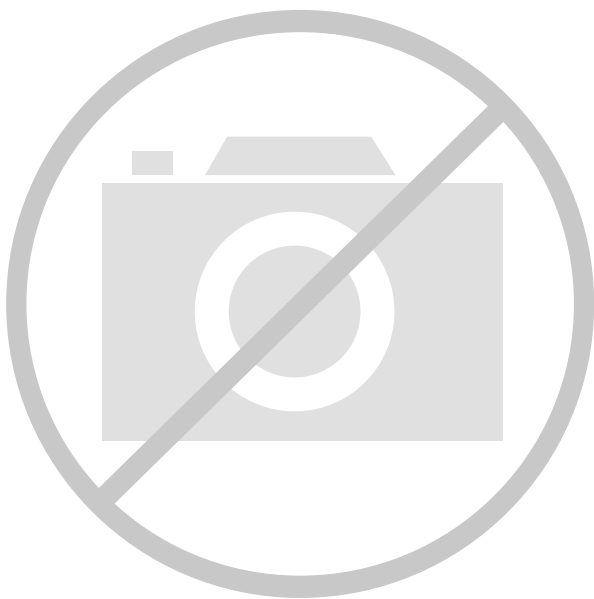




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	28750
Number of Logic Elements/Cells	115000
Total RAM Bits	7987200
Number of I/O	660
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga115ep1-6ffn1152i

Architecture Overview

The LatticeSC architecture contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR). The upper left and upper right corners of the devices contain SERDES blocks and their associated PCS blocks, as shown in Figure 2-1.

Top left and top right corner of the device contain blocks of SERDES. Each block of SERDES contains four channels (quad). Each channel contains a single serializer and de-serializer, synchronization and word alignment logic. The SERDES quad connects with the Physical Coding Sub-layer (PCS) blocks that contain logic to simultaneously perform alignment, coding, de-coding and other functions. The SERDES quad block has separate supply, ground and reference voltage pins.

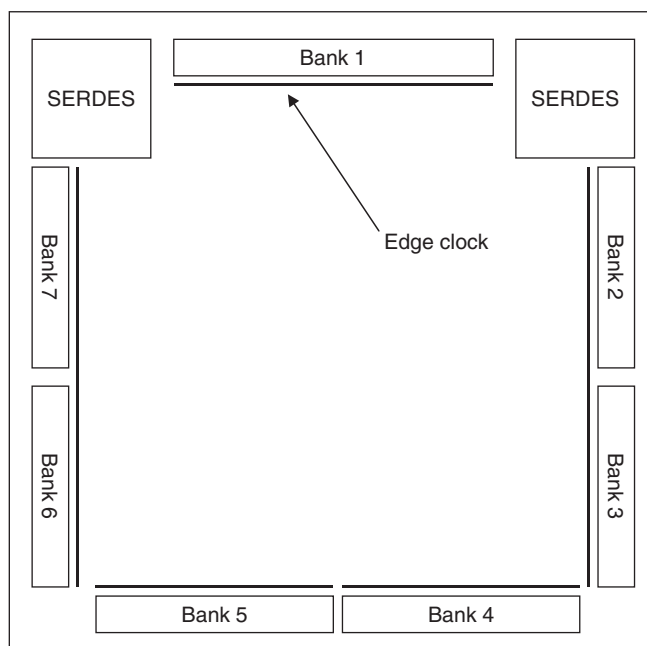
The PICs contain logic to facilitate the conditioning of signals to and from the I/O before they leave or enter the FPGA fabric. The block provides DDR and shift register capabilities that act as a gearbox between high speed I/O and the FPGA fabric. The blocks also contain programmable Adaptive Input Logic that adjusts the delay applied to signals as they enter the device to optimize setup and hold times and ensure robust performance.

sysMEM EBRs are large dedicated fast memory blocks. They can be configured as RAM, ROM or FIFO. These blocks have dedicated logic to simplify the implementation of FIFOs.

The PFU, PIC and EBR blocks are arranged in a two-dimensional grid with rows and columns as shown in Figure 2-1. These blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

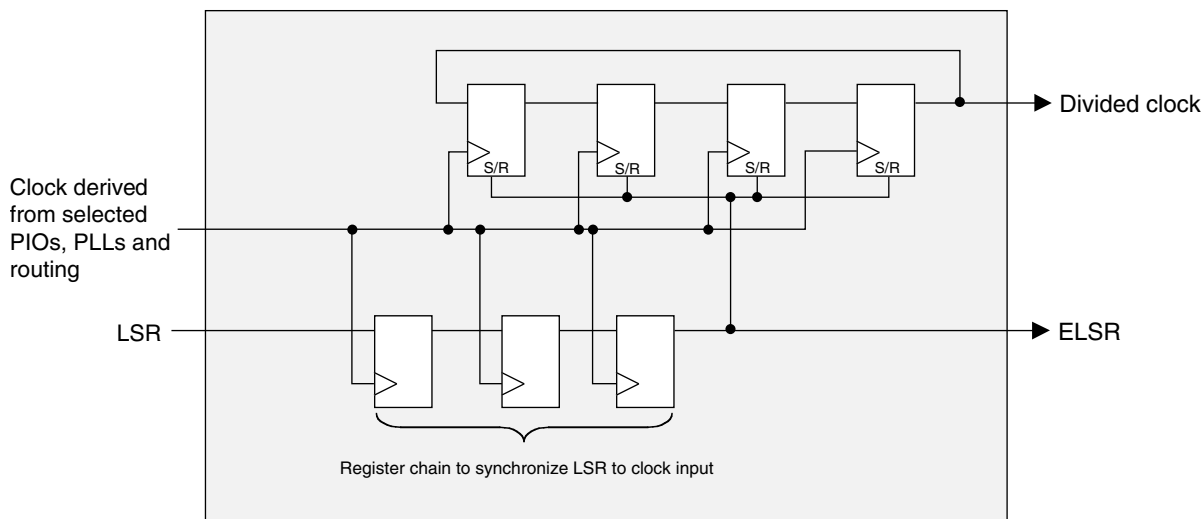
The corners contain the sysCLOCK Analog Phase Locked Loop (PLL) and Delay Locked Loop (DLL) Blocks. The PLLs have multiply, divide and phase shifting capability; they are used to manage the phase relationship of the clocks. The LatticeSC architecture provides eight analog PLLs per device and 12 DLLs. The DLLs provide a simple delay capability and can also be used to calibrate other delays within the device.

Every device in the family has a JTAG Port with internal Logic Analyzer (ispTRACY) capability. The sysCONFIG™ port which allows for serial or parallel device configuration. The system bus simplifies the connections of the external microprocessor to the device for tasks such as SERDES and PCS configuration or interface to the general FPGA logic. The LatticeSC devices use 1.2V as their core voltage operation with 1.0V operation also possible.

Figure 2-7. Edge Clock Resources

Precision Clock Divider

Each set of edge clocks has four high-speed dividers associated with it. These are intended for generating a slower speed system clock from the high-speed edge clock. The block operates in a DIV2 or DIV4 mode and maintains a known phase relationship between the divided down clock and high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PIOs, PLLs and routing. The clock divider outputs serve as primary clock sources. This circuit also generates an edge local set/reset (ELSR) signal which is fed to the PIOs via the edge clock network and is used for the rest of the I/O gearing logic.

Figure 2-8. Clock Divider Circuit

Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved irrespective of where the select signal is

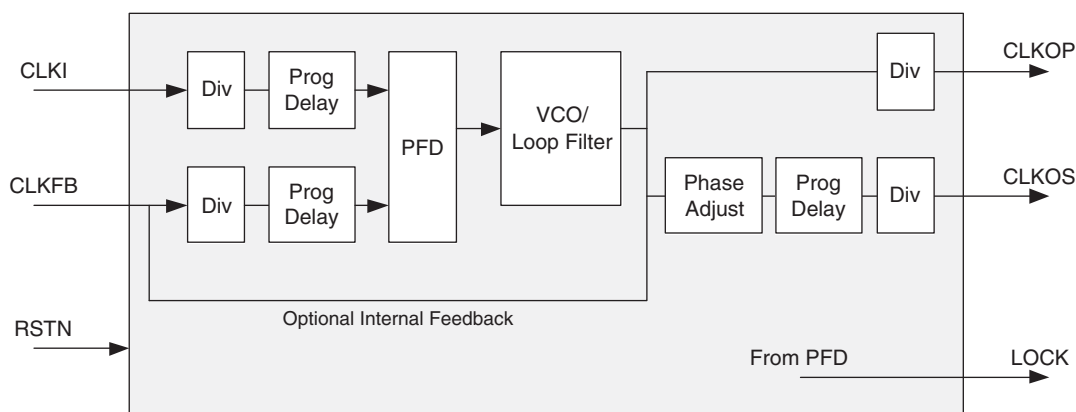
The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically.

The Phase Select block can modify the phase of the clock signal if desired. The Spread Spectrum block supports the modulation of the PLL output frequency. This reduces the peak energy in the fundamental and its harmonics providing for lower EMI (Electro Magnetic Interference).

The sysCLOCK PLL can be configured at power-up and then, if desired, reconfigured dynamically through the serial memory interface bus which connects with the on-chip system bus. For example, the user can select inputs, loop filters, divider setting, delay settings and phase shift settings. The user can also directly access the SMI bus through the routing.

The PLL clock input, from pin or routing, feeds into an input divider. There are four sources of feedback signal to the feedback divider: from the clock net, directly from the voltage controlled oscillator (VCO) output, from the routing or from an external pin. The signal from the input clock divider and the feedback divider are passed through the programmable delay before entering the phase frequency detector (PFD) unit. The output of this PFD is used to control the voltage controlled oscillator. There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

Figure 2-11. PLL Diagram



For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

Spread Spectrum Clocking (SSC)

The PLL supports spread spectrum clocking to reduce peak EMI by using “down-spread” modulation. The spread spectrum operation will vary the output frequency (at 30KHz to 500KHz) in a range that is between its nominal value, down to a frequency that is a programmable 1%, 2%, or 3% lower than normal.

Digital Locked Loop (DLLs)

In addition to PLLs, the LatticeSC devices have up to 12 DLLs per device. DLLs assist in the management of clocks and strobes. DLLs are well suited to applications where the clock may be stopped or transferring jitter from input to output is important, for example forward clocked interfaces. PLLs are good for applications requiring the lowest output jitter or jitter filtering. All DLL outputs are routed as primary/edge clock sources.

The DLL has two independent clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine phase shift and divider blocks to allow this output to be further modified, if required. The fine phase shift block allows the CLKOS output to be phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. LOCK output signal is asserted when the DLL is locked. The ALU HOLD signal setting allows users to freeze the DLL at its current delay setting.

- 8-bit SERDES Only
- 10-bit SERDES Only
- SONET (STS-12/STS-48)
- Gigabit Ethernet
- Fibre Channel
- XAUI
- Serial RapidIO
- PCI-Express
- Generic 8b10b

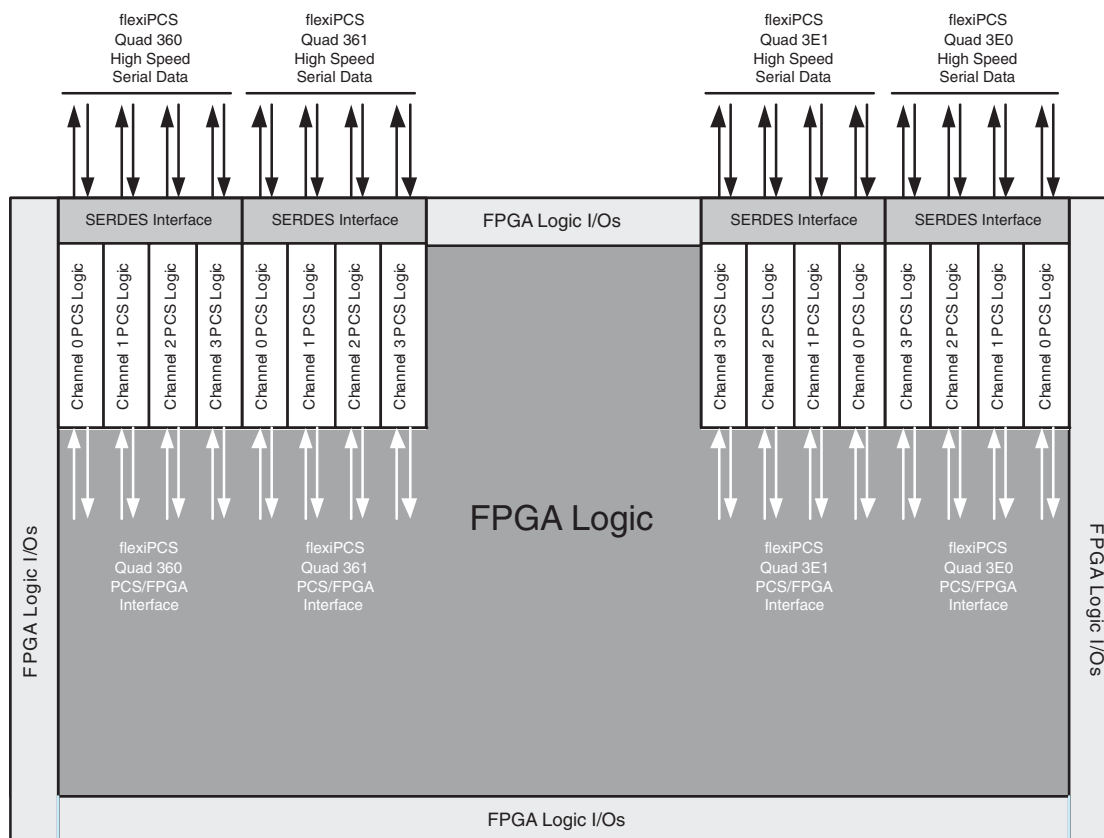
flexiPCS Quad

The flexiPCS logic is arranged in quads containing logic for four independent full-duplex data channels. Each device in the LatticeSC family has up to eight quads of flexiPCS logic. The LatticeSC Family Selection Guide table on the first page of this data sheet contains the number of flexiPCS channels present on the chip. Note that in some packages (particularly lower pin count packages), not all channels from all quads on a given device may be bonded to package pins.

Each quad supports up to four channels of full-duplex data and can be programmed into any one of several protocol based modes. Each quad requires its own reference clock which can be sourced externally or from the FPGA logic. The user can utilize between one and four channels in a quad, depending on the application.

Figure 2-30 shows an example of four flexiPCS quads in a LatticeSC device. Quads are labeled according to the address of their software controlled registers.

Figure 2-30. LatticeSC flexiPCS



Since each quad has its own reference clock, different quads can support different standards on the same chip. This feature makes the LatticeSC family of devices ideal for bridging between different standards.

Absolute Maximum Ratings

Supply Voltage V_{CC} , V_{CC12} , V_{DDIB} , V_{DDOB}	-0.5 to 1.6V
Supply Voltage V_{CCAUX} , V_{DDAX25} , V_{TT}	-0.5 to 2.75V
Supply Voltage V_{CCJ}	-0.5 to 3.6V
Supply Voltage V_{CCIO} (Banks 1, 4, 5)	-0.5 to 3.6V
Supply Voltage V_{CCIO} (Banks 2, 3, 6, 7)	-0.5 to 2.75V
Input or I/O Tristate Voltage Applied (Banks 1, 4, 5)	-0.5 to 3.6V
Input or I/O Tristate Voltage Applied (Banks 2, 3, 6, 7)	-0.5 to 2.75V
Storage Temperature (Ambient)	-65 to 150°C
Junction Temperature Under Bias (Tj)	+125°C

Notes:

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Undershoot and overshoot of -2V to (VIHMAX +2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}^5	Core Supply Voltage (Nominal 1.2V Operation)	0.95	1.26	V
V_{CCAUX}^6	Programmable I/O Auxiliary Supply Voltage	2.375	2.625	V
$V_{CCIO}^{1,2,5,6}$	Programmable I/O Driver Supply Voltage (Banks 1, 4, 5)	1.14	3.45	V
$V_{CCIO}^{1,2,5,6}$	Programmable I/O Driver Supply Voltage (Banks 2, 3, 6, 7)	1.14	2.625	V
$V_{CC12}^{4,5}$	Internal 1.2V Power Supply Voltage for Configuration Logic and FPGA PLL, SERDES PLL Power Supply Voltage and SERDES Analog Supply Voltage	1.14	1.26	V
V_{DDIB}	SERDES Input Buffer Supply Voltage	1.14	1.575	V
V_{DDOB}	SERDES Output Buffer Supply Voltage	1.14	1.575	V
V_{DDAX25}	SERDES Termination Auxiliary Supply Voltage	2.375	2.625	V
$V_{CCJ}^{1,5}$	Supply Voltage for IEEE 1149.1 Test Access Port	1.71	3.45	V
$V_{TT}^{2,3}$	Programmable I/O Termination Power Supply	0.5	$V_{CCAUX} - 0.5$	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	+85	C
t_{JIND}	Junction Temperature, Industrial Operation	-40	105	C

1. If V_{CCIO} or V_{CCJ} is set to 2.5V, they must be connected to the same power supply as V_{CCAUX} .
2. See recommended voltages by I/O standard in subsequent table.
3. When V_{TT} termination is not required, or used to provide the common mode termination voltage (V_{CMT}), these pins can be left unconnected on the device.
4. V_{CC12} cannot be lower than V_{CC} at any time. For 1.2V operation, it is recommended that the V_{CC} and V_{CC12} supplies be tied together with proper noise decoupling between the digital VCC and analog VCC12 supplies.
5. V_{CC} , V_{CCIO} (all banks), V_{CC12} and V_{CCJ} must reach their minimum values before configuration will proceed.
6. If V_{CCIO} for a bank is nominally 1.2V/1.5V/1.8V, then V_{CCAUX} must always be higher than V_{CCIO} during power up.

Figure 3-8. Read Mode with Input and Output Registers

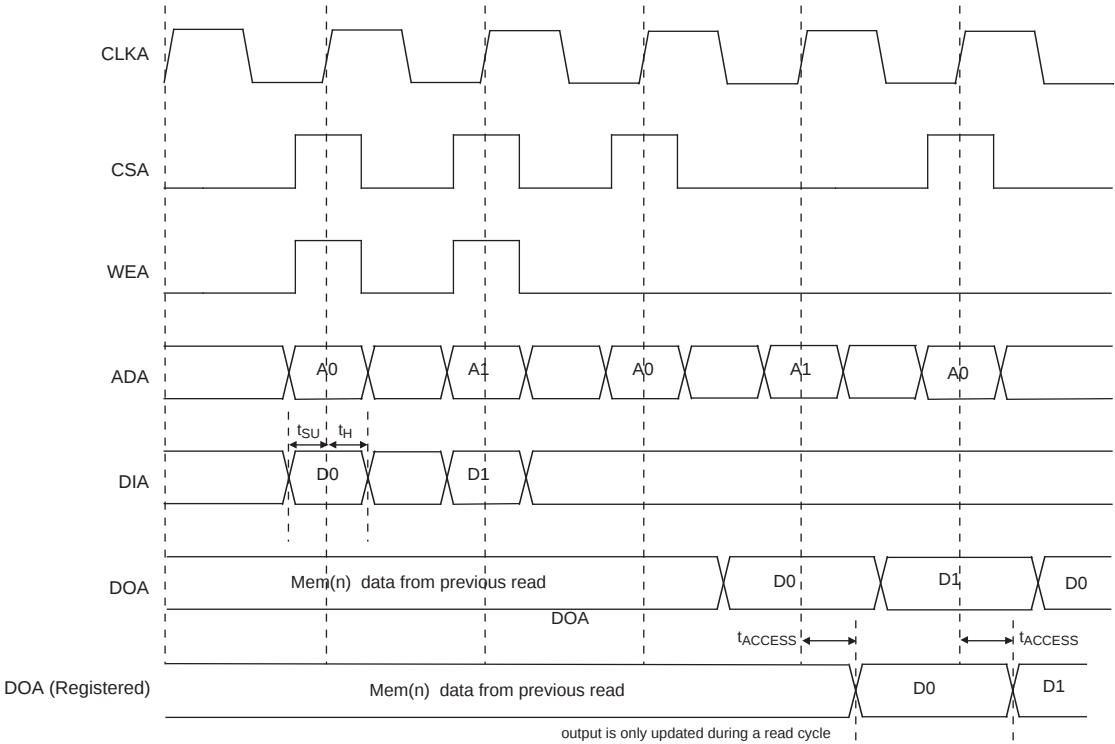
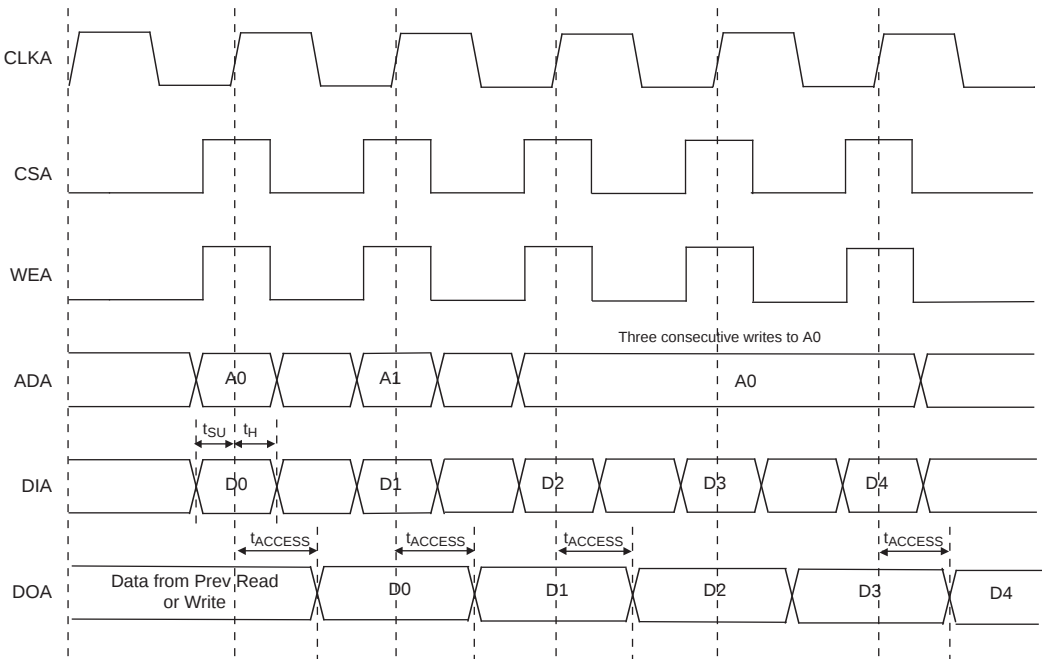


Figure 3-9. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

LatticeSC/M sysCONFIG Port Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
General Configuration Timing				
t_{SMODE}	M[3:0] Setup Time to INITN High	0	—	ns
t_{HMODE}	M[3:0] Hold Time from INITN High	600	—	ns
t_{RW}	RESETN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
t_{PGW}	PROGRAMN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
$f_{ESB_CLK_FRQ}$	System Bus ESB_CLK Frequency (No Wait States)	—	133	MHz
sysCONFIG Master Parallel Configuration Mode				
t_{SMB}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMB}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMB}	RCLK Low Time (Non-compressed Bitstreams)	0.5	0.5	CCLK periods
	RCLK Low Time (Compressed Bitstreams)	0.5	7.5	CCLK periods
t_{CHMB}	RCLK High Time	0.5	0.5	CCLK periods
sysCONFIG SPI Port				
t_{CFGX}	INITN High to CSCK Low	—	80	ns
t_{CSSPI}	INITN High to CSSPIN Low	0	2	μ s
t_{SCK}	CSCK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CSCK Low to Output Valid	—	15	ns
t_{CSPID}	CSSPIN Low to CSCK high Setup Time	—	15	ns
f_{MAXSPI}	Max CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN=0)	—	50	MHz
t_{SUSPI}	SOSPI/D0 Data Setup Time Before CSCK	7	—	ns
t_{HSPI}	SOSPI/D0 Data Hold Time After CSCK	2	—	ns
	Master Clock Frequency	Selected value - 30%	Selected value + 30%	MHz
	Duty Cycle	40	60	%
sysCONFIG Master Serial Configuration Mode				
t_{SMS}	DIN Setup Time	4.4	—	ns
t_{HMS}	DIN Hold Time	0	—	ns
f_{CMS}	CCLK Frequency (No Divider)	90	190	MHz
f_{C_DIV}	CCLK Frequency (Div 128)	0.70	1.48	MHz
t_D	CCLK to DOUT Delay	—	7.5	ns
sysCONFIG Master Parallel Configuration Mode				
t_{AVMP}	RCLK to Address Valid	—	10	ns
t_{SMP}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMP}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMP}	RCLK Low Time (Non-compressed Bitstream)	7.5	7.5	CCLK periods
	RCLK Low Time (Compressed Bitstream)	0.5	63.5	CCLK periods
t_{CHMP}	RCLK High Time	0.5	0.5	CCLK periods
t_{DMP}	CCLK to DOUT	—	7.5	ns

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
A29	RESP_URC	-		RESP_URC	-	
D26	VCC12	-		VCC12	-	
C30	A_REFCLKN_R	-		A_REFCLKN_R	-	
B30	A_REFCLKP_R	-		A_REFCLKP_R	-	
F24	A_VDDAX25_R	-		A_VDDAX25_R	-	
D25	VCC12	-		VCC12	-	
C28	A_VDDIB0_R	-		A_VDDIB0_R	-	
B28	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P
B27	A_HDINN0_R	-	PCS 3E0 CH 0 IN N	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
E25	VCC12	-		VCC12	-	
A28	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P
C27	A_VDDOB0_R	-		A_VDDOB0_R	-	
A27	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N
C26	A_VDDOB1_R	-		A_VDDOB1_R	-	
A26	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N
D24	VCC12	-		VCC12	-	
A25	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P
B26	A_HDINN1_R	-	PCS 3E0 CH 1 IN N	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
B25	A_HDINP1_R	-	PCS 3E0 CH 1 IN P	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
E24	VCC12	-		VCC12	-	
C25	A_VDDIB1_R	-		A_VDDIB1_R	-	
D23	VCC12	-		VCC12	-	
C24	A_VDDIB2_R	-		A_VDDIB2_R	-	
B24	A_HDINP2_R	-	PCS 3E0 CH 2 IN P	A_HDINP2_R	-	PCS 3E0 CH 2 IN P
B23	A_HDINN2_R	-	PCS 3E0 CH 2 IN N	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
E23	VCC12	-		VCC12	-	
A24	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
C23	A_VDDOB2_R	-		A_VDDOB2_R	-	
A23	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
C22	A_VDDOB3_R	-		A_VDDOB3_R	-	
A22	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
D22	VCC12	-		VCC12	-	
A21	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
B22	A_HDINN3_R	-	PCS 3E0 CH 3 IN N	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
B21	A_HDINP3_R	-	PCS 3E0 CH 3 IN P	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
E22	VCC12	-		VCC12	-	
C21	A_VDDIB3_R	-		A_VDDIB3_R	-	
G22	PT43D	1	HDC/SI	PT49D	1	HDC/SI
F22	PT43C	1	LDCN/SCS	PT49C	1	LDCN/SCS
B20	PT41B	1	D8/MPI_DATA8	PT49B	1	D8/MPI_DATA8
B19	PT41A	1	CS1/MPI_CS1	PT49A	1	CS1/MPI_CS1
A20	PT40D	1	D9/MPI_DATA9	PT47D	1	D9/MPI_DATA9
A19	PT40C	1	D10/MPI_DATA10	PT47C	1	D10/MPI_DATA10
D19	PT39B	1	CS0N/MPI_CS0N	PT47B	1	CS0N/MPI_CS0N
D18	PT39A	1	RDN/MPI_STRB_N	PT47A	1	RDN/MPI_STRB_N

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P22	VCCIO2	-		VCCIO2	-	
R22	VCCIO2	-		VCCIO2	-	
AA23	VCCIO3	-		VCCIO3	-	
AA24	VCCIO3	-		VCCIO3	-	
AB23	VCCIO3	-		VCCIO3	-	
AB24	VCCIO3	-		VCCIO3	-	
T22	VCCIO3	-		VCCIO3	-	
U22	VCCIO3	-		VCCIO3	-	
V22	VCCIO3	-		VCCIO3	-	
W22	VCCIO3	-		VCCIO3	-	
Y22	VCCIO3	-		VCCIO3	-	
Y23	VCCIO3	-		VCCIO3	-	
Y24	VCCIO3	-		VCCIO3	-	
AB16	VCCIO4	-		VCCIO4	-	
AB17	VCCIO4	-		VCCIO4	-	
AB18	VCCIO4	-		VCCIO4	-	
AB19	VCCIO4	-		VCCIO4	-	
AB20	VCCIO4	-		VCCIO4	-	
AC20	VCCIO4	-		VCCIO4	-	
AC21	VCCIO4	-		VCCIO4	-	
AC22	VCCIO4	-		VCCIO4	-	
AD20	VCCIO4	-		VCCIO4	-	
AD21	VCCIO4	-		VCCIO4	-	
AD22	VCCIO4	-		VCCIO4	-	
AB11	VCCIO5	-		VCCIO5	-	
AB12	VCCIO5	-		VCCIO5	-	
AB13	VCCIO5	-		VCCIO5	-	
AB14	VCCIO5	-		VCCIO5	-	
AB15	VCCIO5	-		VCCIO5	-	
AC10	VCCIO5	-		VCCIO5	-	
AC11	VCCIO5	-		VCCIO5	-	
AC9	VCCIO5	-		VCCIO5	-	
AD10	VCCIO5	-		VCCIO5	-	
AD11	VCCIO5	-		VCCIO5	-	
AD9	VCCIO5	-		VCCIO5	-	
AA7	VCCIO6	-		VCCIO6	-	
AA8	VCCIO6	-		VCCIO6	-	
AB7	VCCIO6	-		VCCIO6	-	
AB8	VCCIO6	-		VCCIO6	-	
T9	VCCIO6	-		VCCIO6	-	
U9	VCCIO6	-		VCCIO6	-	
V9	VCCIO6	-		VCCIO6	-	
W9	VCCIO6	-		VCCIO6	-	
Y7	VCCIO6	-		VCCIO6	-	
Y8	VCCIO6	-		VCCIO6	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P17	VCC	-		VCC	-	
P19	VCC	-		VCC	-	
R13	VCC	-		VCC	-	
R15	VCC	-		VCC	-	
R18	VCC	-		VCC	-	
R20	VCC	-		VCC	-	
T13	VCC	-		VCC	-	
T14	VCC	-		VCC	-	
T16	VCC	-		VCC	-	
T17	VCC	-		VCC	-	
T19	VCC	-		VCC	-	
T20	VCC	-		VCC	-	
U13	VCC	-		VCC	-	
U14	VCC	-		VCC	-	
U16	VCC	-		VCC	-	
U17	VCC	-		VCC	-	
U19	VCC	-		VCC	-	
U20	VCC	-		VCC	-	
V13	VCC	-		VCC	-	
V15	VCC	-		VCC	-	
V18	VCC	-		VCC	-	
V20	VCC	-		VCC	-	
W14	VCC	-		VCC	-	
W16	VCC	-		VCC	-	
W17	VCC	-		VCC	-	
W19	VCC	-		VCC	-	
Y13	VCC	-		VCC	-	
Y15	VCC	-		VCC	-	
Y16	VCC	-		VCC	-	
Y17	VCC	-		VCC	-	
Y18	VCC	-		VCC	-	
Y20	VCC	-		VCC	-	
C17	VCCIO1	-		VCCIO1	-	
D16	VCCIO1	-		VCCIO1	-	
F15	VCCIO1	-		VCCIO1	-	
F24	VCCIO1	-		VCCIO1	-	
G18	VCCIO1	-		VCCIO1	-	
G9	VCCIO1	-		VCCIO1	-	
J11	VCCIO1	-		VCCIO1	-	
J19	VCCIO1	-		VCCIO1	-	
K14	VCCIO1	-		VCCIO1	-	
K22	VCCIO1	-		VCCIO1	-	
G4	VCCIO2	-		VCCIO2	-	
J7	VCCIO2	-		VCCIO2	-	
K3	VCCIO2	-		VCCIO2	-	
L10	VCCIO2	-		VCCIO2	-	
M6	VCCIO2	-		VCCIO2	-	
N4	VCCIO2	-		VCCIO2	-	
P9	VCCIO2	-		VCCIO2	-	
R7	VCCIO2	-		VCCIO2	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AL11	GND	-		GND	-	
AL17	GND	-		GND	-	
AL21	GND	-		GND	-	
AL27	GND	-		GND	-	
AL5	GND	-		GND	-	
AM14	GND	-		GND	-	
AM18	GND	-		GND	-	
AM24	GND	-		GND	-	
AM30	GND	-		GND	-	
AM8	GND	-		GND	-	
AN1	GND	-		GND	-	
AN34	GND	-		GND	-	
AP2	GND	-		GND	-	
AP33	GND	-		GND	-	
B1	GND	-		GND	-	
B34	GND	-		GND	-	
C11	GND	-		GND	-	
C12	GND	-		GND	-	
C13	GND	-		GND	-	
C14	GND	-		GND	-	
C17	GND	-		GND	-	
C21	GND	-		GND	-	
C22	GND	-		GND	-	
C23	GND	-		GND	-	
C24	GND	-		GND	-	
C26	GND	-		GND	-	
C27	GND	-		GND	-	
C30	GND	-		GND	-	
C31	GND	-		GND	-	
C4	GND	-		GND	-	
C5	GND	-		GND	-	
C8	GND	-		GND	-	
C9	GND	-		GND	-	
D18	GND	-		GND	-	
E32	GND	-		GND	-	
E4	GND	-		GND	-	
F19	GND	-		GND	-	
G16	GND	-		GND	-	
G29	GND	-		GND	-	
G7	GND	-		GND	-	
H3	GND	-		GND	-	
H31	GND	-		GND	-	
J10	GND	-		GND	-	
J15	GND	-		GND	-	
J26	GND	-		GND	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AL4	PR117B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AL3	PR117A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD10	PR116D	3	
AD9	PR116C	3	
AH4	PR116B	3	
AJ4	PR116A	3	
AK5	PR115D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AJ5	PR115C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AM1	PR115B	3	
AL1	PR115A	3	
AH5	PR112D	3	
AG5	PR112C	3	
AL2	PR112B	3	
AK2	PR112A	3	
AB9	PR109D	3	
AC9	PR109C	3	
AH1	PR109B	3	
AG1	PR109A	3	
AE8	PR107D	3	VREF2_3
AD8	PR107C	3	
AJ3	PR107B	3	
AH3	PR107A	3	
AD7	PR104D	3	
AC7	PR104C	3	
AJ2	PR104B	3	
AH2	PR104A	3	
AF6	PR103D	3	
AF5	PR103C	3	
AF4	PR103B	3	
AE4	PR103A	3	
AD6	PR99D	3	
AC6	PR99C	3	
AG2	PR99B	3	
AF2	PR99A	3	
AC8	PR98D	3	
AB8	PR98C	3	
AK1	PR98B	3	
AJ1	PR98A	3	
AB10	PR96D	3	
AA10	PR96C	3	
AF3	PR96B	3	
AE3	PR96A	3	
AE5	PR94D	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
L21	PT55D	1	A16/MPI_ADDR30
L20	PT55C	1	D13/MPI_DATA13
D20	PT55B	1	A15/MPI_ADDR29
E20	PT55A	1	A17/MPI_ADDR31
L19	PT54D	1	A19/MPI_TSIZ1
K19	PT54C	1	A20/MPI_BDIP
D21	PT54B	1	A18/MPI_TSIZ0
E21	PT54A	1	MPI_TEA
M20	PT51D	1	D14/MPI_DATA14
M19	PT51C	1	DP1/MPI_PAR1
F21	PT51B	1	A21/MPI_BURST
G21	PT51A	1	D15/MPI_DATA15
H24	B_REFCLKP_L	-	
J24	B_REFCLKN_L	-	
L22	VCC12	-	
E26	B_VDDIB3_L	-	
G22	VCC12	-	
E22	B_HDINP3_L	-	PCS 361 CH 3 IN P
F22	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
L24	VCC12	-	
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D22	B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D23	B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
K24	VCC12	-	
F23	B_HDINN2_L	-	PCS 361 CH 2 IN N
E23	B_HDINP2_L	-	PCS 361 CH 2 IN P
D26	B_VDDIB2_L	-	
G23	VCC12	-	
D27	B_VDDIB1_L	-	
G24	VCC12	-	
E24	B_HDINP1_L	-	PCS 361 CH 1 IN P
F24	B_HDINN1_L	-	PCS 361 CH 1 IN N
A23	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
L25	VCC12	-	
B23	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
D24	B_VDDOB1_L	-	
B24	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
D25	B_VDDOB0_L	-	
A24	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
K25	VCC12	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P38	PL26B	7		PL40B	7	
N35	PL26C	7		PL40C	7	
N36	PL26D	7		PL40D	7	
N39	PL29A	7		PL43A	7	
P39	PL29B	7		PL43B	7	
R34	PL29C	7	VREF1_7	PL43C	7	VREF1_7
T34	PL29D	7	DIFFR_7	PL43D	7	DIFFR_7
L41	PL30A	7		PL44A	7	
M41	PL30B	7		PL44B	7	
W29	PL30C	7		PL44C	7	
Y29	PL30D	7		PL44D	7	
L42	PL31A	7		PL45A	7	
M42	PL31B	7		PL45B	7	
U32	PL31C	7		PL45C	7	
V32	PL31D	7		PL45D	7	
R37	PL33A	7		PL47A	7	
T37	PL33B	7		PL47B	7	
M36	PL33C	7		PL47C	7	
M37	PL33D	7		PL47D	7	
P40	PL34A	7		PL48A	7	
N40	PL34B	7		PL48B	7	
R35	PL34C	7		PL48C	7	
T35	PL34D	7		PL48D	7	
N41	PL35A	7		PL49A	7	
P41	PL35B	7		PL49B	7	
V33	PL35C	7		PL49C	7	
U33	PL35D	7		PL49D	7	
R38	PL37A	7		PL51A	7	
T38	PL37B	7		PL51B	7	
R36	PL37C	7		PL51C	7	
T36	PL37D	7		PL51D	7	
N42	PL38A	7		PL52A	7	
P42	PL38B	7		PL52B	7	
Y31	PL38C	7		PL52C	7	
AA31	PL38D	7		PL52D	7	
U37	PL39A	7		PL53A	7	
V37	PL39B	7		PL53B	7	
U34	PL39C	7		PL53C	7	
V34	PL39D	7		PL53D	7	
U39	PL41A	7		PL55A	7	
T39	PL41B	7		PL55B	7	
V35	PL41C	7		PL55C	7	
W35	PL41D	7		PL55D	7	
R41	PL42A	7		PL56A	7	
T41	PL42B	7		PL56B	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AL23	PB56D	5		PB58D	5	
AW24	PB57A	5		PB61A	5	
AW23	PB57B	5		PB61B	5	
AN23	PB57C	5		PB61C	5	
AP23	PB57D	5		PB61D	5	
AY23	PB59A	5		PB63A	5	
AY24	PB59B	5		PB63B	5	
AU23	PB59C	5		PB63C	5	
AU22	PB59D	5		PB63D	5	
AV23	PB60A	5		PB66A	5	
AV22	PB60B	5		PB66B	5	
AM22	PB60C	5		PB66C	5	
AL22	PB60D	5		PB66D	5	
BA23	PB61A	5		PB69A	5	
BA22	PB61B	5		PB69B	5	
AN22	PB61C	5		PB69C	5	
AP22	PB61D	5		PB69D	5	
BB23	PB63A	5		PB71A	5	
BB22	PB63B	5		PB71B	5	
AT22	PB63C	5		PB71C	5	
AR22	PB63D	5		PB71D	5	
BB21	PB65A	4		PB73A	4	
BB20	PB65B	4		PB73B	4	
AR21	PB65C	4		PB73C	4	
AT21	PB65D	4		PB73D	4	
BA21	PB66A	4		PB75A	4	
BA20	PB66B	4		PB75B	4	
AP21	PB66C	4		PB75C	4	
AN21	PB66D	4		PB75D	4	
AV21	PB67A	4		PB78A	4	
AV20	PB67B	4		PB78B	4	
AM21	PB67C	4		PB78C	4	
AL21	PB67D	4		PB78D	4	
AY20	PB69A	4		PB81A	4	
AY19	PB69B	4		PB81B	4	
AU21	PB69C	4		PB81C	4	
AU20	PB69D	4		PB81D	4	
AW20	PB70A	4		PB83A	4	
AW19	PB70B	4		PB83B	4	
AP20	PB70C	4		PB83C	4	
AN20	PB70D	4		PB83D	4	
BB19	PB71A	4		PB86A	4	
BB18	PB71B	4		PB86B	4	
AM20	PB71C	4		PB86C	4	
AL20	PB71D	4		PB86D	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AE1	PR74A	3		PR88A	3	
AF12	PR73D	3		PR87D	3	
AE12	PR73C	3		PR87C	3	
AF2	PR73B	3		PR87B	3	
AE2	PR73A	3		PR87A	3	
AF11	PR72D	3		PR86D	3	
AE11	PR72C	3		PR86C	3	
AF5	PR72B	3		PR86B	3	
AE5	PR72A	3		PR86A	3	
AF10	PR69D	3		PR83D	3	
AE10	PR69C	3		PR83C	3	
AD1	PR69B	3		PR83B	3	
AC1	PR69A	3		PR83A	3	
AF9	PR68D	3		PR82D	3	
AE9	PR68C	3		PR82C	3	
AD2	PR68B	3		PR82B	3	
AC2	PR68A	3		PR82A	3	
AF6	PR67D	3		PR81D	3	
AE6	PR67C	3		PR81C	3	
AD3	PR67B	3		PR81B	3	
AC3	PR67A	3		PR81A	3	
AE8	PR65D	3		PR79D	3	
AD8	PR65C	3		PR79C	3	
AD4	PR65B	3		PR79B	3	
AC4	PR65A	3		PR79A	3	
AE7	PR64D	3		PR78D	3	
AD7	PR64C	3		PR78C	3	
AD5	PR64B	3		PR78B	3	
AC5	PR64A	3		PR78A	3	
AD6	PR63D	3		PR77D	3	
AC6	PR63C	3		PR77C	3	
AB1	PR63B	3		PR77B	3	
AA1	PR63A	3		PR77A	3	
AD9	PR61D	3		PR75D	3	
AC9	PR61C	3		PR75C	3	
AB2	PR61B	3		PR75B	3	
AA2	PR61A	3		PR75A	3	
AD14	PR60D	3		PR74D	3	
AC14	PR60C	3		PR74C	3	
AB5	PR60B	3		PR74B	3	
AA5	PR60A	3		PR74A	3	
AD10	PR59D	3		PR73D	3	
AC10	PR59C	3		PR73C	3	
Y1	PR59B	3		PR73B	3	
W1	PR59A	3		PR73A	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB6	PR57D	3		PR71D	3	
AA6	PR57C	3		PR71C	3	
Y2	PR57B	3		PR71B	3	
W2	PR57A	3		PR71A	3	
AB7	PR56D	3		PR70D	3	
AA7	PR56C	3		PR70C	3	
Y3	PR56B	3		PR70B	3	
W3	PR56A	3		PR70A	3	
AC11	PR55D	3		PR69D	3	
AB11	PR55C	3	VREF1_3	PR69C	3	VREF1_3
Y4	PR55B	3		PR69B	3	
W4	PR55A	3		PR69A	3	
AB8	PR52D	3	PCLKC3_2	PR66D	3	PCLKC3_2
AA8	PR52C	3	PCLKT3_2	PR66C	3	PCLKT3_2
Y5	PR52B	3		PR66B	3	
W5	PR52A	3		PR66A	3	
AC12	PR51D	3	PCLKC3_3	PR65D	3	PCLKC3_3
AB12	PR51C	3	PCLKT3_3	PR65C	3	PCLKT3_3
V1	PR51B	3		PR65B	3	
U1	PR51A	3		PR65A	3	
W7	PR50D	3	PCLKC3_1	PR64D	3	PCLKC3_1
V7	PR50C	3	PCLKT3_1	PR64C	3	PCLKT3_1
V2	PR50B	3	PCLKC3_0	PR64B	3	PCLKC3_0
U2	PR50A	3	PCLKT3_0	PR64A	3	PCLKT3_0
AB9	PR48D	2	PCLKC2_2	PR62D	2	PCLKC2_2
AA9	PR48C	2	PCLKT2_2	PR62C	2	PCLKT2_2
T1	PR48B	2	PCLKC2_0	PR62B	2	PCLKC2_0
R1	PR48A	2	PCLKT2_0	PR62A	2	PCLKT2_0
AB10	PR47D	2	PCLKC2_3	PR61D	2	PCLKC2_3
AA10	PR47C	2	PCLKT2_3	PR61C	2	PCLKT2_3
U3	PR47B	2	PCLKC2_1	PR61B	2	PCLKC2_1
T3	PR47A	2	PCLKT2_1	PR61A	2	PCLKT2_1
Y9	PR46D	2		PR60D	2	
W9	PR46C	2		PR60C	2	
V5	PR46B	2		PR60B	2	
U5	PR46A	2		PR60A	2	
AA11	PR43D	2		PR57D	2	
Y11	PR43C	2		PR57C	2	
Y6	PR43B	2		PR57B	2	
W6	PR43A	2		PR57A	2	
Y10	PR42D	2		PR56D	2	
W10	PR42C	2		PR56C	2	
T2	PR42B	2		PR56B	2	
R2	PR42A	2		PR56A	2	
W8	PR41D	2		PR55D	2	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
V8	PR41C	2		PR55C	2	
T4	PR41B	2		PR55B	2	
U4	PR41A	2		PR55A	2	
V9	PR39D	2		PR53D	2	
U9	PR39C	2		PR53C	2	
V6	PR39B	2		PR53B	2	
U6	PR39A	2		PR53A	2	
AA12	PR38D	2		PR52D	2	
Y12	PR38C	2		PR52C	2	
P1	PR38B	2		PR52B	2	
N1	PR38A	2		PR52A	2	
T7	PR37D	2		PR51D	2	
R7	PR37C	2		PR51C	2	
T5	PR37B	2		PR51B	2	
R5	PR37A	2		PR51A	2	
U10	PR35D	2		PR49D	2	
V10	PR35C	2		PR49C	2	
P2	PR35B	2		PR49B	2	
N2	PR35A	2		PR49A	2	
T8	PR34D	2		PR48D	2	
R8	PR34C	2		PR48C	2	
N3	PR34B	2		PR48B	2	
P3	PR34A	2		PR48A	2	
M6	PR33D	2		PR47D	2	
M7	PR33C	2		PR47C	2	
T6	PR33B	2		PR47B	2	
R6	PR33A	2		PR47A	2	
V11	PR31D	2		PR45D	2	
U11	PR31C	2		PR45C	2	
M1	PR31B	2		PR45B	2	
L1	PR31A	2		PR45A	2	
Y14	PR30D	2		PR44D	2	
W14	PR30C	2		PR44C	2	
M2	PR30B	2		PR44B	2	
L2	PR30A	2		PR44A	2	
T9	PR29D	2	DIFFR_2	PR43D	2	DIFFR_2
R9	PR29C	2	VREF1_2	PR43C	2	VREF1_2
P4	PR29B	2		PR43B	2	
N4	PR29A	2		PR43A	2	
N7	PR26D	2		PR40D	2	
N8	PR26C	2		PR40C	2	
P5	PR26B	2		PR40B	2	
N5	PR26A	2		PR40A	2	
K7	PR25D	2		PR38D	2	
J7	PR25C	2		PR38C	2	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AC24	GND	-		GND	-	
AC26	GND	-		GND	-	
AC35	GND	-		GND	-	
AC8	GND	-		GND	-	
AD12	GND	-		GND	-	
AD16	GND	-		GND	-	
AD18	GND	-		GND	-	
AD20	GND	-		GND	-	
AD23	GND	-		GND	-	
AD25	GND	-		GND	-	
AD27	GND	-		GND	-	
AD31	GND	-		GND	-	
AE17	GND	-		GND	-	
AE19	GND	-		GND	-	
AE24	GND	-		GND	-	
AE26	GND	-		GND	-	
AE3	GND	-		GND	-	
AE39	GND	-		GND	-	
AF18	GND	-		GND	-	
AF20	GND	-		GND	-	
AF23	GND	-		GND	-	
AF25	GND	-		GND	-	
AF36	GND	-		GND	-	
AF7	GND	-		GND	-	
AG11	GND	-		GND	-	
AG16	GND	-		GND	-	
AG19	GND	-		GND	-	
AG24	GND	-		GND	-	
AG27	GND	-		GND	-	
AG32	GND	-		GND	-	
AH15	GND	-		GND	-	
AH28	GND	-		GND	-	
AH4	GND	-		GND	-	
AH40	GND	-		GND	-	
AJ35	GND	-		GND	-	
AJ8	GND	-		GND	-	
AK12	GND	-		GND	-	
AK31	GND	-		GND	-	
AL13	GND	-		GND	-	
AL19	GND	-		GND	-	
AL24	GND	-		GND	-	
AL3	GND	-		GND	-	
AL30	GND	-		GND	-	
AL39	GND	-		GND	-	
AM16	GND	-		GND	-	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-7FC1152C ¹	-7	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-7FC1704C ¹	-7	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-7FC1152C ¹	-7	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FC1704C ¹	-7	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-6FF1152C	-6	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-5FF1152C	-5	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-6FF1704C	-6	Organic fcBGA	1704	COM	115.2
LFSC3GA115E-5FF1704C	-5	Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).