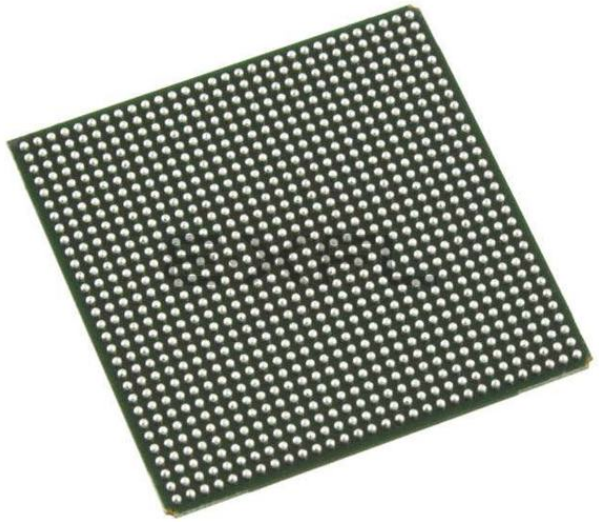
Lattice Semiconductor Corporation - LFSCM3GA15EP1-6F900C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3750
Number of Logic Elements/Cells	15000
Total RAM Bits	1054720
Number of I/O	300
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga15ep1-6f900c

Table 1-1. LatticeSC Family Selection Guide[1]

Device	SC15	SC25	SC40	SC80	SC115
LUT4s (K)	15	25	40	80	115
sysMEM Blocks (18Kb)	56	104	216	308	424
Embedded Memory (Mbits)	1.03	1.92	3.98	5.68	7.8
Max. Distributed Memory (Mbits)	0.24	0.41	0.65	1.28	1.84
Number of 3.8Gbps SERDES (Max.)	8	16	16	32	32
DLLs	12	12	12	12	12
Analog PLLs	8	8	8	8	8
MACO Blocks	4	6	10	10	12
Package I/O/SERDES Combinations (1mm ball pitch)					
256-ball fpBGA (17 x 17mm)	139/4				
900-ball fpBGA (31 x 31mm)	300/8	378/8			
1020-ball fcBGA (33 x 33mm)[2]		476/16	562/16		
1152-ball fcBGA (35 x 35mm)[3]			604/16	660/16	660/16
1704-ball fcBGA (42.5 x 42.5mm)[3]				904/32	942/32

1. The information in this preliminary data sheet is by definition not final and subject to change. Please consult the Lattice web site and your local Lattice sales office to ensure you have the latest information regarding the specifications for these products as you make critical design decisions.
2. Organic fcBGA converted to organic fcBGA revision 2 per PCN #02A-10.
3. Ceramic fcBGA converted to organic fcBGA per PCN #01A-10.

The LatticeSCM devices add MACO-enabled IP functionality to the base LatticeSC devices. Table 1-2 shows the type and number of each pre-engineered IP core.

Table 1-2. LatticeSCM Family

Device	SCM15	SCM25	SCM40	SCM80	SCM115
flexiMAC Blocks • 1GbE Mode • 10GbE Mode • PCI Express Mode	1	2	2	2	4
SPI4.2 Blocks	1	2	2	2	2
Memory Controller Blocks • DDR/DDR2 DRAM Mode • QDR II/II+ SRAM Mode • RLDRAM I • RLDRAM II CIO/SIO	1	2	2	2	2
Low-Speed CDR Blocks	0	0	2	2	2
PCI Express LTSSM (PHY) Blocks	1	0	2	2	2

Note: See each IP core user's guide for more information about support for specific LatticeSCM devices.

Introduction

The LatticeSC family of FPGAs combines a high-performance FPGA fabric, high-speed SERDES, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated in a state of the art technology to provide one of the highest performing FPGAs in the industry.

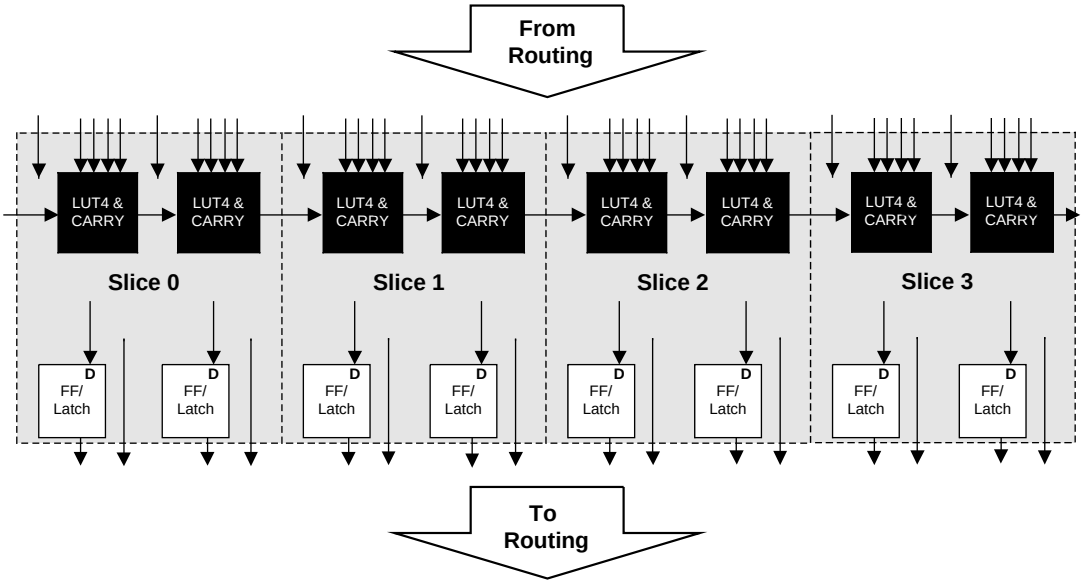
This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding sub-layer), up to 7.8 Mbits of sysMEM embedded block RAM, dedicated logic to support system level standards such as RAPIDIO, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. The devices in this family feature clock multiply, divide and phase shift PLLs, numerous

PFU Blocks

The core of the LatticeSC devices consists of PFU blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-2. PFU Diagram

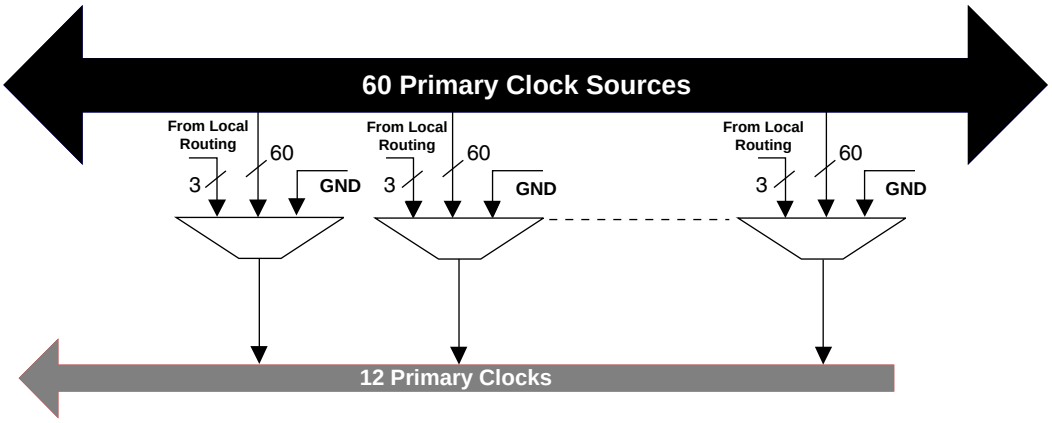


Slice

Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to implement 5, 6, 7 and 8 Input LUTs (LUT5, LUT6, LUT7 and LUT8). There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

Figure 2-6. Per Quadrant Clock Selection



Note: GND is available to switch off the network.

Secondary Clocks

In addition to the primary clock network and edge clocks the LatticeSC devices also contain a secondary clock network. Built of X6 style routing elements this secondary clock network is ideal for routing slower speed clock and control signals throughout the device preserving high-speed clock networks for the most timing critical signals.

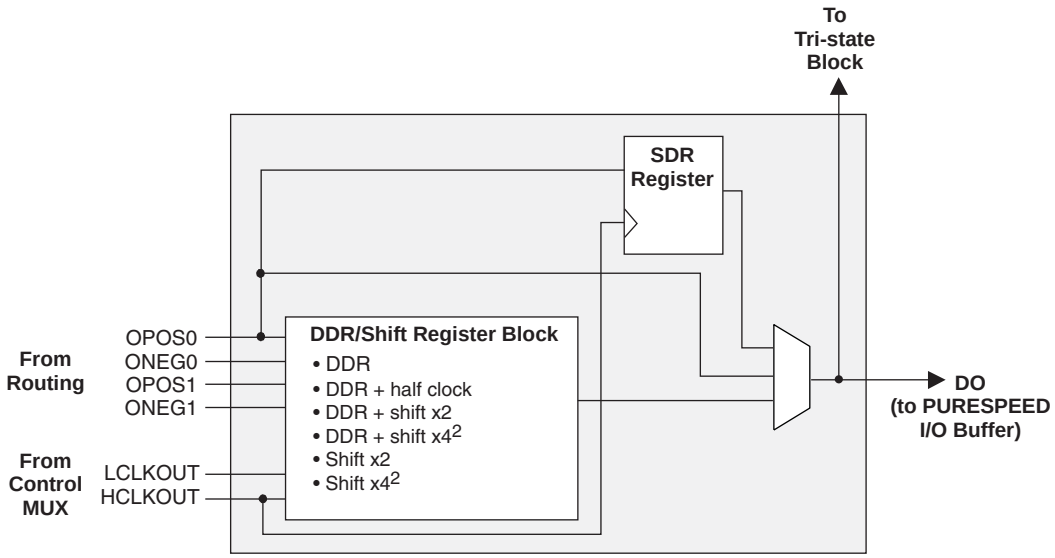
Edge Clocks

LatticeSC devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are eight edge clocks per bank for the top and bottom of the device. The left and right sides have eight edge clocks per side for both banks located on that side. Figure 2-7 shows the arrangement of edge clocks.

Edge clock resources can be driven from a variety of sources. Edge clock resources can be driven from:

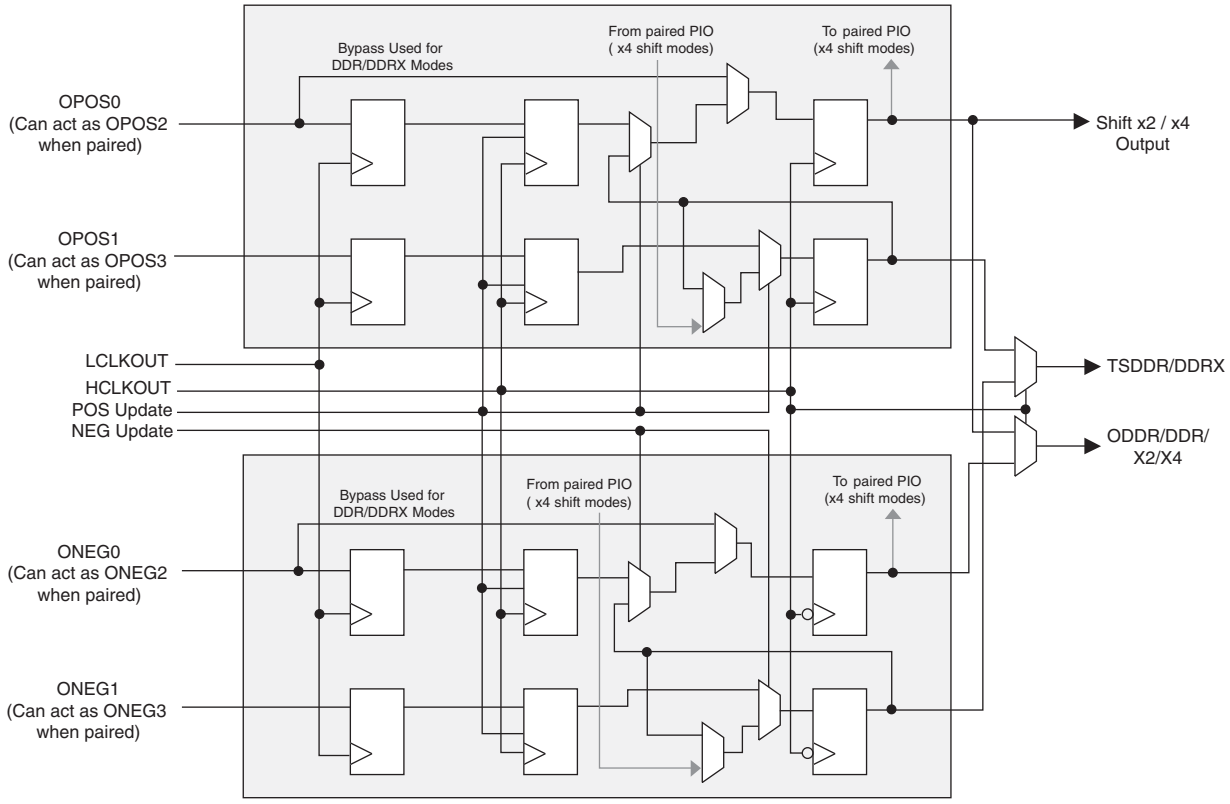
- Edge clock PIOs in the same bank
- Primary clock PIOs in the same bank
- Routing
- Adjacent PLLs and DLLs
- ELSR output from the clock divider

Figure 2-22. Output Register Block[1]



Notes:
1. CE, Update, Set and Reset not shown for clarity.
2. By four shift modes utilizes DDR/Shift register block from paired PIO.
3. DDR/Shift register block shared with tristate block.

Figure 2-23. Output/Tristate DDR/Shift Register Block



LatticeSC/M Family Data Sheet DC and Switching Characteristics

December 2011 **Data Sheet DS1004**

Absolute Maximum Ratings

Supply Voltage V_{CC}, V_{CC12}, V_{DDIB}, V_{DDOB} . . . . . -0.5 to 1.6V

Supply Voltage V_{CCAUX}, V_{DDAX25}, V_{TT} . . . . . -0.5 to 2.75V

Supply Voltage V_{CCJ} . . . . . -0.5 to 3.6V

Supply Voltage V_{CCIO} (Banks 1, 4, 5) . . . . . -0.5 to 3.6V

Supply Voltage V_{CCIO} (Banks 2, 3, 6, 7) . . . . . -0.5 to 2.75V

Input or I/O Tristate Voltage Applied (Banks 1, 4, 5) . . . . . -0.5 to 3.6V

Input or I/O Tristate Voltage Applied (Banks 2, 3, 6, 7) . . . . . -0.5 to 2.75V

Storage Temperature (Ambient) . . . . . -65 to 150°C

Junction Temperature Under Bias (Tj) . . . . . +125°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Undershoot and overshoot of -2V to (VIHMAX +2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}[5]	Core Supply Voltage (Nominal 1.2V Operation)	0.95	1.26	V
V_{CCAUX}[6]	Programmable I/O Auxiliary Supply Voltage	2.375	2.625	V
V_{CCIO}[1, 2, 5, 6]	Programmable I/O Driver Supply Voltage (Banks 1, 4, 5)	1.14	3.45	V
V_{CCIO}[1, 2, 5, 6]	Programmable I/O Driver Supply Voltage (Banks 2, 3, 6, 7)	1.14	2.625	V
V_{CC12}[4, 5]	Internal 1.2V Power Supply Voltage for Configuration Logic and FPGA PLL, SERDES PLL Power Supply Voltage and SERDES Analog Supply Voltage	1.14	1.26	V
V_{DDIB}	SERDES Input Buffer Supply Voltage	1.14	1.575	V
V_{DDOB}	SERDES Output Buffer Supply Voltage	1.14	1.575	V
V_{DDAX25}	SERDES Termination Auxiliary Supply Voltage	2.375	2.625	V
V_{CCJ}[1, 5]	Supply Voltage for IEEE 1149.1 Test Access Port	1.71	3.45	V
V_{TT}[2, 3]	Programmable I/O Termination Power Supply	0.5	V_{CCAUX} - 0.5	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	+85	C
t_{JIND}	Junction Temperature, Industrial Operation	-40	105	C

1. If V_{CCIO} or V_{CCJ} is set to 2.5V, they must be connected to the same power supply as V_{CCAUX}.
2. See recommended voltages by I/O standard in subsequent table.
3. When V_{TT} termination is not required, or used to provide the common mode termination voltage (V_{CMT}), these pins can be left unconnected on the device.
4. V_{CC12} cannot be lower than V_{CC} at any time. For 1.2V operation, it is recommended that the V_{CC} and V_{CC12} supplies be tied together with proper noise decoupling between the digital VCC and analog VCC12 supplies.
5. V_{CC}, V_{CCIO} (all banks), V_{CC12} and V_{CCJ} must reach their minimum values before configuration will proceed.
6. If V_{CCIO} for a bank is nominally 1.2V/1.5V/1.8V, then V_{CCAUX} must always be higher than V_{CCIO} during power up.

LatticeSC/M Family Timing Adders

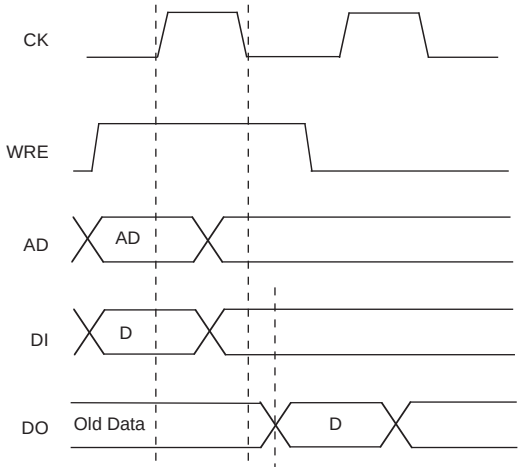
Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Input Adjusters								
LVDS	LVDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
RSDS	RSDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
BLVDS25	BLVDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
MLVDS25	MLVDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
LVPECL33	LVPECL	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
HSTL18_I	HSTL_18 class I	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL18_II	HSTL_18 class II	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL18_III	HSTL_18 class III	-0.016	-0.018	0.008	0.003	0.032	0.023	ns
HSTL18_IV	HSTL_18 class IV	-0.016	-0.018	0.008	0.003	0.032	0.023	ns
HSTL18D_I	Differential HSTL 18 class I	0.006	0.001	0.029	0.024	0.052	0.046	ns
HSTL18D_II	Differential HSTL 18 class II	0.006	0.001	0.029	0.024	0.052	0.046	ns
HSTL15_I	HSTL_15 class I	-0.005	-0.016	0.026	-0.001	0.057	0.014	ns
HSTL15_II	HSTL_15 class II	-0.005	-0.016	0.026	-0.001	0.057	0.014	ns
HSTL15_III	HSTL_15 class III	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL15_IV	HSTL_15 class IV	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL15D_I	Differential HSTL 15 class I	-0.021	-0.022	0.001	-0.009	0.022	0.003	ns
HSTL15D_II	Differential HSTL 15 class II	-0.021	-0.022	0.001	-0.009	0.022	0.003	ns
SSTL33_I	SSTL_3 class I	-0.036	-0.061	-0.181	-0.313	-0.326	-0.565	ns
SSTL33_II	SSTL_3 class II	-0.036	-0.061	-0.181	-0.313	-0.326	-0.565	ns
SSTL33D_I	Differential SSTL_3 class I	0.012	0.012	0.034	0.028	0.055	0.043	ns
SSTL33D_II	Differential SSTL_3 class II	0.012	0.012	0.034	0.028	0.055	0.043	ns
SSTL25_I	SSTL_2 class I	0.003	-0.008	0.03	0.011	0.058	0.03	ns
SSTL25_II	SSTL_2 class II	0.003	-0.008	0.03	0.011	0.058	0.03	ns
SSTL25D_I	Differential SSTL_2 class I	0.006	0	0.031	0.023	0.056	0.046	ns
SSTL25D_II	Differential SSTL_2 class II	0.006	0	0.031	0.023	0.056	0.046	ns
SSTL18_I	SSTL_18 class I	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
SSTL18_II	SSTL_18 class II	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
SSTL18D_I	Differential SSTL_18 class I	0.006	0.001	0.029	0.024	0.052	0.046	ns
SSTL18D_II	Differential SSTL_18 class II	0.006	0.001	0.029	0.024	0.052	0.046	ns
LVTTL33	LVTTL	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
LVCMOS33	LVCMOS 3.3	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
LVCMOS25	LVCMOS 2.5	0	0	0	0	0	0	ns
LVCMOS18	LVCMOS 1.8	-0.068	-0.068	-0.087	-0.087	-0.105	-0.105	ns
LVCMOS15	LVCMOS 1.5	-0.131	-0.131	-0.186	-0.186	-0.241	-0.241	ns
LVCMOS12	LVCMOS 1.2	-0.238	-0.238	-0.364	-0.364	-0.49	-0.49	ns
PCI33	PCI	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
PCIX33	PCI-X 3.3	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
PCIX15	PCI-X 1.5	-0.005	-0.016	0.026	-0.001	0.057	0.014	ns
AGP1X33	AGP-1X 3.3	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
AGP2X33	AGP-2X	-0.036	-0.061	-0.181	-0.313	-0.326	-0.565	ns

Timing Diagrams

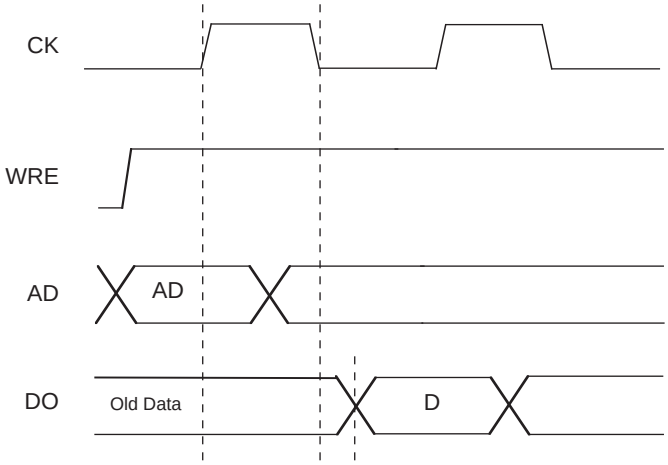
PFU Timing Diagrams

Figure 3-4. Slice Single/Dual Port Write Cycle Timing



Notes:
- Rising Edge for latching WREN, WAD and DATAIN.
- WREN must continue past falling edge clock.
- Data output occurs on negative edge.

Figure 3-5. Slice Single/Dual Port Read Cycle Timing



Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PIC row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
VREF1_x, VREF2_x	—	The reference supply pins for I/O bank x. Any I/O pin in a bank can be assigned as a reference supply pin, but software defaults use designated pin.
NC	—	No connect. NC pins should not be connected to any active signals, VCC or GND.
Non-SERDES Power Supplies		
VCCIOx	—	VCCIO - The power supply pins for I/O bank x. Dedicated pins.
VCC12[1]	—	1.2V supply for configuration logic, PLLs and SERDES Rx, Tx and PLL. All VCC12 pins must be connected. As VCC12 supplies power for analog circuitry, VCC12 should be quiet and isolated from noisy digital board supplies.
VTT_x	—	Termination voltage for bank x. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. VCMT function is not used in the bank. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.
GND	—	GND - Ground. Dedicated pins. All grounds must be electrically connected at the board level.
VCC	—	VCC - The power supply pins for core logic. Dedicated pins (1.2V/ 1.0V).
VCCAUX	—	VCCAUX - Auxiliary power supply pin - powers all differential and referenced input buffers. Dedicated pins (2.5V).
VCCJ	—	VCCJ - The power supply pin for JTAG Test Access Port.
PROBE_VCC	—	VCC signal - Connected to internal VCC node. Can be used for feedback to control an external board power converter. Can be unconnected if not used.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AF4	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AE5	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AG3	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AH2	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AD6	PB4C	5		PB4C	5	
AJ2	PB5A	5		PB5A	5	
AK2	PB5B	5		PB5B	5	
AD7	PB5C	5		PB5C	5	
AD8	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AH3	PB7A	5		PB11A	5	
AJ3	PB7B	5		PB11B	5	
AF9	PB7C	5		PB11C	5	
AE10	PB7D	5		PB11D	5	
AK3	PB8A	5		PB12A	5	
AJ4	PB8B	5		PB12B	5	
AE11	PB9A	5		PB13A	5	
AF10	PB9B	5		PB13B	5	
AK4	PB11A	5		PB16A	5	
AK5	PB11B	5		PB16B	5	
AH10	PB12A	5	PCLKT5_3	PB20A	5	PCLKT5_3
AH11	PB12B	5	PCLKC5_3	PB20B	5	PCLKC5_3
AF13	PB12C	5	PCLKT5_4	PB20C	5	PCLKT5_4
AE14	PB12D	5	PCLKC5_4	PB20D	5	PCLKC5_4
AK6	PB13A	5	PCLKT5_5	PB21A	5	PCLKT5_5
AK7	PB13B	5	PCLKC5_5	PB21B	5	PCLKC5_5
AF14	PB13C	5		PB21C	5	
AJ11	PB15A	5	PCLKT5_0	PB23A	5	PCLKT5_0
AJ12	PB15B	5	PCLKC5_0	PB23B	5	PCLKC5_0
AH13	PB15D	5	VREF2_5	PB23D	5	VREF2_5
AK8	PB16A	5	PCLKT5_1	PB24A	5	PCLKT5_1
AK9	PB16B	5	PCLKC5_1	PB24B	5	PCLKC5_1
AH14	PB17A	5	PCLKT5_2	PB25A	5	PCLKT5_2
AG14	PB17B	5	PCLKC5_2	PB25B	5	PCLKC5_2
AK10	PB19A	5		PB28A	5	
AK11	PB19B	5		PB28B	5	
AH15	PB20A	5		PB29A	5	
AG15	PB20B	5		PB29B	5	
AH12	PB21A	5		PB31A	5	
AJ13	PB21B	5		PB31B	5	
AD15	PB21C	5		PB31C	5	
AE15	PB21D	5		PB31D	5	
AK12	PB23A	5		PB32A	5	
AK13	PB23B	5		PB32B	5	
AJ14	PB24A	5		PB33A	5	
AJ15	PB24B	5		PB33B	5	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH29	PB48B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB68B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AE26	PB48C	4		PB68C	4	
AD25	PB48D	4		PB68D	4	
AJ30	PB49A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB69A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AH30	PB49B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB69B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AG28	PB49C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB69C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AG29	PB49D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB69D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF26	VCC12	-		VCC12	-	
AD27	PROBE_VCC	-		PROBE_VCC	-	
AG27	VCC12	-		VCC12	-	
AE28	PROBE_GND	-		PROBE_GND	-	
AC25	PR45D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR57D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AD26	PR45C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR57C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AF28	PR45B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR57B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AF29	PR45A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR57A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AC26	PR44D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR55D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AB26	PR44C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR55C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AG30	PR44B	3		PR55B	3	
AF30	PR44A	3		PR55A	3	
AC28	PR43B	3		PR52B	3	
AB28	PR43A	3		PR52A	3	
AB27	PR41D	3	VREF2_3	PR51D	3	VREF2_3
AE30	PR41B	3		PR51B	3	
AD30	PR41A	3		PR51A	3	
AB25	PR40B	3		PR49B	3	
AA25	PR40A	3		PR49A	3	
AA30	PR39B	3		PR48B	3	
Y30	PR39A	3		PR48A	3	
W29	PR37B	3		PR44B	3	
V29	PR37A	3		PR44A	3	
U30	PR36B	3		PR43B	3	
T30	PR36A	3		PR43A	3	
V25	PR35D	3	DIFFR_3	PR42D	3	DIFFR_3
W28	PR35B	3		PR42B	3	
V28	PR35A	3		PR42A	3	
R30	PR33B	3		PR38B	3	
P30	PR33A	3		PR38A	3	
N30	PR32B	3		PR35B	3	
M29	PR32A	3		PR35A	3	
U26	PR31D	3		PR34D	3	
T26	PR31C	3	VREF1_3	PR34C	3	VREF1_3
U28	PR31B	3		PR34B	3	
T28	PR31A	3		PR34A	3	
M30	PR28D	3	PCLKC3_2	PR31D	3	PCLKC3_2
L29	PR28C	3	PCLKT3_2	PR31C	3	PCLKT3_2

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
N17	GND	-		GND	-	
N18	GND	-		GND	-	
N19	GND	-		GND	-	
N20	GND	-		GND	-	
P11	GND	-		GND	-	
P12	GND	-		GND	-	
P13	GND	-		GND	-	
P14	GND	-		GND	-	
P15	GND	-		GND	-	
P16	GND	-		GND	-	
P17	GND	-		GND	-	
P18	GND	-		GND	-	
P19	GND	-		GND	-	
P20	GND	-		GND	-	
R10	GND	-		GND	-	
R11	GND	-		GND	-	
R12	GND	-		GND	-	
R13	GND	-		GND	-	
R14	GND	-		GND	-	
R15	GND	-		GND	-	
R16	GND	-		GND	-	
R17	GND	-		GND	-	
R18	GND	-		GND	-	
R19	GND	-		GND	-	
R20	GND	-		GND	-	
R21	GND	-		GND	-	
T10	GND	-		GND	-	
T11	GND	-		GND	-	
T12	GND	-		GND	-	
T13	GND	-		GND	-	
T14	GND	-		GND	-	
T15	GND	-		GND	-	
T16	GND	-		GND	-	
T17	GND	-		GND	-	
T18	GND	-		GND	-	
T19	GND	-		GND	-	
T20	GND	-		GND	-	
T21	GND	-		GND	-	
U11	GND	-		GND	-	
U12	GND	-		GND	-	
U13	GND	-		GND	-	
U14	GND	-		GND	-	
U15	GND	-		GND	-	
U16	GND	-		GND	-	
U17	GND	-		GND	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
B29	NC	-		NC	-	

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M15 and LatticeSC/M25 in a 900-pin package supports a 16-bit MPI interface.

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2]

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C28	A_REFCLKP_L	-		A_REFCLKP_L	-	
D28	A_REFCLKN_L	-		A_REFCLKN_L	-	
B28	VCC12	-		VCC12	-	
F28	RESP_ULC	-		RESP_ULC	-	
J21	RESETN	1		RESETN	1	
J20	TSALLN	1		TSALLN	1	
K20	DONE	1		DONE	1	
K21	INITN	1		INITN	1	
K23	M0	1		M0	1	
J23	M1	1		M1	1	
J24	M2	1		M2	1	
K24	M3	1		M3	1	
K25	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
J25	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
K26	PL16C	7		PL16C	7	
K27	PL16D	7		PL16D	7	
D32	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
D31	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
M23	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
N23	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
E32	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
E31	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
J28	PL18C	7		PL18C	7	
K28	PL18D	7	VREF2_7	PL18D	7	VREF2_7
F32	PL20A	7		PL21A	7	
F31	PL20B	7		PL21B	7	
L25	PL20C	7		PL21C	7	
L26	PL20D	7		PL21D	7	
G31	PL21A	7		PL22A	7	
G32	PL21B	7		PL22B	7	
J29	PL22A	7		PL25A	7	
H29	PL22B	7		PL25B	7	
M25	PL22C	7		PL25C	7	
N25	PL22D	7		PL25D	7	
H31	PL25A	7		PL23A	7	
H32	PL25B	7		PL23B	7	
M24	PL25C	7	VREF1_7	PL23C	7	VREF1_7
N24	PL25D	7	DIFFR_7	PL23D	7	DIFFR_7
L32	PL26A	7	PCLKT7_1	PL35A	7	PCLKT7_1
M32	PL26B	7	PCLKC7_1	PL35B	7	PCLKC7_1
R25	PL26C	7	PCLKT7_3	PL35C	7	PCLKT7_3
R24	PL26D	7	PCLKC7_3	PL35D	7	PCLKC7_3
N31	PL27A	7	PCLKT7_0	PL36A	7	PCLKT7_0
N32	PL27B	7	PCLKC7_0	PL36B	7	PCLKC7_0
P27	PL27C	7	PCLKT7_2	PL36C	7	PCLKT7_2
P28	PL27D	7	PCLKC7_2	PL36D	7	PCLKC7_2
P30	PL29A	6	PCLKT6_0	PL38A	6	PCLKT6_0
P29	PL29B	6	PCLKC6_0	PL38B	6	PCLKC6_0
T23	PL29C	6	PCLKT6_1	PL38C	6	PCLKT6_1
T24	PL29D	6	PCLKC6_1	PL38D	6	PCLKC6_1

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y4	PR48B	3		PR63B	3	
W4	PR48A	3		PR63A	3	
W11	PR47D	3		PR60D	3	
V11	PR47C	3		PR60C	3	
W2	PR47B	3		PR60B	3	
V2	PR47A	3		PR60A	3	
W9	PR45D	3		PR57D	3	
V9	PR45C	3		PR57C	3	
V1	PR45B	3		PR57B	3	
U1	PR45A	3		PR57A	3	
W10	PR44D	3		PR56D	3	
V10	PR44C	3		PR56C	3	
U2	PR44B	3		PR56B	3	
T2	PR44A	3		PR56A	3	
Y8	PR43D	3		PR55D	3	
W8	PR43C	3	VREF1_3	PR55C	3	VREF1_3
W5	PR43B	3		PR55B	3	
V5	PR43A	3		PR55A	3	
V7	PR40D	3	PCLKC3_2	PR52D	3	PCLKC3_2
U7	PR40C	3	PCLKT3_2	PR52C	3	PCLKT3_2
T1	PR40B	3		PR52B	3	
R1	PR40A	3		PR52A	3	
V8	PR39D	3	PCLKC3_3	PR51D	3	PCLKC3_3
U8	PR39C	3	PCLKT3_3	PR51C	3	PCLKT3_3
U5	PR39B	3		PR51B	3	
T5	PR39A	3		PR51A	3	
V6	PR38D	3	PCLKC3_1	PR50D	3	PCLKC3_1
U6	PR38C	3	PCLKT3_1	PR50C	3	PCLKT3_1
T4	PR38B	3	PCLKC3_0	PR50B	3	PCLKC3_0
T3	PR38A	3	PCLKT3_0	PR50A	3	PCLKT3_0
U9	PR36D	2	PCLKC2_2	PR48D	2	PCLKC2_2
T9	PR36C	2	PCLKT2_2	PR48C	2	PCLKT2_2
R2	PR36B	2	PCLKC2_0	PR48B	2	PCLKC2_0
P2	PR36A	2	PCLKT2_0	PR48A	2	PCLKT2_0
T11	PR35D	2	PCLKC2_3	PR47D	2	PCLKC2_3
U11	PR35C	2	PCLKT2_3	PR47C	2	PCLKT2_3
R4	PR35B	2	PCLKC2_1	PR47B	2	PCLKC2_1
R3	PR35A	2	PCLKT2_1	PR47A	2	PCLKT2_1
T8	PR34D	2		PR46D	2	
R8	PR34C	2		PR46C	2	
P1	PR34B	2		PR46B	2	
N1	PR34A	2		PR46A	2	
R6	PR31D	2		PR43D	2	
P6	PR31C	2		PR43C	2	
M1	PR31B	2		PR43B	2	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C2	VCCJ	-		VCCJ	-	
M9	TDO	-	TDO	TDO	-	TDO
L9	TMS	-		TMS	-	
D1	TCK	-		TCK	-	
C1	TDI	-		TDI	-	
J8	PROGRAMN	1		PROGRAMN	1	
K8	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
B2	CCLK	1		CCLK	1	
H9	RESP_URC	-		RESP_URC	-	
H10	VCC12	-		VCC12	-	
H8	A_REFCLKN_R	-		A_REFCLKN_R	-	
G8	A_REFCLKP_R	-		A_REFCLKP_R	-	
C3	VCC12	-		VCC12	-	
D3	A_VDDIB0_R	-		A_VDDIB0_R	-	
A3	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P
B3	A_HDINN0_R	-	PCS 3E0 CH 0 IN N	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
E5	VCC12	-		VCC12	-	
A4	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P
F6	A_VDDOB0_R	-		A_VDDOB0_R	-	
B4	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N
F7	A_VDDOB1_R	-		A_VDDOB1_R	-	
B5	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N
E6	VCC12	-		VCC12	-	
A5	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P
B6	A_HDINN1_R	-	PCS 3E0 CH 1 IN N	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
A6	A_HDINP1_R	-	PCS 3E0 CH 1 IN P	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
C6	VCC12	-		VCC12	-	
D4	A_VDDIB1_R	-		A_VDDIB1_R	-	
C7	VCC12	-		VCC12	-	
D5	A_VDDIB2_R	-		A_VDDIB2_R	-	
A7	A_HDINP2_R	-	PCS 3E0 CH 2 IN P	A_HDINP2_R	-	PCS 3E0 CH 2 IN P
B7	A_HDINN2_R	-	PCS 3E0 CH 2 IN N	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
E7	VCC12	-		VCC12	-	
A8	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
F8	A_VDDOB2_R	-		A_VDDOB2_R	-	
B8	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
F9	A_VDDOB3_R	-		A_VDDOB3_R	-	
B9	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
E8	VCC12	-		VCC12	-	
A9	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
B10	A_HDINN3_R	-	PCS 3E0 CH 3 IN N	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
A10	A_HDINP3_R	-	PCS 3E0 CH 3 IN P	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
C10	VCC12	-		VCC12	-	
D6	A_VDDIB3_R	-		A_VDDIB3_R	-	
G10	VCC12	-		VCC12	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB15	VCC12	-		VCC12	-	
AB20	VCC12	-		VCC12	-	
N15	VCC12	-		VCC12	-	
N20	VCC12	-		VCC12	-	
R13	VCC12	-		VCC12	-	
R22	VCC12	-		VCC12	-	
Y13	VCC12	-		VCC12	-	
Y22	VCC12	-		VCC12	-	
AA12	VCCAUX	-		VCCAUX	-	
AA23	VCCAUX	-		VCCAUX	-	
AB12	VCCAUX	-		VCCAUX	-	
AB16	VCCAUX	-		VCCAUX	-	
AB17	VCCAUX	-		VCCAUX	-	
AB18	VCCAUX	-		VCCAUX	-	
AB19	VCCAUX	-		VCCAUX	-	
AB23	VCCAUX	-		VCCAUX	-	
AC12	VCCAUX	-		VCCAUX	-	
AC13	VCCAUX	-		VCCAUX	-	
Y19	GND	-		GND	-	
AC14	VCCAUX	-		VCCAUX	-	
AC17	VCCAUX	-		VCCAUX	-	
AC21	VCCAUX	-		VCCAUX	-	
AC22	VCCAUX	-		VCCAUX	-	
AC23	VCCAUX	-		VCCAUX	-	
M13	VCCAUX	-		VCCAUX	-	
M14	VCCAUX	-		VCCAUX	-	
M18	VCCAUX	-		VCCAUX	-	
M21	VCCAUX	-		VCCAUX	-	
M22	VCCAUX	-		VCCAUX	-	
N12	VCCAUX	-		VCCAUX	-	
N16	VCCAUX	-		VCCAUX	-	
N17	VCCAUX	-		VCCAUX	-	
N18	VCCAUX	-		VCCAUX	-	
N19	VCCAUX	-		VCCAUX	-	
N23	VCCAUX	-		VCCAUX	-	
P12	VCCAUX	-		VCCAUX	-	
P23	VCCAUX	-		VCCAUX	-	
T13	VCCAUX	-		VCCAUX	-	
T22	VCCAUX	-		VCCAUX	-	
U12	VCCAUX	-		VCCAUX	-	
U13	VCCAUX	-		VCCAUX	-	
U22	VCCAUX	-		VCCAUX	-	
V13	VCCAUX	-		VCCAUX	-	
V22	VCCAUX	-		VCCAUX	-	
V23	VCCAUX	-		VCCAUX	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
W30	PL69B	6	
W27	PL69C	6	VREF1_6
Y27	PL69D	6	
T33	PL70A	6	
U33	PL70B	6	
V25	PL70C	6	
W25	PL70D	6	
U34	PL71A	6	
V34	PL71B	6	
V26	PL71C	6	
W26	PL71D	6	
V33	PL74A	6	
W33	PL74B	6	
V24	PL74C	6	
W24	PL74D	6	
W31	PL77A	6	
Y31	PL77B	6	
Y29	PL77C	6	
AA29	PL77D	6	
Y33	PL79A	6	
AA33	PL79B	6	
Y28	PL79C	6	
AA28	PL79D	6	
AB32	PL90A	6	
AC32	PL90B	6	
AA26	PL90C	6	
AA27	PL90D	6	DIFFR_6
AB31	PL91A	6	
AC31	PL91B	6	
Y24	PL91C	6	
AA24	PL91D	6	
AE34	PL92A	6	
AF34	PL92B	6	
AB30	PL92C	6	
AC30	PL92D	6	
AD33	PL94A	6	
AE33	PL94B	6	
AD30	PL94C	6	
AE30	PL94D	6	
AE32	PL96A	6	
AF32	PL96B	6	
AA25	PL96C	6	
AB25	PL96D	6	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
L5	PR38B	2	
K5	PR38A	2	
G2	PR34B	2	
F2	PR34A	2	
F1	PR30B	2	
E1	PR30A	2	
A2	GND	-	
A33	GND	-	
AA15	GND	-	
AA20	GND	-	
AA32	GND	-	
AA4	GND	-	
AB28	GND	-	
AB6	GND	-	
AC11	GND	-	
AC18	GND	-	
AC25	GND	-	
AD23	GND	-	
AD3	GND	-	
AD31	GND	-	
AE12	GND	-	
AE15	GND	-	
AE29	GND	-	
AE7	GND	-	
AE9	GND	-	
AF20	GND	-	
AF26	GND	-	
AG32	GND	-	
AG4	GND	-	
AH13	GND	-	
AH19	GND	-	
AH25	GND	-	
AH7	GND	-	
AJ10	GND	-	
AJ16	GND	-	
AJ22	GND	-	
AJ28	GND	-	
AK3	GND	-	
AK31	GND	-	
AL11	GND	-	
AL17	GND	-	
AL21	GND	-	
AL27	GND	-	

Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-6FF1020I[1]	-6	Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-5FF1020I[1]	-5	Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-6FFA1020I	-6	Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-5FFA1020I	-5	Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-6FC1152I[2]	-6	Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FC1152I[2]	-5	Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-6FF1152I	-6	Organic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FF1152I	-5	Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-6FC1152I[1]	-6	Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-5FC1152I[1]	-5	Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-6FF1152I	-6	Organic fcBGA	1152	IND	80.1
LFSC3GA80E-5FF1152I	-5	Organic fcBGA	1152	IND	80.1
LFSC3GA80E-6FC1704I[1]	-6	Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-5FC1704I[1]	-5	Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-6FF1704I	-6	Organic fcBGA	1704	IND	80.1
LFSC3GA80E-5FF1704I	-5	Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-6FC1152I[1]	-6	Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FC1152I[1]	-5	Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FF1152I	-6	Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FF1152I	-5	Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FC1704I[1]	-6	Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FC1704I[1]	-5	Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-6FF1704I	-6	Organic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FF1704I	-5	Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per PCN #01A-10.

LatticeSC/M Family Data Sheet Supplemental Information

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For Further Information

For further information about the flexiPCS, see the LatticeSC/M Family flexiPCS Data Sheet.

A variety of technical notes for the LatticeSC/M family are also available on the Lattice Semiconductor website at www.latticesemi.com.

- LatticeSC PURESPEED I/O Usage Guide (TN1088)
- LatticeSC PURESPEED I/O Adaptive Input Logic User's Guide (TN1158)
- LatticeSC sysCLOCK PLL/DLL User's Guide (TN1098)
- On-Chip Memory Usage Guide for LatticeSC Devices (TN1094)
- LatticeSC/M DDR/DDR2 SDRAM Memory Interface User's Guide (TN1099)
- LatticeSC QDRII/II+ SRAM Memory Interface User's Guide (TN1096)
- LatticeSC sysCONFIG Usage Guide (TN1080)
- LatticeSC MPI/System Bus (TN1085)
- SPI Serial Flash Programming Using ispJTAG in LatticeSC Devices (TN1100)
- Power Estimation and Management for LatticeSC Devices (TN1101)
- LatticeSC SERDES Jitter (TN1084)
- LatticeSC FPGAs: Implementing 3.3V Interfaces in 2.5V VCCIO Banks (TN1110)
- Lattice PCI Express Basic Demo User's Guide (UG08)
- LatticeSC flexiPCS/SERDES Design Guide (TN1145)
- Temperature Sensing Diode in LatticeSC Devices (TN1115)
- SPI4.2 Interoperability Between ORSPI4 and LatticeSC Devices (TN1116)

For further information on Interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- Optical Interface (SPI-4.2, XSBI, CSIX and XGMII): www.oiforum.com
- RAPIDIO: www.rapidio.org
- PCI/PCIX: ww.pcisig.com