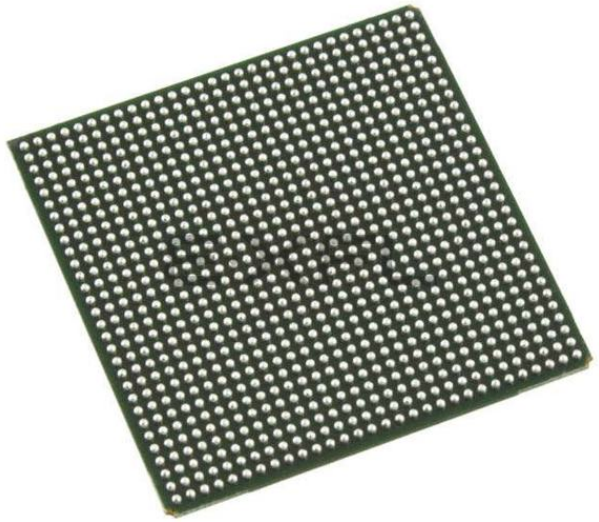
Lattice Semiconductor Corporation - LFSCM3GA15EP1-6FN900C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3750
Number of Logic Elements/Cells	15000
Total RAM Bits	1054720
Number of I/O	300
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga15ep1-6fn900c

LatticeSC/M Family Data Sheet Introduction

January 2010 Data Sheet DS1004

Features

- **High Performance FPGA Fabric**
  - 15K to 115K four input Look-up Tables (LUT4s)
  - 139 to 942 I/Os
  - 700MHz global clock; 1GHz edge clocks
- **4 to 32 High Speed SERDES and flexiPCS™ (per Device)**
  - Performance ranging from 600Mbps to 3.8Gbps
  - Excellent Rx jitter tolerance (0.8UI at 3.125Gbps)
  - Low Tx jitter (0.25UI typical at 3.125Gbps)
  - Built-in Pre-emphasis and equalization
  - Low power (typically 105mW per channel)
  - Embedded Physical Coding Sublayer (PCS) provides pre-engineered implementation for the following standards:
    - GbE, XAUI, PCI Express, SONET, Serial RapidIO, 1G Fibre Channel, 2G Fibre Channel
- **2Gbps High Performance PURESPEED™ I/O**
  - Supports the following performance bandwidths
    - Differential I/O up to 2Gbps DDR (1GHz Clock)
    - Single-ended memory interfaces up to 800Mbps
  - 144 Tap programmable Input Delay (INDEL) block on every I/O dynamically aligns data to clock for robust performance
    - Dynamic bit Adaptive Input Logic (AIL) monitoring and control circuitry per pin that automatically ensures proper set-up and hold
    - Dynamic bus: uses control bus from DLL
    - Static per bit
  - Electrical standards supported:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2, LVTTL
    - SSTL 3/2/18 I, II; HSTL 18/15 I, II
    - PCI, PCI-X
    - LVDS, Mini-LVDS, Bus-LVDS, MLVDS, LVPECL, RSDS
  - Programmable On Die Termination (ODT)
    - Includes Thevenin Equivalent and low power V_{TT} termination options
- **Memory Intensive FPGA**
  - sysMEM™ embedded Block RAM
    - 1 to 7.8 Mbits memory
    - True Dual Port/Pseudo Dual Port/Single Port
    - Dedicated FIFO logic for all block RAM
    - 500MHz performance
  - Additional 240K to 1.8Mbits distributed RAM
- **sysCLOCK™ Network**
  - Eight analog PLLs per device
    - Frequency range from 15MHz to 1GHz
    - Spread spectrum support
  - 12 DLLs per device with direct control of I/O delay
    - Frequency range from 100MHz to 700MHz
  - Extensive clocking network
    - 700MHz primary and 325 MHz secondary clocks
    - 1GHz I/O-connected edge clocks
  - Precision Clock Divider
    - Phase matched x2 and x4 division of incoming clocks
  - Dynamic Clock Select (DCS)
    - Glitch free clock MUX
- **Masked Array for Cost Optimization (MACO™) Blocks**
  - On-chip structured ASIC Blocks provide pre-engineered IP for low power, low cost system level integration
- **High Performance System Bus**
  - Ties FPGA elements together with a standard bus framework
    - Connects to peripheral user interfaces for run-time dynamic configuration
- **System Level Support**
  - IEEE standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer
  - IEEE Standard 1532 in-system configuration
  - 1.2V and 1.0V operation
  - Onboard oscillator for initialization and general use
  - Embedded PowerPC microprocessor interface
  - Low cost wire-bond and high pin count flip-chip packaging
  - Low cost SPI Flash RAM configuration

toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-9 illustrates the DCS Block diagram.

Figure 2-9. DCS Block Diagram

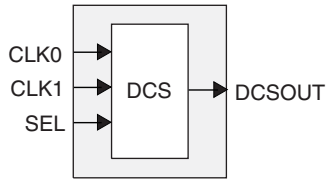
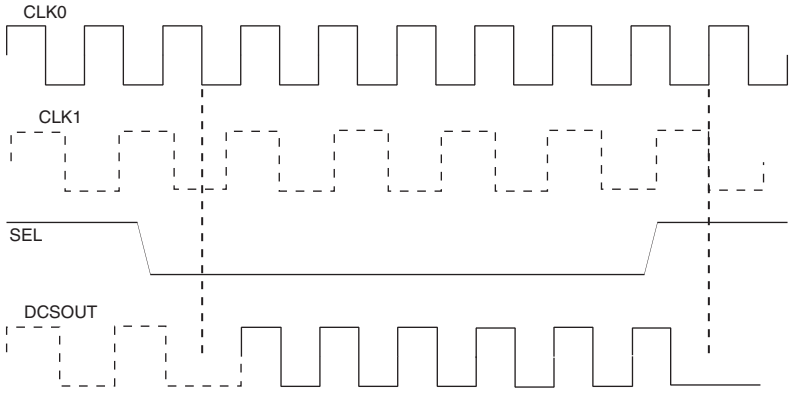


Figure 2-10 shows timing waveforms for one of the DCS operating modes. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

Figure 2-10. DCS Waveforms



Clock Boosting

There are programmable delays available in the clock signal paths in the PFU, PIC and EBR blocks. These allow setup and clock-to-output times to be traded to meet critical timing without slowing the system clock. If this feature is enabled then the design tool automatically uses these delays to improve timing performance.

Global Set/Reset

There is a global set/reset (GSR) network on the device that is distributed to all FFs, PLLs, DLLs and other blocks on the device. This GSR network can operate in two modes:

a) asynchronous - no clock is required to get into or out of the reset state.

b) synchronous - The global GSR net is synchronized to a user selected clock. In this mode it continues to be asynchronous to get into the reset state, but is synchronous to get out of the reset state. This allows all registers on the device to become operational in the same clock period. The synchronous GSR goes out of reset in two cycles from the clock edge where the setup time of the FF was met (not from the GSR being released).

sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider and two clock output dividers. The input divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal.

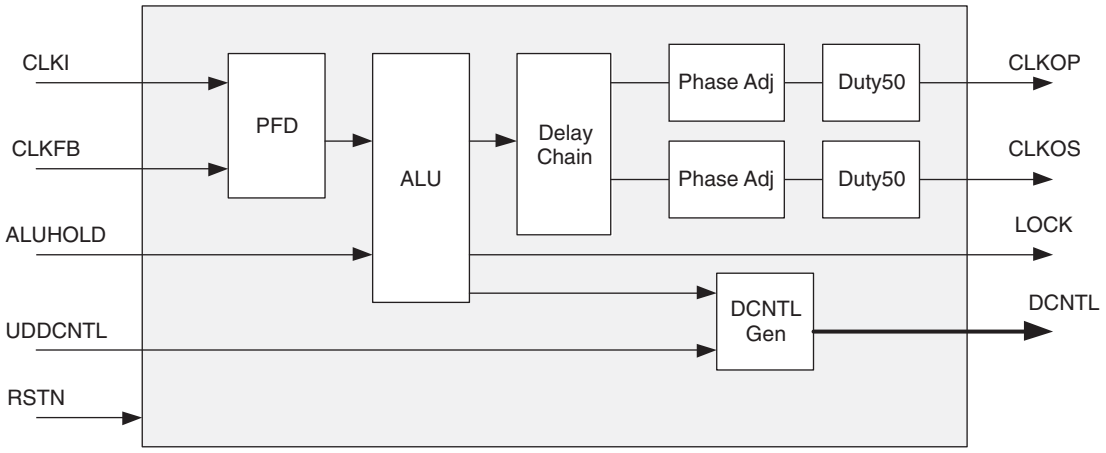
There is a Digital Control (DCNTL) bus available from the DLL block. This Digital Control bus is available to the delay lines in the PIC blocks in the adjacent banks. The UDDCNTL signal allows the user to latch the current value on the digital control bus.

Figure 2-12 shows the DLL block diagram of the DLL inputs and outputs. The output of the phase frequency detector controls an arithmetic logic unit (ALU) to add or subtract one delay tap. The digital output of this ALU is used to control the delay value of the delay chain and this digital code is transmitted via the DCNTL bus.

The sysCLOCK DLL can be configured at power-up, then, if desired, reconfigured dynamically through the Serial Memory Interface bus which interfaces with the on-chip Microprocessor Interface (MPI) bus. In addition, users can drive the SMI interface from routing if desired.

The user can configure the DLL for many common functions such as clock injection match and single delay cell. Lattice provides primitives in its design for time reference delay (DDR memory) and clock injection delay removal.

Figure 2-12. DLL Diagram



PLL/DLL Cascading

The LatticeSC devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are as follows:

- PLL to PLL
- PLL to DLL
- DLL to DLL
- DLL to PLL

DLLs are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLL and PLLs.

When cascading the DLL to the PLL, the DLL can be used to drive the PLL to create fine phase shifts of an input clock signal. Figure 2-13 shows a shift of all outputs for CLKOP and CLKOS out in time.

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
FIFO	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output. A clock is required even in asynchronous read mode.

The EBR memory supports two forms of write behavior for dual port operation:

1. **Normal** — data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output.

2. **Write Through** — a copy of the input data appears at the output of the same port.

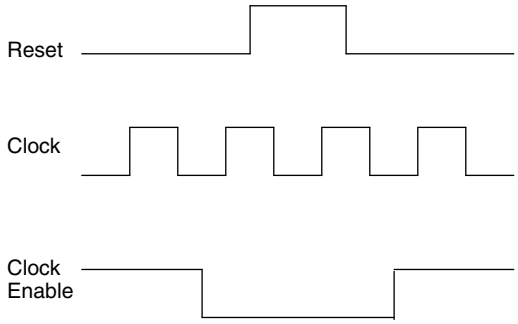
FIFO Configuration

The FIFO has a write port with Data-in, WCE, WE and WCLK signals. There is a separate read port with Data-out, RCE, RE and RCLK signals. The FIFO internally generates Almost Full, Full, Almost Empty, and Empty Flags. The Full and Almost Full flags are registered with WCLK. The Empty and Almost Empty flags are registered with RCLK.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the low-to-high transition of the reset, as shown in Figure 2-16.

Figure 2-16. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM, FIFO and shift register implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-16. The reset timing rules apply to the RPReset input vs. the RE input and the RST input vs. the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For the EBR shift register mode, the GSR signal is always enabled and the local RESET pin is always asynchronous.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled. For more information about on-chip memory, see TN1094, On-Chip Memory Usage Guide for LatticeSC Devices.

Programmable I/O Cells (PIC)

Each PIC contains four PIOs connected to their respective PURESPEED I/O Buffer which are then connected to the PADs as shown in Figure 2-17. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to PURESPEED I/O buffer, and receives input (DI) from the buffer. The PIO contains advanced capabilities to allow the support of speeds up to 2Gbps. These include dedicated shift and DDR logic and adaptive input logic. The dedicated resources simplify the design of robust interfaces.

Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the PURESPEED I/O buffers. The block contains a register for SDR operation and a group of three registers for DDR and shift register operation. The output signal tri-state control signal (TO) can be derived directly from one of the inputs (bypass mode), the SDR shift register, the DDR registers or the data associated with the buffer (for open drain emulation). Figure 2-24 shows the diagram of the Tristate Register Block.

Tristate SDR Register/Latch Block

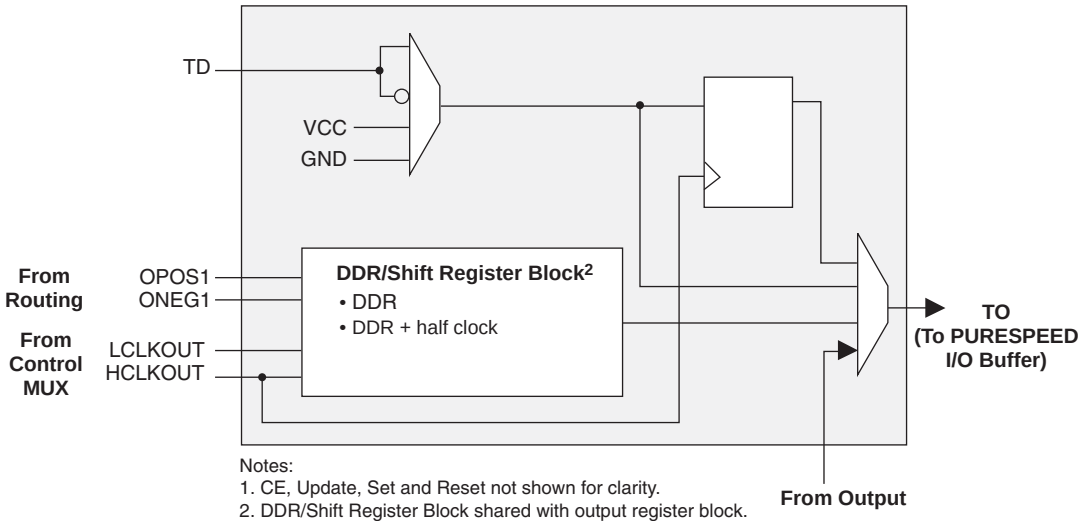
The SDR register operates on the positive edge of the high-speed clock. In it has a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR and Global Set Reset GSR enable or disable. The register LSR input is driven from LSRO, which is generated from the PIO control MUX. The GSR input is driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

Tristate DDR/Shift Register Block

The DDR/Shift block is shared with the output block allowing DDR support using the high-speed clock and the associated transfer from the low-speed clock domain. It functions as a gearbox allowing low–speed parallel data from the FPGA fabric to provide a high-speed tri-state control stream.

There is a special mode for DDR-II memory interfaces where the termination is controlled by the output tristate signal. During WRITE cycle when the FPGA is driving the lines, the parallel terminations are turned off. During READ cycle when the FPGA is receiving data, the parallel terminations are turned on.

Figure 2-24. Tristate Register Block[1]



I/O Architecture Rules

Table 2-6 shows the PIO usage for x1, x2, x4 gearing. The checkmarks in the columns show the specific PIOs that are used for each gearing mode. When using x2 or x4 gearing, any PIO which is not used for gearing can still be used as an output.

Table 2-9. Supported Input Standards

Input Standard	V_{REF} (Nom.)	V_{CCIO}[1] (Nom.)	On-chip Termination
Single Ended Interfaces			
LVTTL33[3]	—	3.3	None
LVCMOS 33, 25, 18, 15, 12[3]	—	3.3/2.5/1.8/1.5/1.2	None
PCI33, PCIX33, AGP1X33[3]	—	3.3	None
PCIX15	0.75	1.5[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
AGP2X33	1.32	—	None
HSTL18_I, II	0.9	1.8[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
HSTL18_III, IV	1.08	1.8[2]	None / V_{CCIO}: 50
HSTL15_I, II	0.75	1.5[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
HSTL15_III, IV	0.9	1.5[2]	None / V_{CCIO}: 50
SSTL33_I, II	1.5	3.3	None
SSTL25_I, II	1.25	2.5[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
SSTL18_I, II	0.9	1.8[2]	None / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
GTL+, GTL	1.0 / 0.8	1.5 / 1.2[2]	None / V_{CCIO}: 50
Differential Interfaces			
SSTL18D_I, II	—	1.8[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
SSTL25D_I, II	—	2.5[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
SSTL33D_I, II	—	3.3	None
HSTL15D_I, II	—	1.5[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
HSTL18D_I, II	—	1.8[2]	None / Diff: 120, 150, 220, 420/ Diff to V_{CMT}: 120, 150, 220, 420 / V_{CCIO} / 2: 50, 60/ V_{TT}: 60, 75, 120, 210
LVDS	—	—	None / Diff: 120, 150, 220, 240/ Diff to V_{CMT}: 120, 150, 220, 240
Mini-LVDS	—	—	None / Diff: 120, 150 / Diff to V_{CMT}: 120, 150
BLVDS25	—	—	None
MLVDS25	—	—	None
RSDS	—	—	None / Diff: 120, 150, 220, 240/ Diff to V_{CMT}: 120, 150, 220, 240
LVPECL33	—	≤2.5	None / Diff: 120, 150, 220, 240/ Diff to V_{CMT}: 120, 150, 220, 240

1. When not specified V_{CCIO} can be set anywhere in the valid operating range.
2. V_{CCIO} needed for on-chip termination to $V_{CCIO}/2$ or V_{CCIO} only. V_{CCIO} is not specified for off-chip termination or V_{TT} termination.
3. All ratioed input buffers and dedicated pin input buffers include hysteresis with a typical value of 50mV.

- 8-bit SERDES Only
- 10-bit SERDES Only
- SONET (STS-12/STS-48)
- Gigabit Ethernet
- Fibre Channel
- XAUI
- Serial RapidIO
- PCI-Express
- Generic 8b10b

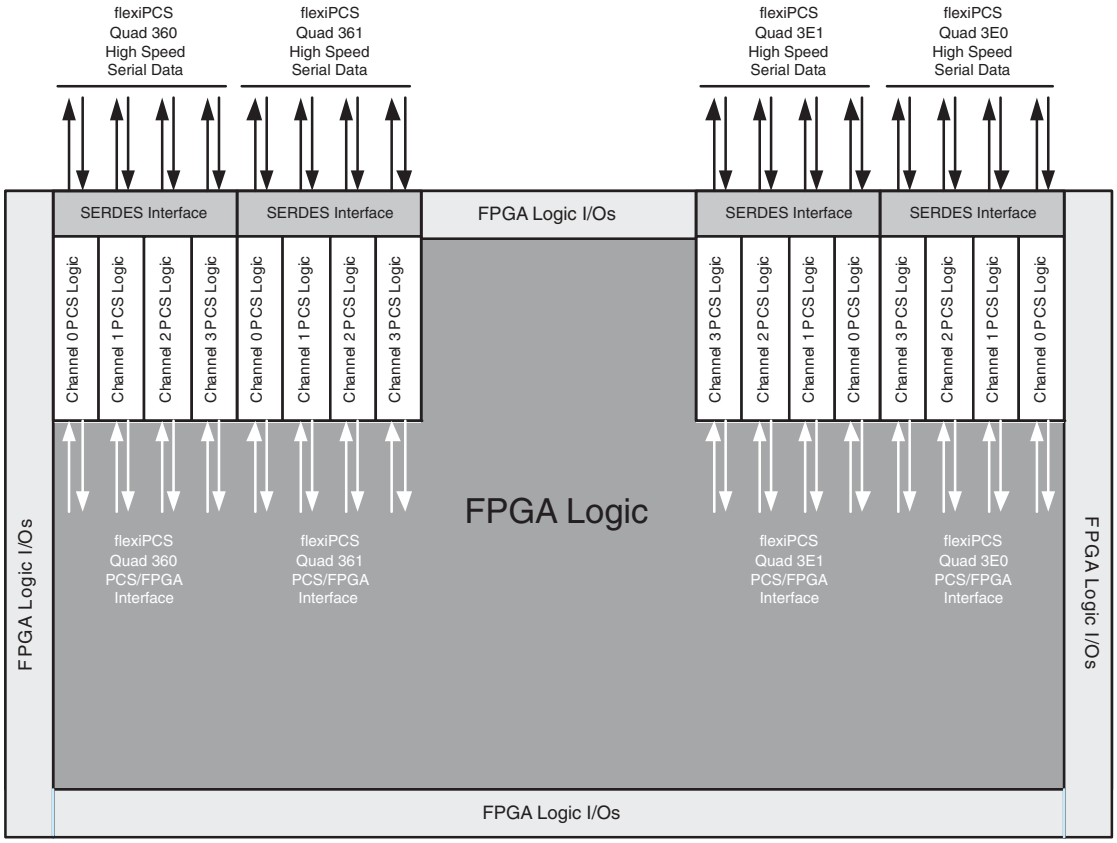
flexiPCS Quad

The flexiPCS logic is arranged in quads containing logic for four independent full-duplex data channels. Each device in the LatticeSC family has up to eight quads of flexiPCS logic. The LatticeSC Family Selection Guide table on the first page of this data sheet contains the number of flexiPCS channels present on the chip. Note that in some packages (particularly lower pin count packages), not all channels from all quads on a given device may be bonded to package pins.

Each quad supports up to four channels of full-duplex data and can be programmed into any one of several protocol based modes. Each quad requires its own reference clock which can be sourced externally or from the FPGA logic. The user can utilize between one and four channels in a quad, depending on the application.

Figure 2-30 shows an example of four flexiPCS quads in a LatticeSC device. Quads are labeled according to the address of their software controlled registers.

Figure 2-30. LatticeSC flexiPCS



Since each quad has its own reference clock, different quads can support different standards on the same chip. This feature makes the LatticeSC family of devices ideal for bridging between different standards.

PURESPEED I/O Single-Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 33	-0.3	0.8	2	3.465	0.4	2.4	24, 16, 8	-24, -16, -8
					0.2	VCCIO - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2	3.465	0.4	2.4	24, 16, 8	-24, -16, -8
					0.2	VCCIO - 0.2	0.1	-0.1
LVCMOS 25	-0.3	0.7	1.7	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVCMOS 18	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVCMOS 15	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVCMOS 12	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.3	VCCIO - 0.3	12, 8, 4, 2	-12, -8, -4, -2
					0.2	VCCIO - 0.2	0.1	-0.1
PCIX15	-0.3	0.3VCCIO	0.5VCCIO	1.5	0.1VCCIO	0.9VCCIO	1.5	-0.5
PCI33	-0.3	0.3VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
PCIX33	-0.3	0.35VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
AGP-1X, AGP-2X	-0.3	0.3VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
SSTL3_I	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.7	VCCIO - 1.1	8	-8
SSTS3_I OST[2]	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.9	VCCIO - 1.3	8	-8
SSTL3_II	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.5	VCCIO - 0.9	16	-16
SSTL3_II OST[2]	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.9	VCCIO - 0.13	16	-16
SSTL2_I	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.54	VCCIO - 0.62	7.6	-7.6
SSTL2_I OST[2]	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.73	VCCIO - 0.81	7.6	-7.6
SSTL2_II	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.35	VCCIO - 0.43	15.2	-15.2
SSTL2_II OST[2]	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.73	VCCIO - 0.81	15.2	-15.2
SSTL18_I	-0.3	VREF - 0.125	VREF + 0.125	2.65	0.28	VCCIO - 0.28	13.4	-13.4
SSTL18_II	-0.3	VREF - 0.125	VREF + 0.125	2.65	0.28	VCCIO - 0.28	13.4	-13.4
HSTL15_I	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	8	-8
HSTL15_II	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	16	-16
HSTL15_III[1]	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL15_IV[1]	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL18_I	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	9.6	-9.6
HSTL18_II	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	19.2	-19.2
HSTL18_III[1]	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL18_IV[1]	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
GTL12[1], GTLPLUS15[1]	-0.3	VREF - 0.2	VREF + 0.2	N/A	N/A	N/A	N/A	N/A

1. Input only.
2. Input with on-chip series termination.

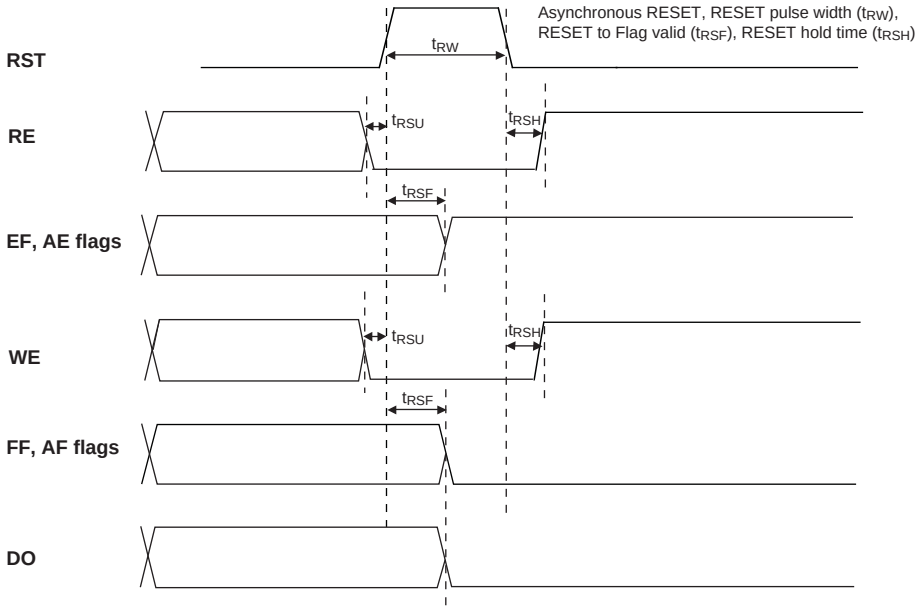
LatticeSC/M External Switching Characteristics[3]

Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (using Primary Clock without PLL)[2]								
t_{CO}	Global Clock Input to Output - PIO Output Register	2.83	5.74	2.83	6.11	2.83	6.49	ns
t_{SU}	Global Clock Input Setup - PIO Input Register without fixed input delay	-0.66	—	-0.66	—	-0.66	—	ns
t_{H}	Global Clock Input Hold - PIO Input Register without fixed input delay	1.73	—	1.95	—	2.16	—	ns
t_{SU_IDLY}	Global Clock Input Setup - PIO Input Register with input delay	0.86	—	1.03	—	1.20	—	ns
t_{H_IDLY}	Global Clock Input Hold - PIO Input Register with input delay	-0.17	—	-0.17	—	-0.17	—	ns
f_{MAX_PFU}	Global Clock frequency of PFU register	—	700	—	700	—	700	MHz
f_{MAX_IO}	Global Clock frequency of I/O register	—	1000	—	1000	—	1000	MHz
t_{GC_SKEW}	Global Clock skew	—	89	—	103	—	116	ps
General I/O Pin Parameters (using Primary Clock with PLL)[1, 2]								
t_{CO}	Global Clock Input to Output - PIO Output Register	2.25	4.81	2.25	5.08	2.25	5.37	ns
t_{SU}	Global Clock Input Setup - PIO Input Register without fixed input delay	-0.07	—	-0.07	—	-0.07	—	ns
t_{H}	Global Clock Input Hold - PIO Input Register without fixed input delay	0.80	—	0.93	—	1.04	—	ns
General I/O Pin Parameters (using Edge Clock without PLL)[2]								
t_{CO}	Edge Clock Input to Output - PIO Output Register	2.38	4.77	2.38	5.04	2.38	5.33	ns
t_{SU}	Edge Clock Input Setup - PIO Input Register without fixed input delay	-0.08	—	-0.08	—	-0.08	—	ns
t_{H}	Edge Clock Input Hold - PIO Input Register	0.49	—	0.58	—	0.66	—	ns
t_{SU_IDLY}	Edge Clock Input Setup - PIO Input Register with input delay	0.81	—	0.97	—	1.12	—	ns
t_{H_IDLY}	Edge Clock Input Hold - PIO Input Register with input delay	-0.34	—	-0.34	—	-0.34	—	ns
t_{EC_SKEW}	Edge Clock skew	—	28	—	32	—	36	ps
General I/O Pin Parameters (using Latch FF without PLL)[2]								
t_{SU}	Latch FF, Input Setup - PIO Input Register without fixed input delay	-0.14	—	-0.14	—	-0.14	—	ns
t_{H}	Latch FF, Input Hold - PIO Input Register without fixed input delay	0.58	—	0.68	—	0.77	—	ns
t_{SU_IDLY}	Latch FF, Input Setup - PIO Input Register with input delay	0.70	—	0.68	—	0.77	—	ns
t_{H_IDLY}	Latch FF, Input Hold - PIO Input Register with input delay	-0.30	—	-0.30	—	-0.30	—	ns

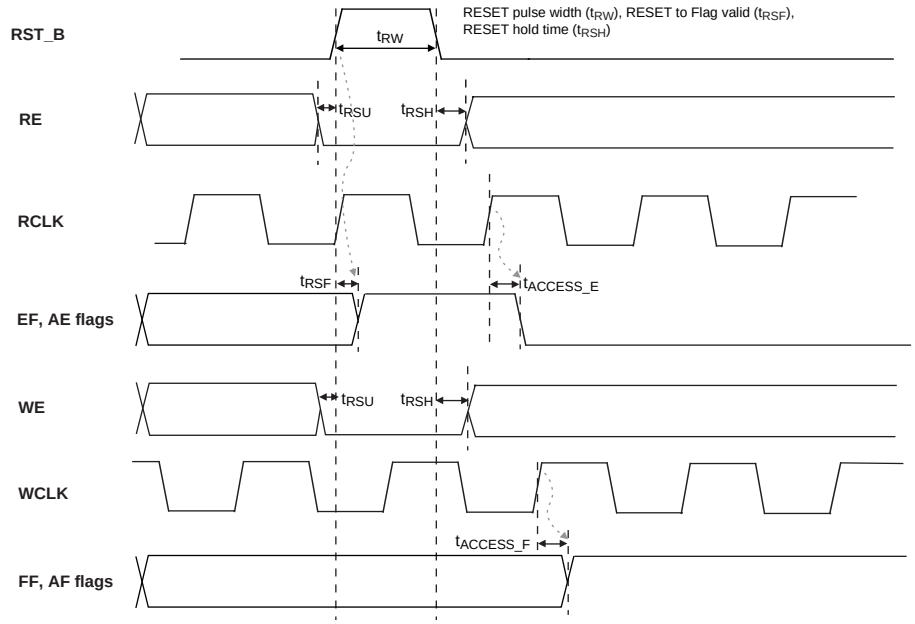
1. No PLL delay tuning (clock injection removal mode, system clock feedback).
2. Using LVCMOS25 12mA I/O. Timing adders for other supported I/O technologies are specified in the LatticeSC Family Timing Adders table.
3. Complete Timing Parameters for a user design are incorporated when running ispLEVER. This is a sampling of the key timing parameters. Timing specs are for non-AIL applications.

Figure 3-10. FIFO Reset Waveform



Note: RE and WE must be deactivated t_{RSU} before the Positive FIFO reset edge and enabled t_{RSH} after the FIFO reset negative edge.

Figure 3-11. Read Pointer Reset Waveform



Note: RE and WE must be deactivated t_{RSU} before the Positive FIFO reset edge and enabled t_{RSH} after the FIFO reset negative edge.

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PIC row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
VREF1_x, VREF2_x	—	The reference supply pins for I/O bank x. Any I/O pin in a bank can be assigned as a reference supply pin, but software defaults use designated pin.
NC	—	No connect. NC pins should not be connected to any active signals, VCC or GND.
Non-SERDES Power Supplies		
VCCIOx	—	VCCIO - The power supply pins for I/O bank x. Dedicated pins.
VCC12[1]	—	1.2V supply for configuration logic, PLLs and SERDES Rx, Tx and PLL. All VCC12 pins must be connected. As VCC12 supplies power for analog circuitry, VCC12 should be quiet and isolated from noisy digital board supplies.
VTT_x	—	Termination voltage for bank x. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. VCMT function is not used in the bank. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.
GND	—	GND - Ground. Dedicated pins. All grounds must be electrically connected at the board level.
VCC	—	VCC - The power supply pins for core logic. Dedicated pins (1.2V/ 1.0V).
VCCAUX	—	VCCAUX - Auxiliary power supply pin - powers all differential and referenced input buffers. Dedicated pins (2.5V).
VCCJ	—	VCCJ - The power supply pin for JTAG Test Access Port.
PROBE_VCC	—	VCC signal - Connected to internal VCC node. Can be used for feedback to control an external board power converter. Can be unconnected if not used.

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ31	PB9A	5		PB9A	5	
AH30	PB9B	5		PB9B	5	
AM30	PB11A	5		PB11A	5	
AM29	PB11B	5		PB11B	5	
AH29	PB11C	5		PB11C	5	
AH28	PB11D	5		PB11D	5	
AJ27	PB12A	5		PB13A	5	
AK27	PB12B	5		PB13B	5	
AE22	PB12C	5		PB13C	5	
AF23	PB12D	5		PB13D	5	
AL28	PB13A	5		PB15A	5	
AL27	PB13B	5		PB15B	5	
AC21	PB13C	5		PB15C	5	
AD21	PB13D	5		PB15D	5	
AM28	PB15A	5		PB17A	5	
AM27	PB15B	5		PB17B	5	
AG23	PB15C	5		PB17C	5	
AF22	PB15D	5		PB17D	5	
AG26	PB16A	5		PB19A	5	
AG25	PB16B	5		PB19B	5	
AL26	PB17A	5		PB22A	5	
AM26	PB17B	5		PB22B	5	
AJ24	PB19A	5		PB25A	5	
AK24	PB19B	5		PB25B	5	
AE21	PB19C	5		PB25C	5	
AE20	PB19D	5		PB25D	5	
AJ22	PB20A	5	PCLKT5_3	PB30A	5	PCLKT5_3
AK22	PB20B	5	PCLKC5_3	PB30B	5	PCLKC5_3
AG22	PB20C	5	PCLKT5_4	PB30C	5	PCLKT5_4
AH22	PB20D	5	PCLKC5_4	PB30D	5	PCLKC5_4
AL23	PB21A	5	PCLKT5_5	PB31A	5	PCLKT5_5
AL22	PB21B	5	PCLKC5_5	PB31B	5	PCLKC5_5
AH23	PB21C	5		PB31C	5	
AH24	PB21D	5		PB31D	5	
AJ21	PB23A	5	PCLKT5_0	PB33A	5	PCLKT5_0
AK21	PB23B	5	PCLKC5_0	PB33B	5	PCLKC5_0
AE19	PB23C	5		PB33C	5	
AF19	PB23D	5	VREF2_5	PB33D	5	VREF2_5
AM23	PB24A	5	PCLKT5_1	PB34A	5	PCLKT5_1
AM22	PB24B	5	PCLKC5_1	PB34B	5	PCLKC5_1
AH25	PB24C	5	PCLKT5_6	PB34C	5	PCLKT5_6
AH26	PB24D	5	PCLKC5_6	PB34D	5	PCLKC5_6
AL21	PB25A	5	PCLKT5_2	PB35A	5	PCLKT5_2
AL20	PB25B	5	PCLKC5_2	PB35B	5	PCLKC5_2
AG20	PB25C	5	PCLKT5_7	PB35C	5	PCLKT5_7
AG19	PB25D	5	PCLKC5_7	PB35D	5	PCLKC5_7
AJ19	PB28A	5		PB37A	5	
AK19	PB28B	5		PB37B	5	
AD18	PB28C	5		PB37C	5	
AE18	PB28D	5		PB37D	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH27	PB5C	5		PB5C	5	
AH26	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AN32	PB7A	5		PB7A	5	
AP32	PB7B	5		PB7B	5	
AF25	PB7C	5		PB7C	5	
AE25	PB7D	5		PB7D	5	
AN31	PB8A	5		PB9A	5	
AN30	PB8B	5		PB9B	5	
AK29	PB8C	5		PB9C	5	
AK28	PB8D	5		PB9D	5	
AP31	PB9A	5		PB11A	5	
AP30	PB9B	5		PB11B	5	
AD24	PB9C	5		PB11C	5	
AE24	PB9D	5		PB11D	5	
AM29	PB11A	5		PB13A	5	
AM28	PB11B	5		PB13B	5	
AJ27	PB11C	5		PB13C	5	
AJ26	PB11D	5		PB13D	5	
AP29	PB13A	5		PB15A	5	
AP28	PB13B	5		PB15B	5	
AK27	PB13C	5		PB15C	5	
AK26	PB13D	5		PB15D	5	
AN29	PB15A	5		PB17A	5	
AN28	PB15B	5		PB17B	5	
AG25	PB15C	5		PB17C	5	
AG24	PB15D	5		PB17D	5	
AL26	PB17A	5		PB19A	5	
AL25	PB17B	5		PB19B	5	
AG23	PB17C	5		PB19C	5	
AG22	PB17D	5		PB19D	5	
AN27	PB19A	5		PB21A	5	
AN26	PB19B	5		PB21B	5	
AF24	PB19C	5		PB21C	5	
AF23	PB19D	5		PB21D	5	
AP27	PB22A	5		PB24A	5	
AP26	PB22B	5		PB24B	5	
AK25	PB22C	5		PB24C	5	
AK24	PB22D	5		PB24D	5	
AN25	PB25A	5		PB27A	5	
AN24	PB25B	5		PB27B	5	
AE22	PB25C	5		PB27C	5	
AE21	PB25D	5		PB27D	5	
AM26	PB26A	5		PB29A	5	
AM25	PB26B	5		PB29B	5	
AF22	PB26C	5		PB29C	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD8	PR65C	3		PR89C	3	
AJ3	PR65B	3		PR89B	3	
AH3	PR65A	3		PR89A	3	
AD7	PR62D	3		PR86D	3	
AC7	PR62C	3		PR86C	3	
AJ2	PR62B	3		PR86B	3	
AH2	PR62A	3		PR86A	3	
AF6	PR61D	3		PR85D	3	
AF5	PR61C	3		PR85C	3	
AF4	PR61B	3		PR85B	3	
AE4	PR61A	3		PR85A	3	
AD6	PR60D	3		PR84D	3	
AC6	PR60C	3		PR84C	3	
AG2	PR60B	3		PR84B	3	
AF2	PR60A	3		PR84A	3	
AC8	PR58D	3		PR82D	3	
AB8	PR58C	3		PR82C	3	
AK1	PR58B	3		PR82B	3	
AJ1	PR58A	3		PR82A	3	
AB10	PR57D	3		PR81D	3	
AA10	PR57C	3		PR81C	3	
AF3	PR57B	3		PR81B	3	
AE3	PR57A	3		PR81A	3	
AE5	PR56D	3		PR80D	3	
AD5	PR56C	3		PR80C	3	
AE2	PR56B	3		PR80B	3	
AD2	PR56A	3		PR80A	3	
AC5	PR53D	3		PR78D	3	
AB5	PR53C	3		PR78C	3	
AF1	PR53B	3		PR78B	3	
AE1	PR53A	3		PR78A	3	
AA11	PR52D	3		PR77D	3	
Y11	PR52C	3		PR77C	3	
AC4	PR52B	3		PR77B	3	
AB4	PR52A	3		PR77A	3	
AA8	PR51D	3	DIFFR_3	PR76D	3	DIFFR_3
AA9	PR51C	3		PR76C	3	
AC3	PR51B	3		PR76B	3	
AB3	PR51A	3		PR76A	3	
AA7	PR49D	3		PR65D	3	
Y7	PR49C	3		PR65C	3	
AA2	PR49B	3		PR65B	3	
Y2	PR49A	3		PR65A	3	
AA6	PR48D	3		PR63D	3	
Y6	PR48C	3		PR63C	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AJ34	PL98A	6	
AK34	PL98B	6	
AB27	PL98C	6	
AC27	PL98D	6	
AF33	PL99A	6	
AG33	PL99B	6	
AC29	PL99C	6	
AD29	PL99D	6	
AE31	PL103A	6	
AF31	PL103B	6	
AF30	PL103C	6	
AF29	PL103D	6	
AH33	PL104A	6	
AJ33	PL104B	6	
AC28	PL104C	6	
AD28	PL104D	6	
AH32	PL107A	6	
AJ32	PL107B	6	
AD27	PL107C	6	
AE27	PL107D	6	VREF2_6
AG34	PL109A	6	
AH34	PL109B	6	
AC26	PL109C	6	
AB26	PL109D	6	
AK33	PL112A	6	
AL33	PL112B	6	
AG30	PL112C	6	
AH30	PL112D	6	
AL34	PL115A	6	
AM34	PL115B	6	
AJ30	PL115C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AK30	PL115D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AJ31	PL116A	6	
AH31	PL116B	6	
AD26	PL116C	6	
AD25	PL116D	6	
AL32	PL117A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AL31	PL117B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AG29	PL117C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AG28	PL117D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AF28	XRES	-	
AF27	TEMP	6	
AM33	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
F25	B_HDINN0_L	-	PCS 361 CH 0 IN N
E25	B_HDINP0_L	-	PCS 361 CH 0 IN P
D28	B_VDDIB0_L	-	
G25	VCC12	-	
D29	A_VDDIB3_L	-	
C25	VCC12	-	
A25	A_HDINP3_L	-	PCS 360 CH 3 IN P
B25	A_HDINN3_L	-	PCS 360 CH 3 IN N
A26	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
E27	VCC12	-	
B26	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
F26	A_VDDOB3_L	-	
B27	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
F27	A_VDDOB2_L	-	
A27	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
E28	VCC12	-	
B28	A_HDINN2_L	-	PCS 360 CH 2 IN N
A28	A_HDINP2_L	-	PCS 360 CH 2 IN P
D30	A_VDDIB2_L	-	
C28	VCC12	-	
D31	A_VDDIB1_L	-	
C29	VCC12	-	
A29	A_HDINP1_L	-	PCS 360 CH 1 IN P
B29	A_HDINN1_L	-	PCS 360 CH 1 IN N
A30	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
E29	VCC12	-	
B30	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
F28	A_VDDOB1_L	-	
B31	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
F29	A_VDDOB0_L	-	
A31	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
E30	VCC12	-	
B32	A_HDINN0_L	-	PCS 360 CH 0 IN N
A32	A_HDINP0_L	-	PCS 360 CH 0 IN P
D32	A_VDDIB0_L	-	
C32	VCC12	-	
E34	PL30A	7	
F34	PL30B	7	
F33	PL34A	7	
G33	PL34B	7	
K30	PL38A	7	
L30	PL38B	7	
G34	PL40A	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W33	PL42C	7		PL56C	7	
Y33	PL42D	7		PL56D	7	
W37	PL43A	7		PL57A	7	
Y37	PL43B	7		PL57B	7	
Y32	PL43C	7		PL57C	7	
AA32	PL43D	7		PL57D	7	
U38	PL46A	7		PL60A	7	
V38	PL46B	7		PL60B	7	
W34	PL46C	7		PL60C	7	
Y34	PL46D	7		PL60D	7	
T40	PL47A	7	PCLKT7_1	PL61A	7	PCLKT7_1
U40	PL47B	7	PCLKC7_1	PL61B	7	PCLKC7_1
AA33	PL47C	7	PCLKT7_3	PL61C	7	PCLKT7_3
AB33	PL47D	7	PCLKC7_3	PL61D	7	PCLKC7_3
R42	PL48A	7	PCLKT7_0	PL62A	7	PCLKT7_0
T42	PL48B	7	PCLKC7_0	PL62B	7	PCLKC7_0
AA34	PL48C	7	PCLKT7_2	PL62C	7	PCLKT7_2
AB34	PL48D	7	PCLKC7_2	PL62D	7	PCLKC7_2
U41	PL50A	6	PCLKT6_0	PL64A	6	PCLKT6_0
V41	PL50B	6	PCLKC6_0	PL64B	6	PCLKC6_0
V36	PL50C	6	PCLKT6_1	PL64C	6	PCLKT6_1
W36	PL50D	6	PCLKC6_1	PL64D	6	PCLKC6_1
U42	PL51A	6		PL65A	6	
V42	PL51B	6		PL65B	6	
AB31	PL51C	6	PCLKT6_3	PL65C	6	PCLKT6_3
AC31	PL51D	6	PCLKC6_3	PL65D	6	PCLKC6_3
W38	PL52A	6		PL66A	6	
Y38	PL52B	6		PL66B	6	
AA35	PL52C	6	PCLKT6_2	PL66C	6	PCLKT6_2
AB35	PL52D	6	PCLKC6_2	PL66D	6	PCLKC6_2
W39	PL55A	6		PL69A	6	
Y39	PL55B	6		PL69B	6	
AB32	PL55C	6	VREF1_6	PL69C	6	VREF1_6
AC32	PL55D	6		PL69D	6	
W40	PL56A	6		PL70A	6	
Y40	PL56B	6		PL70B	6	
AA36	PL56C	6		PL70C	6	
AB36	PL56D	6		PL70D	6	
W41	PL57A	6		PL71A	6	
Y41	PL57B	6		PL71B	6	
AA37	PL57C	6		PL71C	6	
AB37	PL57D	6		PL71D	6	
W42	PL59A	6		PL73A	6	
Y42	PL59B	6		PL73B	6	
AC33	PL59C	6		PL73C	6	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AF40	PL76A	6		PL90A	6	
AG40	PL76B	6		PL90B	6	
AG36	PL76C	6		PL90C	6	
AH36	PL76D	6	DIFFR_6	PL90D	6	DIFFR_6
AF39	PL77A	6		PL91A	6	
AG39	PL77B	6		PL91B	6	
AF29	PL77C	6		PL91C	6	
AG29	PL77D	6		PL91D	6	
AH42	PL78A	6		PL92A	6	
AG42	PL78B	6		PL92B	6	
AG35	PL78C	6		PL92C	6	
AH35	PL78D	6		PL92D	6	
AG41	PL80A	6		PL94A	6	
AH41	PL80B	6		PL94B	6	
AG34	PL80C	6		PL94C	6	
AH34	PL80D	6		PL94D	6	
AJ42	PL81A	6		PL96A	6	
AK42	PL81B	6		PL96B	6	
AG33	PL81C	6		PL96C	6	
AH33	PL81D	6		PL96D	6	
AJ41	PL82A	6		PL98A	6	
AK41	PL82B	6		PL98B	6	
AJ37	PL82C	6		PL98C	6	
AK37	PL82D	6		PL98D	6	
AJ40	PL84A	6		PL99A	6	
AK40	PL84B	6		PL99B	6	
AJ34	PL84C	6		PL99C	6	
AK34	PL84D	6		PL99D	6	
AJ38	PL85A	6		PL103A	6	
AK38	PL85B	6		PL103B	6	
AH32	PL85C	6		PL103C	6	
AJ32	PL85D	6		PL103D	6	
AL42	PL86A	6		PL104A	6	
AM42	PL86B	6		PL104B	6	
AK36	PL86C	6		PL104C	6	
AL36	PL86D	6		PL104D	6	
AL38	PL89A	6		PL107A	6	
AM38	PL89B	6		PL107B	6	
AJ33	PL89C	6		PL107C	6	
AK33	PL89D	6	VREF2_6	PL107D	6	VREF2_6
AN42	PL90A	6		PL109A	6	
AP42	PL90B	6		PL109B	6	
AH31	PL90C	6		PL109C	6	
AJ31	PL90D	6		PL109D	6	
AN41	PL91A	6		PL112A	6	

Industrial

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-6FN256I	-6	Lead-Free fpBGA	256	IND	15.2
LFSC3GA15E-5FN256I	-5	Lead-Free fpBGA	256	IND	15.2
LFSC3GA15E-6FN900I	-6	Lead-Free fpBGA	900	IND	15.2
LFSC3GA15E-5FN900I	-5	Lead-Free fpBGA	900	IND	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-6FN256I	-6	Lead-Free fpBGA	256	IND	15.2
LFSCM3GA15EP1-5FN256I	-5	Lead-Free fpBGA	256	IND	15.2
LFSCM3GA15EP1-6FN900I	-6	Lead-Free fpBGA	900	IND	15.2
LFSCM3GA15EP1-5FN900I	-5	Lead-Free fpBGA	900	IND	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-6FN900I	-6	Lead-Free fpBGA	900	IND	25.4
LFSC3GA25E-5FN900I	-5	Lead-Free fpBGA	900	IND	25.4
LFSC3GA25E-6FFN1020I[1]	-6	Lead-Free Organic fcBGA	1020	IND	25.4
LFSC3GA25E-5FFN1020I[1]	-5	Lead-Free Organic fcBGA	1020	IND	25.4
LFSC3GA25E-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4
LFSC3GA25E-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-6FN900I	-6	Lead-Free fpBGA	900	IND	25.4
LFSCM3GA25EP1-5FN900I	-5	Lead-Free fpBGA	900	IND	25.4
LFSCM3GA25EP1-6FFN1020I[1]	-6	Lead-Free Organic fcBGA	1020	IND	25.4
LFSCM3GA25EP1-5FFN1020I[1]	-5	Lead-Free Organic fcBGA	1020	IND	25.4
LFSCM3GA25EP1-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4
LFSCM3GA25EP1-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA40E-6FFN1020I[1]	-6	Lead-Free Organic fcBGA	1020	IND	40.4
LFSC3GA40E-5FFN1020I[1]	-5	Lead-Free Organic fcBGA	1020	IND	40.4
LFSC3GA40E-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSC3GA40E-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSC3GA40E-6FCN1152I[2]	-6	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSC3GA40E-5FCN1152I[2]	-5	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSC3GA40E-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	40.4
LFSC3GA40E-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.