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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	3750
Number of Logic Elements/Cells	15000
Total RAM Bits	1054720
Number of I/O	139
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga15ep1-7f256c

Architecture Overview

The LatticeSC architecture contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR). The upper left and upper right corners of the devices contain SERDES blocks and their associated PCS blocks, as shown in Figure 2-1.

Top left and top right corner of the device contain blocks of SERDES. Each block of SERDES contains four channels (quad). Each channel contains a single serializer and de-serializer, synchronization and word alignment logic. The SERDES quad connects with the Physical Coding Sub-layer (PCS) blocks that contain logic to simultaneously perform alignment, coding, de-coding and other functions. The SERDES quad block has separate supply, ground and reference voltage pins.

The PICs contain logic to facilitate the conditioning of signals to and from the I/O before they leave or enter the FPGA fabric. The block provides DDR and shift register capabilities that act as a gearbox between high speed I/O and the FPGA fabric. The blocks also contain programmable Adaptive Input Logic that adjusts the delay applied to signals as they enter the device to optimize setup and hold times and ensure robust performance.

sysMEM EBRs are large dedicated fast memory blocks. They can be configured as RAM, ROM or FIFO. These blocks have dedicated logic to simplify the implementation of FIFOs.

The PFU, PIC and EBR blocks are arranged in a two-dimensional grid with rows and columns as shown in Figure 2-1. These blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

The corners contain the sysCLOCK Analog Phase Locked Loop (PLL) and Delay Locked Loop (DLL) Blocks. The PLLs have multiply, divide and phase shifting capability; they are used to manage the phase relationship of the clocks. The LatticeSC architecture provides eight analog PLLs per device and 12 DLLs. The DLLs provide a simple delay capability and can also be used to calibrate other delays within the device.

Every device in the family has a JTAG Port with internal Logic Analyzer (ispTRACY) capability. The sysCONFIG™ port which allows for serial or parallel device configuration. The system bus simplifies the connections of the external microprocessor to the device for tasks such as SERDES and PCS configuration or interface to the general FPGA logic. The LatticeSC devices use 1.2V as their core voltage operation with 1.0V operation also possible.

Figure 2-3. Slice Diagram

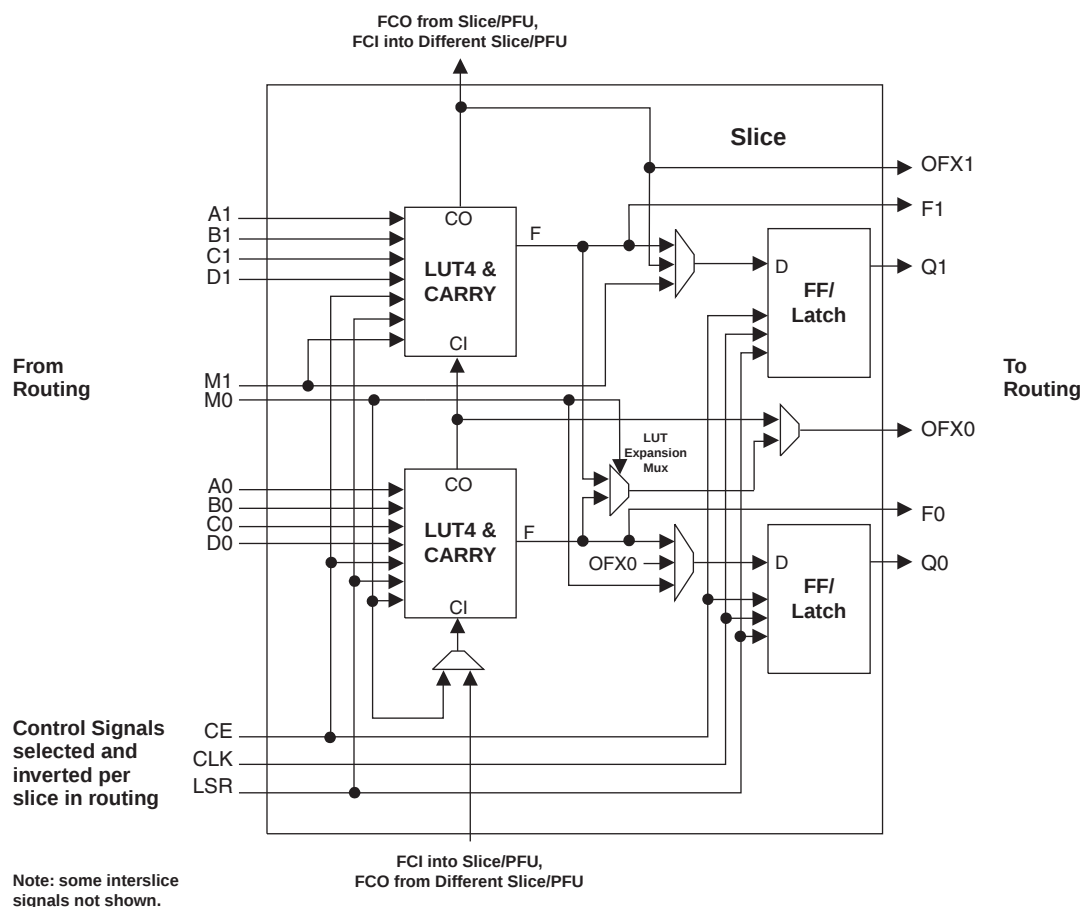


Table 2-1. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry In ¹
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register Outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice
Output	Inter-PFU signal	FCO	For the right most PFU the fast carry chain output ²

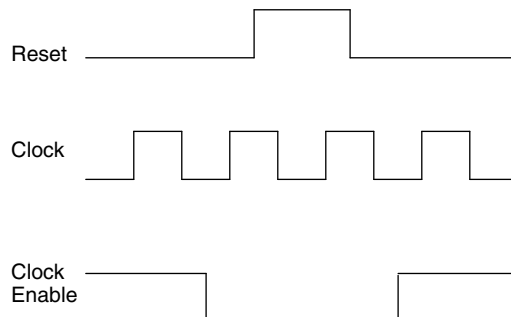
1. See Figure 2-2 for connection details.

2. Requires two PFUs.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the low-to-high transition of the reset, as shown in Figure 2-16.

Figure 2-16. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM, FIFO and shift register implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-16. The reset timing rules apply to the RPRreset input vs. the RE input and the RST input vs. the WE and RE inputs. Both RST and RPRreset are always asynchronous EBR inputs. For the EBR shift register mode, the GSR signal is always enabled and the local RESET pin is always asynchronous.

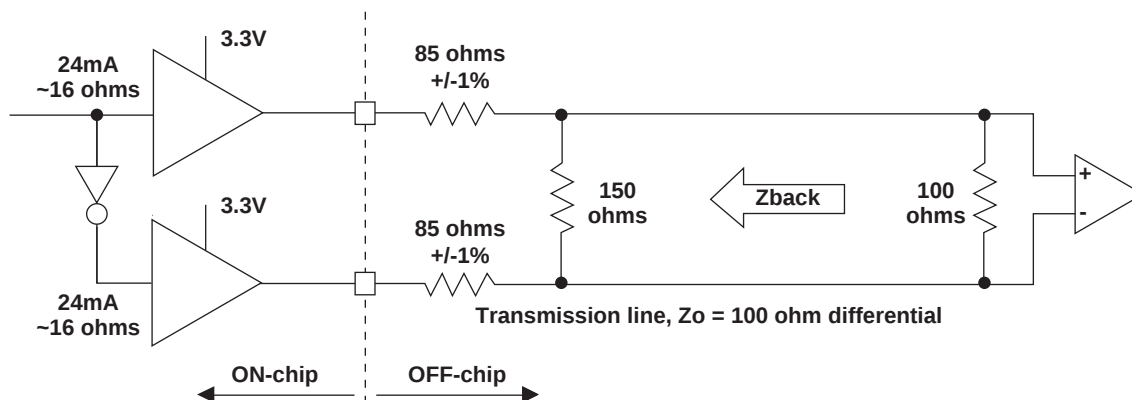
Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled. For more information about on-chip memory, see TN1094, [On-Chip Memory Usage Guide for LatticeSC Devices](#).

Programmable I/O Cells (PIC)

Each PIC contains four PIOs connected to their respective PURESPEED I/O Buffer which are then connected to the PADs as shown in Figure 2-17. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to PURESPEED I/O buffer, and receives input (DI) from the buffer. The PIO contains advanced capabilities to allow the support of speeds up to 2Gbps. These include dedicated shift and DDR logic and adaptive input logic. The dedicated resources simplify the design of robust interfaces.

LVPECL

The LatticeSC devices support differential LVPECL standard. This standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL**Table 3-3. LVPECL DC Conditions¹****Over Recommended Operating Conditions**

Symbol	Description	Nominal	Units
Z_{OUT}	Output impedance	16	ohm
R_S	Driver series resistor	85	ohm
R_P	Driver parallel resistor	150	ohm
R_T	Receiver termination	100	ohm
V_{OH}	Output high voltage	2.03	V
V_{OL}	Output low voltage	1.27	V
V_{OD}	Output differential voltage	0.76	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	86	ohm
I_{DC}	DC output current	12.6	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, BLVDS, MLVDS and other differential interfaces please see details of additional technical documentation at the end of this data sheet.

On-die Differential Common Mode Termination

Symbol	Description	Min.	Typ.	Max.	Units
C_{CMT}	Capacitance V_{CMT} to GND	—	40	—	pF

LatticeSC/M Internal Timing Parameters¹

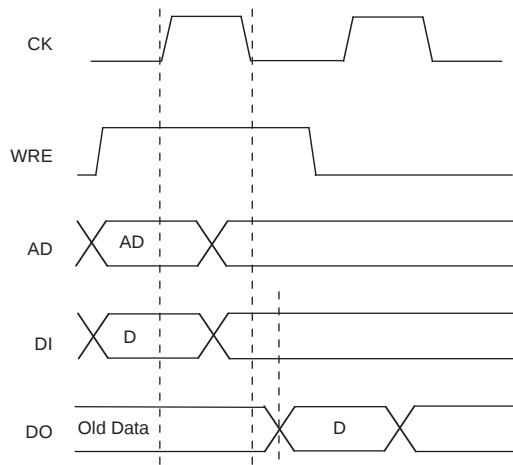
Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

Parameter	Symbol	Description	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
PFU Logic Mode Timing									
t _{LUT4_PFU}	CTOF_DEL	LUT4 delay (A to D inputs to F output)	—	0.045	—	0.050	—	0.054	ns
t _{LUT5_PFU}	MTOOFX_DEL	LUT5 delay (inputs to output)	—	0.152	—	0.172	—	0.192	ns
t _{LSR_PFU}	LSR_DEL	Set/Reset to output (asynchronous)	—	0.378	—	0.426	—	0.474	ns
t _{SUM_PFU}	M_SET	Clock to Mux (M0,M1) input setup time	0.113	—	0.131	—	0.148	—	ns
t _{HM_PFU}	M_HLD	Clock to Mux (M0,M1) input hold time	-0.041	—	-0.046	—	-0.052	—	ns
t _{SUD_PFU}	DIN_SET	Clock to D input setup time	0.072	—	0.083	—	0.094	—	ns
t _{HD_PFU}	DIN_HLD	Clock to D input hold time	-0.028	—	-0.032	—	-0.035	—	ns
t _{CK2Q_PFU}	REG_DEL	Clock to Q delay, D-type register configuration	—	0.224	—	0.252	—	0.279	ns
t _{LE2Q_PFU}	LTCH_DEL	Clock to Q delay latch configuration	—	0.294	—	0.331	—	0.367	ns
t _{LD2Q_PFU}	TLTCH_DEL	D to Q throughput delay when latch is enabled	—	0.300	—	0.338	—	0.376	ns
PFU Memory Mode Timing									
t _{CORAM_PFU}	CLKTOF_DEL	Clock to Output	—	0.575	—	0.649	—	0.724	ns
t _{SUDATA_PFU}	DIN_SET	Data Setup Time	-0.024	—	-0.026	—	-0.027	—	ns
t _{HDATA_PFU}	DIN_HLD	Data Hold Time	0.075	—	0.084	—	0.094	—	ns
t _{SUADDR_PFU}	WAD_SET	Address Setup Time	-0.176	—	-0.196	—	-0.215	—	ns
t _{HADDR_PFU}	WAD_HLD	Address Hold Time	0.110	—	0.124	—	0.138	—	ns
t _{SUWREN_PFU}	WE_SET	Write/Read Enable Setup Time	0.014	—	0.019	—	0.024	—	ns
t _{HWREN_PFU}	WE_HLD	Write/Read Enable Hold Time	0.078	—	0.086	—	0.094	—	ns
PIC Timing									
PIO Input/Output Buffer Timing									
t _{IN_PIO}	IN_DEL	Input Buffer Delay(LVCMOS25)	—	0.578	—	0.661	—	0.744	ns
t _{OUT_PIO}	DOPADI_DEL	Output Buffer Delay(LVCMOS25)	—	2.712	—	3.027	—	3.395	ns
t _{SUI_PIO}	DIN_SET	Input Register Setup Time (Data Before Clock)	0.277	—	0.312	—	0.348	—	ns
t _{HI_PIO}	DIN_HLD	Input Register Hold Time (Data after Clock)	-0.267	—	-0.306	—	-0.345	—	ns
t _{COO_PIO}	CK_DEL	Output Register Clock to Output Delay	—	0.513	—	0.571	—	0.639	ns
t _{SUCE_PIO}	CE_SET	Input Register Clock Enable Setup Time	—	0.000	—	0.000	—	0.000	ns
t _{HCE_PIO}	CE_HLD	Input Register Clock Enable Hold Time	—	0.129	—	0.145	—	0.161	ns
t _{SULSR_PIO}	LSR_SET	Set/Reset Setup Time	0.057	—	0.060	—	0.063	—	ns
t _{HLSR_PIO}	LSR_HLD	Set/Reset Hold Time	-0.151	—	-0.159	—	-0.169	—	ns
t _{LE2Q_PIO}	CK_DEL	Input Register Clock to Q delay latch configuration	—	0.335	—	0.372	—	0.410	ns
t _{LD2Q_PIO}	DIN_DEL	Input Register D to Q throughput delay when latch is enabled	—	0.578	—	0.647	—	0.717	ns

Timing Diagrams

PFU Timing Diagrams

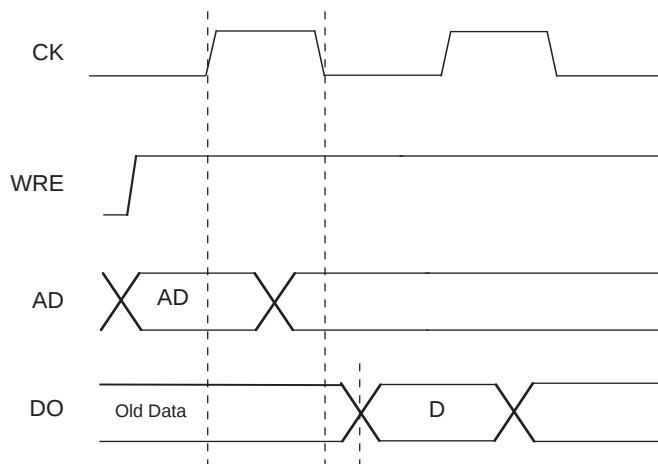
Figure 3-4. Slice Single/Dual Port Write Cycle Timing



Notes:

- Rising Edge for latching WREN, WAD and DATAIN.
- WREN must continue past falling edge clock.
- Data output occurs on negative edge.

Figure 3-5. Slice Single/Dual Port Read Cycle Timing



sysCLOCK DLL Timing**Over Recommended Operating Conditions**

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)		100	—	700	MHz
f_{OUTOP}	Output Clock Frequency (CLKOP)		100	—	700	MHz
f_{OUTOS}	Output Clock Frequency (CLKOS)		25	—	700	MHz
AC Characteristics						
t_{DUTY}	Output Clock Duty Cycle	Output Clock Duty Cycle (at 50% levels, 50% duty cycle input clock, duty cycle correction turned off, time reference delay mode)	38	—	62	%
t_{DUTYRD}	Output Clock Duty Cycle	Output Clock Duty Cycle (at 50% levels, arbitrary duty cycle input clock, duty cycle correction turned on, time reference delay mode)	45	—	55	%
$t_{DUTYCIR}$	Output Clock Duty Cycle	Output Clock Duty Cycle (at 50% levels, arbitrary duty cycle input clock, duty cycle correction turned on, clock injection removal mode)	40	—	60	%
t_{OPJIT}^1	Output Clock Period Jitter		—	—	200	ps
t_{CPJIT}^1	Output Clock Cycle-to-Cycle Jitter		—	—	200	ps
t_{SKEW}	Output Clock to Clock Skew (Between Two Outputs with the Same Phase Setting)		—	—	100	ps
t_{LOCK}	DLL Lock-in Time		8	—	18500	cycles
t_{IDUTY}	Input Clock Duty Cycle	Applies to all operating conditions	35	—	65	%
t_{IPJIT}	Input Clock Period Jitter		—	—	+/- 250	ps
t_{HI}	Input Clock High Time	At 80% level	500	—	—	ps
t_{LO}	Input Clock Low Time	At 20% level	500	—	—	ps
t_{RSWD}	Reset Signal Pulse Width		3	—	—	ns
t_{FDEL}	Timeshift Delay Step Size		35	45	80	ps
t_{DLL}	Delay Through the DLL when No Delay Taps are Chosen but Not in Bypass Mode.		—	760	—	ps

1. Values are measured with FPGA logic active, no additional I/Os toggling and REFCLK total jitter = 30 ps.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
RESETN		Reset. (Also sent to general routing). During configuration it resets the configuration state machine. After configuration this pin can perform the global set/reset (GSR) functions or can be used as a general input pin.
CFGIRQN	O	MPI Interrupt request active low signal is controlled by system bus interrupt controller and may be sourced from any bus error or MPI configuration error. It can be connected to one of MPC860 IRQ pins.
TSALLN	I	Tristates all I/O.
Configuration Pads (User I/O if not used. Used during sysCONFIG.)		
HDC/SI	O	High During Configuration is output high until configuration is complete. It is used as a control output, indicating that configuration is not complete. For SPI modes, this pin is used to download the read command and initial read address into the Flash memory device on the falling edge of SCK. This pin will be connected to SI of the memory. If the SPI mode is used, the 8-bit instruction code 0x03 will be downloaded followed by a 24-bit starting address of 0x000000 or a non-zero stat address for partial reconfiguration. If the SPIX mode has been selected, the 8-bit instruction captured on D[7:0] at power-up will be shifted in and followed by a 32-bit starting address of 0x000000.
LDCN/SCS	O	Low During Configuration is output low until configuration is complete. It is used as a control output, indicating that configuration is not complete. For SPI modes, this is an active low chip select for Flash memories. It will go active after INITN goes high but before SCK begins. During power up LDCN will be low. Once INITN goes high, LDCN will go high for 100ns-200ns after which time it will go back low and configuration can begin. During the 100ns-200ns period, the read instruction will be latched for SPIX mode.
DOUT	O	Serial data output that can drive the D0/DIN of daisy-chained slave devices. The data-stream from this output will propagate preamble bits of the bitstream to daisy-chained devices. Data out on DOUT changes on the rising edge of CCLK.
QOUT/CEON	O	During daisy-chaining configuration, QOUT is the serial data output that can drive the D0/DIN of daisy-chained slave devices that do not propagate preamble bits. Data out on QOUT changes on the rising edge of CCLK. During parallel-chaining configuration, active low CEON enables the cascaded slave device to receive bitstream data.
RDN	I	Used in the asynchronous peripheral configuration mode. A low on RDN changes D[7:3] into status outputs. WRN and RDN should not be used simultaneously. If they are, the write strobe overrides.
WRN	I	When the FPGA is selected, a low on the write strobe, WRN, loads the data on D[7:0] inputs into an internal data buffer.
CS0N CS1	I	Used in the asynchronous peripheral, slave parallel and MPI modes. The FPGA is selected when CS0N is low and CS1 is high. During configuration, a pull-up is enabled on both except with MPI DMA access control.
A[21:0]	I/O	In master parallel mode, A[21:0] is an output and will address the configuration EPROMs up to 4 MB space. For MPI configuration mode, A[17:0] will be the MPI address MPL_ADDR[31:14], A[19:18] will be the transfer size and A[21:20] will be the burst mode and burst in process.

Pin Information Summary (Cont.)

Pin Type		1152 fcBGA			1704 fcBGA	
		LFSC/M40	LFSC/M80	LFSC/M115	LFSC/M80	LFSC/M115
Single Ended User I/O		604	660	660	904	942
Differential Pair User I/O		302	330	330	452	470
LVDS Output Pairs		78	102	102	114	132
Configuration	Dedicated	11	11	11	11	11
	Muxes/MPI sysBus	72	72	72	72	72
JTAG (excluding VCCJ)		4	4	4	4	4
Dedicated Pins		4	4	4	4	4
VCC		44	44	44	76	76
VCC12		52	52	52	88	88
VCCAUX		38	38	38	52	52
VCCIO	Bank 1	10	10	10	10	10
	Bank 2	9	9	9	12	12
	Bank 3	12	12	12	14	14
	Bank 4	12	12	12	14	14
	Bank 5	12	12	12	14	14
	Bank 6	12	12	12	14	14
	Bank 7	9	9	9	12	12
VTT	Bank 2	3	3	3	4	4
	Bank 3	3	3	3	4	4
	Bank 4	3	3	3	5	5
	Bank 5	3	3	3	5	5
	Bank 6	3	3	3	4	4
	Bank 7	3	3	3	4	4
GND		130	130	130	184	184
NC		62	6	6	52	14
Single Ended User / Differential I/O per Bank	Bank 1	80/40	80/40	80/40	80/40	80/40
	Bank 2	60/30	76/38	76/38	96/48	103/51
	Bank 3	96/48	108/54	108/54	132/66	144/72
	Bank 4	106/53	106/53	106/53	184/92	184/92
	Bank 5	106/53	106/53	106/53	184/92	184/92
	Bank 6	96/48	108/54	108/54	132/66	144/72
	Bank 7	60/30	76/38	76/38	96/48	103/51
LVDS Output Pairs Per Bank	Bank 2	15	21	21	24	27
	Bank 3	24	30	30	33	39
	Bank 6	24	30	30	33	39
	Bank 7	15	21	21	24	27
VCCJ		1	1	1	1	1
SERDES (signal + power supply)		108	108	108	212	212
Total		1152	1152	1152	1704	1704

LFSC/M15 Logic Signal Connections: 256 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
N12	PB39C	4	
T15	PB40A	4	PCLKT4_3
R16	PB40B	4	PCLKC4_3
L12	PB43A	4	
M12	PB43B	4	
P16	PB44A	4	
N16	PB44B	4	
R14	PB47C	4	VREF1_4
P15	PB48A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
M13	PB48B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
N13	PB49A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
P14	PB49B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
M16	PR45B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
L16	PR45A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
M14	PR43B	3	
M15	PR43A	3	
K16	PR41D	3	VREF2_3
J16	PR37B	3	
H16	PR37A	3	
L13	PR35D	3	DIFFR_3
L14	PR35B	3	
L15	PR35A	3	
K12	PR31C	3	VREF1_3
J13	PR28D	3	PCLKC3_2
K13	PR28C	3	PCLKT3_2
H15	PR28B	3	
F16	PR28A	3	
J11	PR26D	3	PCLKC3_1
J12	PR26C	3	PCLKT3_1
J15	PR26B	3	PCLKC3_0
J14	PR26A	3	PCLKT3_0
E16	PR24D	2	PCLKC2_2
D16	PR24C	2	PCLKT2_2
H11	PR24B	2	PCLKC2_0
H12	PR24A	2	PCLKT2_0
H13	PR23B	2	PCLKC2_1
H14	PR23A	2	PCLKT2_1
G12	PR22D	2	DIFFR_2
G13	PR22C	2	VREF1_2
F8	PR22B	2	
F9	PR22A	2	
G16	PR18D	2	VREF2_2
F15	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D

LFSC/M15 Logic Signal Connections: 256 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
F14	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
E15	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
E14	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
D9	VCCJ	-	
C16	TDO	-	TDO
B15	TMS	-	
B16	TCK	-	
E13	TDI	-	
C14	PROGRAMN	1	
C15	CCLK	1	
A15	PT43D	1	HDC/SI
A14	PT43C	1	LDCN/SCS
B14	PT41A	1	CS1
E12	PT39B	1	CS0N
D13	PT39A	1	RDN
D12	PT37D	1	WRN
E10	PT37C	1	D7
C11	PT37B	1	D6
D10	PT37A	1	D5
A13	PT36D	1	D4
B12	PT36C	1	D3
A12	PT35B	1	D2
C12	PT35A	1	D1
A11	PT33B	1	D0
B11	PT33A	1	QOUT/CEON
E9	PT32D	1	VREF2_1
E8	PT32B	1	DOUT
D8	PT28C	1	BUSYN/RCLK/SCK
A10	PT27B	1	PCLKC1_0
C10	PT27A	1	PCLKT1_0
E7	PT21C	1	VREF1_1
C9	A_VDDIB3_L	-	
A9	A_HDINP3_L	-	PCS 360 CH 3 IN P
B9	A_HDINN3_L	-	PCS 360 CH 3 IN N
A8	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
B8	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
C8	A_VDDOB3_L	-	
B7	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
C7	A_VDDOB2_L	-	
A7	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
B6	A_HDINN2_L	-	PCS 360 CH 2 IN N
A6	A_HDINP2_L	-	PCS 360 CH 2 IN P
C6	A_VDDIB2_L	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W24	VCCAUX	-		VCCAUX	-	
AC17	VCCAUX	-		VCCAUX	-	
AC18	VCCAUX	-		VCCAUX	-	
AC19	VCCAUX	-		VCCAUX	-	
AD17	VCCAUX	-		VCCAUX	-	
AD18	VCCAUX	-		VCCAUX	-	
AD19	VCCAUX	-		VCCAUX	-	
AC12	VCCAUX	-		VCCAUX	-	
AC13	VCCAUX	-		VCCAUX	-	
AC14	VCCAUX	-		VCCAUX	-	
AD12	VCCAUX	-		VCCAUX	-	
AD13	VCCAUX	-		VCCAUX	-	
AD14	VCCAUX	-		VCCAUX	-	
U7	VCCAUX	-		VCCAUX	-	
U8	VCCAUX	-		VCCAUX	-	
V7	VCCAUX	-		VCCAUX	-	
V8	VCCAUX	-		VCCAUX	-	
W7	VCCAUX	-		VCCAUX	-	
W8	VCCAUX	-		VCCAUX	-	
M7	VCCAUX	-		VCCAUX	-	
M8	VCCAUX	-		VCCAUX	-	
N7	VCCAUX	-		VCCAUX	-	
N8	VCCAUX	-		VCCAUX	-	
H10	VCCIO1	-		VCCIO1	-	
H21	VCCIO1	-		VCCIO1	-	
H22	VCCIO1	-		VCCIO1	-	
H9	VCCIO1	-		VCCIO1	-	
J11	VCCIO1	-		VCCIO1	-	
J12	VCCIO1	-		VCCIO1	-	
J13	VCCIO1	-		VCCIO1	-	
J14	VCCIO1	-		VCCIO1	-	
J15	VCCIO1	-		VCCIO1	-	
J16	VCCIO1	-		VCCIO1	-	
J17	VCCIO1	-		VCCIO1	-	
J18	VCCIO1	-		VCCIO1	-	
J19	VCCIO1	-		VCCIO1	-	
J20	VCCIO1	-		VCCIO1	-	
J23	VCCIO2	-		VCCIO2	-	
J24	VCCIO2	-		VCCIO2	-	
K23	VCCIO2	-		VCCIO2	-	
K24	VCCIO2	-		VCCIO2	-	
L22	VCCIO2	-		VCCIO2	-	
L23	VCCIO2	-		VCCIO2	-	
M22	VCCIO2	-		VCCIO2	-	
N22	VCCIO2	-		VCCIO2	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
H1	PR25B	2		PR23B	2	
H2	PR25A	2		PR23A	2	
N8	PR22D	2		PR25D	2	
M8	PR22C	2		PR25C	2	
H4	PR22B	2		PR25B	2	
J4	PR22A	2		PR25A	2	
G1	PR21B	2		PR22B	2	
G2	PR21A	2		PR22A	2	
L7	PR20D	2		PR21D	2	
L8	PR20C	2		PR21C	2	
F2	PR20B	2		PR21B	2	
F1	PR20A	2		PR21A	2	
K5	PR18D	2	VREF2_2	PR18D	2	VREF2_2
J5	PR18C	2		PR18C	2	
E2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
E1	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
N10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
M10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
D2	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
D1	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
K6	PR16D	2		PR16D	2	
K7	PR16C	2		PR16C	2	
J8	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
K8	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
J10	VCCJ	-		VCCJ	-	
J9	TDO	-	TDO	TDO	-	TDO
K9	TMS	-		TMS	-	
J12	TCK	-		TCK	-	
J13	TDI	-		TDI	-	
K12	PROGRAMN	1		PROGRAMN	1	
K13	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
K10	CCLK	1		CCLK	1	
F5	RESP_URC	-		RESP_URC	-	
B5	VCC12	-		VCC12	-	
D5	A_REFCLKN_R	-		A_REFCLKN_R	-	
C5	A_REFCLKP_R	-		A_REFCLKP_R	-	
B2	A_VDDIB0_R	-		A_VDDIB0_R	-	
C1	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P
C2	A_HDINN0_R	-	PCS 3E0 CH 0 IN N	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
A3	A_HDOUPT0_R	-	PCS 3E0 CH 0 OUT P	A_HDOUPT0_R	-	PCS 3E0 CH 0 OUT P
D3	A_VDDOB0_R	-		A_VDDOB0_R	-	
B3	A_HDOUPTN0_R	-	PCS 3E0 CH 0 OUT N	A_HDOUPTN0_R	-	PCS 3E0 CH 0 OUT N
D4	A_VDDOB1_R	-		A_VDDOB1_R	-	
B4	A_HDOUPTN1_R	-	PCS 3E0 CH 1 OUT N	A_HDOUPTN1_R	-	PCS 3E0 CH 1 OUT N
A4	A_HDOUPT1_R	-	PCS 3E0 CH 1 OUT P	A_HDOUPT1_R	-	PCS 3E0 CH 1 OUT P
H5	A_HDINN1_R	-	PCS 3E0 CH 1 IN N	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
G5	A_HDINP1_R	-	PCS 3E0 CH 1 IN P	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
F4	A_VDDIB1_R	-		A_VDDIB1_R	-	
H6	A_VDDIB2_R	-		A_VDDIB2_R	-	
F6	A_HDINP2_R	-	PCS 3E0 CH 2 IN P	A_HDINP2_R	-	PCS 3E0 CH 2 IN P

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G27	A_REFCLKP_L	-		A_REFCLKP_L	-	
H27	A_REFCLKN_L	-		A_REFCLKN_L	-	
H25	VCC12	-		VCC12	-	
H26	RESP_ULC	-		RESP_ULC	-	
B33	RESETN	1		RESETN	1	
C34	TSALLN	1		TSALLN	1	
D34	DONE	1		DONE	1	
C33	INITN	1		INITN	1	
J27	M0	1		M0	1	
K27	M1	1		M1	1	
M26	M2	1		M2	1	
L26	M3	1		M3	1	
F30	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
G30	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
H28	PL16C	7		PL16C	7	
J28	PL16D	7		PL16D	7	
F31	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
G31	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N25	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P25	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
D33	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
E33	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
H29	PL18C	7		PL18C	7	
J29	PL18D	7	VREF2_7	PL18D	7	VREF2_7
F32	PL21A	7		PL20A	7	
G32	PL21B	7		PL20B	7	
P26	PL21C	7		PL20C	7	
N26	PL21D	7		PL20D	7	
H30	PL22A	7		PL21A	7	
J30	PL22B	7		PL21B	7	
L28	PL22C	7		PL21C	7	
M28	PL22D	7		PL21D	7	
J31	PL23A	7		PL29A	7	
K31	PL23B	7		PL29B	7	
L27	PL23C	7	VREF1_7	PL29C	7	VREF1_7
M27	PL23D	7	DIFFR_7	PL29D	7	DIFFR_7
J32	PL25A	7		PL31A	7	
K32	PL25B	7		PL31B	7	
L29	PL25C	7		PL31C	7	
M29	PL25D	7		PL31D	7	
H33	PL26A	7		PL33A	7	
J33	PL26B	7		PL33B	7	
N27	PL26C	7		PL33C	7	
P27	PL26D	7		PL33D	7	
K33	PL27A	7		PL35A	7	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AG18	PB42C	5		PB61C	5	
AF18	PB42D	5		PB61D	5	
AP19	PB43A	5		PB63A	5	
AP18	PB43B	5		PB63B	5	
AJ18	PB43C	5		PB63C	5	
AH18	PB43D	5		PB63D	5	
AP17	PB45A	4		PB65A	4	
AP16	PB45B	4		PB65B	4	
AJ17	PB45C	4		PB65C	4	
AH17	PB45D	4		PB65D	4	
AN17	PB46A	4		PB66A	4	
AN16	PB46B	4		PB66B	4	
AE17	PB46C	4		PB66C	4	
AD17	PB46D	4		PB66D	4	
AK17	PB47A	4		PB67A	4	
AK16	PB47B	4		PB67B	4	
AG17	PB47C	4		PB67C	4	
AF17	PB47D	4		PB67D	4	
AM16	PB49A	4		PB69A	4	
AM15	PB49B	4		PB69B	4	
AJ15	PB49C	4		PB69C	4	
AJ14	PB49D	4		PB69D	4	
AL16	PB50A	4		PB70A	4	
AL15	PB50B	4		PB70B	4	
AG16	PB50C	4		PB70C	4	
AF16	PB50D	4		PB70D	4	
AP15	PB51A	4		PB71A	4	
AP14	PB51B	4		PB71B	4	
AH15	PB51C	4		PB71C	4	
AH14	PB51D	4		PB71D	4	
AN15	PB53A	4	PCLKT4_2	PB74A	4	PCLKT4_2
AN14	PB53B	4	PCLKC4_2	PB74B	4	PCLKC4_2
AE16	PB53C	4	PCLKT4_7	PB74C	4	PCLKT4_7
AD16	PB53D	4	PCLKC4_7	PB74D	4	PCLKC4_7
AK15	PB54A	4	PCLKT4_1	PB75A	4	PCLKT4_1
AK14	PB54B	4	PCLKC4_1	PB75B	4	PCLKC4_1
AG15	PB54C	4	PCLKT4_6	PB75C	4	PCLKT4_6
AG14	PB54D	4	PCLKC4_6	PB75D	4	PCLKC4_6
AM13	PB55A	4	PCLKT4_0	PB77A	4	PCLKT4_0
AM12	PB55B	4	PCLKC4_0	PB77B	4	PCLKC4_0
AJ12	PB55C	4	VREF2_4	PB77C	4	VREF2_4
AJ11	PB55D	4		PB77D	4	
AL13	PB57A	4	PCLKT4_5	PB79A	4	PCLKT4_5
AL12	PB57B	4	PCLKC4_5	PB79B	4	PCLKC4_5
AH12	PB57C	4		PB79C	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
N27	PL47C	7	
P27	PL47D	7	
K33	PL49A	7	
L33	PL49B	7	
M30	PL49C	7	
N30	PL49D	7	
M31	PL51A	7	
N31	PL51B	7	
P24	PL51C	7	
R24	PL51D	7	
M33	PL56A	7	
N33	PL56B	7	
U25	PL56C	7	
T25	PL56D	7	
L34	PL57A	7	
M34	PL57B	7	
P29	PL57C	7	
R29	PL57D	7	
N34	PL60A	7	
P34	PL60B	7	
R27	PL60C	7	
T27	PL60D	7	
R32	PL61A	7	PCLKT7_1
R31	PL61B	7	PCLKC7_1
U24	PL61C	7	PCLKT7_3
T24	PL61D	7	PCLKC7_3
P33	PL62A	7	PCLKT7_0
R33	PL62B	7	PCLKC7_0
T26	PL62C	7	PCLKT7_2
U26	PL62D	7	PCLKC7_2
T32	PL64A	6	PCLKT6_0
T31	PL64B	6	PCLKC6_0
U29	PL64C	6	PCLKT6_1
V29	PL64D	6	PCLKC6_1
T30	PL65A	6	
U30	PL65B	6	
U27	PL65C	6	PCLKT6_3
V27	PL65D	6	PCLKC6_3
R34	PL66A	6	
T34	PL66B	6	
U28	PL66C	6	PCLKT6_2
V28	PL66D	6	PCLKC6_2
V30	PL69A	6	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP20	PB61B	5	
AH21	PB61C	5	
AH20	PB61D	5	
AM20	PB63A	5	
AM19	PB63B	5	
AJ21	PB63C	5	
AJ20	PB63D	5	
AK19	PB66A	5	
AK18	PB66B	5	
AE18	PB66C	5	
AD18	PB66D	5	
AN19	PB69A	5	
AN18	PB69B	5	
AG18	PB69C	5	
AF18	PB69D	5	
AP19	PB71A	5	
AP18	PB71B	5	
AJ18	PB71C	5	
AH18	PB71D	5	
AP17	PB73A	4	
AP16	PB73B	4	
AJ17	PB73C	4	
AH17	PB73D	4	
AN17	PB75A	4	
AN16	PB75B	4	
AE17	PB75C	4	
AD17	PB75D	4	
AK17	PB78A	4	
AK16	PB78B	4	
AG17	PB78C	4	
AF17	PB78D	4	
AM16	PB81A	4	
AM15	PB81B	4	
AJ15	PB81C	4	
AJ14	PB81D	4	
AL16	PB83A	4	
AL15	PB83B	4	
AG16	PB83C	4	
AF16	PB83D	4	
AP15	PB86A	4	
AP14	PB86B	4	
AH15	PB86C	4	
AH14	PB86D	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
V8	PR65D	3	PCLKC3_3
U8	PR65C	3	PCLKT3_3
U5	PR65B	3	
T5	PR65A	3	
V6	PR64D	3	PCLKC3_1
U6	PR64C	3	PCLKT3_1
T4	PR64B	3	PCLKC3_0
T3	PR64A	3	PCLKT3_0
U9	PR62D	2	PCLKC2_2
T9	PR62C	2	PCLKT2_2
R2	PR62B	2	PCLKC2_0
P2	PR62A	2	PCLKT2_0
T11	PR61D	2	PCLKC2_3
U11	PR61C	2	PCLKT2_3
R4	PR61B	2	PCLKC2_1
R3	PR61A	2	PCLKT2_1
T8	PR60D	2	
R8	PR60C	2	
P1	PR60B	2	
N1	PR60A	2	
R6	PR57D	2	
P6	PR57C	2	
M1	PR57B	2	
L1	PR57A	2	
T10	PR56D	2	
U10	PR56C	2	
N2	PR56B	2	
M2	PR56A	2	
R11	PR51D	2	
P11	PR51C	2	
N4	PR51B	2	
M4	PR51A	2	
N5	PR49D	2	
M5	PR49C	2	
L2	PR49B	2	
K2	PR49A	2	
P8	PR47D	2	
N8	PR47C	2	
J2	PR47B	2	
H2	PR47A	2	
M6	PR45D	2	
L6	PR45C	2	
K3	PR45B	2	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AG38	NC	-		PL95A	6	
AH38	NC	-		PL95B	6	
AJ39	NC	-		PL100A	6	
AK39	NC	-		PL100B	6	
AL41	NC	-		PL105A	6	
AM41	NC	-		PL105B	6	
AN40	NC	-		PL108A	6	
AM40	NC	-		PL108B	6	
AM39	NC	-		PL111A	6	
AN39	NC	-		PL111B	6	
AR42	NC	-		PL113A	6	
AT42	NC	-		PL113B	6	
AT1	NC	-		PR113B	3	
AR1	NC	-		PR113A	3	
AN4	NC	-		PR111B	3	
AM4	NC	-		PR111A	3	
AM3	NC	-		PR108B	3	
AN3	NC	-		PR108A	3	
AM2	NC	-		PR105B	3	
AL2	NC	-		PR105A	3	
AK4	NC	-		PR100B	3	
AJ4	NC	-		PR100A	3	
AH5	NC	-		PR95B	3	
AG5	NC	-		PR95A	3	
P6	NC	-		PR39B	2	
N6	NC	-		PR39A	2	
L3	NC	-		PR36B	2	
K3	NC	-		PR36A	2	
M5	NC	-		PR35A	2	
L4	NC	-		PR32B	2	
K4	NC	-		PR32A	2	
A2	GND	-		GND	-	
A41	GND	-		GND	-	
AA20	GND	-		GND	-	
AA23	GND	-		GND	-	
AA3	GND	-		GND	-	
AA39	GND	-		GND	-	
AB20	GND	-		GND	-	
AB23	GND	-		GND	-	
AB4	GND	-		GND	-	
AB40	GND	-		GND	-	
AC17	GND	-		GND	-	
AC19	GND	-		GND	-	
AC21	GND	-		GND	-	
AC22	GND	-		GND	-	

Date	Version	Section	Change Summary
September 2007	01.7	Pinout Information	Added Thermal Management text section.
		Supplemental Information	Updated title list.
November 2007	01.8	Ordering Information	Removed -7 speed grade information for 115K LUT devices in the Ordering Information tables.
January 2008	01.9	Introduction	Corrections/Additions to memory controller list (Tables 1-2).
		Architecture	AIL Overview – Modified power used by AIL block.
			PURESPEED I/O Buffer Banks – Modified VTT termination info. Added info about complimentary drivers for all banks.
			Supported Source Synchronous Interfaces – Modified data for DDRII in Table 2-11.
		DC and Switching Characteristics	Recommended Operating Conditions – Changed footnote 3.
			Initialization and Standby Supply Current – Inserted a paragraph with info regarding the table. Also updated the table.
			Typical Building Block Function Performance – Added VCC=1.2V=1.2V+/-5% above Pin to Pin Performance table.
			LatticeSC External Switching Characteristics – Added VCC=1.2V=1.2V+/-5% above table. Reworded footnote 3.
			LatticeSC Family Timing Adders – Added VCC=1.2V=1.2V+/-5% above table.
			LatticeSC Internal Timing Parameters – Added VCC=1.2V=1.2V+/-5% above table. Reworded footnote 1.
			GSR Timing – Added a new table for Internal System Bus Timing after GSR Timing.
			LatticeSC sysCONFIG Port Timing – Corrected sysCONFIG SPI Port information.
		Pinout Information	Signal Descriptions – Modified info for VTT_x, PROBE_VCC, and PROBE_GND. Modified info for [LOC]_DLL[T,C]_IN[C,D,E,F].
		Supplemental Information	Updated list of technical notes, added reference to LatticeSC/M flexiPCS Data Sheet.
March 2008	02.0	DC and Switching Characteristics	Updated Internal Timing Parameters table.
			Updated Read Mode timing diagram.
			Updated Read Mode with Input Registers Only timing diagram.
June 2008	02.1	—	Data sheet status changed from preliminary to final.
		Architecture	Removed Read-Before-Write sysMEM EBR mode.
		DC and Switching Characteristics	Updated LatticeSC/M External Switching Characteristics table.
			Updated LatticeSC/M Internal Timing Parameters table.
December 2008	02.2	Architecture	Removed Read-Before-Write sysMEM EBR mode.
			Output/Tristate DDR/Shift Register Block Diagram - corrected connection to POS.
			DC and Switching Characteristics table - updated data for t_{SUI_PIO} .
		Multiple	Added T_R , T_F parameter to PURESPEED I/O Differential Electrical Characteristics (LVDS) table.
January 2010	02.3	Multiple	Removed references to HyperTransport throughout the data sheet.
		Introduction	Updated per PCN #01A-10 (ceramic fcBGA conversion to organic fcBGA for the 1152-ball and 1704-ball fcBGA packages) and PCN #02A-10 (1020-ball organic fcBGA conversion to 1020-ball organic fcBGA revision 2 package).
		Ordering Information	