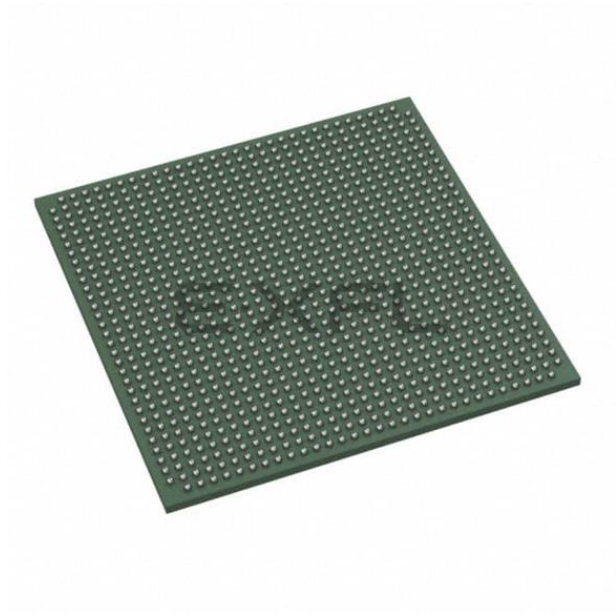
# Lattice Semiconductor Corporation - LFSCM3GA25EP1-5FF1020C Datasheet



**Welcome to E-XFL.COM**

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 6250 |
| Number of Logic Elements/Cells | 25000 |
| Total RAM Bits | 1966080 |
| Number of I/O | 476 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1020-BBGA, FCBGA |
| Supplier Device Package | 1020-OFCBGA (33x33) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga25ep1-5ff1020c |

# LatticeSC/M Family Data Sheet Introduction

January 2010 Data Sheet DS1004

## Features

- **High Performance FPGA Fabric**
  - 15K to 115K four input Look-up Tables (LUT4s)
  - 139 to 942 I/Os
  - 700MHz global clock; 1GHz edge clocks
- **4 to 32 High Speed SERDES and flexiPCS™ (per Device)**
  - Performance ranging from 600Mbps to 3.8Gbps
  - Excellent Rx jitter tolerance (0.8UI at 3.125Gbps)
  - Low Tx jitter (0.25UI typical at 3.125Gbps)
  - Built-in Pre-emphasis and equalization
  - Low power (typically 105mW per channel)
  - Embedded Physical Coding Sublayer (PCS) provides pre-engineered implementation for the following standards:
    - GbE, XAUI, PCI Express, SONET, Serial RapidIO, 1G Fibre Channel, 2G Fibre Channel
- **2Gbps High Performance PURESPEED™ I/O**
  - Supports the following performance bandwidths
    - Differential I/O up to 2Gbps DDR (1GHz Clock)
    - Single-ended memory interfaces up to 800Mbps
  - 144 Tap programmable Input Delay (INDEL) block on every I/O dynamically aligns data to clock for robust performance
    - Dynamic bit Adaptive Input Logic (AIL) monitoring and control circuitry per pin that automatically ensures proper set-up and hold
    - Dynamic bus: uses control bus from DLL
    - Static per bit
  - Electrical standards supported:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2, LVTTL
    - SSTL 3/2/18 I, II; HSTL 18/15 I, II
    - PCI, PCI-X
    - LVDS, Mini-LVDS, Bus-LVDS, MLVDS, LVPECL, RSDS
  - Programmable On Die Termination (ODT)
    - Includes Thevenin Equivalent and low power $V_{TT}$ termination options
- **Memory Intensive FPGA**
  - sysMEM™ embedded Block RAM
    - 1 to 7.8 Mbits memory
    - True Dual Port/Pseudo Dual Port/Single Port
    - Dedicated FIFO logic for all block RAM
    - 500MHz performance
  - Additional 240K to 1.8Mbits distributed RAM
- **sysCLOCK™ Network**
  - Eight analog PLLs per device
    - Frequency range from 15MHz to 1GHz
    - Spread spectrum support
  - 12 DLLs per device with direct control of I/O delay
    - Frequency range from 100MHz to 700MHz
  - Extensive clocking network
    - 700MHz primary and 325 MHz secondary clocks
    - 1GHz I/O-connected edge clocks
  - Precision Clock Divider
    - Phase matched x2 and x4 division of incoming clocks
  - Dynamic Clock Select (DCS)
    - Glitch free clock MUX
- **Masked Array for Cost Optimization (MACO™) Blocks**
  - On-chip structured ASIC Blocks provide pre-engineered IP for low power, low cost system level integration
- **High Performance System Bus**
  - Ties FPGA elements together with a standard bus framework
    - Connects to peripheral user interfaces for run-time dynamic configuration
- **System Level Support**
  - IEEE standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer
  - IEEE Standard 1532 in-system configuration
  - 1.2V and 1.0V operation
  - Onboard oscillator for initialization and general use
  - Embedded PowerPC microprocessor interface
  - Low cost wire-bond and high pin count flip-chip packaging
  - Low cost SPI Flash RAM configuration

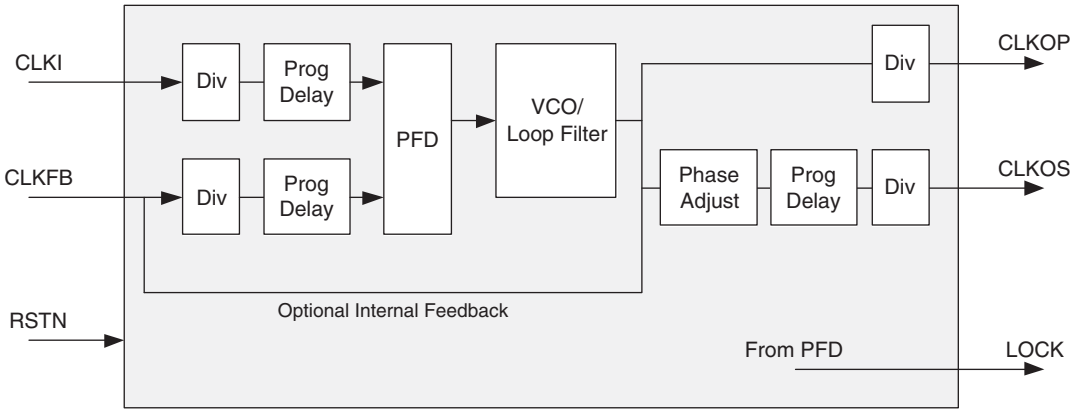
The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically.

The Phase Select block can modify the phase of the clock signal if desired. The Spread Spectrum block supports the modulation of the PLL output frequency. This reduces the peak energy in the fundamental and its harmonics providing for lower EMI (Electro Magnetic Interference).

The sysCLOCK PLL can be configured at power-up and then, if desired, reconfigured dynamically through the serial memory interface bus which connects with the on-chip system bus. For example, the user can select inputs, loop filters, divider setting, delay settings and phase shift settings. The user can also directly access the SMI bus through the routing.

The PLL clock input, from pin or routing, feeds into an input divider. There are four sources of feedback signal to the feedback divider: from the clock net, directly from the voltage controlled oscillator (VCO) output, from the routing or from an external pin. The signal from the input clock divider and the feedback divider are passed through the programmable delay before entering the phase frequency detector (PFD) unit. The output of this PFD is used to control the voltage controlled oscillator. There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

***Figure 2-11. PLL Diagram***




For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

## Spread Spectrum Clocking (SSC)

The PLL supports spread spectrum clocking to reduce peak EMI by using “down-spread” modulation. The spread spectrum operation will vary the output frequency (at 30KHz to 500KHz) in a range that is between its nominal value, down to a frequency that is a programmable 1%, 2%, or 3% lower than normal.

## Digital Locked Loop (DLLs)

In addition to PLLs, the LatticeSC devices have up to 12 DLLs per device. DLLs assist in the management of clocks and strobes. DLLs are well suited to applications where the clock may be stopped or transferring jitter from input to output is important, for example forward clocked interfaces. PLLs are good for applications requiring the lowest output jitter or jitter filtering. All DLL outputs are routed as primary/edge clock sources.

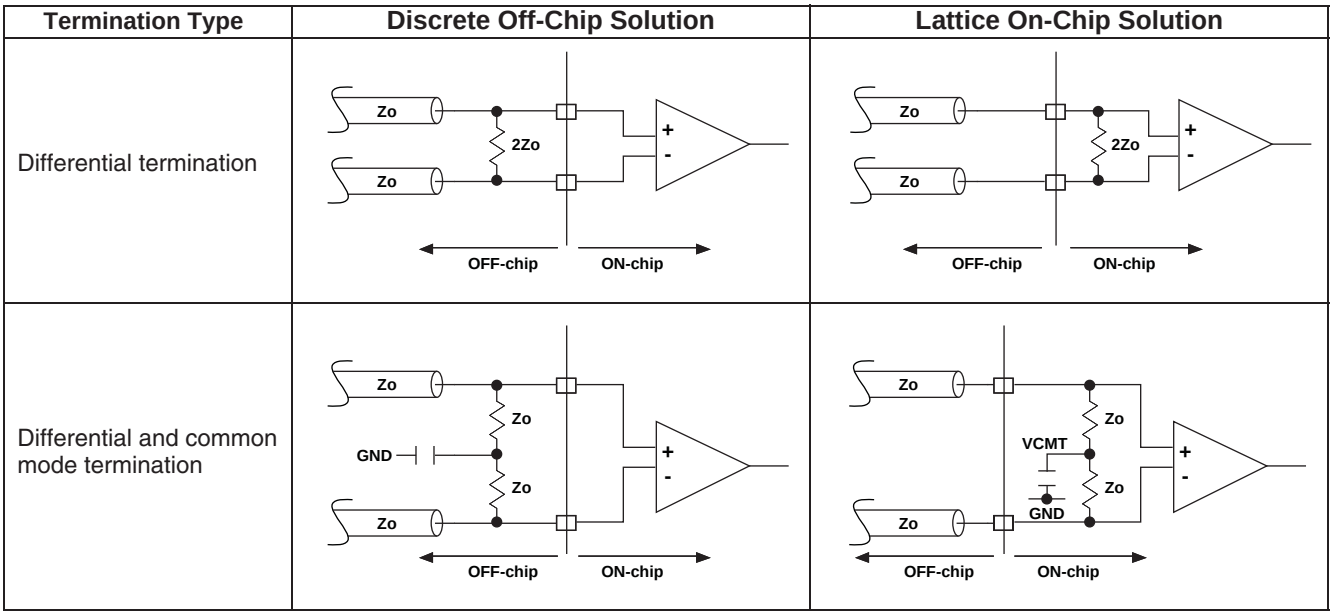
The DLL has two independent clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine phase shift and divider blocks to allow this output to be further modified, if required. The fine phase shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. LOCK output signal is asserted when the DLL is locked. The ALU HOLD signal setting allows users to freeze the DLL at its current delay setting.

**Differential Input Termination**

The LatticeSC device allows two types of differential termination. The first is a single resistor across the differential inputs. The second is a center-tapped system where each input is terminated to the on-chip termination bus $V_{CMT}$. The $V_{CMT}$ bus is DC-coupled through an internal capacitor to ground.

Figure 2-29 shows the differential termination schemes and Table 2-9 shows the nominal values of the termination resistors.

***Figure 2-29. Differential Termination Scheme***




**Calibration**

There are two calibration sources that are associated with the termination scheme used in the LatticeSC devices:

- DIFFR – This pin occurs in each bank that supports differential drivers and must be connected through a 1K+/-1% resistor to ground if differential outputs are used. Note that differential drivers are not supported in banks 1, 4 and 5.
- XRES – There is one of these pins per device. It is used for several functions including calibrating on-chip termination. This pin should always be connected through a 1K+/-1% resistor to ground.

The LatticeSC devices support two modes of calibration:

- Continuous – In this mode the SC devices continually calibrate the termination resistances. Calibration happens several times a second. Using this mode ensures that termination resistances remain calibrated as the silicon junction temperature changes.
- User Request – In this mode the calibration circuit operates continuously. However, the termination resistor values are only updated on the assertion of the calibration_update signal available to the core logic.

For more information on calibration, refer to the details of additional technical documentation at the end of this data sheet.

## Hot Socketing

The LatticeSC devices have been carefully designed to ensure predictable behavior during power-up and power-down. To ensure proper power sequencing, care must be taken during power-up and power-down as described below. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits,

## Power Supply Ramp Rates

| Symbol | Parameter | Condition | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $t_{RAMP}$ | Power supply ramp rates for all power supplies | Over process, voltage, temperature | 3.45 | — | — | mV/µs |
| | | | — | — | 75 | ms |

1. See the Power-up and Power-Down requirements section for more details on power sequencing.
2. From 0.5V to minimum operating voltage.

## Hot Socketing Specifications[1]

| Symbol | Parameter | Condition | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $I_{DK}$ | Programmable and dedicated Input or I/O leakage current[2, 3, 4, 5, 6] | 0 <= $V_{IN}$ <= $V_{IH}$ (MAX) | — | — | ±1500 | µA |
| $I_{HDIN}$ | SERDES average input current when device powered down and inputs driven[7] | | — | — | 4 | mA |

1. See Hot Socket power up/down information in Chapter 2 of this document.
2. Assumes monotonic rise/fall rates for all power supplies.
3. Sensitive to power supply sequencing as described in hot socketing section.
4. Assumes power supplies are between 0 and maximum recommended operations conditions.
5. IDK is additive to $I_{PU}$, $I_{PD}$ or $I_{BH}$.
6. Represents DC conditions. For the first 20ns after hot insertion, current specification is 8 mA.
7. Assumes that the device is powered down with all supplies grounded, both P and N inputs driven by a CML driver with maximum allowed VDDOB of 1.575V, 8b/10b data and internal AC coupling.

## DC Electrical Characteristics[5]

**Over Recommended Operating Conditions**

| Symbol | Parameter | Condition | Min.[3] | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IL}$, $I_{IH}$[1] | Input or I/O Low leakage | 0 ≤ $V_{IN}$ ≤ $V_{IH}$ (MAX) | — | — | 10 | µA |
| $I_{PU}$ | I/O Active Pull-up Current | 0 ≤ $V_{IN}$ ≤ 0.7 $V_{CCIO}$ | -30 | — | -210 | µA |
| $I_{PD}$ | I/O Active Pull-down Current | $V_{IL}$ (MAX) ≤ $V_{IN}$ ≤ $V_{IH}$ (MAX) | 30 | — | 210 | µA |
| $I_{BHLS}$ | Bus Hold Low Sustaining Current | $V_{IN}$ = $V_{IL}$ (MAX) | 30 | — | — | µA |
| $I_{BHHS}$ | Bus Hold High Sustaining Current | $V_{IN}$ = 0.7$V_{CCIO}$ | -30 | — | — | µA |
| $I_{BHLO}$ | Bus Hold Low Overdrive Current | 0 ≤ $V_{IN}$ ≤ $V_{IH}$ (MAX) | — | — | 210 | µA |
| $I_{BHLH}$ | Bus Hold High Overdrive Current | 0 ≤ $V_{IN}$ ≤ $V_{IH}$ (MAX) | — | — | -210 | µA |
| $I_{CL}$ | PCI Low Clamp Current | -3 < $V_{IN}$ ≤ -1 | -25 + ($V_{IN}$ + 1)/0.015 | — | — | mA |
| $I_{CH}$ | PCI High Clamp Current | $V_{CC}$ + 4 > $V_{IN}$ ≥ $V_{CC}$ + 1 | 25 + ($V_{IN}$ - $V_{CC}$ -1)/ 0.015 | — | — | mA |
| $V_{BHT}$ | Bus Hold trip Points | 0 ≤ $V_{IN}$ ≤ $V_{IH}$ (MAX) | $V_{IL}$ (MAX) | — | $V_{IH}$ (MIN) | V |
| C1 | I/O Capacitance[2] | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{CCIP2}$ = 1.2V, $V_{CCAUX}$ = 2.5, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 8 | — | pf |
| C3[2] | Dedicated Input Capacitance[2] | $V_{CCIO}$ = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, $V_{CC}$ = 1.2V, $V_{CCIP2}$ = 1.2V, $V_{CCAUX}$ = 2.5, $V_{IO}$ = 0 to $V_{IH}$ (MAX) | — | 6 | — | pf |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. $T_A$ 25°C, f = 1.0MHz
3. $I_{PU}$, $I_{PD}$, $I_{BHLS}$ and $I_{BHHS}$ have minimum values of 15 or -15µA if $V_{CCIO}$ is set to 1.2V nominal.
4. This table does not apply to SERDES pins.
5. For programmable I/Os.

## Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

### MLVDS

The LatticeSC devices support the MLVDS standard. This industry standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. MLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-1 is one possible solution for bi-directional multi-point differential signals.

***Figure 3-1. MLVDS Multi-Point Output Example***

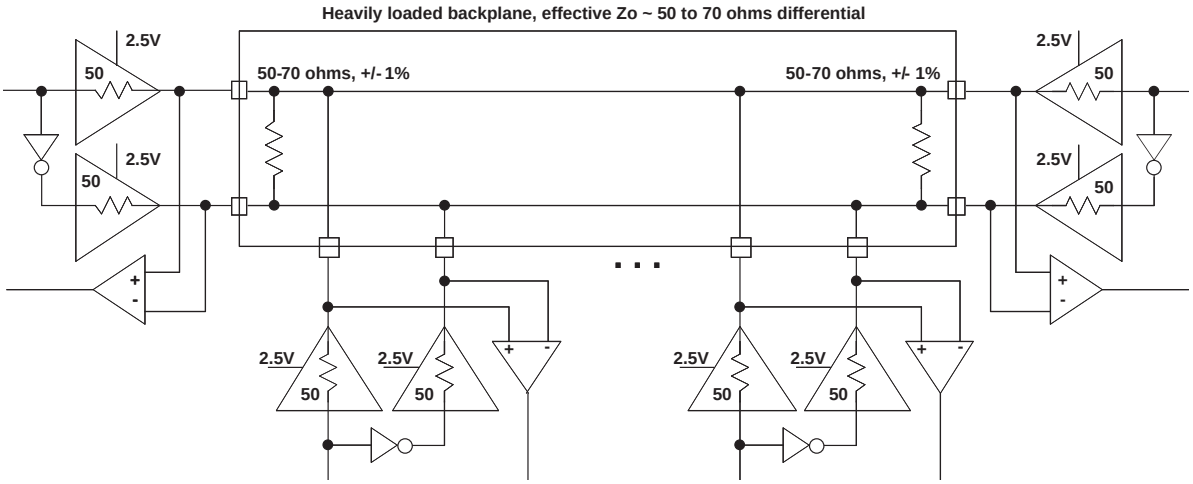



***Table 3-1. MLVDS DC Conditions[1]***

**Over Recommended Operating Conditions**

| Symbol | Description | Nominal | | Units |
|---|---|---|---|---|
| | | Zo = 50 | Zo = 70 | |
| $Z_{OUT}$ | Output impedance | 50 | 50 | ohm |
| $R_{TLEFT}$ | Left end termination | 50 | 70 | ohm |
| $R_{TRIGHT}$ | Right end termination | 50 | 70 | ohm |
| $V_{OH}$ | Output high voltage | 1.50 | 1.575 | V |
| $V_{OL}$ | Output low voltage | 1.00 | 0.925 | V |
| $V_{OD}$ | Output differential voltage | 0.50 | 0.65 | V |
| $V_{CM}$ | Output common mode voltage | 1.25 | 1.25 | V |
| $I_{DC}$ | DC output current | 20.0 | 18.5 | mA |

1. For input buffer, see LVDS table.

# sysCLOCK PLL Timing

**Over Recommended Operating Conditions**

| Parameter | Description | Conditions | Min. | Typ | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Clock Frequency (CLKI, CLKFB) | | 2 | — | 1000 | MHz |
| $f_{OUT}$ | Output Clock Frequency (CLKOP, CLKOS) | | 1.5625 | — | 1000 | MHz |
| $f_{VCO}$ | PLL VCO Frequency | | 100 | — | 1000 | MHz |
| $f_{PFD}$ | Phase Detector Input Frequency | | 2 | — | 700 | MHz |
| **AC Characteristics** | | | | | | |
| $t_{DT}$ | Output Clock Duty Cycle | Default duty cycle selected (at 50% levels) | 45 | — | 55 | % |
| $t_{OPJIT}$[1] | Output Clock Period Jitter | 2 MHz ≤ $f_{PFD}$ ≤ 10 MHz | — | — | 200 | ps |
| | | $f_{PFD}$ > 10 MHz | — | — | 100 | ps |
| $t_{CPJIT}$[1] | Output Clock Cycle-to-Cycle Jitter | | — | — | 100 | ps |
| $t_{SKEW}$ | Output Clock-to-Clock Skew (Between Two Outputs with the Same Phase Setting) | | — | — | 20 | ps |
| $t_{LOCK}$ | PLL Lock-in Time | | — | — | 1 | ms |
| $t_{IPJIT}$ | Input Clock Period Jitter | | — | — | ±250 | ps |
| $t_{HI}$ | Input Clock High Time | At 80% level | 350 | — | — | ps |
| $t_{LO}$ | Input Clock Low Time | At 20% level | 350 | — | — | ps |
| $t_{RSWA}$ | Analog Reset Signal Pulse Width | | 100 | — | — | ns |
| $t_{RSWD}$ | Digital Reset Signal Pulse Width | | 3 | — | — | ns |
| $t_{DEL}$ | Timeshift Delay Step Size | | 40 | 80 | 120 | ps |
| $t_{RANGE}$ | Timeshift Delay Range | | — | +/- 560 | — | ps |
| $f_{SS}$ | Spread Spectrum Modulation Frequency | | 30 | — | 500 | KHz |
| % Spread | Percentage Downspread for SS Mode | | 0.5 | — | 1.5 | % |
| | VCO Clock Phase Adjustment Accuracy | | -5 | — | 5 | ° |

1. Values are measured with FPGA logic active, no additional I/Os toggling and REFCLK total jitter = 30 ps

## Pin Information Summary

| Pin Type | | 256 fpBGA | 900 fpBGA | | 1020 fcBGA | |
|---|---|---|---|---|---|---|
| | | LFSC/M15 | LFSC/M15 | LFSC/M25 | LFSC/M25 | LFSC/M40 |
| Single Ended User I/O | | 139 | 300 | 378 | 476 | 562 |
| Differential Pair User I/O | | 60 | 141 | 182 | 235 | 277 |
| LVDS Output Pairs | | 22 | 44 | 60 | 60 | 78 |
| Configuration | Dedicated | 9 | 11 | 11 | 11 | 11 |
| | Muxes/MPI sysBus | 0 | 55 | 55 | 55 | 72 |
| JTAG (excluding VCCJ) | | 4 | 4 | 4 | 4 | 4 |
| Dedicated Pins | | 2 | 4 | 4 | 4 | 4 |
| VCC | | 10 | 46 | 46 | 40 | 40 |
| VCC12 | | 10 | 35 | 35 | 36 | 36 |
| VCCAUX | | 10 | 36 | 36 | 32 | 32 |
| VCCIO | Bank 1 | 3 | 18 | 18 | 10 | 10 |
| | Bank 2 | 2 | 14 | 14 | 8 | 8 |
| | Bank 3 | 2 | 15 | 15 | 10 | 10 |
| | Bank 4 | 3 | 15 | 15 | 10 | 10 |
| | Bank 5 | 3 | 15 | 15 | 10 | 10 |
| | Bank 6 | 2 | 15 | 15 | 10 | 10 |
| | Bank 7 | 2 | 16 | 16 | 8 | 8 |
| VTT | Bank 2 | 0 | 2 | 2 | 2 | 2 |
| | Bank 3 | 0 | 3 | 3 | 3 | 3 |
| | Bank 4 | 0 | 3 | 3 | 3 | 3 |
| | Bank 5 | 0 | 3 | 3 | 3 | 3 |
| | Bank 6 | 0 | 3 | 3 | 3 | 3 |
| | Bank 7 | 0 | 2 | 2 | 2 | 2 |
| GND | | 26 | 177 | 177 | 134 | 134 |
| NC | | 0 | 102 | 24 | 92 | 6 |
| Single Ended User / Differential I/O per Bank | Bank 1 | 21/8 | 63/30 | 63/30 | 68/32 | 68/32 |
| | Bank 2 | 15/7 | 26/13 | 30/15 | 34/17 | 54/27 |
| | Bank 3 | 19/8 | 43/20 | 62/29 | 84/42 | 94/47 |
| | Bank 4 | 25/11 | 50/22 | 66/32 | 84/41 | 99/48 |
| | Bank 5 | 25/11 | 49/23 | 65/32 | 88/44 | 99/49 |
| | Bank 6 | 19/8 | 43/20 | 62/29 | 84/42 | 94/47 |
| | Bank 7 | 15/7 | 26/13 | 30/15 | 34/17 | 54/27 |
| LVDS Output Pairs Per Bank | Bank 2 | 5 | 7 | 9 | 9 | 15 |
| | Bank 3 | 6 | 15 | 21 | 21 | 24 |
| | Bank 6 | 6 | 15 | 21 | 21 | 24 |
| | Bank 7 | 5 | 7 | 9 | 9 | 15 |
| VCCJ | | 1 | 1 | 1 | 1 | 1 |
| SERDES (signal + power supply) | | 28 | 60 | 60 | 108 | 108 |
| Total | | 256 | 900 | 900 | 1020 | 1152 |

# LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

| Ball Number | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| N17 | GND | - | | GND | - | |
| N18 | GND | - | | GND | - | |
| N19 | GND | - | | GND | - | |
| N20 | GND | - | | GND | - | |
| P11 | GND | - | | GND | - | |
| P12 | GND | - | | GND | - | |
| P13 | GND | - | | GND | - | |
| P14 | GND | - | | GND | - | |
| P15 | GND | - | | GND | - | |
| P16 | GND | - | | GND | - | |
| P17 | GND | - | | GND | - | |
| P18 | GND | - | | GND | - | |
| P19 | GND | - | | GND | - | |
| P20 | GND | - | | GND | - | |
| R10 | GND | - | | GND | - | |
| R11 | GND | - | | GND | - | |
| R12 | GND | - | | GND | - | |
| R13 | GND | - | | GND | - | |
| R14 | GND | - | | GND | - | |
| R15 | GND | - | | GND | - | |
| R16 | GND | - | | GND | - | |
| R17 | GND | - | | GND | - | |
| R18 | GND | - | | GND | - | |
| R19 | GND | - | | GND | - | |
| R20 | GND | - | | GND | - | |
| R21 | GND | - | | GND | - | |
| T10 | GND | - | | GND | - | |
| T11 | GND | - | | GND | - | |
| T12 | GND | - | | GND | - | |
| T13 | GND | - | | GND | - | |
| T14 | GND | - | | GND | - | |
| T15 | GND | - | | GND | - | |
| T16 | GND | - | | GND | - | |
| T17 | GND | - | | GND | - | |
| T18 | GND | - | | GND | - | |
| T19 | GND | - | | GND | - | |
| T20 | GND | - | | GND | - | |
| T21 | GND | - | | GND | - | |
| U11 | GND | - | | GND | - | |
| U12 | GND | - | | GND | - | |
| U13 | GND | - | | GND | - | |
| U14 | GND | - | | GND | - | |
| U15 | GND | - | | GND | - | |
| U16 | GND | - | | GND | - | |
| U17 | GND | - | | GND | - | |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| Y24 | PL48C | 6 | | PL61C | 6 | |
| Y23 | PL48D | 6 | | PL61D | 6 | |
| AD29 | PL49A | 6 | | PL62A | 6 | |
| AD30 | PL49B | 6 | | PL62B | 6 | |
| AF28 | PL49C | 6 | | PL62C | 6 | |
| AE28 | PL49D | 6 | | PL62D | 6 | |
| AC28 | PL51A | 6 | | PL65A | 6 | |
| AD28 | PL51B | 6 | | PL65B | 6 | |
| AB26 | PL51C | 6 | | PL65C | 6 | |
| AC26 | PL51D | 6 | VREF2_6 | PL65D | 6 | VREF2_6 |
| AC32 | PL52A | 6 | | PL66A | 6 | |
| AD32 | PL52B | 6 | | PL66B | 6 | |
| AA24 | PL52C | 6 | | PL66C | 6 | |
| AA23 | PL52D | 6 | | PL66D | 6 | |
| AE30 | PL53A | 6 | | PL67A | 6 | |
| AE29 | PL53B | 6 | | PL67B | 6 | |
| AC25 | PL53C | 6 | | PL67C | 6 | |
| AB25 | PL53D | 6 | | PL67D | 6 | |
| AE31 | PL55A | 6 | | PL69A | 6 | |
| AE32 | PL55B | 6 | | PL69B | 6 | |
| AE26 | PL55C | 6 | LLC_DLLT_IN_E/LLC_DLLT_FB_F | PL69C | 6 | LLC_DLLT_IN_E/LLC_DLLT_FB_F |
| AE27 | PL55D | 6 | LLC_DLLC_IN_E/LLC_DLLC_FB_F | PL69D | 6 | LLC_DLLC_IN_E/LLC_DLLC_FB_F |
| AF32 | PL56A | 6 | | PL70A | 6 | |
| AF31 | PL56B | 6 | | PL70B | 6 | |
| AC24 | PL56C | 6 | | PL70C | 6 | |
| AD25 | PL56D | 6 | | PL70D | 6 | |
| AG32 | PL57A | 6 | LLC_DLLT_IN_F/LLC_DLLT_FB_E | PL71A | 6 | LLC_DLLT_IN_F/LLC_DLLT_FB_E |
| AG31 | PL57B | 6 | LLC_DLLC_IN_F/LLC_DLLC_FB_E | PL71B | 6 | LLC_DLLC_IN_F/LLC_DLLC_FB_E |
| AC23 | PL57C | 6 | LLC_PLLT_IN_B/LLC_PLLT_FB_A | PL71C | 6 | LLC_PLLT_IN_B/LLC_PLLT_FB_A |
| AD24 | PL57D | 6 | LLC_PLLC_IN_B/LLC_PLLC_FB_A | PL71D | 6 | LLC_PLLC_IN_B/LLC_PLLC_FB_A |
| AH32 | XRES | - | | XRES | - | |
| AH31 | TEMP | 6 | | TEMP | 6 | |
| AJ32 | PB3A | 5 | LLC_PLLT_IN_A/LLC_PLLT_FB_B | PB3A | 5 | LLC_PLLT_IN_A/LLC_PLLT_FB_B |
| AK32 | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B | PB3B | 5 | LLC_PLLC_IN_A/LLC_PLLC_FB_B |
| AF27 | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D | PB3C | 5 | LLC_DLLT_IN_C/LLC_DLLT_FB_D |
| AG28 | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D | PB3D | 5 | LLC_DLLC_IN_C/LLC_DLLC_FB_D |
| AK31 | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C | PB4A | 5 | LLC_DLLT_IN_D/LLC_DLLT_FB_C |
| AL31 | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C | PB4B | 5 | LLC_DLLC_IN_D/LLC_DLLC_FB_C |
| AE25 | PB4C | 5 | | PB4C | 5 | |
| AE24 | PB4D | 5 | | PB4D | 5 | |
| AK30 | PB5A | 5 | | PB5A | 5 | |
| AL30 | PB5B | 5 | | PB5B | 5 | |
| AD23 | PB5C | 5 | | PB5C | 5 | |
| AE23 | PB5D | 5 | VREF1_5 | PB5D | 5 | VREF1_5 |
| AK29 | PB7A | 5 | | PB7A | 5 | |
| AL29 | PB7B | 5 | | PB7B | 5 | |
| AF26 | PB7C | 5 | | PB7C | 5 | |
| AF25 | PB7D | 5 | | PB7D | 5 | |
| AJ28 | PB8A | 5 | | PB8A | 5 | |
| AK28 | PB8B | 5 | | PB8B | 5 | |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AH11 | PB47C | 4 | PCLKT4_6 | PB54C | 4 | PCLKT4_6 |
| AH10 | PB47D | 4 | PCLKC4_6 | PB54D | 4 | PCLKC4_6 |
| AK12 | PB49A | 4 | PCLKT4_0 | PB55A | 4 | PCLKT4_0 |
| AJ12 | PB49B | 4 | PCLKC4_0 | PB55B | 4 | PCLKC4_0 |
| AF14 | PB49C | 4 | VREF2_4 | PB55C | 4 | VREF2_4 |
| AE14 | PB49D | 4 | | PB55D | 4 | |
| AL11 | PB51A | 4 | PCLKT4_5 | PB57A | 4 | PCLKT4_5 |
| AL10 | PB51B | 4 | PCLKC4_5 | PB57B | 4 | PCLKC4_5 |
| AH9 | PB51C | 4 | | PB57C | 4 | |
| AH8 | PB51D | 4 | | PB57D | 4 | |
| AK11 | PB52A | 4 | PCLKT4_3 | PB58A | 4 | PCLKT4_3 |
| AJ11 | PB52B | 4 | PCLKC4_3 | PB58B | 4 | PCLKC4_3 |
| AH7 | PB52C | 4 | PCLKT4_4 | PB58C | 4 | PCLKT4_4 |
| AH6 | PB52D | 4 | PCLKC4_4 | PB58D | 4 | PCLKC4_4 |
| AK8 | PB53A | 4 | | PB67A | 4 | |
| AJ8 | PB53B | 4 | | PB67B | 4 | |
| AF11 | PB53C | 4 | | PB67C | 4 | |
| AD12 | PB55A | 4 | | PB69A | 4 | |
| AE12 | PB55B | 4 | | PB69B | 4 | |
| AM6 | PB56A | 4 | | PB70A | 4 | |
| AM5 | PB56B | 4 | | PB70B | 4 | |
| AC12 | PB56C | 4 | | PB70C | 4 | |
| AL6 | PB57A | 4 | | PB73A | 4 | |
| AL5 | PB57B | 4 | | PB73B | 4 | |
| AG7 | PB59A | 4 | | PB74A | 4 | |
| AG8 | PB59B | 4 | | PB74B | 4 | |
| AK6 | PB60A | 4 | | PB75A | 4 | |
| AJ6 | PB60B | 4 | | PB75B | 4 | |
| AF10 | PB60C | 4 | | PB75C | 4 | |
| AE11 | PB60D | 4 | | PB75D | 4 | |
| AM4 | PB61A | 4 | | PB77A | 4 | |
| AM3 | PB61B | 4 | | PB77B | 4 | |
| AH5 | PB63A | 4 | | PB78A | 4 | |
| AH4 | PB63B | 4 | | PB78B | 4 | |
| AK5 | PB64A | 4 | | PB79A | 4 | |
| AJ5 | PB64B | 4 | | PB79B | 4 | |
| AF8 | PB64C | 4 | | PB79C | 4 | |
| AF7 | PB64D | 4 | | PB79D | 4 | |
| AL4 | PB65A | 4 | | PB81A | 4 | |
| AL3 | PB65B | 4 | | PB81B | 4 | |
| AG5 | PB65C | 4 | | PB81C | 4 | |
| AF6 | PB65D | 4 | | PB81D | 4 | |
| AK3 | PB67A | 4 | | PB82A | 4 | |
| AJ3 | PB67B | 4 | | PB82B | 4 | |
| AE10 | PB67C | 4 | VREF1_4 | PB82C | 4 | VREF1_4 |
| AD10 | PB67D | 4 | | PB82D | 4 | |
| AL2 | PB68A | 4 | LRC_DLLT_IN_C/LRC_DLLT_FB_D | PB83A | 4 | LRC_DLLT_IN_C/LRC_DLLT_FB_D |
| AK2 | PB68B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D | PB83B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D |
| AE9 | PB68C | 4 | | PB83C | 4 | |
| AE8 | PB68D | 4 | | PB83D | 4 | |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AA21 | VCCAUX | - | | VCCAUX | - | |
| AA22 | VCCAUX | - | | VCCAUX | - | |
| AB11 | VCCAUX | - | | VCCAUX | - | |
| AB12 | VCCAUX | - | | VCCAUX | - | |
| AB15 | VCCAUX | - | | VCCAUX | - | |
| AB16 | VCCAUX | - | | VCCAUX | - | |
| AB17 | VCCAUX | - | | VCCAUX | - | |
| AB18 | VCCAUX | - | | VCCAUX | - | |
| AB21 | VCCAUX | - | | VCCAUX | - | |
| AB22 | VCCAUX | - | | VCCAUX | - | |
| L11 | VCCAUX | - | | VCCAUX | - | |
| L12 | VCCAUX | - | | VCCAUX | - | |
| L14 | VCCAUX | - | | VCCAUX | - | |
| L15 | VCCAUX | - | | VCCAUX | - | |
| L18 | VCCAUX | - | | VCCAUX | - | |
| L19 | VCCAUX | - | | VCCAUX | - | |
| L21 | VCCAUX | - | | VCCAUX | - | |
| L22 | VCCAUX | - | | VCCAUX | - | |
| M11 | VCCAUX | - | | VCCAUX | - | |
| M12 | VCCAUX | - | | VCCAUX | - | |
| M21 | VCCAUX | - | | VCCAUX | - | |
| M22 | VCCAUX | - | | VCCAUX | - | |
| P11 | VCCAUX | - | | VCCAUX | - | |
| P22 | VCCAUX | - | | VCCAUX | - | |
| R11 | VCCAUX | - | | VCCAUX | - | |
| R22 | VCCAUX | - | | VCCAUX | - | |
| V11 | VCCAUX | - | | VCCAUX | - | |
| V22 | VCCAUX | - | | VCCAUX | - | |
| W11 | VCCAUX | - | | VCCAUX | - | |
| W22 | VCCAUX | - | | VCCAUX | - | |
| N11 | VTT_2 | 2 | | VTT_2 | 2 | |
| R10 | VTT_2 | 2 | | VTT_2 | 2 | |
| T11 | VTT_3 | 3 | | VTT_3 | 3 | |
| U11 | VTT_3 | 3 | | VTT_3 | 3 | |
| Y11 | VTT_3 | 3 | | VTT_3 | 3 | |
| AB13 | VTT_4 | 4 | | VTT_4 | 4 | |
| AB14 | VTT_4 | 4 | | VTT_4 | 4 | |
| AC15 | VTT_4 | 4 | | VTT_4 | 4 | |
| AB19 | VTT_5 | 5 | | VTT_5 | 5 | |
| AB20 | VTT_5 | 5 | | VTT_5 | 5 | |
| AC18 | VTT_5 | 5 | | VTT_5 | 5 | |
| T22 | VTT_6 | 6 | | VTT_6 | 6 | |
| U22 | VTT_6 | 6 | | VTT_6 | 6 | |
| Y22 | VTT_6 | 6 | | VTT_6 | 6 | |
| N22 | VTT_7 | 7 | | VTT_7 | 7 | |
| R23 | VTT_7 | 7 | | VTT_7 | 7 | |
| M17 | VCC12 | - | | VCC12 | - | |
| M16 | VCC12 | - | | VCC12 | - | |
| T12 | VCC12 | - | | VCC12 | - | |
| T21 | VCC12 | - | | VCC12 | - | |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AD8 | PR65C | 3 | | PR89C | 3 | |
| AJ3 | PR65B | 3 | | PR89B | 3 | |
| AH3 | PR65A | 3 | | PR89A | 3 | |
| AD7 | PR62D | 3 | | PR86D | 3 | |
| AC7 | PR62C | 3 | | PR86C | 3 | |
| AJ2 | PR62B | 3 | | PR86B | 3 | |
| AH2 | PR62A | 3 | | PR86A | 3 | |
| AF6 | PR61D | 3 | | PR85D | 3 | |
| AF5 | PR61C | 3 | | PR85C | 3 | |
| AF4 | PR61B | 3 | | PR85B | 3 | |
| AE4 | PR61A | 3 | | PR85A | 3 | |
| AD6 | PR60D | 3 | | PR84D | 3 | |
| AC6 | PR60C | 3 | | PR84C | 3 | |
| AG2 | PR60B | 3 | | PR84B | 3 | |
| AF2 | PR60A | 3 | | PR84A | 3 | |
| AC8 | PR58D | 3 | | PR82D | 3 | |
| AB8 | PR58C | 3 | | PR82C | 3 | |
| AK1 | PR58B | 3 | | PR82B | 3 | |
| AJ1 | PR58A | 3 | | PR82A | 3 | |
| AB10 | PR57D | 3 | | PR81D | 3 | |
| AA10 | PR57C | 3 | | PR81C | 3 | |
| AF3 | PR57B | 3 | | PR81B | 3 | |
| AE3 | PR57A | 3 | | PR81A | 3 | |
| AE5 | PR56D | 3 | | PR80D | 3 | |
| AD5 | PR56C | 3 | | PR80C | 3 | |
| AE2 | PR56B | 3 | | PR80B | 3 | |
| AD2 | PR56A | 3 | | PR80A | 3 | |
| AC5 | PR53D | 3 | | PR78D | 3 | |
| AB5 | PR53C | 3 | | PR78C | 3 | |
| AF1 | PR53B | 3 | | PR78B | 3 | |
| AE1 | PR53A | 3 | | PR78A | 3 | |
| AA11 | PR52D | 3 | | PR77D | 3 | |
| Y11 | PR52C | 3 | | PR77C | 3 | |
| AC4 | PR52B | 3 | | PR77B | 3 | |
| AB4 | PR52A | 3 | | PR77A | 3 | |
| AA8 | PR51D | 3 | DIFFR_3 | PR76D | 3 | DIFFR_3 |
| AA9 | PR51C | 3 | | PR76C | 3 | |
| AC3 | PR51B | 3 | | PR76B | 3 | |
| AB3 | PR51A | 3 | | PR76A | 3 | |
| AA7 | PR49D | 3 | | PR65D | 3 | |
| Y7 | PR49C | 3 | | PR65C | 3 | |
| AA2 | PR49B | 3 | | PR65B | 3 | |
| Y2 | PR49A | 3 | | PR65A | 3 | |
| AA6 | PR48D | 3 | | PR63D | 3 | |
| Y6 | PR48C | 3 | | PR63C | 3 | |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| Y4 | PR48B | 3 | | PR63B | 3 | |
| W4 | PR48A | 3 | | PR63A | 3 | |
| W11 | PR47D | 3 | | PR60D | 3 | |
| V11 | PR47C | 3 | | PR60C | 3 | |
| W2 | PR47B | 3 | | PR60B | 3 | |
| V2 | PR47A | 3 | | PR60A | 3 | |
| W9 | PR45D | 3 | | PR57D | 3 | |
| V9 | PR45C | 3 | | PR57C | 3 | |
| V1 | PR45B | 3 | | PR57B | 3 | |
| U1 | PR45A | 3 | | PR57A | 3 | |
| W10 | PR44D | 3 | | PR56D | 3 | |
| V10 | PR44C | 3 | | PR56C | 3 | |
| U2 | PR44B | 3 | | PR56B | 3 | |
| T2 | PR44A | 3 | | PR56A | 3 | |
| Y8 | PR43D | 3 | | PR55D | 3 | |
| W8 | PR43C | 3 | VREF1_3 | PR55C | 3 | VREF1_3 |
| W5 | PR43B | 3 | | PR55B | 3 | |
| V5 | PR43A | 3 | | PR55A | 3 | |
| V7 | PR40D | 3 | PCLKC3_2 | PR52D | 3 | PCLKC3_2 |
| U7 | PR40C | 3 | PCLKT3_2 | PR52C | 3 | PCLKT3_2 |
| T1 | PR40B | 3 | | PR52B | 3 | |
| R1 | PR40A | 3 | | PR52A | 3 | |
| V8 | PR39D | 3 | PCLKC3_3 | PR51D | 3 | PCLKC3_3 |
| U8 | PR39C | 3 | PCLKT3_3 | PR51C | 3 | PCLKT3_3 |
| U5 | PR39B | 3 | | PR51B | 3 | |
| T5 | PR39A | 3 | | PR51A | 3 | |
| V6 | PR38D | 3 | PCLKC3_1 | PR50D | 3 | PCLKC3_1 |
| U6 | PR38C | 3 | PCLKT3_1 | PR50C | 3 | PCLKT3_1 |
| T4 | PR38B | 3 | PCLKC3_0 | PR50B | 3 | PCLKC3_0 |
| T3 | PR38A | 3 | PCLKT3_0 | PR50A | 3 | PCLKT3_0 |
| U9 | PR36D | 2 | PCLKC2_2 | PR48D | 2 | PCLKC2_2 |
| T9 | PR36C | 2 | PCLKT2_2 | PR48C | 2 | PCLKT2_2 |
| R2 | PR36B | 2 | PCLKC2_0 | PR48B | 2 | PCLKC2_0 |
| P2 | PR36A | 2 | PCLKT2_0 | PR48A | 2 | PCLKT2_0 |
| T11 | PR35D | 2 | PCLKC2_3 | PR47D | 2 | PCLKC2_3 |
| U11 | PR35C | 2 | PCLKT2_3 | PR47C | 2 | PCLKT2_3 |
| R4 | PR35B | 2 | PCLKC2_1 | PR47B | 2 | PCLKC2_1 |
| R3 | PR35A | 2 | PCLKT2_1 | PR47A | 2 | PCLKT2_1 |
| T8 | PR34D | 2 | | PR46D | 2 | |
| R8 | PR34C | 2 | | PR46C | 2 | |
| P1 | PR34B | 2 | | PR46B | 2 | |
| N1 | PR34A | 2 | | PR46A | 2 | |
| R6 | PR31D | 2 | | PR43D | 2 | |
| P6 | PR31C | 2 | | PR43C | 2 | |
| M1 | PR31B | 2 | | PR43B | 2 | |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| H21 | PT38D | 1 | D28/PCLKC1_6/MPI_DATA28 | PT57D | 1 | D28/PCLKC1_6/MPI_DATA28 |
| J21 | PT38C | 1 | D29/PCLKT1_6/MPI_DATA29 | PT57C | 1 | D29/PCLKT1_6/MPI_DATA29 |
| A19 | PT38B | 1 | A9/MPI_ADDR23 | PT57B | 1 | A9/MPI_ADDR23 |
| B19 | PT38A | 1 | A10/MPI_ADDR24 | PT57A | 1 | A10/MPI_ADDR24 |
| H22 | PT37D | 1 | D30/PCLKC1_7/MPI_DATA30 | PT56D | 1 | D30/PCLKC1_7/MPI_DATA30 |
| J22 | PT37C | 1 | D31/PCLKT1_7/MPI_DATA31 | PT56C | 1 | D31/PCLKT1_7/MPI_DATA31 |
| F20 | PT37B | 1 | A11/MPI_ADDR25 | PT56B | 1 | A11/MPI_ADDR25 |
| G20 | PT37A | 1 | A12/MPI_ADDR26 | PT56A | 1 | A12/MPI_ADDR26 |
| K21 | PT35D | 1 | D11/MPI_DATA11 | PT55D | 1 | D11/MPI_DATA11 |
| K22 | PT35C | 1 | D12/MPI_DATA12 | PT55C | 1 | D12/MPI_DATA12 |
| A20 | PT35B | 1 | A13/MPI_ADDR27 | PT55B | 1 | A13/MPI_ADDR27 |
| B20 | PT35A | 1 | A14/MPI_ADDR28 | PT55A | 1 | A14/MPI_ADDR28 |
| L21 | PT33D | 1 | A16/MPI_ADDR30 | PT53D | 1 | A16/MPI_ADDR30 |
| L20 | PT33C | 1 | D13/MPI_DATA13 | PT53C | 1 | D13/MPI_DATA13 |
| D20 | PT33B | 1 | A15/MPI_ADDR29 | PT53B | 1 | A15/MPI_ADDR29 |
| E20 | PT33A | 1 | A17/MPI_ADDR31 | PT53A | 1 | A17/MPI_ADDR31 |
| L19 | PT30D | 1 | A19/MPI_TSIZ1 | PT52D | 1 | A19/MPI_TSIZ1 |
| K19 | PT30C | 1 | A20/MPI_BDIP | PT52C | 1 | A20/MPI_BDIP |
| D21 | PT30B | 1 | A18/MPI_TSIZ0 | PT52B | 1 | A18/MPI_TSIZ0 |
| E21 | PT30A | 1 | MPI_TEA | PT52A | 1 | MPI_TEA |
| M20 | PT28D | 1 | D14/MPI_DATA14 | PT51D | 1 | D14/MPI_DATA14 |
| M19 | PT28C | 1 | DP1/MPI_PAR1 | PT51C | 1 | DP1/MPI_PAR1 |
| F21 | PT27B | 1 | A21/MPI_BURST | PT51B | 1 | A21/MPI_BURST |
| G21 | PT27A | 1 | D15/MPI_DATA15 | PT51A | 1 | D15/MPI_DATA15 |
| H24 | B_REFCLKP_L | - | | B_REFCLKP_L | - | |
| J24 | B_REFCLKN_L | - | | B_REFCLKN_L | - | |
| L22 | VCC12 | - | | VCC12 | - | |
| E26 | B_VDDIB3_L | - | | B_VDDIB3_L | - | |
| G22 | VCC12 | - | | VCC12 | - | |
| E22 | B_HDINP3_L | - | PCS 361 CH 3 IN P | B_HDINP3_L | - | PCS 361 CH 3 IN P |
| F22 | B_HDINN3_L | - | PCS 361 CH 3 IN N | B_HDINN3_L | - | PCS 361 CH 3 IN N |
| A21 | B_HDOUTP3_L | - | PCS 361 CH 3 OUT P | B_HDOUTP3_L | - | PCS 361 CH 3 OUT P |
| L24 | VCC12 | - | | VCC12 | - | |
| B21 | B_HDOUTN3_L | - | PCS 361 CH 3 OUT N | B_HDOUTN3_L | - | PCS 361 CH 3 OUT N |
| D22 | B_VDDOB3_L | - | | B_VDDOB3_L | - | |
| B22 | B_HDOUTN2_L | - | PCS 361 CH 2 OUT N | B_HDOUTN2_L | - | PCS 361 CH 2 OUT N |
| D23 | B_VDDOB2_L | - | | B_VDDOB2_L | - | |
| A22 | B_HDOUTP2_L | - | PCS 361 CH 2 OUT P | B_HDOUTP2_L | - | PCS 361 CH 2 OUT P |
| K24 | VCC12 | - | | VCC12 | - | |
| F23 | B_HDINN2_L | - | PCS 361 CH 2 IN N | B_HDINN2_L | - | PCS 361 CH 2 IN N |
| E23 | B_HDINP2_L | - | PCS 361 CH 2 IN P | B_HDINP2_L | - | PCS 361 CH 2 IN P |
| D26 | B_VDDIB2_L | - | | B_VDDIB2_L | - | |
| G23 | VCC12 | - | | VCC12 | - | |
| D27 | B_VDDIB1_L | - | | B_VDDIB1_L | - | |
| G24 | VCC12 | - | | VCC12 | - | |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| K20 | GND | - | | GND | - | |
| K23 | GND | - | | GND | - | |
| K26 | GND | - | | GND | - | |
| K28 | GND | - | | GND | - | |
| K6 | GND | - | | GND | - | |
| K9 | GND | - | | GND | - | |
| L12 | GND | - | | GND | - | |
| L32 | GND | - | | GND | - | |
| L4 | GND | - | | GND | - | |
| M10 | GND | - | | GND | - | |
| M17 | GND | - | | GND | - | |
| M24 | GND | - | | GND | - | |
| N29 | GND | - | | GND | - | |
| N7 | GND | - | | GND | - | |
| P15 | GND | - | | GND | - | |
| P20 | GND | - | | GND | - | |
| P3 | GND | - | | GND | - | |
| P31 | GND | - | | GND | - | |
| R10 | GND | - | | GND | - | |
| R14 | GND | - | | GND | - | |
| R16 | GND | - | | GND | - | |
| R19 | GND | - | | GND | - | |
| R21 | GND | - | | GND | - | |
| R26 | GND | - | | GND | - | |
| T15 | GND | - | | GND | - | |
| T17 | GND | - | | GND | - | |
| T18 | GND | - | | GND | - | |
| T20 | GND | - | | GND | - | |
| T28 | GND | - | | GND | - | |
| T6 | GND | - | | GND | - | |
| U16 | GND | - | | GND | - | |
| U19 | GND | - | | GND | - | |
| U23 | GND | - | | GND | - | |
| U32 | GND | - | | GND | - | |
| U4 | GND | - | | GND | - | |
| V12 | GND | - | | GND | - | |
| V16 | GND | - | | GND | - | |
| V19 | GND | - | | GND | - | |
| V3 | GND | - | | GND | - | |
| V31 | GND | - | | GND | - | |
| W15 | GND | - | | GND | - | |
| W17 | GND | - | | GND | - | |
| W18 | GND | - | | GND | - | |
| W20 | GND | - | | GND | - | |
| W29 | GND | - | | GND | - | |

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| G27 | A_REFCLKP_L | - | |
| H27 | A_REFCLKN_L | - | |
| H25 | VCC12 | - | |
| H26 | RESP_ULC | - | |
| B33 | RESETN | 1 | |
| C34 | TSALLN | 1 | |
| D34 | DONE | 1 | |
| C33 | INITN | 1 | |
| J27 | M0 | 1 | |
| K27 | M1 | 1 | |
| M26 | M2 | 1 | |
| L26 | M3 | 1 | |
| F30 | PL15A | 7 | ULC_PLLT_IN_A/ULC_PLLT_FB_B |
| G30 | PL15B | 7 | ULC_PLLC_IN_A/ULC_PLLC_FB_B |
| H28 | PL15C | 7 | |
| J28 | PL15D | 7 | |
| F31 | PL17A | 7 | ULC_DLLT_IN_C/ULC_DLLT_FB_D |
| G31 | PL17B | 7 | ULC_DLLC_IN_C/ULC_DLLC_FB_D |
| N25 | PL17C | 7 | ULC_PLLT_IN_B/ULC_PLLT_FB_A |
| P25 | PL17D | 7 | ULC_PLLC_IN_B/ULC_PLLC_FB_A |
| D33 | PL18A | 7 | ULC_DLLT_IN_D/ULC_DLLT_FB_C |
| E33 | PL18B | 7 | ULC_DLLC_IN_D/ULC_DLLC_FB_C |
| H29 | PL18C | 7 | |
| J29 | PL18D | 7 | VREF2_7 |
| F32 | PL19A | 7 | |
| G32 | PL19B | 7 | |
| P26 | PL19C | 7 | |
| N26 | PL19D | 7 | |
| H30 | PL26A | 7 | |
| J30 | PL26B | 7 | |
| L28 | PL26C | 7 | |
| M28 | PL26D | 7 | |
| J31 | PL43A | 7 | |
| K31 | PL43B | 7 | |
| L27 | PL43C | 7 | VREF1_7 |
| M27 | PL43D | 7 | DIFFR_7 |
| J32 | PL45A | 7 | |
| K32 | PL45B | 7 | |
| L29 | PL45C | 7 | |
| M29 | PL45D | 7 | |
| H33 | PL47A | 7 | |
| J33 | PL47B | 7 | |

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| AD5 | PR94C | 3 | |
| AE2 | PR94B | 3 | |
| AD2 | PR94A | 3 | |
| AC5 | PR92D | 3 | |
| AB5 | PR92C | 3 | |
| AF1 | PR92B | 3 | |
| AE1 | PR92A | 3 | |
| AA11 | PR91D | 3 | |
| Y11 | PR91C | 3 | |
| AC4 | PR91B | 3 | |
| AB4 | PR91A | 3 | |
| AA8 | PR90D | 3 | DIFFR_3 |
| AA9 | PR90C | 3 | |
| AC3 | PR90B | 3 | |
| AB3 | PR90A | 3 | |
| AA7 | PR79D | 3 | |
| Y7 | PR79C | 3 | |
| AA2 | PR79B | 3 | |
| Y2 | PR79A | 3 | |
| AA6 | PR77D | 3 | |
| Y6 | PR77C | 3 | |
| Y4 | PR77B | 3 | |
| W4 | PR77A | 3 | |
| W11 | PR74D | 3 | |
| V11 | PR74C | 3 | |
| W2 | PR74B | 3 | |
| V2 | PR74A | 3 | |
| W9 | PR71D | 3 | |
| V9 | PR71C | 3 | |
| V1 | PR71B | 3 | |
| U1 | PR71A | 3 | |
| W10 | PR70D | 3 | |
| V10 | PR70C | 3 | |
| U2 | PR70B | 3 | |
| T2 | PR70A | 3 | |
| Y8 | PR69D | 3 | |
| W8 | PR69C | 3 | VREF1_3 |
| W5 | PR69B | 3 | |
| V5 | PR69A | 3 | |
| V7 | PR66D | 3 | PCLKC3_2 |
| U7 | PR66C | 3 | PCLKT3_2 |
| T1 | PR66B | 3 | |
| R1 | PR66A | 3 | |

## LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| Ball Number | LFSC/M115 | | |
|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function |
| Y18 | VCC | - | |
| Y20 | VCC | - | |
| AB15 | VCC12 | - | |
| AB20 | VCC12 | - | |
| N15 | VCC12 | - | |
| N20 | VCC12 | - | |
| R13 | VCC12 | - | |
| R22 | VCC12 | - | |
| Y13 | VCC12 | - | |
| Y22 | VCC12 | - | |
| AA12 | VCCAUX | - | |
| AA23 | VCCAUX | - | |
| AB12 | VCCAUX | - | |
| AB16 | VCCAUX | - | |
| AB17 | VCCAUX | - | |
| AB18 | VCCAUX | - | |
| AB19 | VCCAUX | - | |
| AB23 | VCCAUX | - | |
| AC12 | VCCAUX | - | |
| AC13 | VCCAUX | - | |
| Y19 | GND | - | |
| AC14 | VCCAUX | - | |
| AC17 | VCCAUX | - | |
| AC21 | VCCAUX | - | |
| AC22 | VCCAUX | - | |
| AC23 | VCCAUX | - | |
| M13 | VCCAUX | - | |
| M14 | VCCAUX | - | |
| M18 | VCCAUX | - | |
| M21 | VCCAUX | - | |
| M22 | VCCAUX | - | |
| N12 | VCCAUX | - | |
| N16 | VCCAUX | - | |
| N17 | VCCAUX | - | |
| N18 | VCCAUX | - | |
| N19 | VCCAUX | - | |
| N23 | VCCAUX | - | |
| P12 | VCCAUX | - | |
| P23 | VCCAUX | - | |
| T13 | VCCAUX | - | |
| T22 | VCCAUX | - | |
| U12 | VCCAUX | - | |
| U13 | VCCAUX | - | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AP26 | PB41C | 5 | | PB43C | 5 | |
| AN26 | PB41D | 5 | | PB43D | 5 | |
| AY30 | PB43A | 5 | | PB45A | 5 | |
| AY29 | PB43B | 5 | | PB45B | 5 | |
| AU30 | PB43C | 5 | | PB45C | 5 | |
| AU31 | PB43D | 5 | | PB45D | 5 | |
| AV27 | PB44A | 5 | | PB46A | 5 | |
| AV26 | PB44B | 5 | | PB46B | 5 | |
| AT28 | PB44C | 5 | | PB46C | 5 | |
| AT27 | PB44D | 5 | | PB46D | 5 | |
| BA29 | PB45A | 5 | | PB47A | 5 | |
| BA28 | PB45B | 5 | | PB47B | 5 | |
| AL25 | PB45C | 5 | | PB47C | 5 | |
| AM25 | PB45D | 5 | | PB47D | 5 | |
| BB29 | PB47A | 5 | | PB49A | 5 | |
| BB28 | PB47B | 5 | | PB49B | 5 | |
| AN25 | PB47C | 5 | | PB49C | 5 | |
| AP25 | PB47D | 5 | | PB49D | 5 | |
| AY27 | PB48A | 5 | PCLKT5_3 | PB50A | 5 | PCLKT5_3 |
| AY26 | PB48B | 5 | PCLKC5_3 | PB50B | 5 | PCLKC5_3 |
| AT25 | PB48C | 5 | PCLKT5_4 | PB50C | 5 | PCLKT5_4 |
| AT24 | PB48D | 5 | PCLKC5_4 | PB50D | 5 | PCLKC5_4 |
| AW27 | PB49A | 5 | PCLKT5_5 | PB51A | 5 | PCLKT5_5 |
| AW26 | PB49B | 5 | PCLKC5_5 | PB51B | 5 | PCLKC5_5 |
| AU29 | PB49C | 5 | | PB51C | 5 | |
| AU28 | PB49D | 5 | | PB51D | 5 | |
| BB27 | PB51A | 5 | PCLKT5_0 | PB53A | 5 | PCLKT5_0 |
| BB26 | PB51B | 5 | PCLKC5_0 | PB53B | 5 | PCLKC5_0 |
| AR25 | PB51C | 5 | | PB53C | 5 | |
| AR24 | PB51D | 5 | VREF2_5 | PB53D | 5 | VREF2_5 |
| BA27 | PB52A | 5 | PCLKT5_1 | PB54A | 5 | PCLKT5_1 |
| BA26 | PB52B | 5 | PCLKC5_1 | PB54B | 5 | PCLKC5_1 |
| AP24 | PB52C | 5 | PCLKT5_6 | PB54C | 5 | PCLKT5_6 |
| AN24 | PB52D | 5 | PCLKC5_6 | PB54D | 5 | PCLKC5_6 |
| AV25 | PB53A | 5 | PCLKT5_2 | PB55A | 5 | PCLKT5_2 |
| AV24 | PB53B | 5 | PCLKC5_2 | PB55B | 5 | PCLKC5_2 |
| AU27 | PB53C | 5 | PCLKT5_7 | PB55C | 5 | PCLKT5_7 |
| AU26 | PB53D | 5 | PCLKC5_7 | PB55D | 5 | PCLKC5_7 |
| BA25 | PB55A | 5 | | PB57A | 5 | |
| BA24 | PB55B | 5 | | PB57B | 5 | |
| AU24 | PB55C | 5 | | PB57C | 5 | |
| AU25 | PB55D | 5 | | PB57D | 5 | |
| BB24 | PB56A | 5 | | PB58A | 5 | |
| BB25 | PB56B | 5 | | PB58B | 5 | |
| AM23 | PB56C | 5 | | PB58C | 5 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| K14 | VCC12 | - | | VCC12 | - | |
| H11 | B_VDDIB2_R | - | | B_VDDIB2_R | - | |
| D8 | B_HDINP2_R | - | PCS 3E1 CH 2 IN P | B_HDINP2_R | - | PCS 3E1 CH 2 IN P |
| E8 | B_HDINN2_R | - | PCS 3E1 CH 2 IN N | B_HDINN2_R | - | PCS 3E1 CH 2 IN N |
| G5 | VCC12 | - | | VCC12 | - | |
| B9 | B_HDOUTP2_R | - | PCS 3E1 CH 2 OUT P | B_HDOUTP2_R | - | PCS 3E1 CH 2 OUT P |
| L12 | B_VDDOB2_R | - | | B_VDDOB2_R | - | |
| A9 | B_HDOUTN2_R | - | PCS 3E1 CH 2 OUT N | B_HDOUTN2_R | - | PCS 3E1 CH 2 OUT N |
| C5 | B_VDDOB3_R | - | | B_VDDOB3_R | - | |
| A10 | B_HDOUTN3_R | - | PCS 3E1 CH 3 OUT N | B_HDOUTN3_R | - | PCS 3E1 CH 3 OUT N |
| H5 | VCC12 | - | | VCC12 | - | |
| B10 | B_HDOUTP3_R | - | PCS 3E1 CH 3 OUT P | B_HDOUTP3_R | - | PCS 3E1 CH 3 OUT P |
| E9 | B_HDINN3_R | - | PCS 3E1 CH 3 IN N | B_HDINN3_R | - | PCS 3E1 CH 3 IN N |
| D9 | B_HDINP3_R | - | PCS 3E1 CH 3 IN P | B_HDINP3_R | - | PCS 3E1 CH 3 IN P |
| J13 | VCC12 | - | | VCC12 | - | |
| H12 | B_VDDIB3_R | - | | B_VDDIB3_R | - | |
| J12 | VCC12 | - | | VCC12 | - | |
| M14 | B_REFCLKN_R | - | | B_REFCLKN_R | - | |
| L14 | B_REFCLKP_R | - | | B_REFCLKP_R | - | |
| J14 | VCC12 | - | | VCC12 | - | |
| G12 | C_VDDIB0_R | - | | C_VDDIB0_R | - | |
| D10 | C_HDINP0_R | - | PCS 3E2 CH 0 IN P | C_HDINP0_R | - | PCS 3E2 CH 0 IN P |
| E10 | C_HDINN0_R | - | PCS 3E2 CH 0 IN N | C_HDINN0_R | - | PCS 3E2 CH 0 IN N |
| H6 | VCC12 | - | | VCC12 | - | |
| B11 | C_HDOUTP0_R | - | PCS 3E2 CH 0 OUT P | C_HDOUTP0_R | - | PCS 3E2 CH 0 OUT P |
| M12 | C_VDDOB0_R | - | | C_VDDOB0_R | - | |
| A11 | C_HDOUTN0_R | - | PCS 3E2 CH 0 OUT N | C_HDOUTN0_R | - | PCS 3E2 CH 0 OUT N |
| L11 | C_VDDOB1_R | - | | C_VDDOB1_R | - | |
| A12 | C_HDOUTN1_R | - | PCS 3E2 CH 1 OUT N | C_HDOUTN1_R | - | PCS 3E2 CH 1 OUT N |
| K11 | VCC12 | - | | VCC12 | - | |
| B12 | C_HDOUTP1_R | - | PCS 3E2 CH 1 OUT P | C_HDOUTP1_R | - | PCS 3E2 CH 1 OUT P |
| E11 | C_HDINN1_R | - | PCS 3E2 CH 1 IN N | C_HDINN1_R | - | PCS 3E2 CH 1 IN N |
| D11 | C_HDINP1_R | - | PCS 3E2 CH 1 IN P | C_HDINP1_R | - | PCS 3E2 CH 1 IN P |
| H13 | VCC12 | - | | VCC12 | - | |
| C6 | C_VDDIB1_R | - | | C_VDDIB1_R | - | |
| H15 | VCC12 | - | | VCC12 | - | |
| G13 | C_VDDIB2_R | - | | C_VDDIB2_R | - | |
| D12 | C_HDINP2_R | - | PCS 3E2 CH 2 IN P | C_HDINP2_R | - | PCS 3E2 CH 2 IN P |
| E12 | C_HDINN2_R | - | PCS 3E2 CH 2 IN N | C_HDINN2_R | - | PCS 3E2 CH 2 IN N |
| J9 | VCC12 | - | | VCC12 | - | |
| B13 | C_HDOUTP2_R | - | PCS 3E2 CH 2 OUT P | C_HDOUTP2_R | - | PCS 3E2 CH 2 OUT P |
| K10 | C_VDDOB2_R | - | | C_VDDOB2_R | - | |
| A13 | C_HDOUTN2_R | - | PCS 3E2 CH 2 OUT N | C_HDOUTN2_R | - | PCS 3E2 CH 2 OUT N |
| J10 | C_VDDOB3_R | - | | C_VDDOB3_R | - | |
| A14 | C_HDOUTN3_R | - | PCS 3E2 CH 3 OUT N | C_HDOUTN3_R | - | PCS 3E2 CH 3 OUT N |