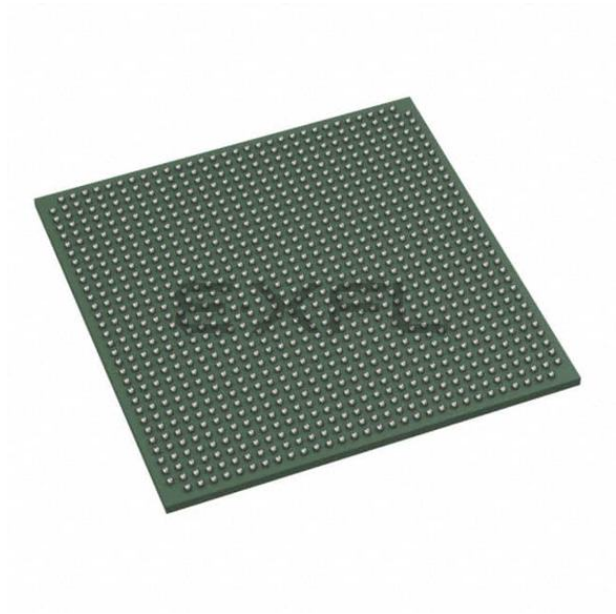
Lattice Semiconductor Corporation - LFSCM3GA25EP1-5FFN1020C Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6250
Number of Logic Elements/Cells	25000
Total RAM Bits	1966080
Number of I/O	476
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-OFCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga25ep1-5ffn1020c

Figure 2-13. DLL to PLL

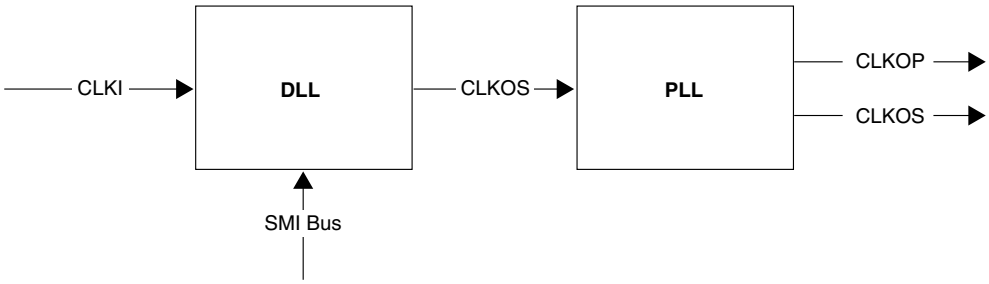


Figure 2-14 shows a shift of only CLKOP out in time.

Figure 2-14. PLL to DLL

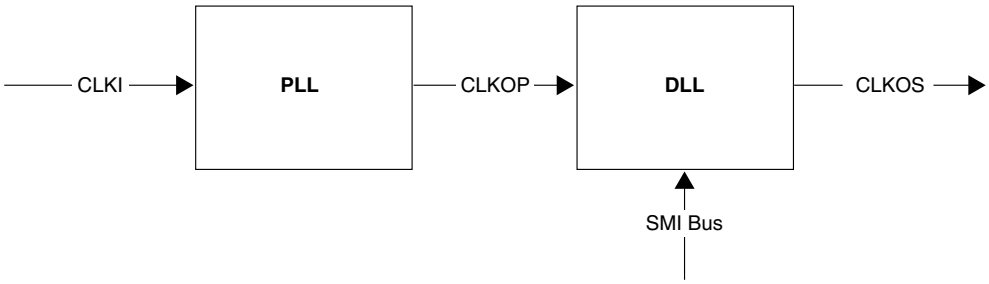
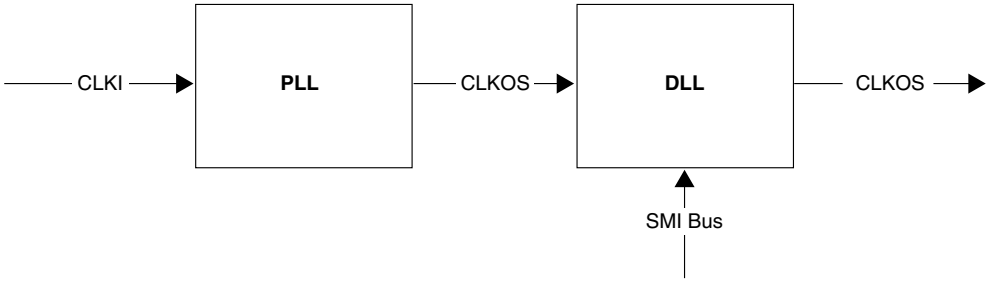


Figure 2-15 shows a shift of only CLKOS out in time.

Figure 2-15. PLL to DLL

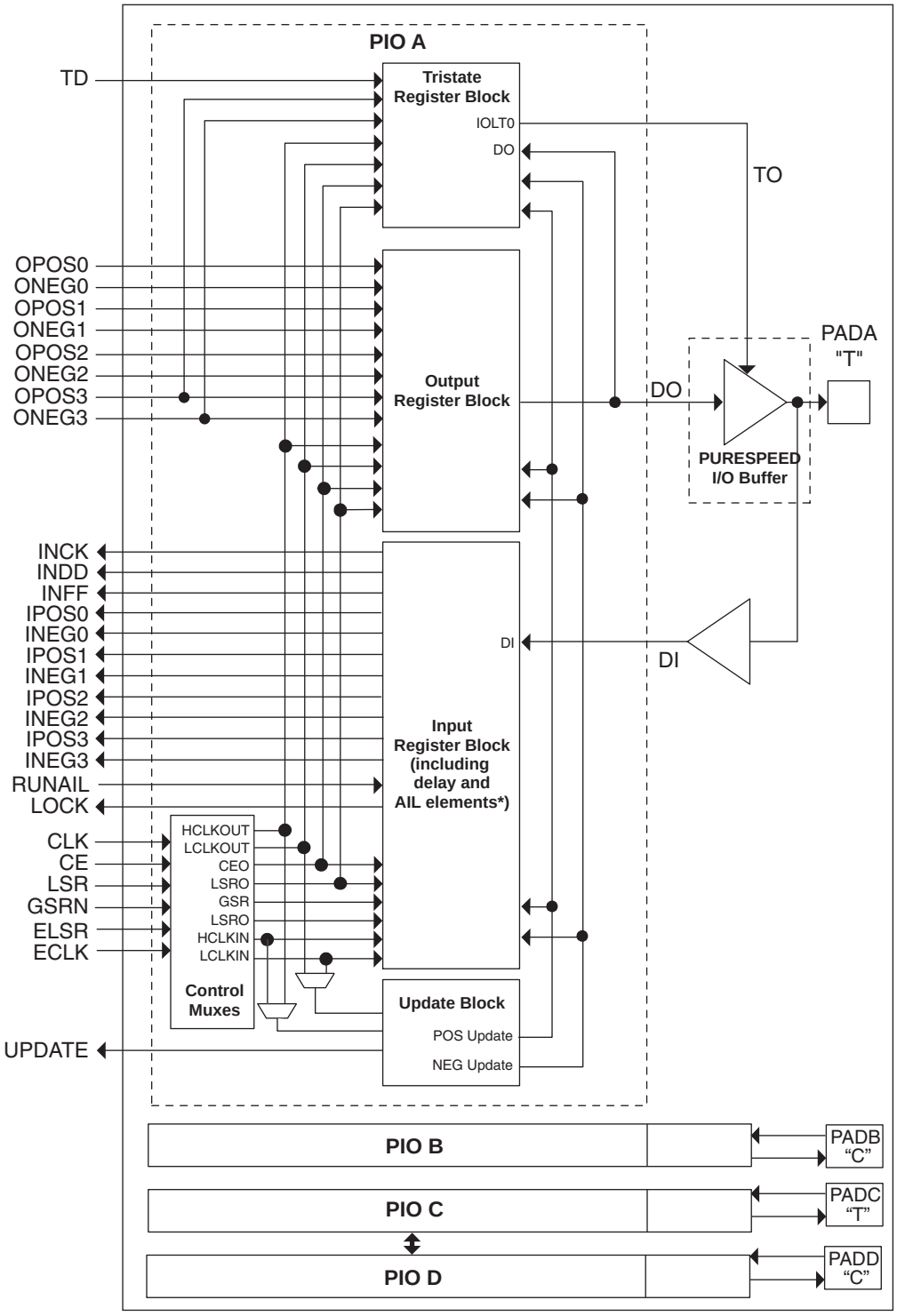


For further information on the DLL, please see details of additional technical documentation at the end of this data sheet.

sysMEM Memory Block

The sysMEM block can implement single port, true dual port, pseudo dual port or FIFO memories. Dedicated FIFO support logic allows the LatticeSC devices to efficiently implement FIFOs without consuming LUTs or routing resources for flag generation. Each block can be used in a variety of depths and widths as shown in Table 2-5. Memory with ranges from x1 to x18 in all modes: single port, pseudo-dual port and FIFO also providing x36.

Figure 2-17. PIC Diagram



*AIL only on A or C pads located on the left, right and bottom of the device.

The A/B PIOs on the left and the right of the device can be paired to form a differentiated driver. The A/B and C/D PIOs on all sides of the device can be paired to form differential receivers. Either A or C PIOs on all sides except the one on top also provide a connection to an adaptive input logic capability that facilitates the implementation of

Figure 2-26. LatticeSC Banks

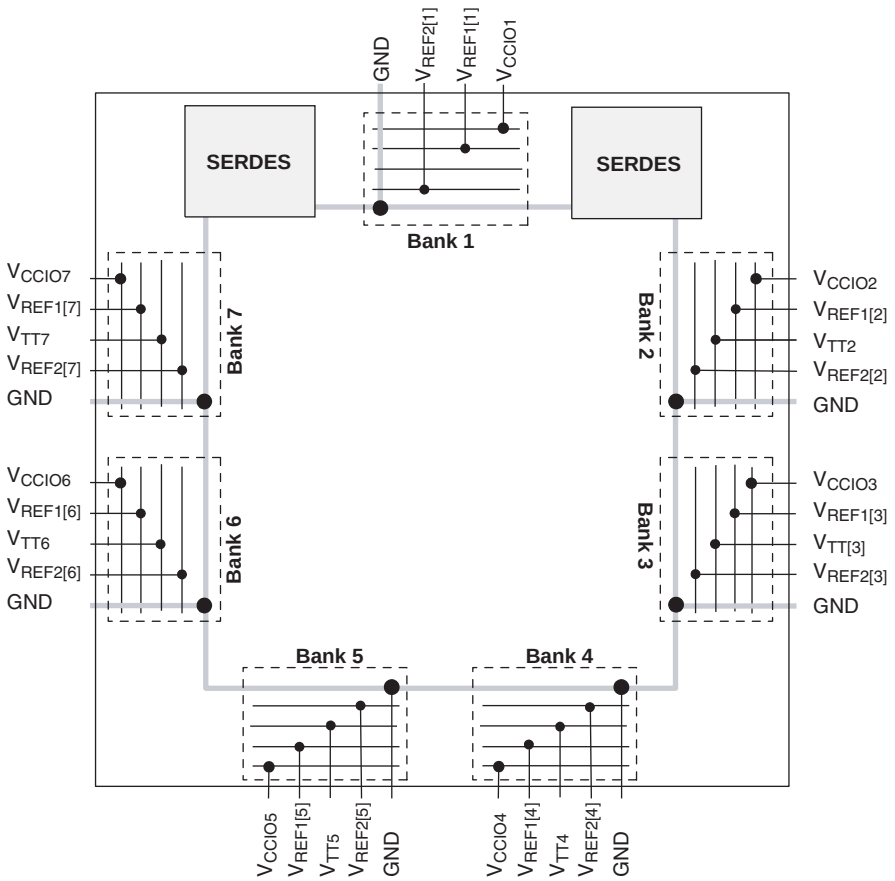


Table 2-7. Maximum Number of I/Os Per Bank in LatticeSC Family

Device	LFSC/M15	LFSC/M25	LFSC/M40	LFSC/M80	LFSC/M115
Bank1	104	80	136	80	136
Bank2	28	36	60	96	136
Bank3	60	84	96	132	156
Bank4	72	100	124	184	208
Bank5	72	100	124	184	208
Bank6	60	84	96	132	156
Bank7	28	36	60	96	136

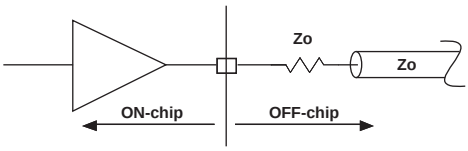
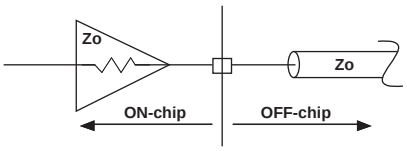
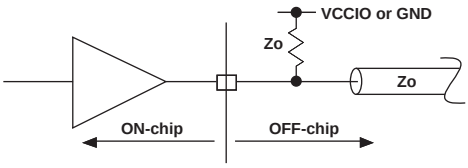
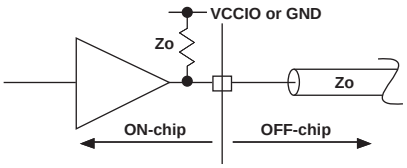
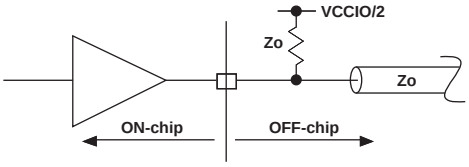
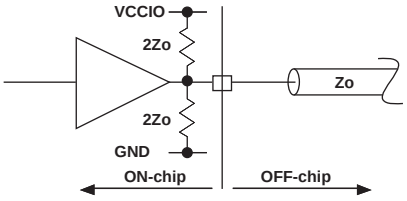
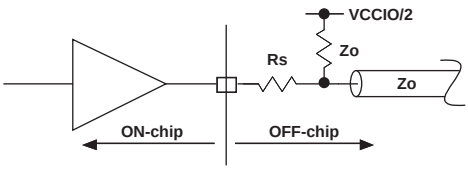
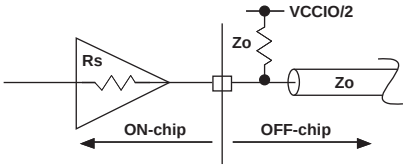
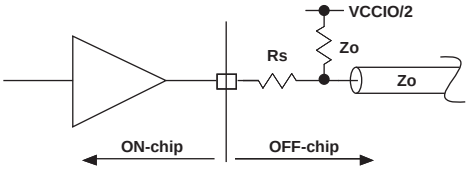
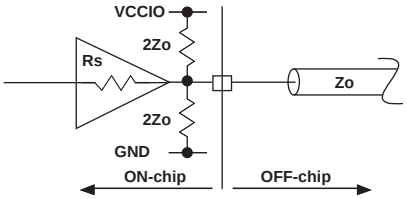
Note: Not all the I/Os of the Banks are available in all the packages

The LatticeSC devices contain three types of PURESPEED I/O buffers:

1. **Left and Right Sides (Banks 2, 3, 6 and 7)**
   These buffers can support LVCMOS standards up to 2.5V. A differential output driver (for LVDS and RSDS) is provided on all primary PIO pairs (A and B) and differential receivers are available on all pairs. Complimentary drivers are available. Adaptive input logic is available on PIOs A or C.

2. **Top Side (Bank 1)**
   These buffers can support LVCMOS standards up to 3.3V, including PCI33, PCI-X33 and SSTL-33. Differential receivers are provided on all PIO pairs but differential drivers for LVDS and RSDS are not available. Adaptive input logic is not available on this side. Complimentary output drivers are available.

Figure 2-27. Output Termination Schemes

Termination Type	Discrete Off-Chip Solution	Lattice On-Chip Solution
Series termination (controlled output impedance)		
Parallel termination to V_{CCIO}, or parallel driving end		
Parallel termination to $V_{CCIO}/2$ driving end		
Combined series + parallel termination to $V_{CCIO}/2$ at driving end (only series termination moved on-chip)		
Combined series + parallel to $V_{CCIO}/2$ driving end		

Density Shifting

The LatticeSC family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

LatticeSC/M Family Data Sheet DC and Switching Characteristics

December 2011 **Data Sheet DS1004**

Absolute Maximum Ratings

Supply Voltage V_{CC}, V_{CC12}, V_{DDIB}, V_{DDOB} . . . . . -0.5 to 1.6V

Supply Voltage V_{CCAUX}, V_{DDAX25}, V_{TT} . . . . . -0.5 to 2.75V

Supply Voltage V_{CCJ} . . . . . -0.5 to 3.6V

Supply Voltage V_{CCIO} (Banks 1, 4, 5) . . . . . -0.5 to 3.6V

Supply Voltage V_{CCIO} (Banks 2, 3, 6, 7) . . . . . -0.5 to 2.75V

Input or I/O Tristate Voltage Applied (Banks 1, 4, 5) . . . . . -0.5 to 3.6V

Input or I/O Tristate Voltage Applied (Banks 2, 3, 6, 7) . . . . . -0.5 to 2.75V

Storage Temperature (Ambient) . . . . . -65 to 150°C

Junction Temperature Under Bias (Tj) . . . . . +125°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Undershoot and overshoot of -2V to (VIHMAX +2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}[5]	Core Supply Voltage (Nominal 1.2V Operation)	0.95	1.26	V
V_{CCAUX}[6]	Programmable I/O Auxiliary Supply Voltage	2.375	2.625	V
V_{CCIO}[1, 2, 5, 6]	Programmable I/O Driver Supply Voltage (Banks 1, 4, 5)	1.14	3.45	V
V_{CCIO}[1, 2, 5, 6]	Programmable I/O Driver Supply Voltage (Banks 2, 3, 6, 7)	1.14	2.625	V
V_{CC12}[4, 5]	Internal 1.2V Power Supply Voltage for Configuration Logic and FPGA PLL, SERDES PLL Power Supply Voltage and SERDES Analog Supply Voltage	1.14	1.26	V
V_{DDIB}	SERDES Input Buffer Supply Voltage	1.14	1.575	V
V_{DDOB}	SERDES Output Buffer Supply Voltage	1.14	1.575	V
V_{DDAX25}	SERDES Termination Auxiliary Supply Voltage	2.375	2.625	V
V_{CCJ}[1, 5]	Supply Voltage for IEEE 1149.1 Test Access Port	1.71	3.45	V
V_{TT}[2, 3]	Programmable I/O Termination Power Supply	0.5	V_{CCAUX} - 0.5	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	+85	C
t_{JIND}	Junction Temperature, Industrial Operation	-40	105	C

1. If V_{CCIO} or V_{CCJ} is set to 2.5V, they must be connected to the same power supply as V_{CCAUX}.
2. See recommended voltages by I/O standard in subsequent table.
3. When V_{TT} termination is not required, or used to provide the common mode termination voltage (V_{CMT}), these pins can be left unconnected on the device.
4. V_{CC12} cannot be lower than V_{CC} at any time. For 1.2V operation, it is recommended that the V_{CC} and V_{CC12} supplies be tied together with proper noise decoupling between the digital VCC and analog VCC12 supplies.
5. V_{CC}, V_{CCIO} (all banks), V_{CC12} and V_{CCJ} must reach their minimum values before configuration will proceed.
6. If V_{CCIO} for a bank is nominally 1.2V/1.5V/1.8V, then V_{CCAUX} must always be higher than V_{CCIO} during power up.

Initialization and Standby Supply Current

The table below indicates initialization and standby supply current while operating at 85°C junction temperature (T_J), which is the high end of the commercial temperature range, and 105°C, which is the high end of the industrial temperature range. This data assumes all outputs are tri-stated and all inputs are configured as LVCMOS and held at V_{CCIO} or GND. The remaining SERDES supply current for V_{DDIB} and V_{DDOB} is detailed in the SERDES section of this data sheet. For power at your design temperature, it is recommended to use the Power Calculator tool which is accessible in ispLEVER or can be used as a standalone tool. For more information on supply current, see the reference to additional technical documentation available at the end of this data sheet.

Over Recommended Operating Conditions

Symbol	Condition	Parameter	Device	25°C Typ.[1]	85°C Max.[2]		105°C Max.[2]	Units
				All	-5, -6	-7	-5, -6	
I_{CC}	(VCC = 1.2V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	65	449	678	755	mA
			LFSC/M25	113	798	1255	1343	mA
			LFSC/M40	159	1178	2006	1981	mA
			LFSC/M80	276	2122	3827	3569	mA
			LFSC/M115	454	3376	—	5679	mA
	(VCC = 1.0V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	45	312	471	524	mA
			LFSC/M25	79	554	872	933	mA
			LFSC/M40	110	818	1393	1375	mA
			LFSC/M80	191	1473	2658	2478	mA
			LFSC/M115	315	2344	—	3943	mA
I_{CC12}		1.2V Power Supply Current for Configuration Logic, FPGA PLL, SERDES PLL and SERDES Analog Supplies	LFSC/M15	23	39	59	35	mA
			LFSC/M25	25	50	78	56	mA
			LFSC/M40	31	78	133	89	mA
			LFSC/M80	50	108	195	123	mA
			LFSC/M115	65	131	—	154	mA
I_{CCAUX}		Auxiliary Operating Power Supply Current	LFSC/M15	7	12	19	14	mA
			LFSC/M25	9	16	25	18	mA
			LFSC/M40	12	23	39	25	mA
			LFSC/M80	13	25	45	23	mA
			LFSC/M115	16	27	—	26	mA
I_{CCIO} and I_{CCJ}		Bank Power Supply Current (per bank)	LFSC/M15	0.1	0.2	0.3	0.2	mA
			LFSC/M25	0.3	0.6	1.0	0.7	mA
			LFSC/M40	0.4	0.9	1.5	1.0	mA
			LFSC/M80	0.5	1.1	2.1	1.3	mA
			LFSC/M115	0.7	1.5	—	1.8	mA

1. I_{CC} is specified at T_J = 25°C and typical V_{CC}.
2. I_{CC} is specified at the respective commercial and industrial maximum T_J and V_{CC} limits.

RSDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
V_{OD}	Output voltage, differential, R_T = 100 ohms	100	200	600	mV
V_{OS}	Output voltage, common mode	0.5	1.2	1.5	V
I_{RSDS}	Differential driver output current	1	2	6	mA
V_{THD}	Input voltage differential	100	—	—	mV
V_{CM}	Input common mode voltage	0.3	—	1.5	V
T_R, T_F	Output rise and fall times, 20% to 80%	—	500	—	ps
T_{ODUTY}	Output clock duty cycle	45	50	55	%

Note: Data is for 2mA drive. Other differential driver current options are available.

BLVDS

The LatticeSC devices support BLVDS standard. This standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

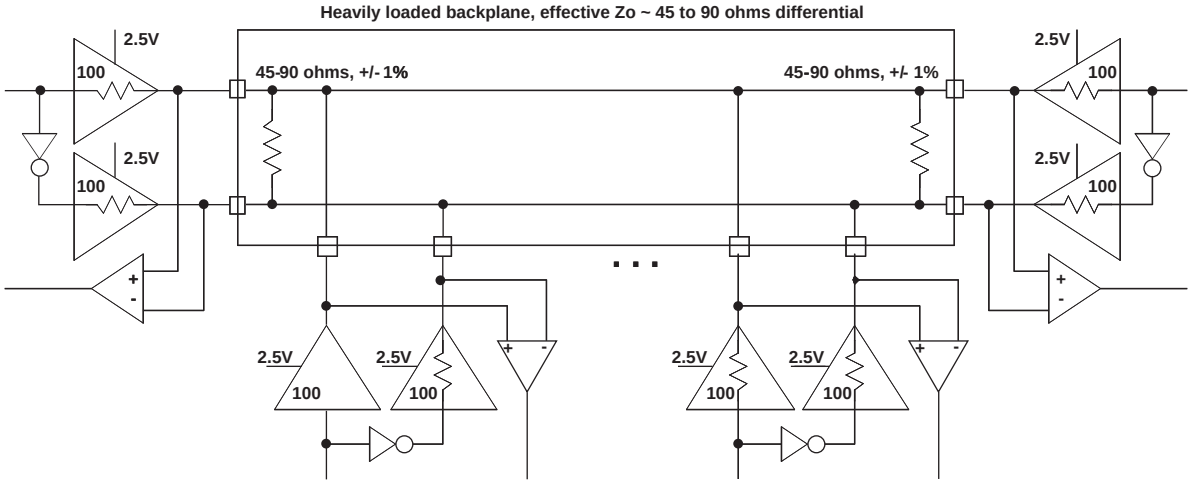


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	100	100	ohm
R_{TLEFT}	Left end termination	45	90	ohm
R_{TRIGHT}	Right end termination	45	90	ohm
V_{OH}	Output high voltage	1.375	1.48	V
V_{OL}	Output low voltage	1.125	1.02	V
V_{OD}	Output differential voltage	0.25	0.46	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

Figure 3-8. Read Mode with Input and Output Registers

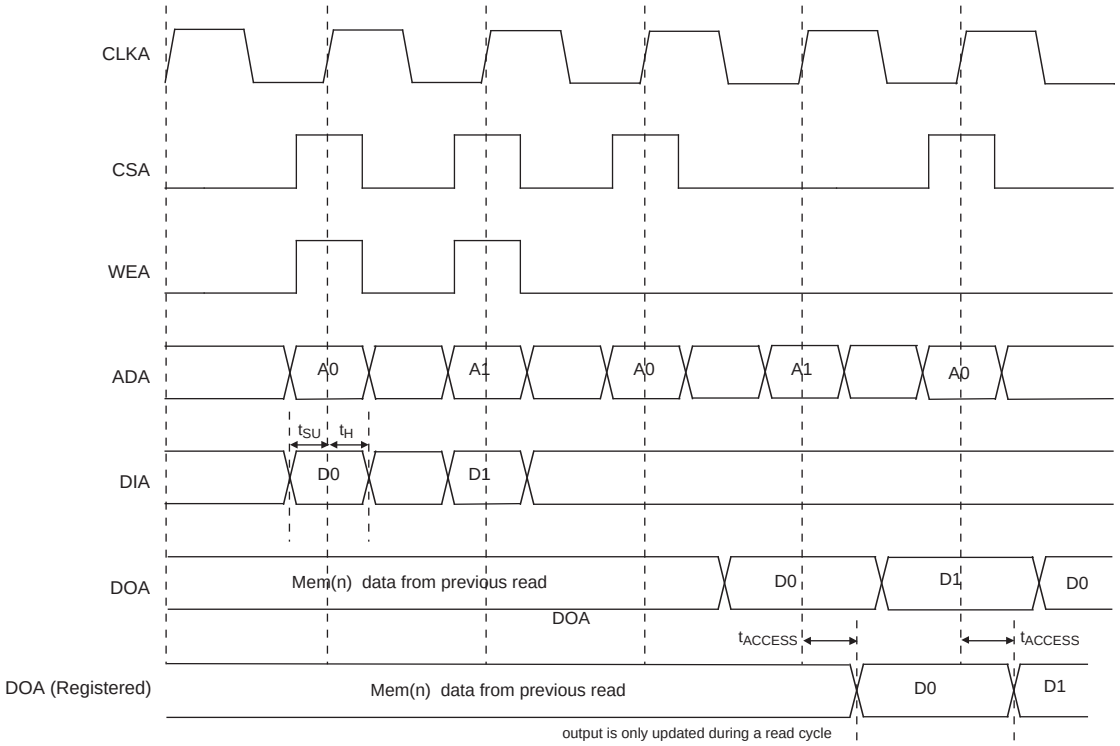
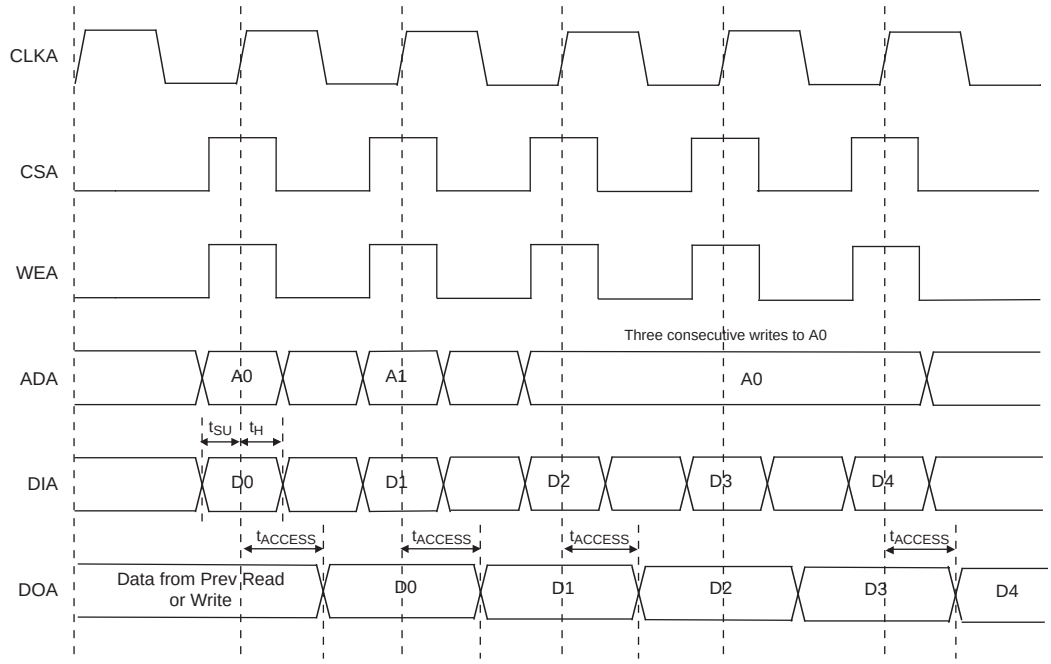


Figure 3-9. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

LatticeSC/M sysCONFIG Port Timing (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Asynchronous Peripheral Configuration Mode				
t_{WRAP}	WRN, CS0N and CS1 Pulse Width	5	-	ns
t_{SAP}	D[7:0] Setup Time	1.5	-	ns
t_{RDYAP}	RDY Delay	—	8	ns
t_{BAP}	RDY Low	1	8	CCLK periods
t_{WR2AP}	Earliest WRN After RDY Goes High	0	—	ns
t_{DENAP}	RDN to D[7:0] Enable/Disable	—	7.5	ns
t_{DAP}	CCLK to DOUT	—	7.5	ns
sysCONFIG Slave Serial Configuration Mode				
t_{SSS}	DIN Setup Time	5.2	—	ns
t_{HSS}	DIN Hold Time	0	—	ns
t_{CHSS}	CCLK High Time	3.75	—	ns
t_{CLSS}	CCLK Low Time	3.75	—	ns
f_{CSS}	CCLK Frequency	—	150	MHz
t_{DSS}	CCLK to DOUT	—	7.5	ns
sysCONFIG Slave Parallel Configuration Mode				
t_{S1SP}	CS0N, CS1, WRN Setup Time	5.2	—	ns
t_{H1SP}	CS0N, CS1, WRN Hold Time	0	—	ns
t_{S2SP}	D[7:0] Setup Time	5.2	—	ns
t_{H2SP}	D[7:0] Hold Time	0	—	ns
t_{CHSP}	CCLK High Time	3.75	—	ns
t_{CL}	CCLK Low Time	3.75	—	ns
f_{CSP}	CCLK Frequency	—	150	MHz

sysCONFIG MPI Port

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{MPICTRL\_SET}$	MPI Control (MPCSTRBN, MPCWRN, MPCCLK, etc.) to MPCCLK Setup Time	4.9	—	5.2	—	5.5	—	ns
t_{MPIADR_SET}	MPI Address to MPCCLK Setup Time	3.9	—	4.2	—	4.5	—	ns
t_{MPIDAT_SET}	MPI Write Data to MPCCLK Setup Time	4.9	—	5.2	—	5.5	—	ns
$t_{MPIDPAR\_SET}$	MPI Write Parity Data to MPCCLK Setup Time	3.9	—	4.2	—	4.5	—	ns
t_{MPI_HLD}	All Hold Times	0	—	0	—	0	—	ns
$t_{MPICTRL\_DEL}$	MPCCLK to MPI Control (MPCTA, MPC-TEA, MPCRETRY)	—	5.6	—	6.7	—	8.7	ns
t_{MPIDAT_DEL}	MPCCLK to MPI Data	—	5.6	—	6.7	—	8.7	ns
$t_{MPIDPAR\_DEL}$	MPCCLK to MPI Parity Data	—	4.9	—	5.7	—	7.7	ns
$f_{MPI\_CLK\_FRQ}$	MPCCLK Frequency	—	100	—	83	—	66	MHz

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D14	PT15B	1	A15/MPI_ADDR29	PT25B	1	A15/MPI_ADDR29
D13	PT15A	1	A17/MPI_ADDR31	PT25A	1	A17/MPI_ADDR31
F12	PT13D	1	A19/MPI_TSIZ1	PT24D	1	A19/MPI_TSIZ1
F13	PT13C	1	A20/MPI_BDIP	PT24C	1	A20/MPI_BDIP
B12	PT11B	1	A18/MPI_TSIZ0	PT24B	1	A18/MPI_TSIZ0
B11	PT11A	1	MPI_TEA	PT24A	1	MPI_TEA
E12	PT10D	1	D14/MPI_DATA14	PT23D	1	D14/MPI_DATA14
D12	PT10C	1	DP1/MPI_PAR1	PT23C	1	DP1/MPI_PAR1
G10	PT9B	1	A21/MPI_BURST	PT23B	1	A21/MPI_BURST
G9	PT9A	1	D15/MPI_DATA15	PT23A	1	D15/MPI_DATA15
C10	A_VDDIB3_L	-		A_VDDIB3_L	-	
E9	VCC12	-		VCC12	-	
B10	A_HDINP3_L	-	PCS 360 CH 3 IN P	A_HDINP3_L	-	PCS 360 CH 3 IN P
B9	A_HDINN3_L	-	PCS 360 CH 3 IN N	A_HDINN3_L	-	PCS 360 CH 3 IN N
A10	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
D9	VCC12	-		VCC12	-	
A9	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
C9	A_VDDOB3_L	-		A_VDDOB3_L	-	
A8	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
C8	A_VDDOB2_L	-		A_VDDOB2_L	-	
A7	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
E8	VCC12	-		VCC12	-	
B8	A_HDINN2_L	-	PCS 360 CH 2 IN N	A_HDINN2_L	-	PCS 360 CH 2 IN N
B7	A_HDINP2_L	-	PCS 360 CH 2 IN P	A_HDINP2_L	-	PCS 360 CH 2 IN P
C7	A_VDDIB2_L	-		A_VDDIB2_L	-	
D8	VCC12	-		VCC12	-	
C6	A_VDDIB1_L	-		A_VDDIB1_L	-	
E7	VCC12	-		VCC12	-	
B6	A_HDINP1_L	-	PCS 360 CH 1 IN P	A_HDINP1_L	-	PCS 360 CH 1 IN P
B5	A_HDINN1_L	-	PCS 360 CH 1 IN N	A_HDINN1_L	-	PCS 360 CH 1 IN N
A6	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
D7	VCC12	-		VCC12	-	
A5	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
C5	A_VDDOB1_L	-		A_VDDOB1_L	-	
A4	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
C4	A_VDDOB0_L	-		A_VDDOB0_L	-	
A3	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
E6	VCC12	-		VCC12	-	
B4	A_HDINN0_L	-	PCS 360 CH 0 IN N	A_HDINN0_L	-	PCS 360 CH 0 IN N
B3	A_HDINP0_L	-	PCS 360 CH 0 IN P	A_HDINP0_L	-	PCS 360 CH 0 IN P
C3	A_VDDIB0_L	-		A_VDDIB0_L	-	
D6	VCC12	-		VCC12	-	
L5	NC	-		PL21A	7	
M5	NC	-		PL21B	7	
G2	NC	-		PL20A	7	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P32	PL30A	6		PL39A	6	
P31	PL30B	6		PL39B	6	
R28	PL30C	6	PCLKT6_3	PL39C	6	PCLKT6_3
T28	PL30D	6	PCLKC6_3	PL39D	6	PCLKC6_3
R30	PL31A	6		PL40A	6	
R29	PL31B	6		PL40B	6	
T25	PL31C	6	PCLKT6_2	PL40C	6	PCLKT6_2
T26	PL31D	6	PCLKC6_2	PL40D	6	PCLKC6_2
R31	PL34A	6		PL43A	6	
R32	PL34B	6		PL43B	6	
U23	PL34C	6	VREF1_6	PL43C	6	VREF1_6
U24	PL34D	6		PL43D	6	
T31	PL35A	6		PL44A	6	
T32	PL35B	6		PL44B	6	
T27	PL35C	6		PL44C	6	
U28	PL35D	6		PL44D	6	
U32	PL36A	6		PL45A	6	
U31	PL36B	6		PL45B	6	
U26	PL36C	6		PL45C	6	
U25	PL36D	6		PL45D	6	
V32	PL38A	6		PL47A	6	
V31	PL38B	6		PL47B	6	
V24	PL38C	6		PL47C	6	
V23	PL38D	6		PL47D	6	
V29	PL39A	6		PL48A	6	
V30	PL39B	6		PL48B	6	
U27	PL39C	6		PL48C	6	
V28	PL39D	6		PL48D	6	
W30	PL40A	6		PL49A	6	
W29	PL40B	6		PL49B	6	
V25	PL40C	6		PL49C	6	
W26	PL40D	6		PL49D	6	
W31	PL42A	6		PL51A	6	
Y31	PL42B	6		PL51B	6	
W27	PL42C	6		PL51C	6	
Y27	PL42D	6	DIFFR_6	PL51D	6	DIFFR_6
W28	PL43A	6		PL52A	6	
Y28	PL43B	6		PL52B	6	
Y26	PL43C	6		PL52C	6	
W25	PL43D	6		PL52D	6	
W32	PL44A	6		PL53A	6	
Y32	PL44B	6		PL53B	6	
AB28	PL44C	6		PL53C	6	
AA28	PL44D	6		PL53D	6	
AB32	PL47A	6		PL60A	6	
AA32	PL47B	6		PL60B	6	
AB27	PL47C	6		PL60C	6	
AC27	PL47D	6		PL60D	6	
AD31	PL48A	6		PL61A	6	
AC31	PL48B	6		PL61B	6	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
U12	VCC12	-		VCC12	-	
U21	VCC12	-		VCC12	-	
AA16	VCC12	-		VCC12	-	
AA17	VCC12	-		VCC12	-	
M14	VCC12	-		VCC12	-	
P12	VCC12	-		VCC12	-	
W12	VCC12	-		VCC12	-	
AA14	VCC12	-		VCC12	-	
AA19	VCC12	-		VCC12	-	
W21	VCC12	-		VCC12	-	
P21	VCC12	-		VCC12	-	
M19	VCC12	-		VCC12	-	
A2	GND	-		GND	-	
A10	GND	-		GND	-	
E28	NC	-		NC	-	
E5	NC	-		NC	-	
F10	NC	-		NC	-	
E10	NC	-		NC	-	
E23	NC	-		NC	-	
F23	NC	-		NC	-	

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M25 and LatticeSC/M40 in a 1020-pin package support a 16-bit MPI interface.

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD29	PL60D	6		PL84D	6	
AE31	PL61A	6		PL85A	6	
AF31	PL61B	6		PL85B	6	
AF30	PL61C	6		PL85C	6	
AF29	PL61D	6		PL85D	6	
AH33	PL62A	6		PL86A	6	
AJ33	PL62B	6		PL86B	6	
AC28	PL62C	6		PL86C	6	
AD28	PL62D	6		PL86D	6	
AH32	PL65A	6		PL89A	6	
AJ32	PL65B	6		PL89B	6	
AD27	PL65C	6		PL89C	6	
AE27	PL65D	6	VREF2_6	PL89D	6	VREF2_6
AG34	PL66A	6		PL90A	6	
AH34	PL66B	6		PL90B	6	
AC26	PL66C	6		PL90C	6	
AB26	PL66D	6		PL90D	6	
AK33	PL67A	6		PL91A	6	
AL33	PL67B	6		PL91B	6	
AG30	PL67C	6		PL91C	6	
AH30	PL67D	6		PL91D	6	
AL34	PL69A	6		PL93A	6	
AM34	PL69B	6		PL93B	6	
AJ30	PL69C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL93C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AK30	PL69D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL93D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AJ31	PL70A	6		PL94A	6	
AH31	PL70B	6		PL94B	6	
AD26	PL70C	6		PL94C	6	
AD25	PL70D	6		PL94D	6	
AL32	PL71A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL95A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AL31	PL71B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL95B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AG29	PL71C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL95C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AG28	PL71D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL95D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AF28	XRES	-		XRES	-	
AF27	TEMP	6		TEMP	6	
AM33	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AN33	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
AH29	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AJ29	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AM32	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AM31	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AG27	PB4C	5		PB4C	5	
AG26	PB4D	5		PB4D	5	
AL29	PB5A	5		PB5A	5	
AL28	PB5B	5		PB5B	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AF21	PB26D	5		PB29D	5	
AN23	PB27A	5		PB45A	5	
AN22	PB27B	5		PB45B	5	
AP23	PB29A	5		PB55A	5	
AP22	PB29B	5		PB55B	5	
AG21	PB29C	5		PB55C	5	
AG20	PB29D	5		PB55D	5	
AP25	PB30A	5	PCLKT5_3	PB48A	5	PCLKT5_3
AP24	PB30B	5	PCLKC5_3	PB48B	5	PCLKC5_3
AD21	PB30C	5	PCLKT5_4	PB48C	5	PCLKT5_4
AD20	PB30D	5	PCLKC5_4	PB48D	5	PCLKC5_4
AL23	PB31A	5	PCLKT5_5	PB49A	5	PCLKT5_5
AL22	PB31B	5	PCLKC5_5	PB49B	5	PCLKC5_5
AH24	PB31C	5		PB49C	5	
AH23	PB31D	5		PB49D	5	
AM23	PB33A	5	PCLKT5_0	PB51A	5	PCLKT5_0
AM22	PB33B	5	PCLKC5_0	PB51B	5	PCLKC5_0
AJ24	PB33C	5		PB51C	5	
AJ23	PB33D	5	VREF2_5	PB51D	5	VREF2_5
AN21	PB34A	5	PCLKT5_1	PB52A	5	PCLKT5_1
AN20	PB34B	5	PCLKC5_1	PB52B	5	PCLKC5_1
AE19	PB34C	5	PCLKT5_6	PB52C	5	PCLKT5_6
AD19	PB34D	5	PCLKC5_6	PB52D	5	PCLKC5_6
AK21	PB35A	5	PCLKT5_2	PB53A	5	PCLKT5_2
AK20	PB35B	5	PCLKC5_2	PB53B	5	PCLKC5_2
AK23	PB35C	5	PCLKT5_7	PB53C	5	PCLKT5_7
AK22	PB35D	5	PCLKC5_7	PB53D	5	PCLKC5_7
AL20	PB37A	5		PB56A	5	
AL19	PB37B	5		PB56B	5	
AG19	PB37C	5		PB56C	5	
AF19	PB37D	5		PB56D	5	
AP21	PB38A	5		PB57A	5	
AP20	PB38B	5		PB57B	5	
AH21	PB38C	5		PB57C	5	
AH20	PB38D	5		PB57D	5	
AM20	PB39A	5		PB59A	5	
AM19	PB39B	5		PB59B	5	
AJ21	PB39C	5		PB59C	5	
AJ20	PB39D	5		PB59D	5	
AK19	PB41A	5		PB60A	5	
AK18	PB41B	5		PB60B	5	
AE18	PB41C	5		PB60C	5	
AD18	PB41D	5		PB60D	5	
AN19	PB42A	5		PB61A	5	
AN18	PB42B	5		PB61B	5	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
N27	PL47C	7	
P27	PL47D	7	
K33	PL49A	7	
L33	PL49B	7	
M30	PL49C	7	
N30	PL49D	7	
M31	PL51A	7	
N31	PL51B	7	
P24	PL51C	7	
R24	PL51D	7	
M33	PL56A	7	
N33	PL56B	7	
U25	PL56C	7	
T25	PL56D	7	
L34	PL57A	7	
M34	PL57B	7	
P29	PL57C	7	
R29	PL57D	7	
N34	PL60A	7	
P34	PL60B	7	
R27	PL60C	7	
T27	PL60D	7	
R32	PL61A	7	PCLKT7_1
R31	PL61B	7	PCLKC7_1
U24	PL61C	7	PCLKT7_3
T24	PL61D	7	PCLKC7_3
P33	PL62A	7	PCLKT7_0
R33	PL62B	7	PCLKC7_0
T26	PL62C	7	PCLKT7_2
U26	PL62D	7	PCLKC7_2
T32	PL64A	6	PCLKT6_0
T31	PL64B	6	PCLKC6_0
U29	PL64C	6	PCLKT6_1
V29	PL64D	6	PCLKC6_1
T30	PL65A	6	
U30	PL65B	6	
U27	PL65C	6	PCLKT6_3
V27	PL65D	6	PCLKC6_3
R34	PL66A	6	
T34	PL66B	6	
U28	PL66C	6	PCLKT6_2
V28	PL66D	6	PCLKC6_2
V30	PL69A	6	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
L21	PT55D	1	A16/MPI_ADDR30
L20	PT55C	1	D13/MPI_DATA13
D20	PT55B	1	A15/MPI_ADDR29
E20	PT55A	1	A17/MPI_ADDR31
L19	PT54D	1	A19/MPI_TSIZ1
K19	PT54C	1	A20/MPI_BDIP
D21	PT54B	1	A18/MPI_TSIZ0
E21	PT54A	1	MPI_TEA
M20	PT51D	1	D14/MPI_DATA14
M19	PT51C	1	DP1/MPI_PAR1
F21	PT51B	1	A21/MPI_BURST
G21	PT51A	1	D15/MPI_DATA15
H24	B_REFCLKP_L	-	
J24	B_REFCLKN_L	-	
L22	VCC12	-	
E26	B_VDDIB3_L	-	
G22	VCC12	-	
E22	B_HDINP3_L	-	PCS 361 CH 3 IN P
F22	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
L24	VCC12	-	
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D22	B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D23	B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
K24	VCC12	-	
F23	B_HDINN2_L	-	PCS 361 CH 2 IN N
E23	B_HDINP2_L	-	PCS 361 CH 2 IN P
D26	B_VDDIB2_L	-	
G23	VCC12	-	
D27	B_VDDIB1_L	-	
G24	VCC12	-	
E24	B_HDINP1_L	-	PCS 361 CH 1 IN P
F24	B_HDINN1_L	-	PCS 361 CH 1 IN N
A23	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
L25	VCC12	-	
B23	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
D24	B_VDDOB1_L	-	
B24	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
D25	B_VDDOB0_L	-	
A24	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
K25	VCC12	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AP8	PB117D	4		PB131D	4	
AY3	PB119A	4		PB133A	4	
AW3	PB119B	4		PB133B	4	
AR6	PB119C	4		PB133C	4	
AR5	PB119D	4		PB133D	4	
AU5	PB120A	4		PB134A	4	
AV5	PB120B	4		PB134B	4	
AL12	PB120C	4		PB134C	4	
AL11	PB120D	4		PB134D	4	
AV3	PB121A	4		PB135A	4	
AV4	PB121B	4		PB135B	4	
AN9	PB121C	4		PB135C	4	
AN8	PB121D	4		PB135D	4	
AW1	PB123A	4		PB138A	4	
AY1	PB123B	4		PB138B	4	
AK14	PB123C	4	VREF1_4	PB138C	4	VREF1_4
AK13	PB123D	4		PB138D	4	
AV2	PB124A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB139A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AW2	PB124B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB139B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AM10	PB124C	4		PB139C	4	
AM9	PB124D	4		PB139D	4	
AV1	PB125A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB141A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AU1	PB125B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB141B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AL10	PB125C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB141C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AL9	PB125D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB141D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AT3	PROBE_VCC	-		PROBE_VCC	-	
AU2	PROBE_GND	-		PROBE_GND	-	
AP7	PR95D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR117D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AN7	PR95C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR117C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AR3	PR95B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR117B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AR4	PR95A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR117A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AP6	PR94D	3		PR116D	3	
AN6	PR94C	3		PR116C	3	
AT2	PR94B	3		PR116B	3	
AR2	PR94A	3		PR116A	3	
AM6	PR93D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR115D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AL6	PR93C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR115C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AP5	PR93B	3		PR115B	3	
AN5	PR93A	3		PR115A	3	
AL8	PR91D	3		PR112D	3	
AK8	PR91C	3		PR112C	3	
AP2	PR91B	3		PR112B	3	
AN2	PR91A	3		PR112A	3	
AJ12	PR90D	3		PR109D	3	
AH12	PR90C	3		PR109C	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
K14	VCC12	-		VCC12	-	
H11	B_VDDIB2_R	-		B_VDDIB2_R	-	
D8	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
E8	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
G5	VCC12	-		VCC12	-	
B9	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
L12	B_VDDOB2_R	-		B_VDDOB2_R	-	
A9	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
C5	B_VDDOB3_R	-		B_VDDOB3_R	-	
A10	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
H5	VCC12	-		VCC12	-	
B10	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
E9	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
D9	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
J13	VCC12	-		VCC12	-	
H12	B_VDDIB3_R	-		B_VDDIB3_R	-	
J12	VCC12	-		VCC12	-	
M14	B_REFCLKN_R	-		B_REFCLKN_R	-	
L14	B_REFCLKP_R	-		B_REFCLKP_R	-	
J14	VCC12	-		VCC12	-	
G12	C_VDDIB0_R	-		C_VDDIB0_R	-	
D10	C_HDINP0_R	-	PCS 3E2 CH 0 IN P	C_HDINP0_R	-	PCS 3E2 CH 0 IN P
E10	C_HDINN0_R	-	PCS 3E2 CH 0 IN N	C_HDINN0_R	-	PCS 3E2 CH 0 IN N
H6	VCC12	-		VCC12	-	
B11	C_HDOUTP0_R	-	PCS 3E2 CH 0 OUT P	C_HDOUTP0_R	-	PCS 3E2 CH 0 OUT P
M12	C_VDDOB0_R	-		C_VDDOB0_R	-	
A11	C_HDOUTN0_R	-	PCS 3E2 CH 0 OUT N	C_HDOUTN0_R	-	PCS 3E2 CH 0 OUT N
L11	C_VDDOB1_R	-		C_VDDOB1_R	-	
A12	C_HDOUTN1_R	-	PCS 3E2 CH 1 OUT N	C_HDOUTN1_R	-	PCS 3E2 CH 1 OUT N
K11	VCC12	-		VCC12	-	
B12	C_HDOUTP1_R	-	PCS 3E2 CH 1 OUT P	C_HDOUTP1_R	-	PCS 3E2 CH 1 OUT P
E11	C_HDINN1_R	-	PCS 3E2 CH 1 IN N	C_HDINN1_R	-	PCS 3E2 CH 1 IN N
D11	C_HDINP1_R	-	PCS 3E2 CH 1 IN P	C_HDINP1_R	-	PCS 3E2 CH 1 IN P
H13	VCC12	-		VCC12	-	
C6	C_VDDIB1_R	-		C_VDDIB1_R	-	
H15	VCC12	-		VCC12	-	
G13	C_VDDIB2_R	-		C_VDDIB2_R	-	
D12	C_HDINP2_R	-	PCS 3E2 CH 2 IN P	C_HDINP2_R	-	PCS 3E2 CH 2 IN P
E12	C_HDINN2_R	-	PCS 3E2 CH 2 IN N	C_HDINN2_R	-	PCS 3E2 CH 2 IN N
J9	VCC12	-		VCC12	-	
B13	C_HDOUTP2_R	-	PCS 3E2 CH 2 OUT P	C_HDOUTP2_R	-	PCS 3E2 CH 2 OUT P
K10	C_VDDOB2_R	-		C_VDDOB2_R	-	
A13	C_HDOUTN2_R	-	PCS 3E2 CH 2 OUT N	C_HDOUTN2_R	-	PCS 3E2 CH 2 OUT N
J10	C_VDDOB3_R	-		C_VDDOB3_R	-	
A14	C_HDOUTN3_R	-	PCS 3E2 CH 3 OUT N	C_HDOUTN3_R	-	PCS 3E2 CH 3 OUT N