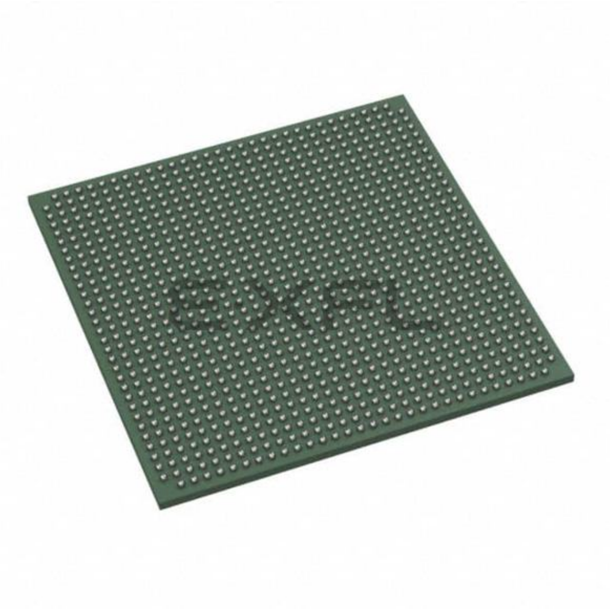

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

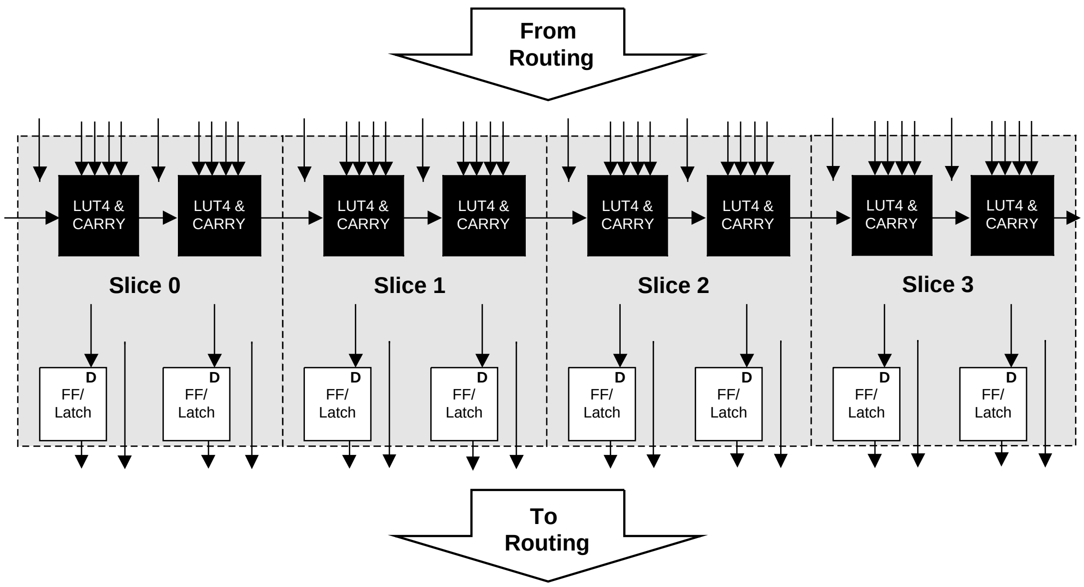
Details	
Product Status	Obsolete
Number of LABs/CLBs	6250
Number of Logic Elements/Cells	25000
Total RAM Bits	1966080
Number of I/O	476
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-OFCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga25ep1-6ff1020c

PFU Blocks

The core of the LatticeSC devices consists of PFU blocks. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 53 inputs and 25 outputs associated with each PFU block.

Figure 2-2. PFU Diagram



Slice

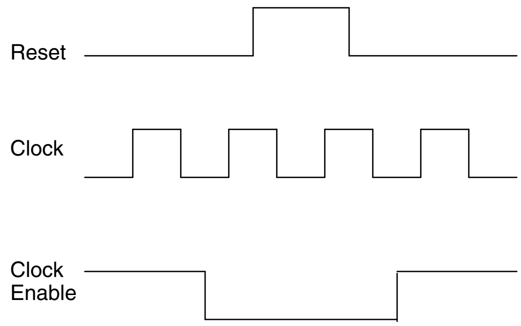
Each slice contains two LUT4 lookup tables feeding two registers (programmed to be in FF or Latch mode), and some associated logic that allows the LUTs to be combined to implement 5, 6, 7 and 8 Input LUTs (LUT5, LUT6, LUT7 and LUT8). There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge/level clocks.

There are 14 input signals: 13 signals from routing and one from the carry-chain (from adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to adjacent PFU). Table 2-1 lists the signals associated with each slice.

EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the low-to-high transition of the reset, as shown in Figure 2-16.

Figure 2-16. EBR Asynchronous Reset (Including GSR) Timing Diagram



If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/Os becoming active.

These instructions apply to all EBR RAM, ROM, FIFO and shift register implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2-16. The reset timing rules apply to the RPReset input vs. the RE input and the RST input vs. the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For the EBR shift register mode, the GSR signal is always enabled and the local RESET pin is always asynchronous.

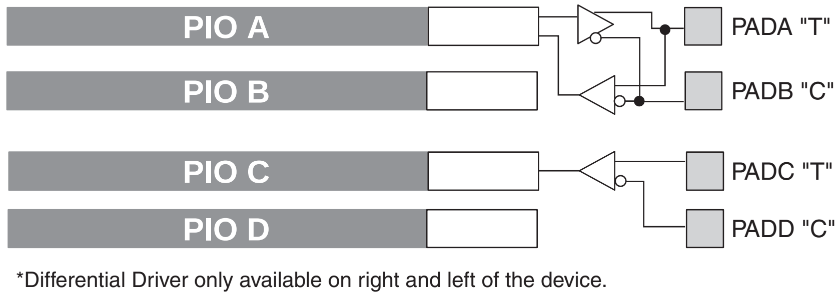
Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled. For more information about on-chip memory, see TN1094, On-Chip Memory Usage Guide for LatticeSC Devices.

Programmable I/O Cells (PIC)

Each PIC contains four PIOs connected to their respective PURESPEED I/O Buffer which are then connected to the PADs as shown in Figure 2-17. The PIO Block supplies the output data (DO) and the Tri-state control signal (TO) to PURESPEED I/O buffer, and receives input (DI) from the buffer. The PIO contains advanced capabilities to allow the support of speeds up to 2Gbps. These include dedicated shift and DDR logic and adaptive input logic. The dedicated resources simplify the design of robust interfaces.

high-speed interfaces in the LatticeSC devices. Figure 2-18 shows how differential receivers and drivers are arranged between PIOs.

Figure 2-18. Differential Drivers and Receivers



PIO

The PIO contains five blocks: an input register block, output register block, tristate register block, update block, and a control logic block. These blocks contain registers for both single data rate (SDR), double data rate (DDR), and shift register operation along with the necessary clock and selection logic.

Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-20 show the diagram of the input register block. The signal from the PURE-SPEED I/O buffer (DI) enters the input register block and can be used for three purposes, as a source for the combinatorial (INDD) and clock outputs (INCK), the input into the SDR register/latch block and the input to the delay block. The output of the delay block can be used as combinatorial (INDD) and clock (INCK) outputs, an input to the DDR/Shift Register Block or an input into the SDR register block.

Input SDR Register/Latch Block

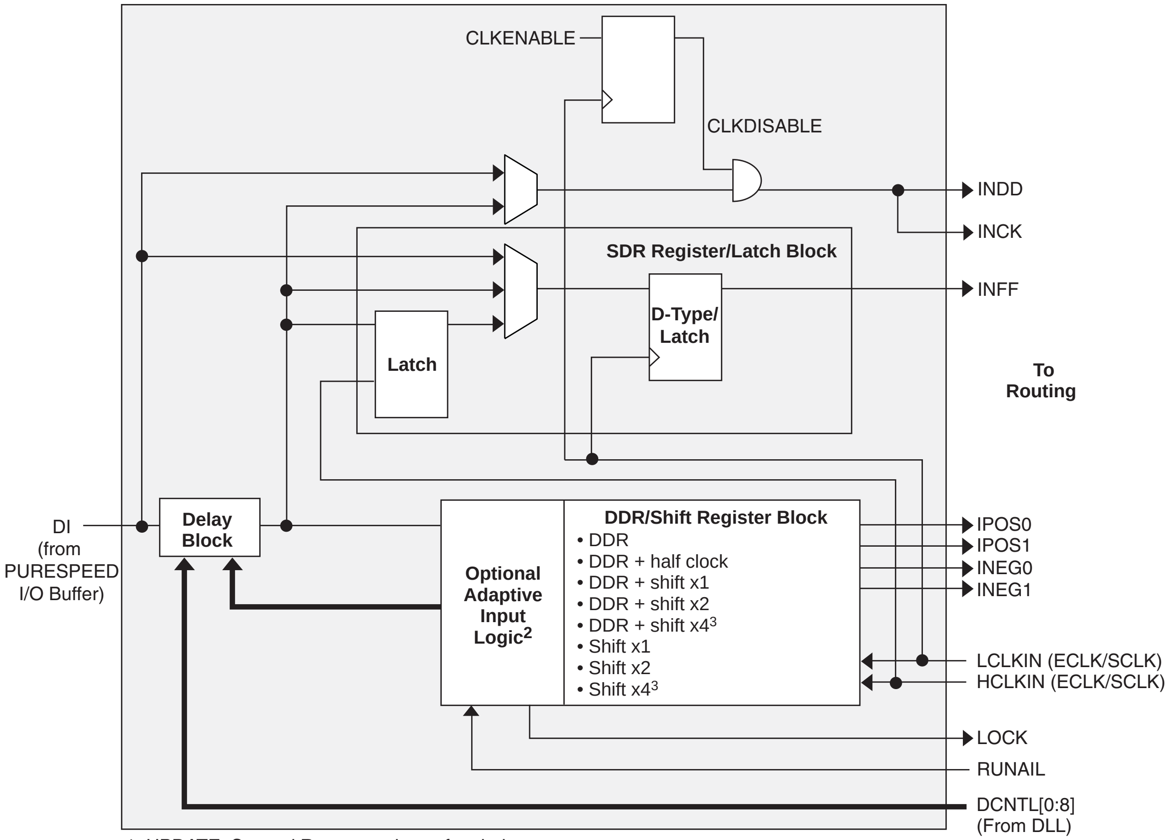
The SDR register/latch block has a latch and a register/latch that can be used in a variety of combinations to provide a registered or latched output (INFF). The latch operates off high-speed input clocks and latches data on the positive going edge. The register/latch operates off the low-speed input clock and registers/latches data on the positive going edge. Both the latch and the register/latch have a clock enable input that is driven by the input clock enable. In addition both have a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR (LSR has precedence over CE) and Global Set Reset GSR enable or disable. The register and latch LSR inputs are driven from LSRI, which is generated from the PIO control MUX. The GSR inputs are driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

Input Delay Block

The delay block uses 144 tapped delay lines to obtain coarse and fine delay resolution. These delays can be adjusted during configuration or automatically via DLL or AIL blocks. The Adaptive Input Logic (AIL) uses this delay block to adjust automatically the delay in the data path to ensure that it has sufficient setup and hold time.

The delay line in this block matches the delay line that is used in the 12 on-chip DLLs. The delay line can be set via configuration bits or driven from a calibration bus that allows the setting to be controlled either from one of the on-chip DLLs or user logic. Controlling the delay from one of the on-chip DLLs allow the delay to be calibrated to the DLL clock and hence compensated for the variations in process, voltage and temperature.

Figure 2-20. Input Register Block[1]



1. UPDATE, Set and Reset not shown for clarity
2. Adaptive input logic is only available in selected PIO
3. By four shift modes utilize DDR/shift register block from paired PIO.
4. CLKDISABLE is used to block the transitions on the DQS pin during post-amble. Its main use is to disable DQS (typically found in DDR memory interfaces) or other clock signals. It can also be used to disable any/all input signals to save power.

PURESPEED I/O Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 33	3.135	3.3	3.465	—	—	—
LVCMOS 25	2.375	2.5	2.625	—	—	—
LVCMOS 18	1.71	1.8	1.89	—	—	—
LVCMOS 15	1.425	1.5	1.575	—	—	—
LVCMOS 12	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
PCIX33	3.135	3.3	3.465	—	—	—
PCIX15	1.425	1.5	1.575	$0.49V_{CCIO}$	$0.5V_{CCIO}$	$0.51V_{CCIO}$
AGP1X33	3.135	3.3	3.465	—	—	—
AGP2X33	3.135	3.3	3.465	$0.39V_{CCIO}$	$0.4V_{CCIO}$	$0.41V_{CCIO}$
SSTL18_I, II[3]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II[3]	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II[3]	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I, II[3]	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15_III[1, 3] and IV[1, 3]	1.425	1.5	1.575	0.68	0.9	0.9
HSTL 18_I[3], II[3]	1.71	1.8	1.89	0.816	0.9	1.08
HSTL 18_ III[1, 3], IV[1, 3]	1.71	1.8	1.89	0.816	1.08	1.08
GTL12[1, 3], GTLPLUS15[1, 3]	—	—	—	0.882	1.0	1.122
LVDS	—	—	—	—	—	—
Mini-LVDS	—	—	—	—	—	—
RSDS	—	—	—	—	—	—
LVPECL33 (outputs)[2]	3.135	3.3	3.465	—	—	—
LVPECL33 (inputs)[2, 4]	—	≤ 2.5	—	—	—	—
BLVDS25[2, 3]	2.375	2.5	2.625	—	—	—
MLVDS25[2, 3]	2.375	2.5	2.625	—	—	—
SSTL18D_I[3], II[3]	1.71	1.8	1.89	—	—	—
SSTL25D_I[3], II[3]	2.375	2.5	2.625	—	—	—
SSTL33D_I[3], II[3]	3.135	3.3	3.465	—	—	—
HSTL15D_I[3], II[3]	1.425	1.5	1.575	—	—	—
HSTL18D_I[3], II[3]	1.71	1.8	1.89	—	—	—

1. Input only.
2. Inputs on chip. Outputs are implemented with the addition of external resisters.
3. Input for this standard does not depend on the value of V_{CCIO}.
4. Inputs for this standard cannot be in 3.3V VCCIO banks (≤ 2.5V only).

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

MLVDS

The LatticeSC devices support the MLVDS standard. This industry standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. MLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-1 is one possible solution for bi-directional multi-point differential signals.

Figure 3-1. MLVDS Multi-Point Output Example

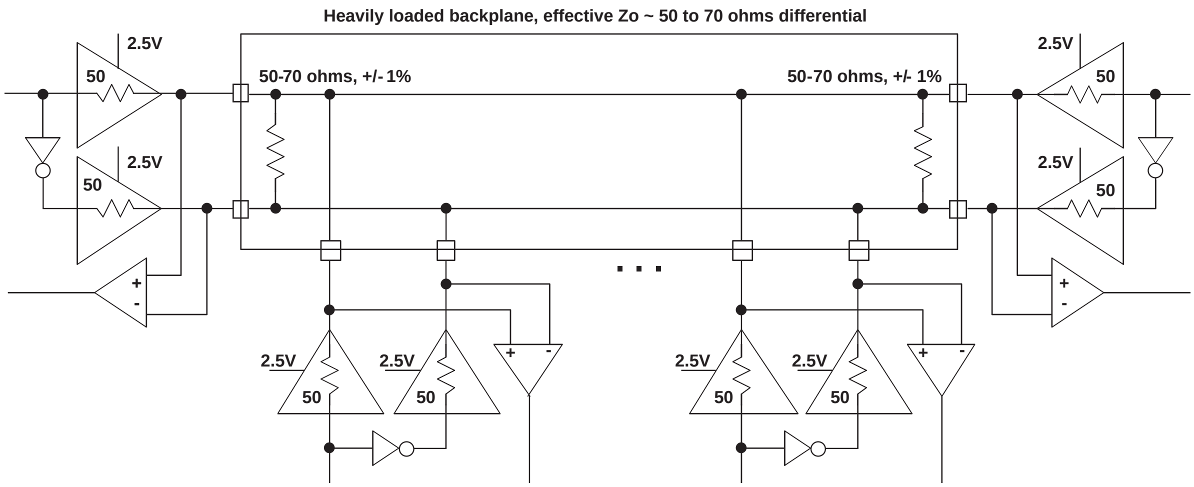


Table 3-1. MLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 50	Zo = 70	
Z_{OUT}	Output impedance	50	50	ohm
R_{TLEFT}	Left end termination	50	70	ohm
R_{TRIGHT}	Right end termination	50	70	ohm
V_{OH}	Output high voltage	1.50	1.575	V
V_{OL}	Output low voltage	1.00	0.925	V
V_{OD}	Output differential voltage	0.50	0.65	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	20.0	18.5	mA

1. For input buffer, see LVDS table.

Typical Building Block Function Performance

Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

Pin to Pin Performance (LVCMOS25 12 mA Drive)

Function	-7*	Units
Basic Functions		
32-bit Decoder	6.65	ns
Combinatorial (Pin to LUT to Pin)	5.58	ns
Embedded Memory Functions (Single Port RAM)		
Pin to EBR Input Register Setup (Global Clock)	1.66	ns
EBR Output Clock to Pin (Global Clock)	8.54	ns
Distributed (PFU) RAM (Single Port RAM)		
Pin to PFU RAM Register Setup (Global Clock)	1.32	ns
PFU RAM Clock to Pin (Global Clock)	6.83	ns

*Typical performance per function

Register-to-Register Performance

Function	-7*	Units
Basic Functions		
32-Bit Decoder	539	MHz
64-Bit Decoder	517	MHz
16:1 MUX	1003	MHz
32:1 MUX	798	MHz
16-Bit Adder	672	MHz
64-Bit Adder	353	MHz
16-Bit Counter	719	MHz
64-Bit Counter	369	MHz
32x8 SP RAM (PFU, Output Registered)	768	MHz
128x8 SP RAM (PFU, Output Registered)	545	MHz
Embedded Memory Functions		
Single Port RAM (512x36 Bits)	372	MHz
True Dual Port RAM 1024x18 Bits (No EBR Out Reg)	326	MHz
True dual port RAM 1024x18 Bits (EBR Reg)	372	MHz
FIFO port (A: x36 bits, B: x9 Bits, No EBR Out Reg)	353	MHz
FIFO port (A: x36 bits, B: x9 Bits, EBR Reg)	375	MHz
True DP RAM Width Cascading (1024x72)	372	MHz
DSP Functions		
9x9 1-stage Multiplier	209	MHz
18x18 1-Stage Multiplier	155	MHz
9x9 3-Stage Pipelined Multiplier	373	MHz
18x18 4-Stage Pipelined Multiplier	314	MHz
9x9 Constant Multiplier	372	MHz

*Typical performance per function

Switching Test Conditions

Figure 3-15 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-4.

Figure 3-15. Output Test Load, LVTTL and LVCMOS Standards

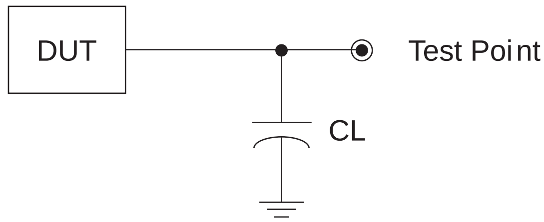


Table 3-4. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	30pF	LVCMOS 3.3 = 1.5V	—
		LVCMOS 2.5 = $V_{CCIO}/2$	—
		LVCMOS 1.8 = $V_{CCIO}/2$	—
		LVCMOS 1.5 = $V_{CCIO}/2$	—
		LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	30pF	$V_{CCIO}/2$	V_{OL}
LVCMOS 2.5 I/O (Z -> L)		$V_{CCIO}/2$	V_{OH}
LVCMOS 2.5 I/O (H -> Z)		V_{OH} - 0.15	V_{OL}
LVCMOS 2.5 I/O (L -> Z)		V_{OL} + 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Lattice Semiconductor Corporation

LatticeSC/M Family Data Sheet
Pinout Information

January 2008 | Data Sheet DS1004

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PIC row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
VREF1_x, VREF2_x	—	The reference supply pins for I/O bank x. Any I/O pin in a bank can be assigned as a reference supply pin, but software defaults use designated pin.
NC	—	No connect. NC pins should not be connected to any active signals, VCC or GND.
Non-SERDES Power Supplies		
VCCIOx	—	VCCIO - The power supply pins for I/O bank x. Dedicated pins.
VCC12[1]	—	1.2V supply for configuration logic, PLLs and SERDES Rx, Tx and PLL. All VCC12 pins must be connected. As VCC12 supplies power for analog circuitry, VCC12 should be quiet and isolated from noisy digital board supplies.
VTT_x	—	Termination voltage for bank x. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. VCMT function is not used in the bank. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.
GND	—	GND - Ground. Dedicated pins. All grounds must be electrically connected at the board level.
VCC	—	VCC - The power supply pins for core logic. Dedicated pins (1.2V/ 1.0V).
VCCAUX	—	VCCAUX - Auxiliary power supply pin - powers all differential and referenced input buffers. Dedicated pins (2.5V).
VCCJ	—	VCCJ - The power supply pin for JTAG Test Access Port.
PROBE_VCC	—	VCC signal - Connected to internal VCC node. Can be used for feedback to control an external board power converter. Can be unconnected if not used.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
U18	GND	-		GND	-	
U19	GND	-		GND	-	
U20	GND	-		GND	-	
V11	GND	-		GND	-	
V12	GND	-		GND	-	
V13	GND	-		GND	-	
V14	GND	-		GND	-	
V15	GND	-		GND	-	
V16	GND	-		GND	-	
V17	GND	-		GND	-	
V18	GND	-		GND	-	
V19	GND	-		GND	-	
V20	GND	-		GND	-	
W11	GND	-		GND	-	
W12	GND	-		GND	-	
W13	GND	-		GND	-	
W14	GND	-		GND	-	
W15	GND	-		GND	-	
W16	GND	-		GND	-	
W17	GND	-		GND	-	
W18	GND	-		GND	-	
W19	GND	-		GND	-	
W20	GND	-		GND	-	
Y11	GND	-		GND	-	
Y12	GND	-		GND	-	
Y13	GND	-		GND	-	
Y14	GND	-		GND	-	
Y15	GND	-		GND	-	
Y16	GND	-		GND	-	
Y17	GND	-		GND	-	
Y18	GND	-		GND	-	
Y19	GND	-		GND	-	
Y20	GND	-		GND	-	
H2	VCCIO7	-		VCCIO7	-	
N4	VCCIO7	-		VCCIO7	-	
N6	VCCIO7	-		VCCIO7	-	
J2	VCCIO7	-		VCCIO7	-	
L2	VCCIO7	-		VCCIO7	-	
H4	VCCIO7	-		VCCIO7	-	
AB2	VCCIO6	-		VCCIO6	-	
AD1	VCCIO6	-		VCCIO6	-	
W4	VCCIO6	-		VCCIO6	-	
AA4	VCCIO6	-		VCCIO6	-	
AE7	VCCIO5	-		VCCIO5	-	
AH6	VCCIO5	-		VCCIO5	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y24	PL48C	6		PL61C	6	
Y23	PL48D	6		PL61D	6	
AD29	PL49A	6		PL62A	6	
AD30	PL49B	6		PL62B	6	
AF28	PL49C	6		PL62C	6	
AE28	PL49D	6		PL62D	6	
AC28	PL51A	6		PL65A	6	
AD28	PL51B	6		PL65B	6	
AB26	PL51C	6		PL65C	6	
AC26	PL51D	6	VREF2_6	PL65D	6	VREF2_6
AC32	PL52A	6		PL66A	6	
AD32	PL52B	6		PL66B	6	
AA24	PL52C	6		PL66C	6	
AA23	PL52D	6		PL66D	6	
AE30	PL53A	6		PL67A	6	
AE29	PL53B	6		PL67B	6	
AC25	PL53C	6		PL67C	6	
AB25	PL53D	6		PL67D	6	
AE31	PL55A	6		PL69A	6	
AE32	PL55B	6		PL69B	6	
AE26	PL55C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL69C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AE27	PL55D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL69D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AF32	PL56A	6		PL70A	6	
AF31	PL56B	6		PL70B	6	
AC24	PL56C	6		PL70C	6	
AD25	PL56D	6		PL70D	6	
AG32	PL57A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL71A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AG31	PL57B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL71B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AC23	PL57C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL71C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AD24	PL57D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL71D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AH32	XRES	-		XRES	-	
AH31	TEMP	6		TEMP	6	
AJ32	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AK32	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
AF27	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AG28	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AK31	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AL31	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AE25	PB4C	5		PB4C	5	
AE24	PB4D	5		PB4D	5	
AK30	PB5A	5		PB5A	5	
AL30	PB5B	5		PB5B	5	
AD23	PB5C	5		PB5C	5	
AE23	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AK29	PB7A	5		PB7A	5	
AL29	PB7B	5		PB7B	5	
AF26	PB7C	5		PB7C	5	
AF25	PB7D	5		PB7D	5	
AJ28	PB8A	5		PB8A	5	
AK28	PB8B	5		PB8B	5	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

	LFSC/M40			LFSC/M80		
Ball Number	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C2	VCCJ	-		VCCJ	-	
M9	TDO	-	TDO	TDO	-	TDO
L9	TMS	-		TMS	-	
D1	TCK	-		TCK	-	
C1	TDI	-		TDI	-	
J8	PROGRAMN	1		PROGRAMN	1	
K8	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
B2	CCLK	1		CCLK	1	
H9	RESP_URC	-		RESP_URC	-	
H10	VCC12	-		VCC12	-	
H8	A_REFCLKN_R	-		A_REFCLKN_R	-	
G8	A_REFCLKP_R	-		A_REFCLKP_R	-	
C3	VCC12	-		VCC12	-	
D3	A_VDDIB0_R	-		A_VDDIB0_R	-	
A3	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P
B3	A_HDINN0_R	-	PCS 3E0 CH 0 IN N	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
E5	VCC12	-		VCC12	-	
A4	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P	A_HDOUTP0_R	-	PCS 3E0 CH 0 OUT P
F6	A_VDDOB0_R	-		A_VDDOB0_R	-	
B4	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N
F7	A_VDDOB1_R	-		A_VDDOB1_R	-	
B5	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N
E6	VCC12	-		VCC12	-	
A5	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P
B6	A_HDINN1_R	-	PCS 3E0 CH 1 IN N	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
A6	A_HDINP1_R	-	PCS 3E0 CH 1 IN P	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
C6	VCC12	-		VCC12	-	
D4	A_VDDIB1_R	-		A_VDDIB1_R	-	
C7	VCC12	-		VCC12	-	
D5	A_VDDIB2_R	-		A_VDDIB2_R	-	
A7	A_HDINP2_R	-	PCS 3E0 CH 2 IN P	A_HDINP2_R	-	PCS 3E0 CH 2 IN P
B7	A_HDINN2_R	-	PCS 3E0 CH 2 IN N	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
E7	VCC12	-		VCC12	-	
A8	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
F8	A_VDDOB2_R	-		A_VDDOB2_R	-	
B8	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
F9	A_VDDOB3_R	-		A_VDDOB3_R	-	
B9	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
E8	VCC12	-		VCC12	-	
A9	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
B10	A_HDINN3_R	-	PCS 3E0 CH 3 IN N	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
A10	A_HDINP3_R	-	PCS 3E0 CH 3 IN P	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
C10	VCC12	-		VCC12	-	
D6	A_VDDIB3_R	-		A_VDDIB3_R	-	
G10	VCC12	-		VCC12	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

	LFSC/M40			LFSC/M80		
Ball Number	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
R7	NC	-		PR39D	2	
P7	NC	-		PR39C	2	
N3	NC	-		PR39B	2	
M3	NC	-		PR39A	2	
H1	NC	-		PR26B	2	
G1	NC	-		PR26A	2	
L5	NC	-		PR25B	2	
K5	NC	-		PR25A	2	
G2	NC	-		PR24B	2	
F2	NC	-		PR24A	2	
F1	NC	-		PR22B	2	
E1	NC	-		PR22A	2	
A2	GND	-		GND	-	
A33	GND	-		GND	-	
AA15	GND	-		GND	-	
AA20	GND	-		GND	-	
AA32	GND	-		GND	-	
AA4	GND	-		GND	-	
AB28	GND	-		GND	-	
AB6	GND	-		GND	-	
AC11	GND	-		GND	-	
AC18	GND	-		GND	-	
AC25	GND	-		GND	-	
AD23	GND	-		GND	-	
AD3	GND	-		GND	-	
AD31	GND	-		GND	-	
AE12	GND	-		GND	-	
AE15	GND	-		GND	-	
AE29	GND	-		GND	-	
AE7	GND	-		GND	-	
AE9	GND	-		GND	-	
AF20	GND	-		GND	-	
AF26	GND	-		GND	-	
AG32	GND	-		GND	-	
AG4	GND	-		GND	-	
AH13	GND	-		GND	-	
AH19	GND	-		GND	-	
AH25	GND	-		GND	-	
AH7	GND	-		GND	-	
AJ10	GND	-		GND	-	
AJ16	GND	-		GND	-	
AJ22	GND	-		GND	-	
AJ28	GND	-		GND	-	
AK3	GND	-		GND	-	
AK31	GND	-		GND	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

	LFSC/M40			LFSC/M80		
Ball Number	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB15	VCC12	-		VCC12	-	
AB20	VCC12	-		VCC12	-	
N15	VCC12	-		VCC12	-	
N20	VCC12	-		VCC12	-	
R13	VCC12	-		VCC12	-	
R22	VCC12	-		VCC12	-	
Y13	VCC12	-		VCC12	-	
Y22	VCC12	-		VCC12	-	
AA12	VCCAUX	-		VCCAUX	-	
AA23	VCCAUX	-		VCCAUX	-	
AB12	VCCAUX	-		VCCAUX	-	
AB16	VCCAUX	-		VCCAUX	-	
AB17	VCCAUX	-		VCCAUX	-	
AB18	VCCAUX	-		VCCAUX	-	
AB19	VCCAUX	-		VCCAUX	-	
AB23	VCCAUX	-		VCCAUX	-	
AC12	VCCAUX	-		VCCAUX	-	
AC13	VCCAUX	-		VCCAUX	-	
Y19	GND	-		GND	-	
AC14	VCCAUX	-		VCCAUX	-	
AC17	VCCAUX	-		VCCAUX	-	
AC21	VCCAUX	-		VCCAUX	-	
AC22	VCCAUX	-		VCCAUX	-	
AC23	VCCAUX	-		VCCAUX	-	
M13	VCCAUX	-		VCCAUX	-	
M14	VCCAUX	-		VCCAUX	-	
M18	VCCAUX	-		VCCAUX	-	
M21	VCCAUX	-		VCCAUX	-	
M22	VCCAUX	-		VCCAUX	-	
N12	VCCAUX	-		VCCAUX	-	
N16	VCCAUX	-		VCCAUX	-	
N17	VCCAUX	-		VCCAUX	-	
N18	VCCAUX	-		VCCAUX	-	
N19	VCCAUX	-		VCCAUX	-	
N23	VCCAUX	-		VCCAUX	-	
P12	VCCAUX	-		VCCAUX	-	
P23	VCCAUX	-		VCCAUX	-	
T13	VCCAUX	-		VCCAUX	-	
T22	VCCAUX	-		VCCAUX	-	
U12	VCCAUX	-		VCCAUX	-	
U13	VCCAUX	-		VCCAUX	-	
U22	VCCAUX	-		VCCAUX	-	
V13	VCCAUX	-		VCCAUX	-	
V22	VCCAUX	-		VCCAUX	-	
V23	VCCAUX	-		VCCAUX	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AN8	PB123B	4	
AG11	PB123C	4	
AG10	PB123D	4	
AP7	PB125A	4	
AP6	PB125B	4	
AG13	PB125C	4	
AG12	PB125D	4	
AN7	PB127A	4	
AN6	PB127B	4	
AK9	PB127C	4	
AK8	PB127D	4	
AP5	PB129A	4	
AP4	PB129B	4	
AD11	PB129C	4	
AE11	PB129D	4	
AM7	PB131A	4	
AM6	PB131B	4	
AJ9	PB131C	4	
AJ8	PB131D	4	
AP3	PB133A	4	
AN3	PB133B	4	
AF10	PB133C	4	
AE10	PB133D	4	
AL7	PB135A	4	
AL6	PB135B	4	
AK7	PB135C	4	
AK6	PB135D	4	
AN5	PB138A	4	
AN4	PB138B	4	
AH9	PB138C	4	VREF1_4
AH8	PB138D	4	
AM3	PB139A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AM4	PB139B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AG9	PB139C	4	
AG8	PB139D	4	
AN2	PB141A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AM2	PB141B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ6	PB141C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH6	PB141D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF7	PROBE_VCC	-	
AF8	PROBE_GND	-	
AG7	PR117D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AG6	PR117C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
R12	VTT_2	2	
T12	VTT_2	2	
AB11	VTT_3	3	
W12	VTT_3	3	
Y12	VTT_3	3	
AC15	VTT_4	4	
AC16	VTT_4	4	
AD13	VTT_4	4	
AC19	VTT_5	5	
AC20	VTT_5	5	
AD22	VTT_5	5	
AB24	VTT_6	6	
W23	VTT_6	6	
Y23	VTT_6	6	
N24	VTT_7	7	
R23	VTT_7	7	
T23	VTT_7	7	
M12	VDDAX25_R	-	
M23	VDDAX25_L	-	
Y16	GND	-	
Y14	GND	-	
N21	VCC12	-	
P22	VCC12	-	
AA22	VCC12	-	
AB21	VCC12	-	
AB14	VCC12	-	
AA13	VCC12	-	
P13	VCC12	-	
N14	VCC12	-	
G26	NC	-	
G9	NC	-	
J12	NC	-	
H12	NC	-	
H23	NC	-	
J23	NC	-	

1. Differential pair grouping within a PCI is A (True) and B (complement) and C (True) and D (Complement).
2. The LatticeSC/M115 in an 1152-pin package supports a 32-bit MPI interface.

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80 Ball Function	LFSC/M80 VCCIO Bank	LFSC/M80 Dual Function	LFSC/M115 Ball Function	LFSC/M115 VCCIO Bank	LFSC/M115 Dual Function
BB12	PB88B	4		PB102B	4	
AM17	PB88C	4		PB102C	4	
AL17	PB88D	4		PB102D	4	
AW14	PB89A	4		PB103A	4	
AW13	PB89B	4		PB103B	4	
AP16	PB89C	4		PB103C	4	
AN16	PB89D	4		PB103D	4	
BA13	PB91A	4		PB105A	4	
BA12	PB91B	4		PB105B	4	
AU13	PB91C	4		PB105C	4	
AU12	PB91D	4		PB105D	4	
BB11	PB92A	4		PB106A	4	
BB10	PB92B	4		PB106B	4	
AP15	PB92C	4		PB106C	4	
AN15	PB92D	4		PB106D	4	
AV13	PB93A	4		PB107A	4	
AV12	PB93B	4		PB107B	4	
AT13	PB93C	4		PB107C	4	
AT12	PB93D	4		PB107D	4	
BA11	PB95A	4		PB109A	4	
BA10	PB95B	4		PB109B	4	
AR13	PB95C	4		PB109C	4	
AR12	PB95D	4		PB109D	4	
AY11	PB96A	4		PB110A	4	
AY10	PB96B	4		PB110B	4	
AP14	PB96C	4		PB110C	4	
AN14	PB96D	4		PB110D	4	
BB9	PB97A	4		PB111A	4	
BB8	PB97B	4		PB111B	4	
AU11	PB97C	4		PB111C	4	
AU10	PB97D	4		PB111D	4	
AW11	PB99A	4		PB113A	4	
AW10	PB99B	4		PB113B	4	
AJ16	PB99C	4		PB113C	4	
AJ17	PB99D	4		PB113D	4	
BA9	PB100A	4		PB114A	4	
BA8	PB100B	4		PB114B	4	
AM15	PB100C	4		PB114C	4	
AL15	PB100D	4		PB114D	4	
AV11	PB101A	4		PB115A	4	
AV10	PB101B	4		PB115B	4	
AP13	PB101C	4		PB115C	4	
AP12	PB101D	4		PB115D	4	
BB7	PB103A	4		PB117A	4	
BB6	PB103B	4		PB117B	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

	LFSC/M80			LFSC/M115		
Ball Number	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D32	C_HDINP1_L	-	PCS 362 CH 1 IN P	C_HDINP1_L	-	PCS 362 CH 1 IN P
E32	C_HDINN1_L	-	PCS 362 CH 1 IN N	C_HDINN1_L	-	PCS 362 CH 1 IN N
B31	C_HDOUTP1_L	-	PCS 362 CH 1 OUT P	C_HDOUTP1_L	-	PCS 362 CH 1 OUT P
K32	VCC12	-		VCC12	-	
A31	C_HDOUTN1_L	-	PCS 362 CH 1 OUT N	C_HDOUTN1_L	-	PCS 362 CH 1 OUT N
L32	C_VDDOB1_L	-		C_VDDOB1_L	-	
A32	C_HDOUTN0_L	-	PCS 362 CH 0 OUT N	C_HDOUTN0_L	-	PCS 362 CH 0 OUT N
M31	C_VDDOB0_L	-		C_VDDOB0_L	-	
B32	C_HDOUTP0_L	-	PCS 362 CH 0 OUT P	C_HDOUTP0_L	-	PCS 362 CH 0 OUT P
H37	VCC12	-		VCC12	-	
E33	C_HDINN0_L	-	PCS 362 CH 0 IN N	C_HDINN0_L	-	PCS 362 CH 0 IN N
D33	C_HDINP0_L	-	PCS 362 CH 0 IN P	C_HDINP0_L	-	PCS 362 CH 0 IN P
G31	C_VDDIB0_L	-		C_VDDIB0_L	-	
J29	VCC12	-		VCC12	-	
L29	B_REFCLKP_L	-		B_REFCLKP_L	-	
M29	B_REFCLKN_L	-		B_REFCLKN_L	-	
J31	VCC12	-		VCC12	-	
H31	B_VDDIB3_L	-		B_VDDIB3_L	-	
J30	VCC12	-		VCC12	-	
D34	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
E34	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
B33	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
H38	VCC12	-		VCC12	-	
A33	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
C38	B_VDDOB3_L	-		B_VDDOB3_L	-	
A34	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
L31	B_VDDOB2_L	-		B_VDDOB2_L	-	
B34	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
G38	VCC12	-		VCC12	-	
E35	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
D35	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
H32	B_VDDIB2_L	-		B_VDDIB2_L	-	
K29	VCC12	-		VCC12	-	
K30	B_VDDIB1_L	-		B_VDDIB1_L	-	
F33	VCC12	-		VCC12	-	
D36	B_HDINP1_L	-	PCS 361 CH 1 IN P	B_HDINP1_L	-	PCS 361 CH 1 IN P
E36	B_HDINN1_L	-	PCS 361 CH 1 IN N	B_HDINN1_L	-	PCS 361 CH 1 IN N
B35	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
L34	VCC12	-		VCC12	-	
A35	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
K35	B_VDDOB1_L	-		B_VDDOB1_L	-	
A36	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
G39	B_VDDOB0_L	-		B_VDDOB0_L	-	
B36	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
J35	VCC12	-		VCC12	-	

Conventional Packaging

Commercial

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-7F256C	-7	fpBGA	256	COM	15.2
LFSC3GA15E-6F256C	-6	fpBGA	256	COM	15.2
LFSC3GA15E-5F256C	-5	fpBGA	256	COM	15.2
LFSC3GA15E-7F900C	-7	fpBGA	900	COM	15.2
LFSC3GA15E-6F900C	-6	fpBGA	900	COM	15.2
LFSC3GA15E-5F900C	-5	fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-7F256C	-7	fpBGA	256	COM	15.2
LFSCM3GA15EP1-6F256C	-6	fpBGA	256	COM	15.2
LFSCM3GA15EP1-5F256C	-5	fpBGA	256	COM	15.2
LFSCM3GA15EP1-7F900C	-7	fpBGA	900	COM	15.2
LFSCM3GA15EP1-6F900C	-6	fpBGA	900	COM	15.2
LFSCM3GA15EP1-5F900C	-5	fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-7F900C	-7	fpBGA	900	COM	25.4
LFSC3GA25E-6F900C	-6	fpBGA	900	COM	25.4
LFSC3GA25E-5F900C	-5	fpBGA	900	COM	25.4
LFSC3GA25E-7FF1020C[1]	-7	Organic fcBGA	1020	COM	25.4
LFSC3GA25E-6FF1020C[1]	-6	Organic fcBGA	1020	COM	25.4
LFSC3GA25E-5FF1020C[1]	-5	Organic fcBGA	1020	COM	25.4
LFSC3GA25E-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-7F900C	-7	fpBGA	900	COM	25.4
LFSCM3GA25EP1-6F900C	-6	fpBGA	900	COM	25.4
LFSCM3GA25EP1-5F900C	-5	fpBGA	900	COM	25.4
LFSCM3GA25EP1-7FF1020C[1]	-7	Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-6FF1020C[1]	-6	Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-5FF1020C[1]	-5	Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-7FFA1020C	-7	Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-6FFA1020C	-6	Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-5FFA1020C	-5	Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FCN1152C[1]	-6	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FCN1152C[1]	-5	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FCN1704C[1]	-6	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FCN1704C[1]	-5	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.