Lattice Semiconductor Corporation - LFSCM3GA25EP1-7FFAN1020C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6250
Number of Logic Elements/Cells	25000
Total RAM Bits	1966080
Number of I/O	476
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-OFcBGA Rev 2 (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga25ep1-7ffan1020c

3. **Bottom Side (Banks 4 and 5)**
   These buffers can support LVCMOS standards up to 3.3V, including PCI33, PCI-X33 and SSTL-33. Differential receivers are provided on all PIO pairs but true HLVDS and RSDS differential drivers are not available. Adaptive input logic is available on PIOs A or C.

Table 2-8 lists the standards supported by each side.

Table 2-8. I/O Standards Supported by Different Banks

Description	Top Side Banks 1	Right Side Banks 2-3	Bottom Side Banks 4-5	Left Side Banks 6-7
I/O Buffer Type	Single-ended, Differential Receiver	Single-ended, Differential Receiver and Driver	Single-ended, Differential Receiver	Single-ended, Differential Receiver and Driver
Output Standards Supported	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II SSTL33_ I, II HSTL15_I, II, III[1], IV[1] HSTL18_I, II,III[1], IV[1] SSTL18D_I, II SSTL25D_I, II SSTL33D_I, II HSTL15D_I, II HSTL18D_I, II PCI33 PCIX15 PCIX33 AGP1X33 AGP2X33 MLVDS/BLVDS GTL[2], GTL+[2]	LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II HSTL15_I,III HSTL18_I,II,III PCIX15 SSTL18D_I, II SSTL25D_I, II HSTL15D_I, II HSTL18D_I, II LVDS/RSDS Mini-LVDS MLVDS/BLVDS GTL[2], GTL+[2]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II SSTL33_ I, II HSTL15_I, II, III[1], IV[1] HSTL18_I, II,III[1], IV[1] SSTL18D_I, II SSTL25D_I, II SSTL33D_I, II HSTL15D_I, II HSTL18D_I, II PCI33 PCIX15 PCIX33 AGP1X33 AGP2X33 MLVDS/BLVDS GTL[2], GTL+[2]	LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18_I, II SSTL25_ I, II HSTL15_I,III HSTL18_I,II,III PCIX15 SSTL18D_I, II SSTL25D_I, II HSTL15D_I, II HSTL18D_I, II LVDS/RSDS Mini-LVDS MLVDS/BLVDS GTL[2], GTL+[2]
Input Standards Supported	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential
Clock Inputs	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential	Single-ended, Differential
Differential Output Support via Emulation	LVDS/MLVDS/BLVDS/ LVPECL	MLVDS/BLVDS/ LVPECL	LVDS/MLVDS/BLVDS/ LVPECL	MLVDS/BLVDS/ LVPECL
AIL Support	No	Yes	Yes	Yes

1. Input only.
2. Input only. Outputs supported by bussing multiple outputs together.

Supported Standards

The LatticeSC PURESPEED I/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 12, 15, 18, 25 and 33 standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, termination resistance, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL, HSTL, GTL (input only), GTL+ (input only), PCI33, PCIX33, PCIX15, AGP-1X33 and AGP-2X33. Differential standards supported include LVDS, RSDS, BLVDS, MLVDS, LVPECL, differential SSTL and differential HSTL. Tables 12 and 13 show the I/O standards (together with their supply and reference voltages) supported by the LatticeSC devices. The tables also provide the available internal termination schemes. For further information on utilizing the PURESPEED I/O buffer to support a variety of standards please see details of additional technical documentation at the end of this data sheet.

Switching Characteristics

All devices are 100% functionally tested. Listed below are representative values of internal and external timing parameters. For more specific, more precise, and worst-case guaranteed data at a particular temperature and voltage, use the values reported by the static timing analyzer in the ispLEVER design tool from Lattice and back-annotate to the simulation net list.

LatticeSC/M Internal Timing Parameters[1] (Continued)

Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

Parameter	Symbol	Description	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
EBR Timing									
t_{CO_EBR}	CK_Q_DEL	Clock (Read) to output from Address or Data	—	1.900	—	2.116	—	2.335	ns
t_{COO_EBR}	CK_Q_DEL	Clock (Write) to output from EBR output Register	0.390	—	0.444	—	0.498	—	ns
t_{SUDATA_EBR}	D_CK_SET	Setup Data to EBR Memory (Write clk)	-0.173	—	-0.192	—	-0.210	—	ns
t_{HDATA_EBR}	D_CK_HLD	Hold Data to EBR Memory (Write clk)	0.276	—	0.305	—	0.335	—	ns
t_{SUADDR_EBR}	A_CK_SET	Setup Address to EBR Memory (Write clk)	-0.165	—	-0.182	—	-0.200	—	ns
t_{HADDR_EBR}	A_CK_HLD	Hold Address to EBR Memory (Write clk)	0.269	—	0.298	—	0.327	—	ns
t_{SUWREN_EBR}	CE_CK_SET	Setup Write/Read Enable to EBR Memory (Write/Read clk)	0.225	—	0.226	—	0.226	—	ns
t_{HWREN_EBR}	CE_CK_HLD	Hold Write/Read Enable to EBR Memory (write/read clk)	0.073	—	0.095	—	0.116	—	ns
t_{SUCE_EBR}	CS_CK_SET	Clock Enable Setup Time to EBR Output Register (Read clk)	0.261	—	0.269	—	0.276	—	ns
t_{HCE_EBR}	CS_CK_HLD	Clock Enable Hold Time to EBR Output Register (Read clk)	0.023	—	0.039	—	0.055	—	ns
t_{RSTO_EBR}	RESET_Q_DEL	Reset To Output Delay Time from EBR Output Register (asynchronous)	—	0.589	—	0.673	—	0.757	ns
Cycle Boosting Timing									
t_{DEL1}	DEL1	Cycle boosting delay 1 applies to PIO, PFU, EBR	—	0.480	—	0.524	—	0.570	ns
t_{DEL2}	DEL2	Cycle boosting delay 2 applies to PIO, PFU, EBR	—	0.922	—	1.005	—	1.090	ns
t_{DEL3}	DEL3	Cycle boosting delay 3 applies to PIO, PFU, EBR	—	1.366	—	1.488	—	1.612	ns

1. Complete timing parameters for a user design will be incorporated when running ispLEVER. This is a sampling of the key timing parameters.

Input Delay Block/AIL Timing

Parameter	Description	Min.	Typ.	Max.	Units
t_{FDEL}	Fine delay time	35	45	80	ps
t_{CDEL}	Coarse delay time	1120	1440	2560	ps
jt_{AIL}	AIL jitter tolerance	1- ((N^1 * t_{FDEL}) / (Clock Period))			UI

1. N = number of fine delays used in a particular AIL setting

GSR Timing

Parameter	Description	VCC	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{SYNC\_GSR\_MAX}$	Maximum operating frequency for synchronous GSR	1.14V	—	438	—	417	—	398	MHz
		0.95V	—	378	—	355	—	337	MHz
$t_{ASYNC\_GSR\_MPW}$	Minimum pulse width of asynchronous input	—	—	—	—	—	3.3	—	ns

Note: Synchronous GSR goes out of reset in two cycles from the clock edge where the setup time of the FF was met.

Internal System Bus Timing

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HCLK}	Maximum operating frequency for internal system bus HCLK.	—	200	—	200	—	200	MHz

Note: There is no minimum frequency. If HCLK is sourced from the embedded oscillator, the minimum frequency limitation of the oscillator/ divider is about 0.3 MHz. Refer to the osciallator data for missing configuration modes.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
E19	NC	-		NC	-	
G21	NC	-		NC	-	
G20	NC	-		NC	-	
G19	NC	-		NC	-	
F9	NC	-		NC	-	
A11	NC	-		NC	-	
G7	NC	-		NC	-	
AH9	NC	-		NC	-	
H8	VCC12	-		VCC12	-	
T8	VCC12	-		VCC12	-	
AB9	VCC12	-		VCC12	-	
AC8	VCC12	-		VCC12	-	
AB22	VCC12	-		VCC12	-	
AC23	VCC12	-		VCC12	-	
R23	VCC12	-		VCC12	-	
H23	VCC12	-		VCC12	-	
H15	VCC12	-		VCC12	-	
L24	VTT_2	2		VTT_2	2	
T23	VTT_2	2		VTT_2	2	
AC24	VTT_3	3		VTT_3	3	
T25	VTT_3	3		VTT_3	3	
W25	VTT_3	3		VTT_3	3	
AD24	VTT_4	4		VTT_4	4	
AE17	VTT_4	4		VTT_4	4	
AE18	VTT_4	4		VTT_4	4	
AC15	VTT_5	5		VTT_5	5	
AD16	VTT_5	5		VTT_5	5	
AE9	VTT_5	5		VTT_5	5	
AA6	VTT_6	6		VTT_6	6	
T7	VTT_6	6		VTT_6	6	
W6	VTT_6	6		VTT_6	6	
L7	VTT_7	7		VTT_7	7	
P7	VTT_7	7		VTT_7	7	
AA10	VCC	-		VCC	-	
AA11	VCC	-		VCC	-	
AA12	VCC	-		VCC	-	
AA13	VCC	-		VCC	-	
AA14	VCC	-		VCC	-	
AA17	VCC	-		VCC	-	
AA18	VCC	-		VCC	-	
AA19	VCC	-		VCC	-	
AA20	VCC	-		VCC	-	
AA21	VCC	-		VCC	-	
AA22	VCC	-		VCC	-	
AA9	VCC	-		VCC	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
B29	NC	-		NC	-	

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M15 and LatticeSC/M25 in a 900-pin package supports a 16-bit MPI interface.

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P32	PL30A	6		PL39A	6	
P31	PL30B	6		PL39B	6	
R28	PL30C	6	PCLKT6_3	PL39C	6	PCLKT6_3
T28	PL30D	6	PCLKC6_3	PL39D	6	PCLKC6_3
R30	PL31A	6		PL40A	6	
R29	PL31B	6		PL40B	6	
T25	PL31C	6	PCLKT6_2	PL40C	6	PCLKT6_2
T26	PL31D	6	PCLKC6_2	PL40D	6	PCLKC6_2
R31	PL34A	6		PL43A	6	
R32	PL34B	6		PL43B	6	
U23	PL34C	6	VREF1_6	PL43C	6	VREF1_6
U24	PL34D	6		PL43D	6	
T31	PL35A	6		PL44A	6	
T32	PL35B	6		PL44B	6	
T27	PL35C	6		PL44C	6	
U28	PL35D	6		PL44D	6	
U32	PL36A	6		PL45A	6	
U31	PL36B	6		PL45B	6	
U26	PL36C	6		PL45C	6	
U25	PL36D	6		PL45D	6	
V32	PL38A	6		PL47A	6	
V31	PL38B	6		PL47B	6	
V24	PL38C	6		PL47C	6	
V23	PL38D	6		PL47D	6	
V29	PL39A	6		PL48A	6	
V30	PL39B	6		PL48B	6	
U27	PL39C	6		PL48C	6	
V28	PL39D	6		PL48D	6	
W30	PL40A	6		PL49A	6	
W29	PL40B	6		PL49B	6	
V25	PL40C	6		PL49C	6	
W26	PL40D	6		PL49D	6	
W31	PL42A	6		PL51A	6	
Y31	PL42B	6		PL51B	6	
W27	PL42C	6		PL51C	6	
Y27	PL42D	6	DIFFR_6	PL51D	6	DIFFR_6
W28	PL43A	6		PL52A	6	
Y28	PL43B	6		PL52B	6	
Y26	PL43C	6		PL52C	6	
W25	PL43D	6		PL52D	6	
W32	PL44A	6		PL53A	6	
Y32	PL44B	6		PL53B	6	
AB28	PL44C	6		PL53C	6	
AA28	PL44D	6		PL53D	6	
AB32	PL47A	6		PL60A	6	
AA32	PL47B	6		PL60B	6	
AB27	PL47C	6		PL60C	6	
AC27	PL47D	6		PL60D	6	
AD31	PL48A	6		PL61A	6	
AC31	PL48B	6		PL61B	6	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y24	PL48C	6		PL61C	6	
Y23	PL48D	6		PL61D	6	
AD29	PL49A	6		PL62A	6	
AD30	PL49B	6		PL62B	6	
AF28	PL49C	6		PL62C	6	
AE28	PL49D	6		PL62D	6	
AC28	PL51A	6		PL65A	6	
AD28	PL51B	6		PL65B	6	
AB26	PL51C	6		PL65C	6	
AC26	PL51D	6	VREF2_6	PL65D	6	VREF2_6
AC32	PL52A	6		PL66A	6	
AD32	PL52B	6		PL66B	6	
AA24	PL52C	6		PL66C	6	
AA23	PL52D	6		PL66D	6	
AE30	PL53A	6		PL67A	6	
AE29	PL53B	6		PL67B	6	
AC25	PL53C	6		PL67C	6	
AB25	PL53D	6		PL67D	6	
AE31	PL55A	6		PL69A	6	
AE32	PL55B	6		PL69B	6	
AE26	PL55C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL69C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AE27	PL55D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL69D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AF32	PL56A	6		PL70A	6	
AF31	PL56B	6		PL70B	6	
AC24	PL56C	6		PL70C	6	
AD25	PL56D	6		PL70D	6	
AG32	PL57A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL71A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AG31	PL57B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL71B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AC23	PL57C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL71C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AD24	PL57D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL71D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AH32	XRES	-		XRES	-	
AH31	TEMP	6		TEMP	6	
AJ32	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AK32	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
AF27	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AG28	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AK31	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AL31	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AE25	PB4C	5		PB4C	5	
AE24	PB4D	5		PB4D	5	
AK30	PB5A	5		PB5A	5	
AL30	PB5B	5		PB5B	5	
AD23	PB5C	5		PB5C	5	
AE23	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AK29	PB7A	5		PB7A	5	
AL29	PB7B	5		PB7B	5	
AF26	PB7C	5		PB7C	5	
AF25	PB7D	5		PB7D	5	
AJ28	PB8A	5		PB8A	5	
AK28	PB8B	5		PB8B	5	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
B30	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
D30	A_VDDOB0_L	-		A_VDDOB0_L	-	
A30	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
C31	A_HDINN0_L	-	PCS 360 CH 0 IN N	A_HDINN0_L	-	PCS 360 CH 0 IN N
C32	A_HDINP0_L	-	PCS 360 CH 0 IN P	A_HDINP0_L	-	PCS 360 CH 0 IN P
B31	A_VDDIB0_L	-		A_VDDIB0_L	-	
AL25	NC	-		PB26A	5	
AL24	NC	-		PB26B	5	
AG27	NC	-		PB26C	5	
AH27	NC	-		PB26D	5	
AM25	NC	-		PB27A	5	
AM24	NC	-		PB27B	5	
AL9	NC	-		PB62A	4	
AL8	NC	-		PB62B	4	
AK9	NC	-		PB63A	4	
AJ9	NC	-		PB63B	4	
AG10	NC	-		PB63C	4	
AG11	NC	-		PB63D	4	
J30	NC	-		PL26A	7	
H30	NC	-		PL26B	7	
M28	NC	-		PL26C	7	
N28	NC	-		PL26D	7	
J32	NC	-		PL27A	7	
J31	NC	-		PL27B	7	
N26	NC	-		PL27C	7	
N27	NC	-		PL27D	7	
K31	NC	-		PL29A	7	
K32	NC	-		PL29B	7	
P25	NC	-		PL29C	7	
P26	NC	-		PL29D	7	
L27	NC	-		PL22C	7	
L28	NC	-		PL22D	7	
M29	NC	-		PL30A	7	
L29	NC	-		PL30B	7	
M30	NC	-		PL31A	7	
L30	NC	-		PL31B	7	
L31	NC	-		PL34A	7	
M31	NC	-		PL34B	7	
AA29	NC	-		PL56A	6	
AA30	NC	-		PL56B	6	
AB31	NC	-		PL57A	6	
AA31	NC	-		PL57B	6	
AG30	NC	-		PL57C	6	
AG29	NC	-		PL57D	6	
AB29	NC	-		PL58A	6	
AB30	NC	-		PL58B	6	
Y25	NC	-		PL58C	6	
AA25	NC	-		PL58D	6	
AA8	NC	-		PR58D	3	
Y8	NC	-		PR58C	3	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
B1	GND	-		GND	-	
B32	GND	-		GND	-	
C11	GND	-		GND	-	
C12	GND	-		GND	-	
C16	GND	-		GND	-	
C21	GND	-		GND	-	
C22	GND	-		GND	-	
C24	GND	-		GND	-	
C25	GND	-		GND	-	
C26	GND	-		GND	-	
C27	GND	-		GND	-	
C29	GND	-		GND	-	
C3	GND	-		GND	-	
C30	GND	-		GND	-	
C4	GND	-		GND	-	
C6	GND	-		GND	-	
C7	GND	-		GND	-	
C8	GND	-		GND	-	
C9	GND	-		GND	-	
D17	GND	-		GND	-	
F18	GND	-		GND	-	
F3	GND	-		GND	-	
F30	GND	-		GND	-	
F9	GND	-		GND	-	
G15	GND	-		GND	-	
G24	GND	-		GND	-	
G29	GND	-		GND	-	
G3	GND	-		GND	-	
J14	GND	-		GND	-	
J22	GND	-		GND	-	
J26	GND	-		GND	-	
J6	GND	-		GND	-	
K11	GND	-		GND	-	
K19	GND	-		GND	-	
K30	GND	-		GND	-	
K4	GND	-		GND	-	
L23	GND	-		GND	-	
L9	GND	-		GND	-	
M13	GND	-		GND	-	
M15	GND	-		GND	-	
M18	GND	-		GND	-	
M20	GND	-		GND	-	
M27	GND	-		GND	-	
M7	GND	-		GND	-	
N12	GND	-		GND	-	
N14	GND	-		GND	-	
N19	GND	-		GND	-	
N21	GND	-		GND	-	
N29	GND	-		GND	-	
N3	GND	-		GND	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P10	GND	-		GND	-	
P13	GND	-		GND	-	
P15	GND	-		GND	-	
P18	GND	-		GND	-	
P20	GND	-		GND	-	
P24	GND	-		GND	-	
R12	GND	-		GND	-	
R14	GND	-		GND	-	
R16	GND	-		GND	-	
R17	GND	-		GND	-	
R19	GND	-		GND	-	
R21	GND	-		GND	-	
R26	GND	-		GND	-	
R6	GND	-		GND	-	
T15	GND	-		GND	-	
T18	GND	-		GND	-	
T30	GND	-		GND	-	
T4	GND	-		GND	-	
U15	GND	-		GND	-	
U18	GND	-		GND	-	
U29	GND	-		GND	-	
U3	GND	-		GND	-	
V12	GND	-		GND	-	
V14	GND	-		GND	-	
V16	GND	-		GND	-	
V17	GND	-		GND	-	
V19	GND	-		GND	-	
V21	GND	-		GND	-	
V27	GND	-		GND	-	
V7	GND	-		GND	-	
W13	GND	-		GND	-	
W15	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W23	GND	-		GND	-	
W9	GND	-		GND	-	
Y12	GND	-		GND	-	
Y14	GND	-		GND	-	
Y19	GND	-		GND	-	
Y21	GND	-		GND	-	
Y30	GND	-		GND	-	
Y4	GND	-		GND	-	
N13	VCC	-		VCC	-	
N15	VCC	-		VCC	-	
N16	VCC	-		VCC	-	
N17	VCC	-		VCC	-	
N18	VCC	-		VCC	-	
N20	VCC	-		VCC	-	
P14	VCC	-		VCC	-	
P16	VCC	-		VCC	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G27	A_REFCLKP_L	-		A_REFCLKP_L	-	
H27	A_REFCLKN_L	-		A_REFCLKN_L	-	
H25	VCC12	-		VCC12	-	
H26	RESP_ULC	-		RESP_ULC	-	
B33	RESETN	1		RESETN	1	
C34	TSALLN	1		TSALLN	1	
D34	DONE	1		DONE	1	
C33	INITN	1		INITN	1	
J27	M0	1		M0	1	
K27	M1	1		M1	1	
M26	M2	1		M2	1	
L26	M3	1		M3	1	
F30	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
G30	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
H28	PL16C	7		PL16C	7	
J28	PL16D	7		PL16D	7	
F31	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
G31	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N25	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P25	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
D33	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
E33	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
H29	PL18C	7		PL18C	7	
J29	PL18D	7	VREF2_7	PL18D	7	VREF2_7
F32	PL21A	7		PL20A	7	
G32	PL21B	7		PL20B	7	
P26	PL21C	7		PL20C	7	
N26	PL21D	7		PL20D	7	
H30	PL22A	7		PL21A	7	
J30	PL22B	7		PL21B	7	
L28	PL22C	7		PL21C	7	
M28	PL22D	7		PL21D	7	
J31	PL23A	7		PL29A	7	
K31	PL23B	7		PL29B	7	
L27	PL23C	7	VREF1_7	PL29C	7	VREF1_7
M27	PL23D	7	DIFFR_7	PL29D	7	DIFFR_7
J32	PL25A	7		PL31A	7	
K32	PL25B	7		PL31B	7	
L29	PL25C	7		PL31C	7	
M29	PL25D	7		PL31D	7	
H33	PL26A	7		PL33A	7	
J33	PL26B	7		PL33B	7	
N27	PL26C	7		PL33C	7	
P27	PL26D	7		PL33D	7	
K33	PL27A	7		PL35A	7	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L1	PR31A	2		PR43A	2	
T10	PR30D	2		PR42D	2	
U10	PR30C	2		PR42C	2	
N2	PR30B	2		PR42B	2	
M2	PR30A	2		PR42A	2	
R11	PR29D	2		PR37D	2	
P11	PR29C	2		PR37C	2	
N4	PR29B	2		PR37B	2	
M4	PR29A	2		PR37A	2	
N5	PR27D	2		PR35D	2	
M5	PR27C	2		PR35C	2	
L2	PR27B	2		PR35B	2	
K2	PR27A	2		PR35A	2	
P8	PR26D	2		PR33D	2	
N8	PR26C	2		PR33C	2	
J2	PR26B	2		PR33B	2	
H2	PR26A	2		PR33A	2	
M6	PR25D	2		PR31D	2	
L6	PR25C	2		PR31C	2	
K3	PR25B	2		PR31B	2	
J3	PR25A	2		PR31A	2	
M8	PR23D	2	DIFFR_2	PR29D	2	DIFFR_2
L8	PR23C	2	VREF1_2	PR29C	2	VREF1_2
K4	PR23B	2		PR29B	2	
J4	PR23A	2		PR29A	2	
M7	PR22D	2		PR21D	2	
L7	PR22C	2		PR21C	2	
J5	PR22B	2		PR21B	2	
H5	PR22A	2		PR21A	2	
N9	PR21D	2		PR20D	2	
P9	PR21C	2		PR20C	2	
G3	PR21B	2		PR20B	2	
F3	PR21A	2		PR20A	2	
J6	PR18D	2	VREF2_2	PR18D	2	VREF2_2
H6	PR18C	2		PR18C	2	
E2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
D2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
G4	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
F4	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
J7	PR16D	2		PR16D	2	
H7	PR16C	2		PR16C	2	
G5	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
F5	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D7	B_VDDIB0_R	-		B_VDDIB0_R	-	
E10	B_HDINP0_R	-	PCS 3E1 CH 0 IN P	B_HDINP0_R	-	PCS 3E1 CH 0 IN P
F10	B_HDINN0_R	-	PCS 3E1 CH 0 IN N	B_HDINN0_R	-	PCS 3E1 CH 0 IN N
K10	VCC12	-		VCC12	-	
A11	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P
D10	B_VDDOB0_R	-		B_VDDOB0_R	-	
B11	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N
D11	B_VDDOB1_R	-		B_VDDOB1_R	-	
B12	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N
L10	VCC12	-		VCC12	-	
A12	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P
F11	B_HDINN1_R	-	PCS 3E1 CH 1 IN N	B_HDINN1_R	-	PCS 3E1 CH 1 IN N
E11	B_HDINP1_R	-	PCS 3E1 CH 1 IN P	B_HDINP1_R	-	PCS 3E1 CH 1 IN P
G11	VCC12	-		VCC12	-	
D8	B_VDDIB1_R	-		B_VDDIB1_R	-	
G12	VCC12	-		VCC12	-	
D9	B_VDDIB2_R	-		B_VDDIB2_R	-	
E12	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
F12	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
K11	VCC12	-		VCC12	-	
A13	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D12	B_VDDOB2_R	-		B_VDDOB2_R	-	
B13	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D13	B_VDDOB3_R	-		B_VDDOB3_R	-	
B14	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
L11	VCC12	-		VCC12	-	
A14	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
F13	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
E13	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
G13	VCC12	-		VCC12	-	
E9	B_VDDIB3_R	-		B_VDDIB3_R	-	
L13	VCC12	-		VCC12	-	
J11	B_REFCLKN_R	-		B_REFCLKN_R	-	
H11	B_REFCLKP_R	-		B_REFCLKP_R	-	
M15	PT61D	1	HDC/SI	PT77D	1	HDC/SI
M16	PT61C	1	LDCN/SCS	PT77C	1	LDCN/SCS
F14	PT59B	1	D8/MPI_DATA8	PT77B	1	D8/MPI_DATA8
G14	PT59A	1	CS1/MPI_CS1	PT77A	1	CS1/MPI_CS1
L15	PT58D	1	D9/MPI_DATA9	PT75D	1	D9/MPI_DATA9
L14	PT58C	1	D10/MPI_DATA10	PT75C	1	D10/MPI_DATA10
D14	PT57B	1	CS0N/MPI_CS0N	PT75B	1	CS0N/MPI_CS0N
E14	PT57A	1	RDN/MPI_STRB_N	PT75A	1	RDN/MPI_STRB_N
L16	PT55D	1	WRN/MPI_WR_N	PT74D	1	WRN/MPI_WR_N
K16	PT55C	1	D7/MPI_DATA7	PT74C	1	D7/MPI_DATA7
G15	PT55B	1	D6/MPI_DATA6	PT74B	1	D6/MPI_DATA6

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AN8	PB123B	4	
AG11	PB123C	4	
AG10	PB123D	4	
AP7	PB125A	4	
AP6	PB125B	4	
AG13	PB125C	4	
AG12	PB125D	4	
AN7	PB127A	4	
AN6	PB127B	4	
AK9	PB127C	4	
AK8	PB127D	4	
AP5	PB129A	4	
AP4	PB129B	4	
AD11	PB129C	4	
AE11	PB129D	4	
AM7	PB131A	4	
AM6	PB131B	4	
AJ9	PB131C	4	
AJ8	PB131D	4	
AP3	PB133A	4	
AN3	PB133B	4	
AF10	PB133C	4	
AE10	PB133D	4	
AL7	PB135A	4	
AL6	PB135B	4	
AK7	PB135C	4	
AK6	PB135D	4	
AN5	PB138A	4	
AN4	PB138B	4	
AH9	PB138C	4	VREF1_4
AH8	PB138D	4	
AM3	PB139A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AM4	PB139B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AG9	PB139C	4	
AG8	PB139D	4	
AN2	PB141A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AM2	PB141B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ6	PB141C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH6	PB141D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF7	PROBE_VCC	-	
AF8	PROBE_GND	-	
AG7	PR117D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AG6	PR117C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P38	PL26B	7		PL40B	7	
N35	PL26C	7		PL40C	7	
N36	PL26D	7		PL40D	7	
N39	PL29A	7		PL43A	7	
P39	PL29B	7		PL43B	7	
R34	PL29C	7	VREF1_7	PL43C	7	VREF1_7
T34	PL29D	7	DIFFR_7	PL43D	7	DIFFR_7
L41	PL30A	7		PL44A	7	
M41	PL30B	7		PL44B	7	
W29	PL30C	7		PL44C	7	
Y29	PL30D	7		PL44D	7	
L42	PL31A	7		PL45A	7	
M42	PL31B	7		PL45B	7	
U32	PL31C	7		PL45C	7	
V32	PL31D	7		PL45D	7	
R37	PL33A	7		PL47A	7	
T37	PL33B	7		PL47B	7	
M36	PL33C	7		PL47C	7	
M37	PL33D	7		PL47D	7	
P40	PL34A	7		PL48A	7	
N40	PL34B	7		PL48B	7	
R35	PL34C	7		PL48C	7	
T35	PL34D	7		PL48D	7	
N41	PL35A	7		PL49A	7	
P41	PL35B	7		PL49B	7	
V33	PL35C	7		PL49C	7	
U33	PL35D	7		PL49D	7	
R38	PL37A	7		PL51A	7	
T38	PL37B	7		PL51B	7	
R36	PL37C	7		PL51C	7	
T36	PL37D	7		PL51D	7	
N42	PL38A	7		PL52A	7	
P42	PL38B	7		PL52B	7	
Y31	PL38C	7		PL52C	7	
AA31	PL38D	7		PL52D	7	
U37	PL39A	7		PL53A	7	
V37	PL39B	7		PL53B	7	
U34	PL39C	7		PL53C	7	
V34	PL39D	7		PL53D	7	
U39	PL41A	7		PL55A	7	
T39	PL41B	7		PL55B	7	
V35	PL41C	7		PL55C	7	
W35	PL41D	7		PL55D	7	
R41	PL42A	7		PL56A	7	
T41	PL42B	7		PL56B	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W33	PL42C	7		PL56C	7	
Y33	PL42D	7		PL56D	7	
W37	PL43A	7		PL57A	7	
Y37	PL43B	7		PL57B	7	
Y32	PL43C	7		PL57C	7	
AA32	PL43D	7		PL57D	7	
U38	PL46A	7		PL60A	7	
V38	PL46B	7		PL60B	7	
W34	PL46C	7		PL60C	7	
Y34	PL46D	7		PL60D	7	
T40	PL47A	7	PCLKT7_1	PL61A	7	PCLKT7_1
U40	PL47B	7	PCLKC7_1	PL61B	7	PCLKC7_1
AA33	PL47C	7	PCLKT7_3	PL61C	7	PCLKT7_3
AB33	PL47D	7	PCLKC7_3	PL61D	7	PCLKC7_3
R42	PL48A	7	PCLKT7_0	PL62A	7	PCLKT7_0
T42	PL48B	7	PCLKC7_0	PL62B	7	PCLKC7_0
AA34	PL48C	7	PCLKT7_2	PL62C	7	PCLKT7_2
AB34	PL48D	7	PCLKC7_2	PL62D	7	PCLKC7_2
U41	PL50A	6	PCLKT6_0	PL64A	6	PCLKT6_0
V41	PL50B	6	PCLKC6_0	PL64B	6	PCLKC6_0
V36	PL50C	6	PCLKT6_1	PL64C	6	PCLKT6_1
W36	PL50D	6	PCLKC6_1	PL64D	6	PCLKC6_1
U42	PL51A	6		PL65A	6	
V42	PL51B	6		PL65B	6	
AB31	PL51C	6	PCLKT6_3	PL65C	6	PCLKT6_3
AC31	PL51D	6	PCLKC6_3	PL65D	6	PCLKC6_3
W38	PL52A	6		PL66A	6	
Y38	PL52B	6		PL66B	6	
AA35	PL52C	6	PCLKT6_2	PL66C	6	PCLKT6_2
AB35	PL52D	6	PCLKC6_2	PL66D	6	PCLKC6_2
W39	PL55A	6		PL69A	6	
Y39	PL55B	6		PL69B	6	
AB32	PL55C	6	VREF1_6	PL69C	6	VREF1_6
AC32	PL55D	6		PL69D	6	
W40	PL56A	6		PL70A	6	
Y40	PL56B	6		PL70B	6	
AA36	PL56C	6		PL70C	6	
AB36	PL56D	6		PL70D	6	
W41	PL57A	6		PL71A	6	
Y41	PL57B	6		PL71B	6	
AA37	PL57C	6		PL71C	6	
AB37	PL57D	6		PL71D	6	
W42	PL59A	6		PL73A	6	
Y42	PL59B	6		PL73B	6	
AC33	PL59C	6		PL73C	6	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AL23	PB56D	5		PB58D	5	
AW24	PB57A	5		PB61A	5	
AW23	PB57B	5		PB61B	5	
AN23	PB57C	5		PB61C	5	
AP23	PB57D	5		PB61D	5	
AY23	PB59A	5		PB63A	5	
AY24	PB59B	5		PB63B	5	
AU23	PB59C	5		PB63C	5	
AU22	PB59D	5		PB63D	5	
AV23	PB60A	5		PB66A	5	
AV22	PB60B	5		PB66B	5	
AM22	PB60C	5		PB66C	5	
AL22	PB60D	5		PB66D	5	
BA23	PB61A	5		PB69A	5	
BA22	PB61B	5		PB69B	5	
AN22	PB61C	5		PB69C	5	
AP22	PB61D	5		PB69D	5	
BB23	PB63A	5		PB71A	5	
BB22	PB63B	5		PB71B	5	
AT22	PB63C	5		PB71C	5	
AR22	PB63D	5		PB71D	5	
BB21	PB65A	4		PB73A	4	
BB20	PB65B	4		PB73B	4	
AR21	PB65C	4		PB73C	4	
AT21	PB65D	4		PB73D	4	
BA21	PB66A	4		PB75A	4	
BA20	PB66B	4		PB75B	4	
AP21	PB66C	4		PB75C	4	
AN21	PB66D	4		PB75D	4	
AV21	PB67A	4		PB78A	4	
AV20	PB67B	4		PB78B	4	
AM21	PB67C	4		PB78C	4	
AL21	PB67D	4		PB78D	4	
AY20	PB69A	4		PB81A	4	
AY19	PB69B	4		PB81B	4	
AU21	PB69C	4		PB81C	4	
AU20	PB69D	4		PB81D	4	
AW20	PB70A	4		PB83A	4	
AW19	PB70B	4		PB83B	4	
AP20	PB70C	4		PB83C	4	
AN20	PB70D	4		PB83D	4	
BB19	PB71A	4		PB86A	4	
BB18	PB71B	4		PB86B	4	
AM20	PB71C	4		PB86C	4	
AL20	PB71D	4		PB86D	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
K14	VCC12	-		VCC12	-	
H11	B_VDDIB2_R	-		B_VDDIB2_R	-	
D8	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
E8	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
G5	VCC12	-		VCC12	-	
B9	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
L12	B_VDDOB2_R	-		B_VDDOB2_R	-	
A9	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
C5	B_VDDOB3_R	-		B_VDDOB3_R	-	
A10	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
H5	VCC12	-		VCC12	-	
B10	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
E9	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
D9	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
J13	VCC12	-		VCC12	-	
H12	B_VDDIB3_R	-		B_VDDIB3_R	-	
J12	VCC12	-		VCC12	-	
M14	B_REFCLKN_R	-		B_REFCLKN_R	-	
L14	B_REFCLKP_R	-		B_REFCLKP_R	-	
J14	VCC12	-		VCC12	-	
G12	C_VDDIB0_R	-		C_VDDIB0_R	-	
D10	C_HDINP0_R	-	PCS 3E2 CH 0 IN P	C_HDINP0_R	-	PCS 3E2 CH 0 IN P
E10	C_HDINN0_R	-	PCS 3E2 CH 0 IN N	C_HDINN0_R	-	PCS 3E2 CH 0 IN N
H6	VCC12	-		VCC12	-	
B11	C_HDOUTP0_R	-	PCS 3E2 CH 0 OUT P	C_HDOUTP0_R	-	PCS 3E2 CH 0 OUT P
M12	C_VDDOB0_R	-		C_VDDOB0_R	-	
A11	C_HDOUTN0_R	-	PCS 3E2 CH 0 OUT N	C_HDOUTN0_R	-	PCS 3E2 CH 0 OUT N
L11	C_VDDOB1_R	-		C_VDDOB1_R	-	
A12	C_HDOUTN1_R	-	PCS 3E2 CH 1 OUT N	C_HDOUTN1_R	-	PCS 3E2 CH 1 OUT N
K11	VCC12	-		VCC12	-	
B12	C_HDOUTP1_R	-	PCS 3E2 CH 1 OUT P	C_HDOUTP1_R	-	PCS 3E2 CH 1 OUT P
E11	C_HDINN1_R	-	PCS 3E2 CH 1 IN N	C_HDINN1_R	-	PCS 3E2 CH 1 IN N
D11	C_HDINP1_R	-	PCS 3E2 CH 1 IN P	C_HDINP1_R	-	PCS 3E2 CH 1 IN P
H13	VCC12	-		VCC12	-	
C6	C_VDDIB1_R	-		C_VDDIB1_R	-	
H15	VCC12	-		VCC12	-	
G13	C_VDDIB2_R	-		C_VDDIB2_R	-	
D12	C_HDINP2_R	-	PCS 3E2 CH 2 IN P	C_HDINP2_R	-	PCS 3E2 CH 2 IN P
E12	C_HDINN2_R	-	PCS 3E2 CH 2 IN N	C_HDINN2_R	-	PCS 3E2 CH 2 IN N
J9	VCC12	-		VCC12	-	
B13	C_HDOUTP2_R	-	PCS 3E2 CH 2 OUT P	C_HDOUTP2_R	-	PCS 3E2 CH 2 OUT P
K10	C_VDDOB2_R	-		C_VDDOB2_R	-	
A13	C_HDOUTN2_R	-	PCS 3E2 CH 2 OUT N	C_HDOUTN2_R	-	PCS 3E2 CH 2 OUT N
J10	C_VDDOB3_R	-		C_VDDOB3_R	-	
A14	C_HDOUTN3_R	-	PCS 3E2 CH 3 OUT N	C_HDOUTN3_R	-	PCS 3E2 CH 3 OUT N

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
A26	D_HDOUTN2_L	-	PCS 363 CH 2 OUT N	D_HDOUTN2_L	-	PCS 363 CH 2 OUT N
C34	D_VDDOB2_L	-		D_VDDOB2_L	-	
B26	D_HDOUTP2_L	-	PCS 363 CH 2 OUT P	D_HDOUTP2_L	-	PCS 363 CH 2 OUT P
C32	VCC12	-		VCC12	-	
E27	D_HDINN2_L	-	PCS 363 CH 2 IN N	D_HDINN2_L	-	PCS 363 CH 2 IN N
D27	D_HDINP2_L	-	PCS 363 CH 2 IN P	D_HDINP2_L	-	PCS 363 CH 2 IN P
G25	D_VDDIB2_L	-		D_VDDIB2_L	-	
F29	VCC12	-		VCC12	-	
H26	D_VDDIB1_L	-		D_VDDIB1_L	-	
F30	VCC12	-		VCC12	-	
D28	D_HDINP1_L	-	PCS 363 CH 1 IN P	D_HDINP1_L	-	PCS 363 CH 1 IN P
E28	D_HDINN1_L	-	PCS 363 CH 1 IN N	D_HDINN1_L	-	PCS 363 CH 1 IN N
B27	D_HDOUTP1_L	-	PCS 363 CH 1 OUT P	D_HDOUTP1_L	-	PCS 363 CH 1 OUT P
F36	VCC12	-		VCC12	-	
A27	D_HDOUTN1_L	-	PCS 363 CH 1 OUT N	D_HDOUTN1_L	-	PCS 363 CH 1 OUT N
F35	D_VDDOB1_L	-		D_VDDOB1_L	-	
A28	D_HDOUTN0_L	-	PCS 363 CH 0 OUT N	D_HDOUTN0_L	-	PCS 363 CH 0 OUT N
M30	D_VDDOB0_L	-		D_VDDOB0_L	-	
B28	D_HDOUTP0_L	-	PCS 363 CH 0 OUT P	D_HDOUTP0_L	-	PCS 363 CH 0 OUT P
F37	VCC12	-		VCC12	-	
E29	D_HDINN0_L	-	PCS 363 CH 0 IN N	D_HDINN0_L	-	PCS 363 CH 0 IN N
D29	D_HDINP0_L	-	PCS 363 CH 0 IN P	D_HDINP0_L	-	PCS 363 CH 0 IN P
H27	D_VDDIB0_L	-		D_VDDIB0_L	-	
G28	VCC12	-		VCC12	-	
J28	C_REFCLKP_L	-		C_REFCLKP_L	-	
K28	C_REFCLKN_L	-		C_REFCLKN_L	-	
F32	VCC12	-		VCC12	-	
G29	C_VDDIB3_L	-		C_VDDIB3_L	-	
C31	VCC12	-		VCC12	-	
D30	C_HDINP3_L	-	PCS 362 CH 3 IN P	C_HDINP3_L	-	PCS 362 CH 3 IN P
E30	C_HDINN3_L	-	PCS 362 CH 3 IN N	C_HDINN3_L	-	PCS 362 CH 3 IN N
B29	C_HDOUTP3_L	-	PCS 362 CH 3 OUT P	C_HDOUTP3_L	-	PCS 362 CH 3 OUT P
F38	VCC12	-		VCC12	-	
A29	C_HDOUTN3_L	-	PCS 362 CH 3 OUT N	C_HDOUTN3_L	-	PCS 362 CH 3 OUT N
J33	C_VDDOB3_L	-		C_VDDOB3_L	-	
A30	C_HDOUTN2_L	-	PCS 362 CH 2 OUT N	C_HDOUTN2_L	-	PCS 362 CH 2 OUT N
K33	C_VDDOB2_L	-		C_VDDOB2_L	-	
B30	C_HDOUTP2_L	-	PCS 362 CH 2 OUT P	C_HDOUTP2_L	-	PCS 362 CH 2 OUT P
J34	VCC12	-		VCC12	-	
F31	C_HDINN2_L	-	PCS 362 CH 2 IN N	C_HDINN2_L	-	PCS 362 CH 2 IN N
E31	C_HDINP2_L	-	PCS 362 CH 2 IN P	C_HDINP2_L	-	PCS 362 CH 2 IN P
G30	C_VDDIB2_L	-		C_VDDIB2_L	-	
H28	VCC12	-		VCC12	-	
C37	C_VDDIB1_L	-		C_VDDIB1_L	-	
H30	VCC12	-		VCC12	-	