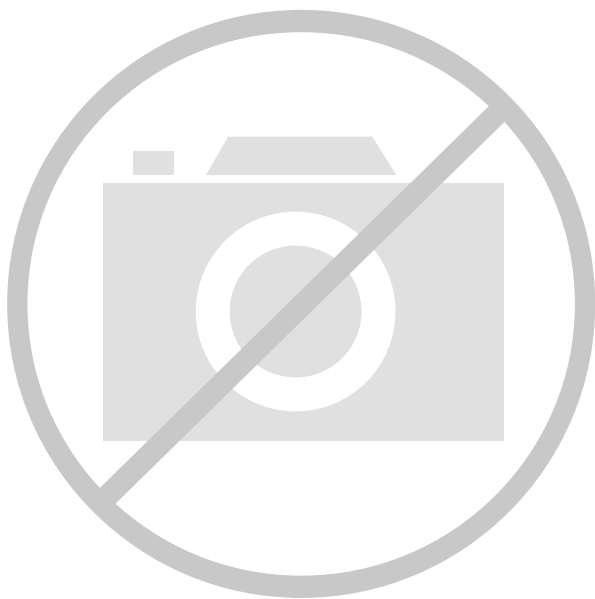




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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	604
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga40ep1-5fcn1152c

DLLs and dynamic glitch free clock MUXs which are required in today's high end system designs. High-speed, high-bandwidth I/O make this family ideal for high-throughput systems.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeSC family of FPGA devices. Synthesis library support for LatticeSC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeSC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeSC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Innovative high-performance FPGA architecture, high-speed SERDES with PCS support, sysMEM embedded memory and high performance I/O are combined in the LatticeSC to provide excellent performance for today's leading edge systems designs. Table 1-3 details the performance of several common functions implemented within the LatticeSC.

Table1-3. Speed Performance for Typical Functions¹

Functions	Performance (MHz) ²
32-bit Address Decoder	539
64-bit Address Decoder	517
32:1 Multiplexer	779
64-bit Adder (ripple)	353
32x8 Distributed Single Port (SP) RAM	768
64-bit Counter (up or down counter, non-loadable)	369
True Dual-Port 1024x18 bits	372
FIFO Port A: x36 bits, B: x9 bits	375

1. For additional information, see Typical Building BLock Function Performance table in this data sheet.

2. Advance information (-7 speed grade).

RSDS**Over Recommended Operating Conditions**

Parameter Symbol	Description	Min.	Typ.	Max.	Units
V_{OD}	Output voltage, differential, $R_T = 100$ ohms	100	200	600	mV
V_{OS}	Output voltage, common mode	0.5	1.2	1.5	V
I_{RSDS}	Differential driver output current	1	2	6	mA
V_{THD}	Input voltage differential	100	—	—	mV
V_{CM}	Input common mode voltage	0.3	—	1.5	V
T_R, T_F	Output rise and fall times, 20% to 80%	—	500	—	ps
T_{ODUTY}	Output clock duty cycle	45	50	55	%

Note: Data is for 2mA drive. Other differential driver current options are available.

LatticeSC/M Family Timing Adders

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Input Adjusters								
LVDS	LVDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
RSDS	RSDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
BLVDS25	BLVDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
MLVDS25	MLVDS	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
LVPECL33	LVPECL	-0.031	-0.031	-0.011	-0.011	0.009	0.009	ns
HSTL18_I	HSTL_18 class I	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL18_II	HSTL_18 class II	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL18_III	HSTL_18 class III	-0.016	-0.018	0.008	0.003	0.032	0.023	ns
HSTL18_IV	HSTL_18 class IV	-0.016	-0.018	0.008	0.003	0.032	0.023	ns
HSTL18D_I	Differential HSTL 18 class I	0.006	0.001	0.029	0.024	0.052	0.046	ns
HSTL18D_II	Differential HSTL 18 class II	0.006	0.001	0.029	0.024	0.052	0.046	ns
HSTL15_I	HSTL_15 class I	-0.005	-0.016	0.026	-0.001	0.057	0.014	ns
HSTL15_II	HSTL_15 class II	-0.005	-0.016	0.026	-0.001	0.057	0.014	ns
HSTL15_III	HSTL_15 class III	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL15_IV	HSTL_15 class IV	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
HSTL15D_I	Differential HSTL 15 class I	-0.021	-0.022	0.001	-0.009	0.022	0.003	ns
HSTL15D_II	Differential HSTL 15 class II	-0.021	-0.022	0.001	-0.009	0.022	0.003	ns
SSTL33_I	SSTL_3 class I	-0.036	-0.061	-0.181	-0.313	-0.326	-0.565	ns
SSTL33_II	SSTL_3 class II	-0.036	-0.061	-0.181	-0.313	-0.326	-0.565	ns
SSTL33D_I	Differential SSTL_3 class I	0.012	0.012	0.034	0.028	0.055	0.043	ns
SSTL33D_II	Differential SSTL_3 class II	0.012	0.012	0.034	0.028	0.055	0.043	ns
SSTL25_I	SSTL_2 class I	0.003	-0.008	0.03	0.011	0.058	0.03	ns
SSTL25_II	SSTL_2 class II	0.003	-0.008	0.03	0.011	0.058	0.03	ns
SSTL25D_I	Differential SSTL_2 class I	0.006	0	0.031	0.023	0.056	0.046	ns
SSTL25D_II	Differential SSTL_2 class II	0.006	0	0.031	0.023	0.056	0.046	ns
SSTL18_I	SSTL_18 class I	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
SSTL18_II	SSTL_18 class II	-0.013	-0.015	0.015	0.007	0.042	0.029	ns
SSTL18D_I	Differential SSTL_18 class I	0.006	0.001	0.029	0.024	0.052	0.046	ns
SSTL18D_II	Differential SSTL_18 class II	0.006	0.001	0.029	0.024	0.052	0.046	ns
LVTTTL33	LVTTTL	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
LVC MOS33	LVC MOS 3.3	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
LVC MOS25	LVC MOS 2.5	0	0	0	0	0	0	ns
LVC MOS18	LVC MOS 1.8	-0.068	-0.068	-0.087	-0.087	-0.105	-0.105	ns
LVC MOS15	LVC MOS 1.5	-0.131	-0.131	-0.186	-0.186	-0.241	-0.241	ns
LVC MOS12	LVC MOS 1.2	-0.238	-0.238	-0.364	-0.364	-0.49	-0.49	ns
PCI33	PCI	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
PCIX33	PCI-X 3.3	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
PCIX15	PCI-X 1.5	-0.005	-0.016	0.026	-0.001	0.057	0.014	ns
AGP1X33	AGP-1X 3.3	0.034	0.034	-0.05	-0.05	-0.134	-0.134	ns
AGP2X33	AGP-2X	-0.036	-0.061	-0.181	-0.313	-0.326	-0.565	ns

Figure 3-12. Waveforms First Read after Full Flag

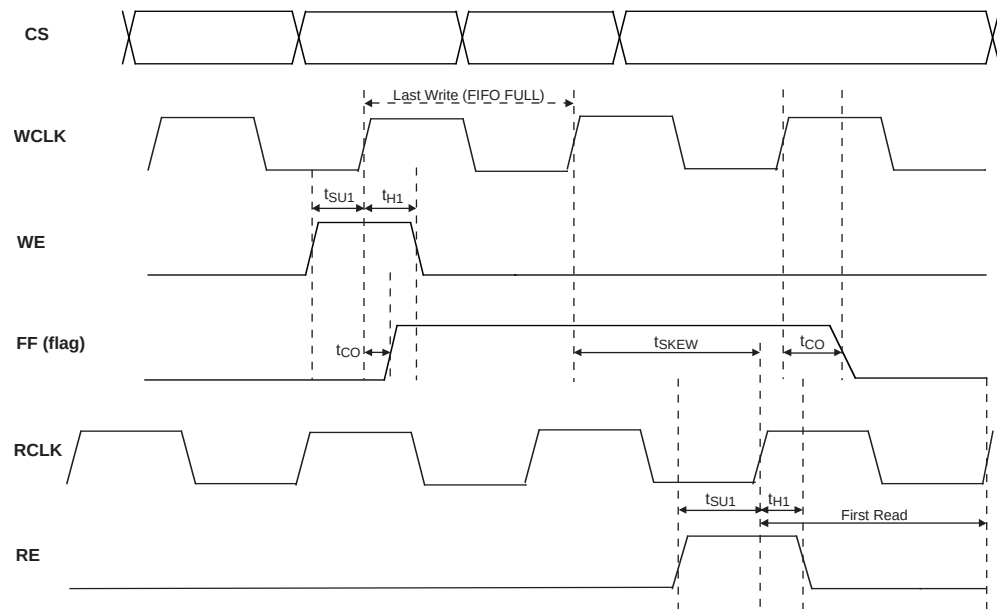
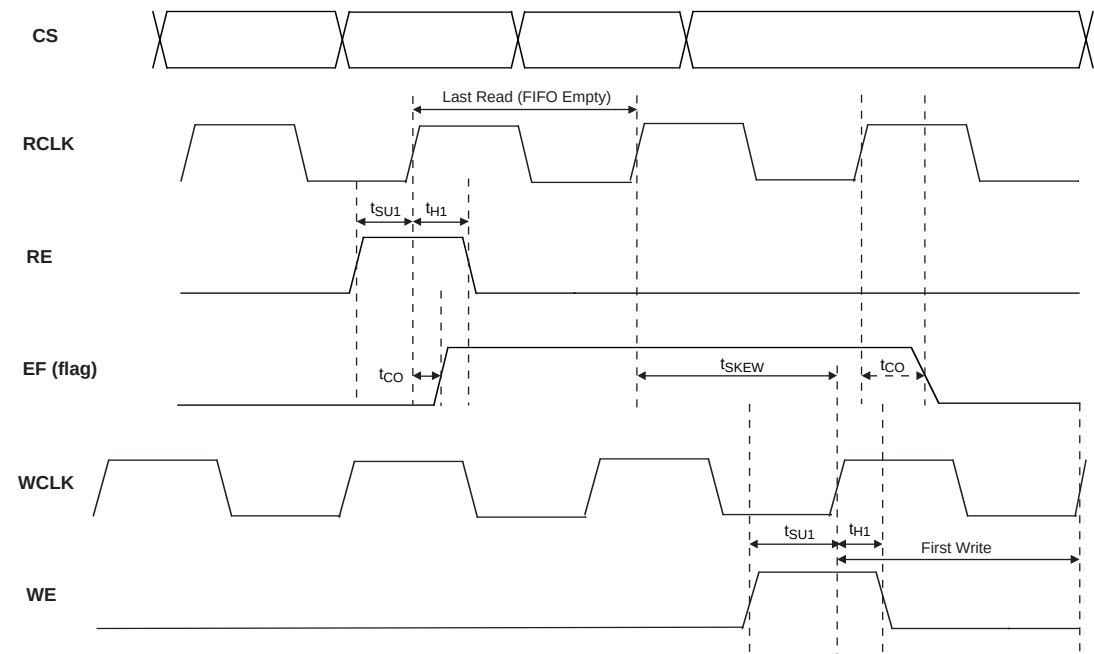


Figure 3-13. Waveform First Write after Empty Flag



LFSC/M15 Logic Signal Connections: 256 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
N12	PB39C	4	
T15	PB40A	4	PCLKT4_3
R16	PB40B	4	PCLKC4_3
L12	PB43A	4	
M12	PB43B	4	
P16	PB44A	4	
N16	PB44B	4	
R14	PB47C	4	VREF1_4
P15	PB48A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
M13	PB48B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
N13	PB49A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
P14	PB49B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
M16	PR45B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
L16	PR45A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
M14	PR43B	3	
M15	PR43A	3	
K16	PR41D	3	VREF2_3
J16	PR37B	3	
H16	PR37A	3	
L13	PR35D	3	DIFFR_3
L14	PR35B	3	
L15	PR35A	3	
K12	PR31C	3	VREF1_3
J13	PR28D	3	PCLKC3_2
K13	PR28C	3	PCLKT3_2
H15	PR28B	3	
F16	PR28A	3	
J11	PR26D	3	PCLKC3_1
J12	PR26C	3	PCLKT3_1
J15	PR26B	3	PCLKC3_0
J14	PR26A	3	PCLKT3_0
E16	PR24D	2	PCLKC2_2
D16	PR24C	2	PCLKT2_2
H11	PR24B	2	PCLKC2_0
H12	PR24A	2	PCLKT2_0
H13	PR23B	2	PCLKC2_1
H14	PR23A	2	PCLKT2_1
G12	PR22D	2	DIFFR_2
G13	PR22C	2	VREF1_2
F8	PR22B	2	
F9	PR22A	2	
G16	PR18D	2	VREF2_2
F15	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W24	VCCAUX	-		VCCAUX	-	
AC17	VCCAUX	-		VCCAUX	-	
AC18	VCCAUX	-		VCCAUX	-	
AC19	VCCAUX	-		VCCAUX	-	
AD17	VCCAUX	-		VCCAUX	-	
AD18	VCCAUX	-		VCCAUX	-	
AD19	VCCAUX	-		VCCAUX	-	
AC12	VCCAUX	-		VCCAUX	-	
AC13	VCCAUX	-		VCCAUX	-	
AC14	VCCAUX	-		VCCAUX	-	
AD12	VCCAUX	-		VCCAUX	-	
AD13	VCCAUX	-		VCCAUX	-	
AD14	VCCAUX	-		VCCAUX	-	
U7	VCCAUX	-		VCCAUX	-	
U8	VCCAUX	-		VCCAUX	-	
V7	VCCAUX	-		VCCAUX	-	
V8	VCCAUX	-		VCCAUX	-	
W7	VCCAUX	-		VCCAUX	-	
W8	VCCAUX	-		VCCAUX	-	
M7	VCCAUX	-		VCCAUX	-	
M8	VCCAUX	-		VCCAUX	-	
N7	VCCAUX	-		VCCAUX	-	
N8	VCCAUX	-		VCCAUX	-	
H10	VCCIO1	-		VCCIO1	-	
H21	VCCIO1	-		VCCIO1	-	
H22	VCCIO1	-		VCCIO1	-	
H9	VCCIO1	-		VCCIO1	-	
J11	VCCIO1	-		VCCIO1	-	
J12	VCCIO1	-		VCCIO1	-	
J13	VCCIO1	-		VCCIO1	-	
J14	VCCIO1	-		VCCIO1	-	
J15	VCCIO1	-		VCCIO1	-	
J16	VCCIO1	-		VCCIO1	-	
J17	VCCIO1	-		VCCIO1	-	
J18	VCCIO1	-		VCCIO1	-	
J19	VCCIO1	-		VCCIO1	-	
J20	VCCIO1	-		VCCIO1	-	
J23	VCCIO2	-		VCCIO2	-	
J24	VCCIO2	-		VCCIO2	-	
K23	VCCIO2	-		VCCIO2	-	
K24	VCCIO2	-		VCCIO2	-	
L22	VCCIO2	-		VCCIO2	-	
L23	VCCIO2	-		VCCIO2	-	
M22	VCCIO2	-		VCCIO2	-	
N22	VCCIO2	-		VCCIO2	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ27	GND	-		GND	-	
AF23	GND	-		GND	-	
AF22	GND	-		GND	-	
AE27	GND	-		GND	-	
AA27	GND	-		GND	-	
AB29	GND	-		GND	-	
Y26	GND	-		GND	-	
AC30	GND	-		GND	-	
Y29	GND	-		GND	-	
F30	GND	-		GND	-	
E27	GND	-		GND	-	
F27	GND	-		GND	-	
P25	GND	-		GND	-	
H29	GND	-		GND	-	
K29	GND	-		GND	-	
R24	GND	-		GND	-	
M28	GND	-		GND	-	
J27	GND	-		GND	-	
N26	GND	-		GND	-	
E20	GND	-		GND	-	
E21	GND	-		GND	-	
F21	GND	-		GND	-	
F23	GND	-		GND	-	
G23	GND	-		GND	-	
D21	GND	-		GND	-	
D20	GND	-		GND	-	
E18	GND	-		GND	-	
C20	GND	-		GND	-	
C11	GND	-		GND	-	
A12	GND	-		GND	-	
E11	GND	-		GND	-	
F8	GND	-		GND	-	
G8	GND	-		GND	-	
D11	GND	-		GND	-	
D10	GND	-		GND	-	
H7	GND	-		GND	-	
F10	GND	-		GND	-	
E10	GND	-		GND	-	
AC16	NC	-		NC	-	
J22	VCC	-		VCC	-	
J9	VCC	-		VCC	-	
B2	NC	-		NC	-	
C2	RESPN_ULC	-		RESPN_ULC	-	
C29	RESPN_URC	-		RESPN_URC	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
E16	PT45C	1	D3/MPI_DATA3	PT54C	1	D3/MPI_DATA3
C13	PT45B	1	D2/MPI_DATA2	PT53B	1	D2/MPI_DATA2
C14	PT45A	1	D1/MPI_DATA1	PT53A	1	D1/MPI_DATA1
B14	PT43B	1	D0/MPI_DATA0	PT51B	1	D0/MPI_DATA0
B13	PT43A	1	QOUT/CEON	PT51A	1	QOUT/CEON
L13	PT42D	1	VREF2_1	PT50D	1	VREF2_1
C15	PT42B	1	DOUT	PT50B	1	DOUT
D15	PT42A	1	MCA_DONE_IN	PT50A	1	MCA_DONE_IN
J16	PT41B	1	MCA_CLK_P1_OUT	PT49B	1	MCA_CLK_P1_OUT
K16	PT41A	1	MCA_CLK_P1_IN	PT49A	1	MCA_CLK_P1_IN
H15	PT39D	1	D21/PCLKC1_1/MPI_DATA21	PT47D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT39C	1	D22/PCLKT1_1/MPI_DATA22	PT47C	1	D22/PCLKT1_1/MPI_DATA22
A14	PT39B	1	MCA_CLK_P2_OUT	PT47B	1	MCA_CLK_P2_OUT
A13	PT39A	1	MCA_CLK_P2_IN	PT47A	1	MCA_CLK_P2_IN
G16	PT38D	1	MCA_DONE_OUT	PT46D	1	MCA_DONE_OUT
F16	PT38C	1	BUSYN/RCLK/SCK	PT46C	1	BUSYN/RCLK/SCK
B16	PT38B	1	DP0/MPI_PAR0	PT46B	1	DP0/MPI_PAR0
B15	PT38A	1	MPI_TA	PT46A	1	MPI_TA
L16	PT37C	1	DP2/MPI_PAR2	PT45C	1	DP2/MPI_PAR2
A16	PT37B	1	PCLKC1_0	PT45B	1	PCLKC1_0
A15	PT37A	1	PCLKT1_0/MPI_CLK	PT45A	1	PCLKT1_0/MPI_CLK
L17	PT35C	1	D24/PCLKT1_4/MPI_DATA24	PT43C	1	D24/PCLKT1_4/MPI_DATA24
A17	PT35B	1	MPI_RETRY	PT43B	1	MPI_RETRY
A18	PT35A	1	A0/MPI_ADDR14	PT43A	1	A0/MPI_ADDR14
F17	PT33D	1	A1/MPI_ADDR15	PT42D	1	A1/MPI_ADDR15
G17	PT33C	1	A2/MPI_ADDR16	PT42C	1	A2/MPI_ADDR16
B17	PT33B	1	A3/MPI_ADDR17	PT42B	1	A3/MPI_ADDR17
B18	PT33A	1	A4/MPI_ADDR18	PT42A	1	A4/MPI_ADDR18
H17	PT32D	1	D25/PCLKC1_5/MPI_DATA25	PT41D	1	D25/PCLKC1_5/MPI_DATA25
H18	PT32C	1	D26/PCLKT1_5/MPI_DATA26	PT41C	1	D26/PCLKT1_5/MPI_DATA26
A19	PT32B	1	A5/MPI_ADDR19	PT41B	1	A5/MPI_ADDR19
A20	PT32A	1	A6/MPI_ADDR20	PT41A	1	A6/MPI_ADDR20
L20	PT31C	1	VREF1_1	PT39C	1	VREF1_1
J17	PT31B	1	A7/MPI_ADDR21	PT39B	1	A7/MPI_ADDR21
K17	PT31A	1	A8/MPI_ADDR22	PT39A	1	A8/MPI_ADDR22
C18	PT29B	1	A9/MPI_ADDR23	PT38B	1	A9/MPI_ADDR23
D18	PT29A	1	A10/MPI_ADDR24	PT38A	1	A10/MPI_ADDR24
B19	PT28B	1	A11/MPI_ADDR25	PT37B	1	A11/MPI_ADDR25
B20	PT28A	1	A12/MPI_ADDR26	PT37A	1	A12/MPI_ADDR26
E17	PT27D	1	D11/MPI_DATA11	PT35D	1	D11/MPI_DATA11
E18	PT27C	1	D12/MPI_DATA12	PT35C	1	D12/MPI_DATA12
C20	PT27B	1	A13/MPI_ADDR27	PT35B	1	A13/MPI_ADDR27
C19	PT27A	1	A14/MPI_ADDR28	PT35A	1	A14/MPI_ADDR28
H19	PT25D	1	A16/MPI_ADDR30	PT33D	1	A16/MPI_ADDR30
G19	PT25C	1	D13/MPI_DATA13	PT33C	1	D13/MPI_DATA13
D20	PT25B	1	A15/MPI_ADDR29	PT33B	1	A15/MPI_ADDR29
D19	PT25A	1	A17/MPI_ADDR31	PT33A	1	A17/MPI_ADDR31
H20	PT24D	1	A19/MPI_TSI21	PT30D	1	A19/MPI_TSI21
G20	PT24C	1	A20/MPI_BDIP	PT30C	1	A20/MPI_BDIP
E19	PT24B	1	A18/MPI_TSI20	PT30B	1	A18/MPI_TSI20

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
B30	A_HDOU TN0_L	-	PCS 360 CH 0 OUT N	A_HDOU TN0_L	-	PCS 360 CH 0 OUT N
D30	A_VDDOB0_L	-		A_VDDOB0_L	-	
A30	A_HDOU TP0_L	-	PCS 360 CH 0 OUT P	A_HDOU TP0_L	-	PCS 360 CH 0 OUT P
C31	A_HDINN0_L	-	PCS 360 CH 0 IN N	A_HDINN0_L	-	PCS 360 CH 0 IN N
C32	A_HDINP0_L	-	PCS 360 CH 0 IN P	A_HDINP0_L	-	PCS 360 CH 0 IN P
B31	A_VDDIB0_L	-		A_VDDIB0_L	-	
AL25	NC	-		PB26A	5	
AL24	NC	-		PB26B	5	
AG27	NC	-		PB26C	5	
AH27	NC	-		PB26D	5	
AM25	NC	-		PB27A	5	
AM24	NC	-		PB27B	5	
AL9	NC	-		PB62A	4	
AL8	NC	-		PB62B	4	
AK9	NC	-		PB63A	4	
AJ9	NC	-		PB63B	4	
AG10	NC	-		PB63C	4	
AG11	NC	-		PB63D	4	
J30	NC	-		PL26A	7	
H30	NC	-		PL26B	7	
M28	NC	-		PL26C	7	
N28	NC	-		PL26D	7	
J32	NC	-		PL27A	7	
J31	NC	-		PL27B	7	
N26	NC	-		PL27C	7	
N27	NC	-		PL27D	7	
K31	NC	-		PL29A	7	
K32	NC	-		PL29B	7	
P25	NC	-		PL29C	7	
P26	NC	-		PL29D	7	
L27	NC	-		PL22C	7	
L28	NC	-		PL22D	7	
M29	NC	-		PL30A	7	
L29	NC	-		PL30B	7	
M30	NC	-		PL31A	7	
L30	NC	-		PL31B	7	
L31	NC	-		PL34A	7	
M31	NC	-		PL34B	7	
AA29	NC	-		PL56A	6	
AA30	NC	-		PL56B	6	
AB31	NC	-		PL57A	6	
AA31	NC	-		PL57B	6	
AG30	NC	-		PL57C	6	
AG29	NC	-		PL57D	6	
AB29	NC	-		PL58A	6	
AB30	NC	-		PL58B	6	
Y25	NC	-		PL58C	6	
AA25	NC	-		PL58D	6	
AA8	NC	-		PR58D	3	
Y8	NC	-		PR58C	3	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D7	B_VDDIB0_R	-		B_VDDIB0_R	-	
E10	B_HDINP0_R	-	PCS 3E1 CH 0 IN P	B_HDINP0_R	-	PCS 3E1 CH 0 IN P
F10	B_HDINN0_R	-	PCS 3E1 CH 0 IN N	B_HDINN0_R	-	PCS 3E1 CH 0 IN N
K10	VCC12	-		VCC12	-	
A11	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P
D10	B_VDDOB0_R	-		B_VDDOB0_R	-	
B11	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N
D11	B_VDDOB1_R	-		B_VDDOB1_R	-	
B12	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N
L10	VCC12	-		VCC12	-	
A12	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P
F11	B_HDINN1_R	-	PCS 3E1 CH 1 IN N	B_HDINN1_R	-	PCS 3E1 CH 1 IN N
E11	B_HDINP1_R	-	PCS 3E1 CH 1 IN P	B_HDINP1_R	-	PCS 3E1 CH 1 IN P
G11	VCC12	-		VCC12	-	
D8	B_VDDIB1_R	-		B_VDDIB1_R	-	
G12	VCC12	-		VCC12	-	
D9	B_VDDIB2_R	-		B_VDDIB2_R	-	
E12	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
F12	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
K11	VCC12	-		VCC12	-	
A13	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D12	B_VDDOB2_R	-		B_VDDOB2_R	-	
B13	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D13	B_VDDOB3_R	-		B_VDDOB3_R	-	
B14	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
L11	VCC12	-		VCC12	-	
A14	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
F13	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
E13	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
G13	VCC12	-		VCC12	-	
E9	B_VDDIB3_R	-		B_VDDIB3_R	-	
L13	VCC12	-		VCC12	-	
J11	B_REFCLKN_R	-		B_REFCLKN_R	-	
H11	B_REFCLKP_R	-		B_REFCLKP_R	-	
M15	PT61D	1	HDC/SI	PT77D	1	HDC/SI
M16	PT61C	1	LDCN/SCS	PT77C	1	LDCN/SCS
F14	PT59B	1	D8/MPI_DATA8	PT77B	1	D8/MPI_DATA8
G14	PT59A	1	CS1/MPI_CS1	PT77A	1	CS1/MPI_CS1
L15	PT58D	1	D9/MPI_DATA9	PT75D	1	D9/MPI_DATA9
L14	PT58C	1	D10/MPI_DATA10	PT75C	1	D10/MPI_DATA10
D14	PT57B	1	CS0N/MPI_CS0N	PT75B	1	CS0N/MPI_CS0N
E14	PT57A	1	RDN/MPI_STRB_N	PT75A	1	RDN/MPI_STRB_N
L16	PT55D	1	WRN/MPI_WR_N	PT74D	1	WRN/MPI_WR_N
K16	PT55C	1	D7/MPI_DATA7	PT74C	1	D7/MPI_DATA7
G15	PT55B	1	D6/MPI_DATA6	PT74B	1	D6/MPI_DATA6

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB15	VCC12	-		VCC12	-	
AB20	VCC12	-		VCC12	-	
N15	VCC12	-		VCC12	-	
N20	VCC12	-		VCC12	-	
R13	VCC12	-		VCC12	-	
R22	VCC12	-		VCC12	-	
Y13	VCC12	-		VCC12	-	
Y22	VCC12	-		VCC12	-	
AA12	VCCAUX	-		VCCAUX	-	
AA23	VCCAUX	-		VCCAUX	-	
AB12	VCCAUX	-		VCCAUX	-	
AB16	VCCAUX	-		VCCAUX	-	
AB17	VCCAUX	-		VCCAUX	-	
AB18	VCCAUX	-		VCCAUX	-	
AB19	VCCAUX	-		VCCAUX	-	
AB23	VCCAUX	-		VCCAUX	-	
AC12	VCCAUX	-		VCCAUX	-	
AC13	VCCAUX	-		VCCAUX	-	
Y19	GND	-		GND	-	
AC14	VCCAUX	-		VCCAUX	-	
AC17	VCCAUX	-		VCCAUX	-	
AC21	VCCAUX	-		VCCAUX	-	
AC22	VCCAUX	-		VCCAUX	-	
AC23	VCCAUX	-		VCCAUX	-	
M13	VCCAUX	-		VCCAUX	-	
M14	VCCAUX	-		VCCAUX	-	
M18	VCCAUX	-		VCCAUX	-	
M21	VCCAUX	-		VCCAUX	-	
M22	VCCAUX	-		VCCAUX	-	
N12	VCCAUX	-		VCCAUX	-	
N16	VCCAUX	-		VCCAUX	-	
N17	VCCAUX	-		VCCAUX	-	
N18	VCCAUX	-		VCCAUX	-	
N19	VCCAUX	-		VCCAUX	-	
N23	VCCAUX	-		VCCAUX	-	
P12	VCCAUX	-		VCCAUX	-	
P23	VCCAUX	-		VCCAUX	-	
T13	VCCAUX	-		VCCAUX	-	
T22	VCCAUX	-		VCCAUX	-	
U12	VCCAUX	-		VCCAUX	-	
U13	VCCAUX	-		VCCAUX	-	
U22	VCCAUX	-		VCCAUX	-	
V13	VCCAUX	-		VCCAUX	-	
V22	VCCAUX	-		VCCAUX	-	
V23	VCCAUX	-		VCCAUX	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W13	VCCAUX	-		VCCAUX	-	
W22	VCCAUX	-		VCCAUX	-	
Y21	GND	-		GND	-	
Y25	GND	-		GND	-	
C18	VCCIO1	-		VCCIO1	-	
D17	VCCIO1	-		VCCIO1	-	
F16	VCCIO1	-		VCCIO1	-	
G19	VCCIO1	-		VCCIO1	-	
J20	VCCIO1	-		VCCIO1	-	
K12	VCCIO1	-		VCCIO1	-	
K15	VCCIO1	-		VCCIO1	-	
L23	VCCIO1	-		VCCIO1	-	
Y9	GND	-		GND	-	
J9	VCCIO1	-		VCCIO1	-	
E3	VCCIO2	-		VCCIO2	-	
G6	VCCIO2	-		VCCIO2	-	
H4	VCCIO2	-		VCCIO2	-	
K7	VCCIO2	-		VCCIO2	-	
L3	VCCIO2	-		VCCIO2	-	
M11	VCCIO2	-		VCCIO2	-	
N6	VCCIO2	-		VCCIO2	-	
P4	VCCIO2	-		VCCIO2	-	
R9	VCCIO2	-		VCCIO2	-	
AA3	VCCIO3	-		VCCIO3	-	
AB7	VCCIO3	-		VCCIO3	-	
AC10	VCCIO3	-		VCCIO3	-	
AD4	VCCIO3	-		VCCIO3	-	
AE6	VCCIO3	-		VCCIO3	-	
AG3	VCCIO3	-		VCCIO3	-	
AK4	VCCIO3	-		VCCIO3	-	
T7	VCCIO3	-		VCCIO3	-	
U3	VCCIO3	-		VCCIO3	-	
V4	VCCIO3	-		VCCIO3	-	
W6	VCCIO3	-		VCCIO3	-	
Y10	VCCIO3	-		VCCIO3	-	
AD12	VCCIO4	-		VCCIO4	-	
AF15	VCCIO4	-		VCCIO4	-	
AF9	VCCIO4	-		VCCIO4	-	
AH10	VCCIO4	-		VCCIO4	-	
AH16	VCCIO4	-		VCCIO4	-	
AJ13	VCCIO4	-		VCCIO4	-	
AJ7	VCCIO4	-		VCCIO4	-	
AL14	VCCIO4	-		VCCIO4	-	
AL8	VCCIO4	-		VCCIO4	-	
AM11	VCCIO4	-		VCCIO4	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AJ34	PL98A	6	
AK34	PL98B	6	
AB27	PL98C	6	
AC27	PL98D	6	
AF33	PL99A	6	
AG33	PL99B	6	
AC29	PL99C	6	
AD29	PL99D	6	
AE31	PL103A	6	
AF31	PL103B	6	
AF30	PL103C	6	
AF29	PL103D	6	
AH33	PL104A	6	
AJ33	PL104B	6	
AC28	PL104C	6	
AD28	PL104D	6	
AH32	PL107A	6	
AJ32	PL107B	6	
AD27	PL107C	6	
AE27	PL107D	6	VREF2_6
AG34	PL109A	6	
AH34	PL109B	6	
AC26	PL109C	6	
AB26	PL109D	6	
AK33	PL112A	6	
AL33	PL112B	6	
AG30	PL112C	6	
AH30	PL112D	6	
AL34	PL115A	6	
AM34	PL115B	6	
AJ30	PL115C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AK30	PL115D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AJ31	PL116A	6	
AH31	PL116B	6	
AD26	PL116C	6	
AD25	PL116D	6	
AL32	PL117A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AL31	PL117B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AG29	PL117C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AG28	PL117D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AF28	XRES	-	
AF27	TEMP	6	
AM33	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
H34	PL40B	7	
M32	PL53A	7	
N32	PL53B	7	
P28	PL53C	7	
R28	PL53D	7	
J34	PL55A	7	
K34	PL55B	7	
P30	PL55C	7	
R30	PL55D	7	
W34	PL73A	6	
Y34	PL73B	6	
W32	PL75A	6	
Y32	PL75B	6	
AA34	PL78A	6	
AB34	PL78B	6	
AC34	PL81A	6	
AD34	PL81B	6	
Y30	PL82A	6	
AA30	PL82B	6	
AB33	PL83A	6	
AC33	PL83B	6	
AC2	PR83B	3	
AB2	PR83A	3	
AA5	PR82B	3	
Y5	PR82A	3	
AD1	PR81B	3	
AC1	PR81A	3	
AB1	PR78B	3	
AA1	PR78A	3	
Y3	PR75B	3	
W3	PR75A	3	
Y1	PR73B	3	
W1	PR73A	3	
R5	PR55D	2	
P5	PR55C	2	
K1	PR55B	2	
J1	PR55A	2	
R7	PR53D	2	
P7	PR53C	2	
N3	PR53B	2	
M3	PR53A	2	
H1	PR40B	2	
G1	PR40A	2	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
K26	GND	-	
K28	GND	-	
K6	GND	-	
K9	GND	-	
L12	GND	-	
L32	GND	-	
L4	GND	-	
M10	GND	-	
M17	GND	-	
M24	GND	-	
N29	GND	-	
N7	GND	-	
P15	GND	-	
P20	GND	-	
P3	GND	-	
P31	GND	-	
R10	GND	-	
R14	GND	-	
R16	GND	-	
R19	GND	-	
R21	GND	-	
R26	GND	-	
T15	GND	-	
T17	GND	-	
T18	GND	-	
T20	GND	-	
T28	GND	-	
T6	GND	-	
U16	GND	-	
U19	GND	-	
U23	GND	-	
U32	GND	-	
U4	GND	-	
V12	GND	-	
V16	GND	-	
V19	GND	-	
V3	GND	-	
V31	GND	-	
W15	GND	-	
W17	GND	-	
W18	GND	-	
W20	GND	-	
W29	GND	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
BB12	PB88B	4		PB102B	4	
AM17	PB88C	4		PB102C	4	
AL17	PB88D	4		PB102D	4	
AW14	PB89A	4		PB103A	4	
AW13	PB89B	4		PB103B	4	
AP16	PB89C	4		PB103C	4	
AN16	PB89D	4		PB103D	4	
BA13	PB91A	4		PB105A	4	
BA12	PB91B	4		PB105B	4	
AU13	PB91C	4		PB105C	4	
AU12	PB91D	4		PB105D	4	
BB11	PB92A	4		PB106A	4	
BB10	PB92B	4		PB106B	4	
AP15	PB92C	4		PB106C	4	
AN15	PB92D	4		PB106D	4	
AV13	PB93A	4		PB107A	4	
AV12	PB93B	4		PB107B	4	
AT13	PB93C	4		PB107C	4	
AT12	PB93D	4		PB107D	4	
BA11	PB95A	4		PB109A	4	
BA10	PB95B	4		PB109B	4	
AR13	PB95C	4		PB109C	4	
AR12	PB95D	4		PB109D	4	
AY11	PB96A	4		PB110A	4	
AY10	PB96B	4		PB110B	4	
AP14	PB96C	4		PB110C	4	
AN14	PB96D	4		PB110D	4	
BB9	PB97A	4		PB111A	4	
BB8	PB97B	4		PB111B	4	
AU11	PB97C	4		PB111C	4	
AU10	PB97D	4		PB111D	4	
AW11	PB99A	4		PB113A	4	
AW10	PB99B	4		PB113B	4	
AJ16	PB99C	4		PB113C	4	
AJ17	PB99D	4		PB113D	4	
BA9	PB100A	4		PB114A	4	
BA8	PB100B	4		PB114B	4	
AM15	PB100C	4		PB114C	4	
AL15	PB100D	4		PB114D	4	
AV11	PB101A	4		PB115A	4	
AV10	PB101B	4		PB115B	4	
AP13	PB101C	4		PB115C	4	
AP12	PB101D	4		PB115D	4	
BB7	PB103A	4		PB117A	4	
BB6	PB103B	4		PB117B	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
A26	D_HDOUTN2_L	-	PCS 363 CH 2 OUT N	D_HDOUTN2_L	-	PCS 363 CH 2 OUT N
C34	D_VDDOB2_L	-		D_VDDOB2_L	-	
B26	D_HDOUTP2_L	-	PCS 363 CH 2 OUT P	D_HDOUTP2_L	-	PCS 363 CH 2 OUT P
C32	VCC12	-		VCC12	-	
E27	D_HDINN2_L	-	PCS 363 CH 2 IN N	D_HDINN2_L	-	PCS 363 CH 2 IN N
D27	D_HDINP2_L	-	PCS 363 CH 2 IN P	D_HDINP2_L	-	PCS 363 CH 2 IN P
G25	D_VDDIB2_L	-		D_VDDIB2_L	-	
F29	VCC12	-		VCC12	-	
H26	D_VDDIB1_L	-		D_VDDIB1_L	-	
F30	VCC12	-		VCC12	-	
D28	D_HDINP1_L	-	PCS 363 CH 1 IN P	D_HDINP1_L	-	PCS 363 CH 1 IN P
E28	D_HDINN1_L	-	PCS 363 CH 1 IN N	D_HDINN1_L	-	PCS 363 CH 1 IN N
B27	D_HDOUTP1_L	-	PCS 363 CH 1 OUT P	D_HDOUTP1_L	-	PCS 363 CH 1 OUT P
F36	VCC12	-		VCC12	-	
A27	D_HDOUTN1_L	-	PCS 363 CH 1 OUT N	D_HDOUTN1_L	-	PCS 363 CH 1 OUT N
F35	D_VDDOB1_L	-		D_VDDOB1_L	-	
A28	D_HDOUTN0_L	-	PCS 363 CH 0 OUT N	D_HDOUTN0_L	-	PCS 363 CH 0 OUT N
M30	D_VDDOB0_L	-		D_VDDOB0_L	-	
B28	D_HDOUTP0_L	-	PCS 363 CH 0 OUT P	D_HDOUTP0_L	-	PCS 363 CH 0 OUT P
F37	VCC12	-		VCC12	-	
E29	D_HDINN0_L	-	PCS 363 CH 0 IN N	D_HDINN0_L	-	PCS 363 CH 0 IN N
D29	D_HDINP0_L	-	PCS 363 CH 0 IN P	D_HDINP0_L	-	PCS 363 CH 0 IN P
H27	D_VDDIB0_L	-		D_VDDIB0_L	-	
G28	VCC12	-		VCC12	-	
J28	C_REFCLKP_L	-		C_REFCLKP_L	-	
K28	C_REFCLKN_L	-		C_REFCLKN_L	-	
F32	VCC12	-		VCC12	-	
G29	C_VDDIB3_L	-		C_VDDIB3_L	-	
C31	VCC12	-		VCC12	-	
D30	C_HDINP3_L	-	PCS 362 CH 3 IN P	C_HDINP3_L	-	PCS 362 CH 3 IN P
E30	C_HDINN3_L	-	PCS 362 CH 3 IN N	C_HDINN3_L	-	PCS 362 CH 3 IN N
B29	C_HDOUTP3_L	-	PCS 362 CH 3 OUT P	C_HDOUTP3_L	-	PCS 362 CH 3 OUT P
F38	VCC12	-		VCC12	-	
A29	C_HDOUTN3_L	-	PCS 362 CH 3 OUT N	C_HDOUTN3_L	-	PCS 362 CH 3 OUT N
J33	C_VDDOB3_L	-		C_VDDOB3_L	-	
A30	C_HDOUTN2_L	-	PCS 362 CH 2 OUT N	C_HDOUTN2_L	-	PCS 362 CH 2 OUT N
K33	C_VDDOB2_L	-		C_VDDOB2_L	-	
B30	C_HDOUTP2_L	-	PCS 362 CH 2 OUT P	C_HDOUTP2_L	-	PCS 362 CH 2 OUT P
J34	VCC12	-		VCC12	-	
F31	C_HDINN2_L	-	PCS 362 CH 2 IN N	C_HDINN2_L	-	PCS 362 CH 2 IN N
E31	C_HDINP2_L	-	PCS 362 CH 2 IN P	C_HDINP2_L	-	PCS 362 CH 2 IN P
G30	C_VDDIB2_L	-		C_VDDIB2_L	-	
H28	VCC12	-		VCC12	-	
C37	C_VDDIB1_L	-		C_VDDIB1_L	-	
H30	VCC12	-		VCC12	-	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-7FCN1152C ¹	-7	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-6FCN1152C ¹	-6	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-5FCN1152C ¹	-5	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-7FFN1152C	-7	Lead-Free Organic fcBGA	1152	COM	80.1
LFSC3GA80E-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	80.1
LFSC3GA80E-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	80.1
LFSC3GA80E-7FCN1704C ¹	-7	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-6FCN1704C ¹	-6	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-5FCN1704C ¹	-5	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-7FFN1704C	-7	Lead-Free Organic fcBGA	1704	COM	80.1
LFSC3GA80E-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	80.1
LFSC3GA80E-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-7FCN1152C ¹	-7	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FCN1152C ¹	-6	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FCN1152C ¹	-5	Lead-Free Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FFN1152C	-7	Lead-Free Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FCN1704C ¹	-7	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FCN1704C ¹	-6	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FCN1704C ¹	-5	Lead-Free Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-7FFN1704C	-7	Lead-Free Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FCN1152C ¹	-6	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-5FCN1152C ¹	-5	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	115.2
LFSC3GA115E-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	115.2
LFSC3GA115E-6FCN1704C ¹	-6	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-5FCN1704C ¹	-5	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	115.2
LFSC3GA115E-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

For Further Information

For further information about the flexiPCS, see the [LatticeSC/M Family flexiPCS Data Sheet](#).

A variety of technical notes for the LatticeSC/M family are also available on the Lattice Semiconductor website at www.latticesemi.com.

- [LatticeSC PURESPEED I/O Usage Guide](#) (TN1088)
- [LatticeSC PURESPEED I/O Adaptive Input Logic User's Guide](#) (TN1158)
- [LatticeSC sysCLOCK PLL/DLL User's Guide](#) (TN1098)
- [On-Chip Memory Usage Guide for LatticeSC Devices](#) (TN1094)
- [LatticeSC/M DDR/DDR2 SDRAM Memory Interface User's Guide](#) (TN1099)
- [LatticeSC QDRII/II+ SRAM Memory Interface User's Guide](#) (TN1096)
- [LatticeSC sysCONFIG Usage Guide](#) (TN1080)
- [LatticeSC MPI/System Bus](#) (TN1085)
- [SPI Serial Flash Programming Using ispJTAG in LatticeSC Devices](#) (TN1100)
- [Power Estimation and Management for LatticeSC Devices](#) (TN1101)
- [LatticeSC SERDES Jitter](#) (TN1084)
- [LatticeSC FPGAs: Implementing 3.3V Interfaces in 2.5V VCCIO Banks](#) (TN1110)
- [Lattice PCI Express Basic Demo User's Guide](#) (UG08)
- [LatticeSC flexiPCS/SERDES Design Guide](#) (TN1145)
- [Temperature Sensing Diode in LatticeSC Devices](#) (TN1115)
- [SPI4.2 Interoperability Between ORSPI4 and LatticeSC Devices](#) (TN1116)

For further information on Interface standards refer to the following websites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- Optical Interface (SPI-4.2, XSBI, CSIX and XGMII): www.oiforum.com
- RAPIDIO: www.rapidio.org
- PCI/PCIX: www.pcisig.com

Date	Version	Section	Change Summary
March 2007 (cont.)	01.5 (cont.)	DC and Switching Characteristics (cont.)	Updated LatticeSC Internal Timing Parameters with ispLEVER 6.1 SP1 results.
			Updated t_{FDEL} and t_{CDEL} specifications.
			Updated LatticeSC Family Timing Adders with ispLEVER 6.1 SP1 results.
			Updated PLL specifications to expand frequency range down to 2 MHz and break out jitter for the different ranges.
			Added footnote to sysCLOCK PLL Timing table specifying the conditions for the jitter measurements.
			Added t_{DLL} specification to sysCLOCK DLL Timing table.
			Added footnote to sysCLOCK DLL Timing table specifying the conditions for the jitter measurements.
			Added sysCONFIG Master Parallel Configuration Mode and sysCONFIG SPI Port to LatticeSC sysCONFIG Port Timing table.
		Pin Information	Updated Pin Information Summary with SC40 information.
			Updated LFSC25 Logic Signal Connections: FF1020 with SC40 information.
			Updated LFSC80 Logic Signal Connections: FC1152 with SC40 information.
August 2007	01.6	General	Changed references of "HDC" to "HDC/SI".
			Changed references of "LDCN" to "LDCN/SCS".
			Changed references of "BUSYN/RCLK" to "BUSYN/RCLK/SCK".
			Changed references of "RDCFGN" to "TSALLN".
			Changed references of "TDO/RDDATA" to "TDO".
		Architecture	Updated text in Ripple Mode section.
			Added information to Global Set/Reset.
			Added information for Spread Spectrum Clocking
			Modified information for PLL/DLL Cascading. DLL to PLL is now supported.
			Modified AIL Block text and figure.
			Modified Figure 2-20 DDR/Shift Register Block.
			Added Information to Hot Socketing.
			Added new information for I/O Architecture Rules.
			Added information to SERDES Power Supply Sequencing Requirements.
		DC and Switching Characteristics	Added footnote to Hot Socketing Specifications table.
			Modified Initialization and Standby Supply Current table.
			Modified GSR Timing table.
			Modified sysCLOCK DLL Timing table to include I_{DUTY} .
			Deleted Readback Timing information from sysCONFIG Port Timing table.
			Modified data in External Switching Characteristics table.
		Pin Information	Added information to the Signal Descriptions table for HDC/SI, LDCN/SCS.
			Added footnote to Signal Descriptions table.
			Modified Description for signal BUSYN/RCLK/SCK.
			Modified data in Pin Information Summary and device-specific Pinout Information tables.