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## Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

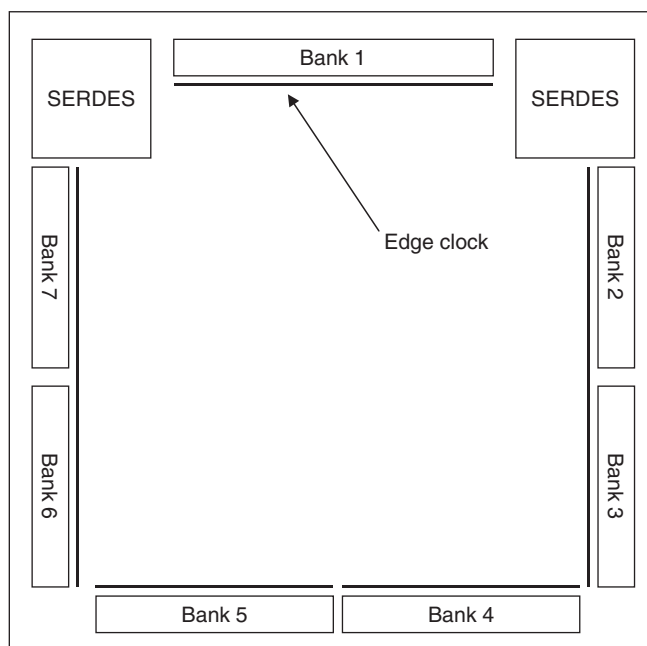
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

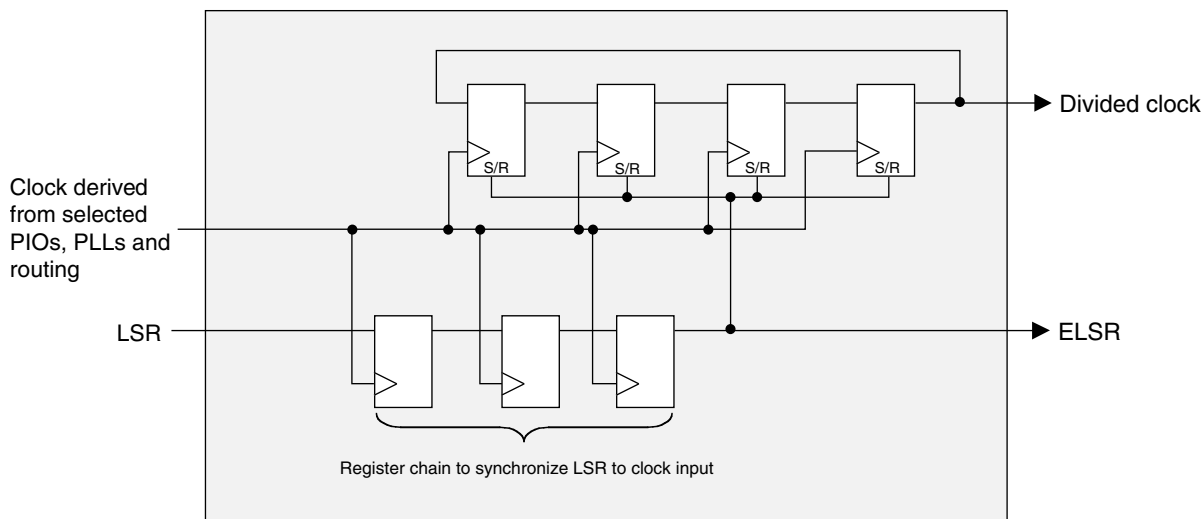
### Details

|                                |                                                                                                                                                                                   |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                                                                          |
| Number of LABs/CLBs            | 10000                                                                                                                                                                             |
| Number of Logic Elements/Cells | 40000                                                                                                                                                                             |
| Total RAM Bits                 | 4075520                                                                                                                                                                           |
| Number of I/O                  | 604                                                                                                                                                                               |
| Number of Gates                | -                                                                                                                                                                                 |
| Voltage - Supply               | 0.95V ~ 1.26V                                                                                                                                                                     |
| Mounting Type                  | Surface Mount                                                                                                                                                                     |
| Operating Temperature          | -40°C ~ 105°C (Tj)                                                                                                                                                                |
| Package / Case                 | 1152-BBGA, FCBGA                                                                                                                                                                  |
| Supplier Device Package        | 1152-FCBGA (35x35)                                                                                                                                                                |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga40ep1-5ff1152i">https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga40ep1-5ff1152i</a> |

**Figure 2-7. Edge Clock Resources**

### Precision Clock Divider

Each set of edge clocks has four high-speed dividers associated with it. These are intended for generating a slower speed system clock from the high-speed edge clock. The block operates in a DIV2 or DIV4 mode and maintains a known phase relationship between the divided down clock and high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PIOs, PLLs and routing. The clock divider outputs serve as primary clock sources. This circuit also generates an edge local set/reset (ELSR) signal which is fed to the PIOs via the edge clock network and is used for the rest of the I/O gearing logic.

**Figure 2-8. Clock Divider Circuit**

### Dynamic Clock Select (DCS)

The DCS is a global clock buffer with smart multiplexer functions. It takes two independent input clock sources and outputs a clock signal without any glitches or runt pulses. This is achieved irrespective of where the select signal is

**Table 2-6. Input/Output/Tristate Gearing Resource Rules**

| PIO | Input/Output Logic |              |              | Tri-State/Bidi |       |
|-----|--------------------|--------------|--------------|----------------|-------|
|     | x1                 | x2           | x4           | x1             | x2/x4 |
| A   | ?                  | ?            | ?            | ?              | N/A   |
| B   | ?                  | No I/O Logic | No I/O Logic | ?              | N/A   |
| C   | ?                  | ?            | No I/O Logic | ?              | N/A   |
| D   | ?                  | No I/O Logic | No I/O Logic | ?              | N/A   |

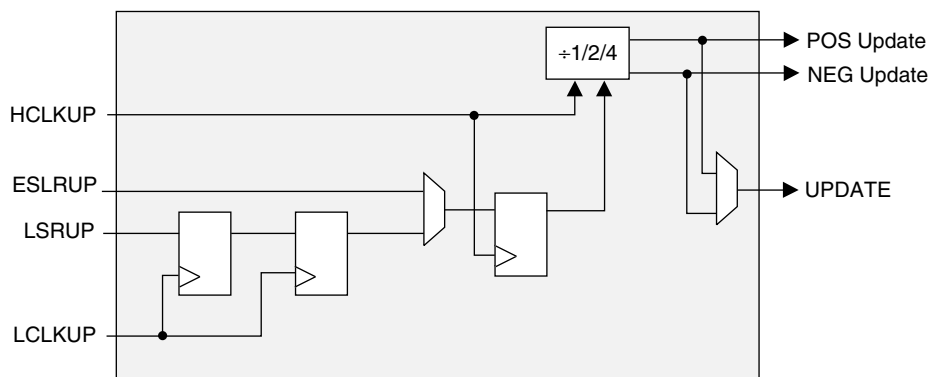
Note: Pin can still be used without I/O logic.

## Control Logic Block

The control logic block allows the modification of control signals selected by the routing before they are used in the PIO. It can optionally invert all signals passing through it except the Global Set/Reset. Global Set/Reset can be enabled or disabled. It can route either the edge clock or the clock to the high-speed clock nets. The clock provided to the PIO by routing is used as the slow-speed clocks. In addition this block contains delays that can be inserted in the clock nets to enable Lattice's unique cycle boosting capability.

## Update Block

The update block is used to generate the POS update and NEG update signals used by the DDR/Shift register blocks within the PIO. Note the update block is only required in shift modes. This is required in order to do the high speed to low speed handoff. One of these update signals is also selected and output from the PIC as the signal UPDATE. It consists of a shift chain that operates off either the high-speed input or output clock. The values of each register in the chain are set or reset depending on the desired mode of operation. The set/reset signal is generated from either the edge reset ELSR or the local reset LSR. These signals are optionally inverted by the Control Logic Block and provided to the update block as ELSRUP and LSRUP. The Lattice design tools automatically configure and connect the update block when one of the DDR or shift register primitives is used.

**Figure 2-25. Update Block**

## PURESPEED I/O Buffer

Each I/O is associated with a flexible buffer referred to as PURESPEED I/O buffer. These buffers are arranged around the periphery of the device in seven groups referred to as Banks. The PURESPEED I/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL. The availability of programmable on-chip termination for both input and output use, further enhances the utility of these buffers.

**3. Bottom Side (Banks 4 and 5)**

These buffers can support LVCMOS standards up to 3.3V, including PCI33, PCI-X33 and SSTL-33. Differential receivers are provided on all PIO pairs but true HLVDS and RSDS differential drivers are not available. Adaptive input logic is available on PIOs A or C.

Table 2-8 lists the standards supported by each side.

**Table 2-8. I/O Standards Supported by Different Banks**

| Description                                  | Top Side<br>Banks 1                                                                                                                                                                                                                                                                                                                                                                                                      | Right Side<br>Banks 2-3                                                                                                                                                                                                                                                           | Bottom Side<br>Banks 4-5                                                                                                                                                                                                                                                                                                                                                                                                 | Left Side<br>Banks 6-7                                                                                                                                                                                                                                                            |
|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I/O Buffer Type                              | Single-ended,<br>Differential Receiver                                                                                                                                                                                                                                                                                                                                                                                   | Single-ended, Differen-<br>tial Receiver and Driver                                                                                                                                                                                                                               | Single-ended,<br>Differential Receiver                                                                                                                                                                                                                                                                                                                                                                                   | Single-ended, Differen-<br>tial Receiver and Driver                                                                                                                                                                                                                               |
| Output Standards<br>Supported                | LVTTL<br>LVCMOS33<br>LVCMOS25<br>LVCMOS18<br>LVCMOS15<br>LVCMOS12<br>SSTL18_I, II<br>SSTL25_I, II<br>SSTL33_I, II<br>HSTL15_I, II, III <sup>1</sup> , IV <sup>1</sup><br>HSTL18_I, II, III <sup>1</sup> , IV <sup>1</sup><br>SSTL18D_I, II<br>SSTL25D_I, II<br>SSTL33D_I, II<br>HSTL15D_I, II<br>HSTL18D_I, II<br>PCI33<br>PCIX15<br>PCIX33<br>AGP1X33<br>AGP2X33<br>MLVDS/BLVDS<br>GTL <sup>2</sup> , GTL+ <sup>2</sup> | LVCMOS25<br>LVCMOS18<br>LVCMOS15<br>LVCMOS12<br>SSTL18_I, II<br>SSTL25_I, II<br>HSTL15_I, III<br>HSTL18_I, II, III<br>PCIX15<br>SSTL18D_I, II<br>SSTL25D_I, II<br>HSTL15D_I, II<br>HSTL18D_I, II<br>LVDS/RSDS<br>Mini-LVDS<br>MLVDS/BLVDS<br>GTL <sup>2</sup> , GTL+ <sup>2</sup> | LVTTL<br>LVCMOS33<br>LVCMOS25<br>LVCMOS18<br>LVCMOS15<br>LVCMOS12<br>SSTL18_I, II<br>SSTL25_I, II<br>SSTL33_I, II<br>HSTL15_I, II, III <sup>1</sup> , IV <sup>1</sup><br>HSTL18_I, II, III <sup>1</sup> , IV <sup>1</sup><br>SSTL18D_I, II<br>SSTL25D_I, II<br>SSTL33D_I, II<br>HSTL15D_I, II<br>HSTL18D_I, II<br>PCI33<br>PCIX15<br>PCIX33<br>AGP1X33<br>AGP2X33<br>MLVDS/BLVDS<br>GTL <sup>2</sup> , GTL+ <sup>2</sup> | LVCMOS25<br>LVCMOS18<br>LVCMOS15<br>LVCMOS12<br>SSTL18_I, II<br>SSTL25_I, II<br>HSTL15_I, III<br>HSTL18_I, II, III<br>PCIX15<br>SSTL18D_I, II<br>SSTL25D_I, II<br>HSTL15D_I, II<br>HSTL18D_I, II<br>LVDS/RSDS<br>Mini-LVDS<br>MLVDS/BLVDS<br>GTL <sup>2</sup> , GTL+ <sup>2</sup> |
| Input Standards<br>Supported                 | Single-ended,<br>Differential                                                                                                                                                                                                                                                                                                                                                                                            | Single-ended,<br>Differential                                                                                                                                                                                                                                                     | Single-ended,<br>Differential                                                                                                                                                                                                                                                                                                                                                                                            | Single-ended,<br>Differential                                                                                                                                                                                                                                                     |
| Clock Inputs                                 | Single-ended,<br>Differential                                                                                                                                                                                                                                                                                                                                                                                            | Single-ended,<br>Differential                                                                                                                                                                                                                                                     | Single-ended,<br>Differential                                                                                                                                                                                                                                                                                                                                                                                            | Single-ended,<br>Differential                                                                                                                                                                                                                                                     |
| Differential Output<br>Support via Emulation | LVDS/MLVDS/BLVDS/<br>LVPECL                                                                                                                                                                                                                                                                                                                                                                                              | MLVDS/BLVDS/<br>LVPECL                                                                                                                                                                                                                                                            | LVDS/MLVDS/BLVDS/<br>LVPECL                                                                                                                                                                                                                                                                                                                                                                                              | MLVDS/BLVDS/<br>LVPECL                                                                                                                                                                                                                                                            |
| AIL Support                                  | No                                                                                                                                                                                                                                                                                                                                                                                                                       | Yes                                                                                                                                                                                                                                                                               | Yes                                                                                                                                                                                                                                                                                                                                                                                                                      | Yes                                                                                                                                                                                                                                                                               |

1. Input only.

2. Input only. Outputs supported by bussing multiple outputs together.

## Supported Standards

The LatticeSC PURESPEED I/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 12, 15, 18, 25 and 33 standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, termination resistance, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL, HSTL, GTL (input only), GTL+ (input only), PCI33, PCIX33, PCIX15, AGP-1X33 and AGP-2X33. Differential standards supported include LVDS, RSDS, BLVDS, MLVDS, LVPECL, differential SSTL and differential HSTL. Tables 12 and 13 show the I/O standards (together with their supply and reference voltages) supported by the LatticeSC devices. The tables also provide the available internal termination schemes. For further information on utilizing the PURESPEED I/O buffer to support a variety of standards please see details of additional technical documentation at the end of this data sheet.

**Table 2-9. Supported Input Standards**

| Input Standard                          | V <sub>REF</sub> (Nom.) | V <sub>CCIO</sub> <sup>1</sup> (Nom.) | On-chip Termination                                                                                                                                |
|-----------------------------------------|-------------------------|---------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Single Ended Interfaces</b>          |                         |                                       |                                                                                                                                                    |
| LVTTL33 <sup>3</sup>                    | —                       | 3.3                                   | None                                                                                                                                               |
| LVC MOS 33, 25, 18, 15, 12 <sup>3</sup> | —                       | 3.3/2.5/1.8/1.5/1.2                   | None                                                                                                                                               |
| PCI33, PCIX33, AGP1X33 <sup>3</sup>     | —                       | 3.3                                   | None                                                                                                                                               |
| PCIX15                                  | 0.75                    | 1.5 <sup>2</sup>                      | None / V <sub>CCIO</sub> / 2: 50, 60/ V <sub>TT</sub> : 60, 75, 120, 210                                                                           |
| AGP2X33                                 | 1.32                    | —                                     | None                                                                                                                                               |
| HSTL18_I, II                            | 0.9                     | 1.8 <sup>2</sup>                      | None / V <sub>CCIO</sub> / 2: 50, 60/ V <sub>TT</sub> : 60, 75, 120, 210                                                                           |
| HSTL18_III, IV                          | 1.08                    | 1.8 <sup>2</sup>                      | None / V <sub>CCIO</sub> : 50                                                                                                                      |
| HSTL15_I, II                            | 0.75                    | 1.5 <sup>2</sup>                      | None / V <sub>CCIO</sub> / 2: 50, 60/ V <sub>TT</sub> : 60, 75, 120, 210                                                                           |
| HSTL15_III, IV                          | 0.9                     | 1.5 <sup>2</sup>                      | None / V <sub>CCIO</sub> : 50                                                                                                                      |
| SSTL33_I, II                            | 1.5                     | 3.3                                   | None                                                                                                                                               |
| SSTL25_I, II                            | 1.25                    | 2.5 <sup>2</sup>                      | None / V <sub>CCIO</sub> / 2: 50, 60/ V <sub>TT</sub> : 60, 75, 120, 210                                                                           |
| SSTL18_I, II                            | 0.9                     | 1.8 <sup>2</sup>                      | None / V <sub>CCIO</sub> / 2: 50, 60/ V <sub>TT</sub> : 60, 75, 120, 210                                                                           |
| GTL+, GTL                               | 1.0 / 0.8               | 1.5 / 1.2 <sup>2</sup>                | None / V <sub>CCIO</sub> : 50                                                                                                                      |
| <b>Differential Interfaces</b>          |                         |                                       |                                                                                                                                                    |
| SSTL18D_I, II                           | —                       | 1.8 <sup>2</sup>                      | None / Diff: 120, 150, 220, 420/ Diff to V <sub>CMT</sub> : 120, 150, 220, 420 / V <sub>CCIO</sub> / 2: 50, 60/ V <sub>TT</sub> : 60, 75, 120, 210 |
| SSTL25D_I, II                           | —                       | 2.5 <sup>2</sup>                      | None / Diff: 120, 150, 220, 420/ Diff to V <sub>CMT</sub> : 120, 150, 220, 420 / V <sub>CCIO</sub> / 2: 50, 60/ V <sub>TT</sub> : 60, 75, 120, 210 |
| SSTL33D_I, II                           | —                       | 3.3                                   | None                                                                                                                                               |
| HSTL15D_I, II                           | —                       | 1.5 <sup>2</sup>                      | None / Diff: 120, 150, 220, 420/ Diff to V <sub>CMT</sub> : 120, 150, 220, 420 / V <sub>CCIO</sub> / 2: 50, 60/ V <sub>TT</sub> : 60, 75, 120, 210 |
| HSTL18D_I, II                           | —                       | 1.8 <sup>2</sup>                      | None / Diff: 120, 150, 220, 420/ Diff to V <sub>CMT</sub> : 120, 150, 220, 420 / V <sub>CCIO</sub> / 2: 50, 60/ V <sub>TT</sub> : 60, 75, 120, 210 |
| LVDS                                    | —                       | —                                     | None / Diff: 120, 150, 220, 240/ Diff to V <sub>CMT</sub> : 120, 150, 220, 240                                                                     |
| Mini-LVDS                               | —                       | —                                     | None / Diff: 120, 150 / Diff to V <sub>CMT</sub> : 120, 150                                                                                        |
| BLVDS25                                 | —                       | —                                     | None                                                                                                                                               |
| MLVDS25                                 | —                       | —                                     | None                                                                                                                                               |
| RSDS                                    | —                       | —                                     | None / Diff: 120, 150, 220, 240/ Diff to V <sub>CMT</sub> : 120, 150, 220, 240                                                                     |
| LVPECL33                                | —                       | ≤2.5                                  | None / Diff: 120, 150, 220, 240/ Diff to V <sub>CMT</sub> : 120, 150, 220, 240                                                                     |

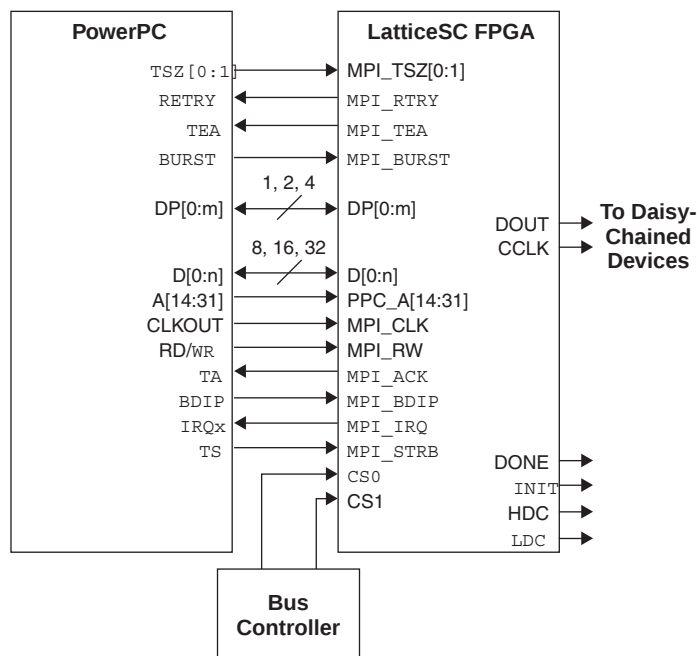
1. When not specified V<sub>CCIO</sub> can be set anywhere in the valid operating range.

2. V<sub>CCIO</sub> needed for on-chip termination to V<sub>CCIO</sub>/2 or V<sub>CCIO</sub> only. V<sub>CCIO</sub> is not specified for off-chip termination or V<sub>TT</sub> termination.

3. All ratioed input buffers and dedicated pin input buffers include hysteresis with a typical value of 50mV.

**Figure 2-27. Output Termination Schemes**

| Termination Type                                                                                              | Discrete Off-Chip Solution | Lattice On-Chip Solution |
|---------------------------------------------------------------------------------------------------------------|----------------------------|--------------------------|
| Series termination (controlled output impedance)                                                              |                            |                          |
| Parallel termination to $V_{CCIO}$ , or parallel driving end                                                  |                            |                          |
| Parallel termination to $V_{CCIO}/2$ driving end                                                              |                            |                          |
| Combined series + parallel termination to $V_{CCIO}/2$ at driving end (only series termination moved on-chip) |                            |                          |
| Combined series + parallel to $V_{CCIO}/2$ driving end                                                        |                            |                          |

**Figure 2-32. PowerPCI and MPI Schematic**

## Configuration and Testing

The following section describes the configuration and testing features of the LatticeSC family of devices.

### IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeSC devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage  $V_{CCJ}$  and can operate with LVCMOS33, 25 and 18 standards. For additional detail refer to technical information at the end of the data sheet.

### Device Configuration

All LatticeSC devices contain three possible ports that can be used for device configuration. The serial port, which supports bit-wide configuration, and the sysCONFIG port that supports both byte-wide and serial configuration. The MPI port supports 8-bit, 16-bit or 32-bit configuration.

The serial port supports both the IEEE Std. 1149.1 Boundary Scan specification and the IEEE Std. 1532 In-System Configuration specification. The sysCONFIG port is a 20-pin interface with six of the I/Os used as dedicated pins and the rest being dual-use pins. When sysCONFIG mode is not used, these dual-use pins are available for general purpose I/O. All I/Os for the sysCONFIG and MPI ports are in I/O bank #1.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port. Once a configuration port is selected, that port is locked and another configuration port cannot be activated until the next re-initialization sequence. For additional detail refer to technical information at the end of the data sheet.

## Power Supply Ramp Rates

| Symbol            | Parameter                                      | Condition                          | Min. | Typ. | Max | Units       |
|-------------------|------------------------------------------------|------------------------------------|------|------|-----|-------------|
| $t_{\text{RAMP}}$ | Power supply ramp rates for all power supplies | Over process, voltage, temperature | 3.45 | —    | —   | mV/ $\mu$ s |
|                   |                                                |                                    | —    | —    | 75  | ms          |

1. See the Power-up and Power-Down requirements section for more details on power sequencing.
2. From 0.5V to minimum operating voltage.

## Hot Socketing Specifications<sup>1</sup>

| Symbol            | Parameter                                                                            | Condition                                              | Min. | Typ. | Max        | Units   |
|-------------------|--------------------------------------------------------------------------------------|--------------------------------------------------------|------|------|------------|---------|
| $I_{\text{DK}}$   | Programmable and dedicated Input or I/O leakage current <sup>2, 3, 4, 5, 6</sup>     | $0 \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$ | —    | —    | $\pm 1500$ | $\mu$ A |
| $I_{\text{HDIN}}$ | SERDES average input current when device powered down and inputs driven <sup>7</sup> |                                                        | —    | —    | 4          | mA      |

1. See Hot Socket power up/down information in Chapter 2 of this document.
2. Assumes monotonic rise/fall rates for all power supplies.
3. Sensitive to power supply sequencing as described in hot socketing section.
4. Assumes power supplies are between 0 and maximum recommended operations conditions.
5.  $I_{\text{DK}}$  is additive to  $I_{\text{PU}}$ ,  $I_{\text{PD}}$  or  $I_{\text{BH}}$ .
6. Represents DC conditions. For the first 20ns after hot insertion, current specification is 8 mA.
7. Assumes that the device is powered down with all supplies grounded, both P and N inputs driven by a CML driver with maximum allowed VDDOB of 1.575V, 8b/10b data and internal AC coupling.

## DC Electrical Characteristics<sup>5</sup>

### Over Recommended Operating Conditions

| Symbol                           | Parameter                                | Condition                                                                                                                                                                                                                                    | Min. <sup>3</sup>                                | Typ. | Max.                         | Units   |
|----------------------------------|------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------|------|------------------------------|---------|
| $I_{\text{IL}}, I_{\text{IH}}^1$ | Input or I/O Low leakage                 | $0 \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$                                                                                                                                                                                       | —                                                | —    | 10                           | $\mu$ A |
| $I_{\text{PU}}$                  | I/O Active Pull-up Current               | $0 \leq V_{\text{IN}} \leq 0.7 V_{\text{CCIO}}$                                                                                                                                                                                              | -30                                              | —    | -210                         | $\mu$ A |
| $I_{\text{PD}}$                  | I/O Active Pull-down Current             | $V_{\text{IL}} (\text{MAX}) \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$                                                                                                                                                              | 30                                               | —    | 210                          | $\mu$ A |
| $I_{\text{BHLS}}$                | Bus Hold Low Sustaining Current          | $V_{\text{IN}} = V_{\text{IL}} (\text{MAX})$                                                                                                                                                                                                 | 30                                               | —    | —                            | $\mu$ A |
| $I_{\text{BHHS}}$                | Bus Hold High Sustaining Current         | $V_{\text{IN}} = 0.7 V_{\text{CCIO}}$                                                                                                                                                                                                        | -30                                              | —    | —                            | $\mu$ A |
| $I_{\text{BHLO}}$                | Bus Hold Low Overdrive Current           | $0 \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$                                                                                                                                                                                       | —                                                | —    | 210                          | $\mu$ A |
| $I_{\text{BHLH}}$                | Bus Hold High Overdrive Current          | $0 \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$                                                                                                                                                                                       | —                                                | —    | -210                         | $\mu$ A |
| $I_{\text{CL}}$                  | PCI Low Clamp Current                    | $-3 < V_{\text{IN}} \leq -1$                                                                                                                                                                                                                 | $-25 + (V_{\text{IN}} + 1)/0.015$                | —    | —                            | mA      |
| $I_{\text{CH}}$                  | PCI High Clamp Current                   | $V_{\text{CC}} + 4 > V_{\text{IN}} \geq V_{\text{CC}} + 1$                                                                                                                                                                                   | $25 + (V_{\text{IN}} - V_{\text{CC}} - 1)/0.015$ | —    | —                            | mA      |
| $V_{\text{BHT}}$                 | Bus Hold trip Points                     | $0 \leq V_{\text{IN}} \leq V_{\text{IH}} (\text{MAX})$                                                                                                                                                                                       | $V_{\text{IL}} (\text{MAX})$                     | —    | $V_{\text{IH}} (\text{MIN})$ | V       |
| C1                               | I/O Capacitance <sup>2</sup>             | $V_{\text{CCIO}} = 3.3\text{V}, 2.5\text{V}, 1.8\text{V}, 1.5\text{V}, 1.2\text{V},$<br>$V_{\text{CC}} = 1.2\text{V}, V_{\text{CCIP2}} = 1.2\text{V},$<br>$V_{\text{CCAUX}} = 2.5, V_{\text{IO}} = 0 \text{ to } V_{\text{IH}} (\text{MAX})$ | —                                                | 8    | —                            | pf      |
| C3 <sup>2</sup>                  | Dedicated Input Capacitance <sup>2</sup> | $V_{\text{CCIO}} = 3.3\text{V}, 2.5\text{V}, 1.8\text{V}, 1.5\text{V}, 1.2\text{V},$<br>$V_{\text{CC}} = 1.2\text{V}, V_{\text{CCIP2}} = 1.2\text{V},$<br>$V_{\text{CCAUX}} = 2.5, V_{\text{IO}} = 0 \text{ to } V_{\text{IH}} (\text{MAX})$ | —                                                | 6    | —                            | pf      |

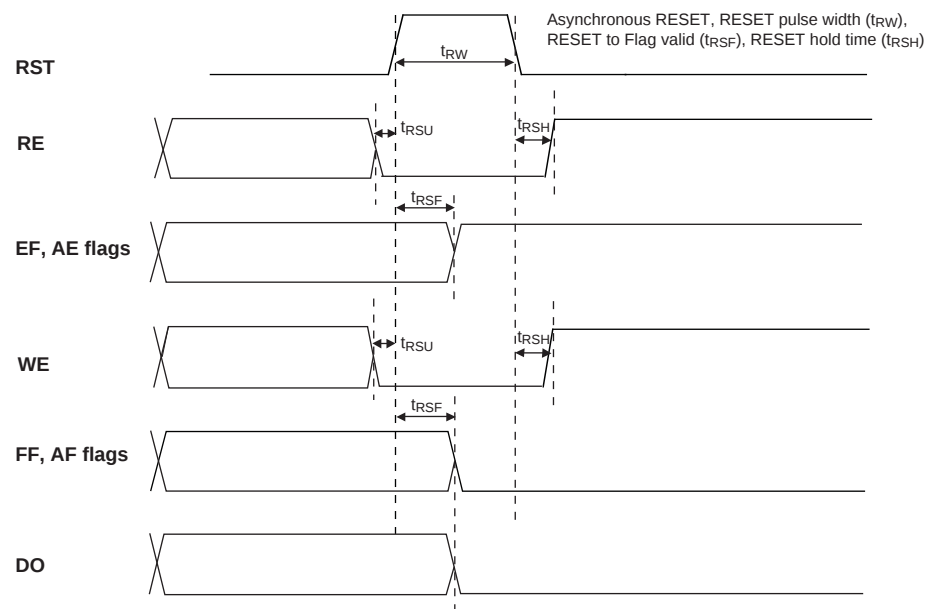
1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2.  $T_{\text{A}} = 25^{\circ}\text{C}$ ,  $f = 1.0\text{MHz}$
3.  $I_{\text{PU}}$ ,  $I_{\text{PD}}$ ,  $I_{\text{BHLS}}$  and  $I_{\text{BHHS}}$  have minimum values of 15 or -15 $\mu$ A if  $V_{\text{CCIO}}$  is set to 1.2V nominal.
4. This table does not apply to SERDES pins.
5. For programmable I/Os.

**LatticeSC/M Internal Timing Parameters<sup>1</sup>**

Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

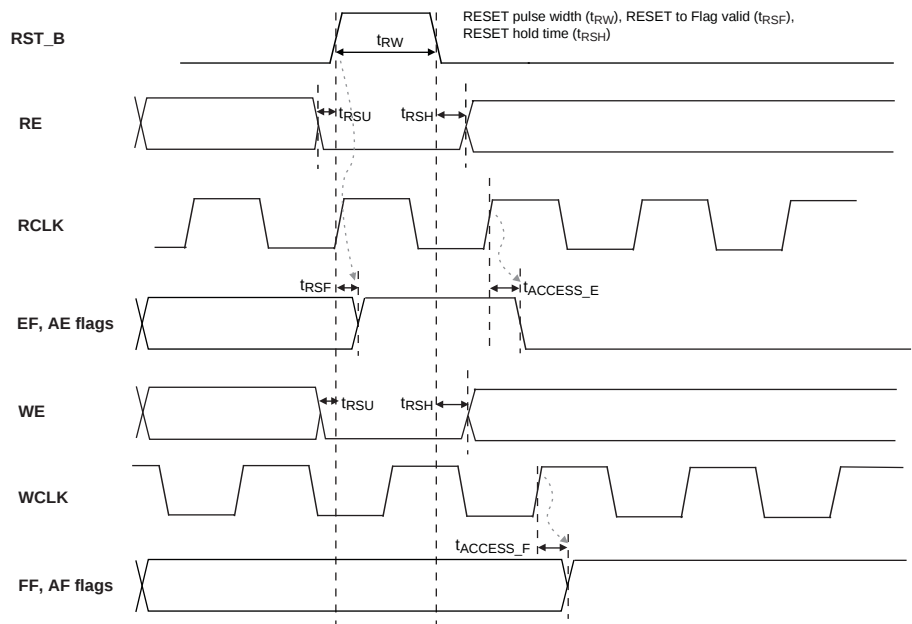
| Parameter                      | Symbol     | Description                                                  | -7     |       | -6     |       | -5     |       | Units |
|--------------------------------|------------|--------------------------------------------------------------|--------|-------|--------|-------|--------|-------|-------|
|                                |            |                                                              | Min.   | Max.  | Min.   | Max.  | Min.   | Max.  |       |
| PFU Logic Mode Timing          |            |                                                              |        |       |        |       |        |       |       |
| t <sub>LUT4_PFU</sub>          | CTOF_DEL   | LUT4 delay (A to D inputs to F output)                       | —      | 0.045 | —      | 0.050 | —      | 0.054 | ns    |
| t <sub>LUT5_PFU</sub>          | MTOOFX_DEL | LUT5 delay (inputs to output)                                | —      | 0.152 | —      | 0.172 | —      | 0.192 | ns    |
| t <sub>LSR_PFU</sub>           | LSR_DEL    | Set/Reset to output (asynchronous)                           | —      | 0.378 | —      | 0.426 | —      | 0.474 | ns    |
| t <sub>SUM_PFU</sub>           | M_SET      | Clock to Mux (M0,M1) input setup time                        | 0.113  | —     | 0.131  | —     | 0.148  | —     | ns    |
| t <sub>HM_PFU</sub>            | M_HLD      | Clock to Mux (M0,M1) input hold time                         | -0.041 | —     | -0.046 | —     | -0.052 | —     | ns    |
| t <sub>SUD_PFU</sub>           | DIN_SET    | Clock to D input setup time                                  | 0.072  | —     | 0.083  | —     | 0.094  | —     | ns    |
| t <sub>HD_PFU</sub>            | DIN_HLD    | Clock to D input hold time                                   | -0.028 | —     | -0.032 | —     | -0.035 | —     | ns    |
| t <sub>CK2Q_PFU</sub>          | REG_DEL    | Clock to Q delay, D-type register configuration              | —      | 0.224 | —      | 0.252 | —      | 0.279 | ns    |
| t <sub>LE2Q_PFU</sub>          | LTCH_DEL   | Clock to Q delay latch configuration                         | —      | 0.294 | —      | 0.331 | —      | 0.367 | ns    |
| t <sub>LD2Q_PFU</sub>          | TLTCH_DEL  | D to Q throughput delay when latch is enabled                | —      | 0.300 | —      | 0.338 | —      | 0.376 | ns    |
| PFU Memory Mode Timing         |            |                                                              |        |       |        |       |        |       |       |
| t <sub>CORAM_PFU</sub>         | CLKTOF_DEL | Clock to Output                                              | —      | 0.575 | —      | 0.649 | —      | 0.724 | ns    |
| t <sub>SUDATA_PFU</sub>        | DIN_SET    | Data Setup Time                                              | -0.024 | —     | -0.026 | —     | -0.027 | —     | ns    |
| t <sub>HDATA_PFU</sub>         | DIN_HLD    | Data Hold Time                                               | 0.075  | —     | 0.084  | —     | 0.094  | —     | ns    |
| t <sub>SUADDR_PFU</sub>        | WAD_SET    | Address Setup Time                                           | -0.176 | —     | -0.196 | —     | -0.215 | —     | ns    |
| t <sub>HADDR_PFU</sub>         | WAD_HLD    | Address Hold Time                                            | 0.110  | —     | 0.124  | —     | 0.138  | —     | ns    |
| t <sub>SUWREN_PFU</sub>        | WE_SET     | Write/Read Enable Setup Time                                 | 0.014  | —     | 0.019  | —     | 0.024  | —     | ns    |
| t <sub>HWREN_PFU</sub>         | WE_HLD     | Write/Read Enable Hold Time                                  | 0.078  | —     | 0.086  | —     | 0.094  | —     | ns    |
| PIC Timing                     |            |                                                              |        |       |        |       |        |       |       |
| PIO Input/Output Buffer Timing |            |                                                              |        |       |        |       |        |       |       |
| t <sub>IN_PIO</sub>            | IN_DEL     | Input Buffer Delay(LVCMOS25)                                 | —      | 0.578 | —      | 0.661 | —      | 0.744 | ns    |
| t <sub>OUT_PIO</sub>           | DOPADI_DEL | Output Buffer Delay(LVCMOS25)                                | —      | 2.712 | —      | 3.027 | —      | 3.395 | ns    |
| t <sub>SUI_PIO</sub>           | DIN_SET    | Input Register Setup Time (Data Before Clock)                | 0.277  | —     | 0.312  | —     | 0.348  | —     | ns    |
| t <sub>HI_PIO</sub>            | DIN_HLD    | Input Register Hold Time (Data after Clock)                  | -0.267 | —     | -0.306 | —     | -0.345 | —     | ns    |
| t <sub>COO_PIO</sub>           | CK_DEL     | Output Register Clock to Output Delay                        | —      | 0.513 | —      | 0.571 | —      | 0.639 | ns    |
| t <sub>SUCE_PIO</sub>          | CE_SET     | Input Register Clock Enable Setup Time                       | —      | 0.000 | —      | 0.000 | —      | 0.000 | ns    |
| t <sub>HCE_PIO</sub>           | CE_HLD     | Input Register Clock Enable Hold Time                        | —      | 0.129 | —      | 0.145 | —      | 0.161 | ns    |
| t <sub>SULSR_PIO</sub>         | LSR_SET    | Set/Reset Setup Time                                         | 0.057  | —     | 0.060  | —     | 0.063  | —     | ns    |
| t <sub>HLSR_PIO</sub>          | LSR_HLD    | Set/Reset Hold Time                                          | -0.151 | —     | -0.159 | —     | -0.169 | —     | ns    |
| t <sub>LE2Q_PIO</sub>          | CK_DEL     | Input Register Clock to Q delay latch configuration          | —      | 0.335 | —      | 0.372 | —      | 0.410 | ns    |
| t <sub>LD2Q_PIO</sub>          | DIN_DEL    | Input Register D to Q throughput delay when latch is enabled | —      | 0.578 | —      | 0.647 | —      | 0.717 | ns    |

Figure 3-10. FIFO Reset Waveform



Note: RE and WE must be deactivated  $t_{RSU}$  before the Positive FIFO reset edge and enabled  $t_{RSH}$  after the FIFO reset negative edge.

Figure 3-11. Read Pointer Reset Waveform



Note: RE and WE must be deactivated  $t_{RSU}$  before the Positive FIFO reset edge and enabled  $t_{RSH}$  after the FIFO reset negative edge.

Switching Test Conditions

Figure 3-15 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-4.

Figure 3-15. Output Test Load, LVTTTL and LVCMOS Standards

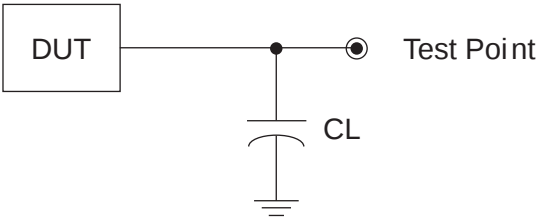


Table 3-4. Test Fixture Required Components, Non-Terminated Interfaces

| Test Condition                                    | C <sub>L</sub> | Timing Ref.                       | V <sub>T</sub>  |
|---------------------------------------------------|----------------|-----------------------------------|-----------------|
| LVTTTL and other LVCMOS settings (L -> H, H -> L) | 30pF           | LVCMOS 3.3 = 1.5V                 | —               |
|                                                   |                | LVCMOS 2.5 = V <sub>CCIO</sub> /2 | —               |
|                                                   |                | LVCMOS 1.8 = V <sub>CCIO</sub> /2 | —               |
|                                                   |                | LVCMOS 1.5 = V <sub>CCIO</sub> /2 | —               |
|                                                   |                | LVCMOS 1.2 = V <sub>CCIO</sub> /2 | —               |
| LVCMOS 2.5 I/O (Z -> H)                           | 30pF           | V <sub>CCIO</sub> /2              | V <sub>OL</sub> |
| LVCMOS 2.5 I/O (Z -> L)                           |                | V <sub>CCIO</sub> /2              | V <sub>OH</sub> |
| LVCMOS 2.5 I/O (H -> Z)                           |                | V <sub>OH</sub> - 0.15            | V <sub>OL</sub> |
| LVCMOS 2.5 I/O (L -> Z)                           |                | V <sub>OL</sub> + 0.15            | V <sub>OH</sub> |

Note: Output test conditions for all other interfaces are determined by the respective standards.

**LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA<sup>1, 2</sup> (Cont.)**

| Ball Number | LFSC/M15      |            |                             | LFSC/M25      |            |                             |
|-------------|---------------|------------|-----------------------------|---------------|------------|-----------------------------|
|             | Ball Function | VCCIO Bank | Dual Function               | Ball Function | VCCIO Bank | Dual Function               |
| AF4         | PB3C          | 5          | LLC_DLLT_IN_C/LLC_DLLT_FB_D | PB3C          | 5          | LLC_DLLT_IN_C/LLC_DLLT_FB_D |
| AE5         | PB3D          | 5          | LLC_DLLC_IN_C/LLC_DLLC_FB_D | PB3D          | 5          | LLC_DLLC_IN_C/LLC_DLLC_FB_D |
| AG3         | PB4A          | 5          | LLC_DLLT_IN_D/LLC_DLLT_FB_C | PB4A          | 5          | LLC_DLLT_IN_D/LLC_DLLT_FB_C |
| AH2         | PB4B          | 5          | LLC_DLLC_IN_D/LLC_DLLC_FB_C | PB4B          | 5          | LLC_DLLC_IN_D/LLC_DLLC_FB_C |
| AD6         | PB4C          | 5          |                             | PB4C          | 5          |                             |
| AJ2         | PB5A          | 5          |                             | PB5A          | 5          |                             |
| AK2         | PB5B          | 5          |                             | PB5B          | 5          |                             |
| AD7         | PB5C          | 5          |                             | PB5C          | 5          |                             |
| AD8         | PB5D          | 5          | VREF1_5                     | PB5D          | 5          | VREF1_5                     |
| AH3         | PB7A          | 5          |                             | PB11A         | 5          |                             |
| AJ3         | PB7B          | 5          |                             | PB11B         | 5          |                             |
| AF9         | PB7C          | 5          |                             | PB11C         | 5          |                             |
| AE10        | PB7D          | 5          |                             | PB11D         | 5          |                             |
| AK3         | PB8A          | 5          |                             | PB12A         | 5          |                             |
| AJ4         | PB8B          | 5          |                             | PB12B         | 5          |                             |
| AE11        | PB9A          | 5          |                             | PB13A         | 5          |                             |
| AF10        | PB9B          | 5          |                             | PB13B         | 5          |                             |
| AK4         | PB11A         | 5          |                             | PB16A         | 5          |                             |
| AK5         | PB11B         | 5          |                             | PB16B         | 5          |                             |
| AH10        | PB12A         | 5          | PCLKT5_3                    | PB20A         | 5          | PCLKT5_3                    |
| AH11        | PB12B         | 5          | PCLKC5_3                    | PB20B         | 5          | PCLKC5_3                    |
| AF13        | PB12C         | 5          | PCLKT5_4                    | PB20C         | 5          | PCLKT5_4                    |
| AE14        | PB12D         | 5          | PCLKC5_4                    | PB20D         | 5          | PCLKC5_4                    |
| AK6         | PB13A         | 5          | PCLKT5_5                    | PB21A         | 5          | PCLKT5_5                    |
| AK7         | PB13B         | 5          | PCLKC5_5                    | PB21B         | 5          | PCLKC5_5                    |
| AF14        | PB13C         | 5          |                             | PB21C         | 5          |                             |
| AJ11        | PB15A         | 5          | PCLKT5_0                    | PB23A         | 5          | PCLKT5_0                    |
| AJ12        | PB15B         | 5          | PCLKC5_0                    | PB23B         | 5          | PCLKC5_0                    |
| AH13        | PB15D         | 5          | VREF2_5                     | PB23D         | 5          | VREF2_5                     |
| AK8         | PB16A         | 5          | PCLKT5_1                    | PB24A         | 5          | PCLKT5_1                    |
| AK9         | PB16B         | 5          | PCLKC5_1                    | PB24B         | 5          | PCLKC5_1                    |
| AH14        | PB17A         | 5          | PCLKT5_2                    | PB25A         | 5          | PCLKT5_2                    |
| AG14        | PB17B         | 5          | PCLKC5_2                    | PB25B         | 5          | PCLKC5_2                    |
| AK10        | PB19A         | 5          |                             | PB28A         | 5          |                             |
| AK11        | PB19B         | 5          |                             | PB28B         | 5          |                             |
| AH15        | PB20A         | 5          |                             | PB29A         | 5          |                             |
| AG15        | PB20B         | 5          |                             | PB29B         | 5          |                             |
| AH12        | PB21A         | 5          |                             | PB31A         | 5          |                             |
| AJ13        | PB21B         | 5          |                             | PB31B         | 5          |                             |
| AD15        | PB21C         | 5          |                             | PB31C         | 5          |                             |
| AE15        | PB21D         | 5          |                             | PB31D         | 5          |                             |
| AK12        | PB23A         | 5          |                             | PB32A         | 5          |                             |
| AK13        | PB23B         | 5          |                             | PB32B         | 5          |                             |
| AJ14        | PB24A         | 5          |                             | PB33A         | 5          |                             |
| AJ15        | PB24B         | 5          |                             | PB33B         | 5          |                             |

**LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA<sup>1, 2</sup> (Cont.)**

| Ball Number | LFSC/M40      |            |               | LFSC/M80      |            |               |
|-------------|---------------|------------|---------------|---------------|------------|---------------|
|             | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AL11        | GND           | -          |               | GND           | -          |               |
| AL17        | GND           | -          |               | GND           | -          |               |
| AL21        | GND           | -          |               | GND           | -          |               |
| AL27        | GND           | -          |               | GND           | -          |               |
| AL5         | GND           | -          |               | GND           | -          |               |
| AM14        | GND           | -          |               | GND           | -          |               |
| AM18        | GND           | -          |               | GND           | -          |               |
| AM24        | GND           | -          |               | GND           | -          |               |
| AM30        | GND           | -          |               | GND           | -          |               |
| AM8         | GND           | -          |               | GND           | -          |               |
| AN1         | GND           | -          |               | GND           | -          |               |
| AN34        | GND           | -          |               | GND           | -          |               |
| AP2         | GND           | -          |               | GND           | -          |               |
| AP33        | GND           | -          |               | GND           | -          |               |
| B1          | GND           | -          |               | GND           | -          |               |
| B34         | GND           | -          |               | GND           | -          |               |
| C11         | GND           | -          |               | GND           | -          |               |
| C12         | GND           | -          |               | GND           | -          |               |
| C13         | GND           | -          |               | GND           | -          |               |
| C14         | GND           | -          |               | GND           | -          |               |
| C17         | GND           | -          |               | GND           | -          |               |
| C21         | GND           | -          |               | GND           | -          |               |
| C22         | GND           | -          |               | GND           | -          |               |
| C23         | GND           | -          |               | GND           | -          |               |
| C24         | GND           | -          |               | GND           | -          |               |
| C26         | GND           | -          |               | GND           | -          |               |
| C27         | GND           | -          |               | GND           | -          |               |
| C30         | GND           | -          |               | GND           | -          |               |
| C31         | GND           | -          |               | GND           | -          |               |
| C4          | GND           | -          |               | GND           | -          |               |
| C5          | GND           | -          |               | GND           | -          |               |
| C8          | GND           | -          |               | GND           | -          |               |
| C9          | GND           | -          |               | GND           | -          |               |
| D18         | GND           | -          |               | GND           | -          |               |
| E32         | GND           | -          |               | GND           | -          |               |
| E4          | GND           | -          |               | GND           | -          |               |
| F19         | GND           | -          |               | GND           | -          |               |
| G16         | GND           | -          |               | GND           | -          |               |
| G29         | GND           | -          |               | GND           | -          |               |
| G7          | GND           | -          |               | GND           | -          |               |
| H3          | GND           | -          |               | GND           | -          |               |
| H31         | GND           | -          |               | GND           | -          |               |
| J10         | GND           | -          |               | GND           | -          |               |
| J15         | GND           | -          |               | GND           | -          |               |
| J26         | GND           | -          |               | GND           | -          |               |

**LFSC/M115 Logic Signal Connections: 1152 fcBGA<sup>1, 2</sup>**

| Ball Number | LFSC/M115     |            |               |
|-------------|---------------|------------|---------------|
|             | Ball Function | VCCIO Bank | Dual Function |
| N27         | PL47C         | 7          |               |
| P27         | PL47D         | 7          |               |
| K33         | PL49A         | 7          |               |
| L33         | PL49B         | 7          |               |
| M30         | PL49C         | 7          |               |
| N30         | PL49D         | 7          |               |
| M31         | PL51A         | 7          |               |
| N31         | PL51B         | 7          |               |
| P24         | PL51C         | 7          |               |
| R24         | PL51D         | 7          |               |
| M33         | PL56A         | 7          |               |
| N33         | PL56B         | 7          |               |
| U25         | PL56C         | 7          |               |
| T25         | PL56D         | 7          |               |
| L34         | PL57A         | 7          |               |
| M34         | PL57B         | 7          |               |
| P29         | PL57C         | 7          |               |
| R29         | PL57D         | 7          |               |
| N34         | PL60A         | 7          |               |
| P34         | PL60B         | 7          |               |
| R27         | PL60C         | 7          |               |
| T27         | PL60D         | 7          |               |
| R32         | PL61A         | 7          | PCLKT7_1      |
| R31         | PL61B         | 7          | PCLKC7_1      |
| U24         | PL61C         | 7          | PCLKT7_3      |
| T24         | PL61D         | 7          | PCLKC7_3      |
| P33         | PL62A         | 7          | PCLKT7_0      |
| R33         | PL62B         | 7          | PCLKC7_0      |
| T26         | PL62C         | 7          | PCLKT7_2      |
| U26         | PL62D         | 7          | PCLKC7_2      |
| T32         | PL64A         | 6          | PCLKT6_0      |
| T31         | PL64B         | 6          | PCLKC6_0      |
| U29         | PL64C         | 6          | PCLKT6_1      |
| V29         | PL64D         | 6          | PCLKC6_1      |
| T30         | PL65A         | 6          |               |
| U30         | PL65B         | 6          |               |
| U27         | PL65C         | 6          | PCLKT6_3      |
| V27         | PL65D         | 6          | PCLKC6_3      |
| R34         | PL66A         | 6          |               |
| T34         | PL66B         | 6          |               |
| U28         | PL66C         | 6          | PCLKT6_2      |
| V28         | PL66D         | 6          | PCLKC6_2      |
| V30         | PL69A         | 6          |               |

**LFSC/M115 Logic Signal Connections: 1152 fcBGA<sup>1, 2</sup>**

| Ball Number | LFSC/M115     |            |                    |
|-------------|---------------|------------|--------------------|
|             | Ball Function | VCCIO Bank | Dual Function      |
| F6          | A_VDDOB0_R    | -          |                    |
| B4          | A_HDOUTN0_R   | -          | PCS 3E0 CH 0 OUT N |
| F7          | A_VDDOB1_R    | -          |                    |
| B5          | A_HDOUTN1_R   | -          | PCS 3E0 CH 1 OUT N |
| E6          | VCC12         | -          |                    |
| A5          | A_HDOUTP1_R   | -          | PCS 3E0 CH 1 OUT P |
| B6          | A_HDINN1_R    | -          | PCS 3E0 CH 1 IN N  |
| A6          | A_HDINP1_R    | -          | PCS 3E0 CH 1 IN P  |
| C6          | VCC12         | -          |                    |
| D4          | A_VDDIB1_R    | -          |                    |
| C7          | VCC12         | -          |                    |
| D5          | A_VDDIB2_R    | -          |                    |
| A7          | A_HDINP2_R    | -          | PCS 3E0 CH 2 IN P  |
| B7          | A_HDINN2_R    | -          | PCS 3E0 CH 2 IN N  |
| E7          | VCC12         | -          |                    |
| A8          | A_HDOUTP2_R   | -          | PCS 3E0 CH 2 OUT P |
| F8          | A_VDDOB2_R    | -          |                    |
| B8          | A_HDOUTN2_R   | -          | PCS 3E0 CH 2 OUT N |
| F9          | A_VDDOB3_R    | -          |                    |
| B9          | A_HDOUTN3_R   | -          | PCS 3E0 CH 3 OUT N |
| E8          | VCC12         | -          |                    |
| A9          | A_HDOUTP3_R   | -          | PCS 3E0 CH 3 OUT P |
| B10         | A_HDINN3_R    | -          | PCS 3E0 CH 3 IN N  |
| A10         | A_HDINP3_R    | -          | PCS 3E0 CH 3 IN P  |
| C10         | VCC12         | -          |                    |
| D6          | A_VDDIB3_R    | -          |                    |
| G10         | VCC12         | -          |                    |
| D7          | B_VDDIB0_R    | -          |                    |
| E10         | B_HDINP0_R    | -          | PCS 3E1 CH 0 IN P  |
| F10         | B_HDINN0_R    | -          | PCS 3E1 CH 0 IN N  |
| K10         | VCC12         | -          |                    |
| A11         | B_HDOUTP0_R   | -          | PCS 3E1 CH 0 OUT P |
| D10         | B_VDDOB0_R    | -          |                    |
| B11         | B_HDOUTN0_R   | -          | PCS 3E1 CH 0 OUT N |
| D11         | B_VDDOB1_R    | -          |                    |
| B12         | B_HDOUTN1_R   | -          | PCS 3E1 CH 1 OUT N |
| L10         | VCC12         | -          |                    |
| A12         | B_HDOUTP1_R   | -          | PCS 3E1 CH 1 OUT P |
| F11         | B_HDINN1_R    | -          | PCS 3E1 CH 1 IN N  |
| E11         | B_HDINP1_R    | -          | PCS 3E1 CH 1 IN P  |
| G11         | VCC12         | -          |                    |
| D8          | B_VDDIB1_R    | -          |                    |
| G12         | VCC12         | -          |                    |

**LFSC/M115 Logic Signal Connections: 1152 fcBGA<sup>1, 2</sup>**

| Ball Number | LFSC/M115     |            |                         |
|-------------|---------------|------------|-------------------------|
|             | Ball Function | VCCIO Bank | Dual Function           |
| J17         | PT81C         | 1          | D20/PCLKT1_2/MPI_DATA20 |
| D16         | PT81B         | 1          | MCA_CLK_P1_OUT          |
| E16         | PT81A         | 1          | MCA_CLK_P1_IN           |
| H15         | PT78D         | 1          | D21/PCLKC1_1/MPI_DATA21 |
| H16         | PT78C         | 1          | D22/PCLKT1_1/MPI_DATA22 |
| C15         | PT78B         | 1          | MCA_CLK_P2_OUT          |
| C16         | PT78A         | 1          | MCA_CLK_P2_IN           |
| L17         | PT75D         | 1          | MCA_DONE_OUT            |
| K17         | PT75C         | 1          | BUSYN/RCLK/SCK          |
| E17         | PT75B         | 1          | DP0/MPI_PAR0            |
| F17         | PT75A         | 1          | MPI_TA                  |
| G17         | PT73D         | 1          | D23/MPI_DATA23          |
| H17         | PT73C         | 1          | DP2/MPI_PAR2            |
| A17         | PT73B         | 1          | PCLKC1_0                |
| B17         | PT73A         | 1          | PCLKT1_0/MPI_CLK        |
| G18         | PT71D         | 1          | DP3/PCLKC1_4/MPI_PAR3   |
| H18         | PT71C         | 1          | D24/PCLKT1_4/MPI_DATA24 |
| E18         | PT71B         | 1          | MPI_RETRY               |
| F18         | PT71A         | 1          | A0/MPI_ADDR14           |
| J18         | PT69D         | 1          | A1/MPI_ADDR15           |
| J19         | PT69C         | 1          | A2/MPI_ADDR16           |
| C20         | PT69B         | 1          | A3/MPI_ADDR17           |
| C19         | PT69A         | 1          | A4/MPI_ADDR18           |
| K18         | PT66D         | 1          | D25/PCLKC1_5/MPI_DATA25 |
| L18         | PT66C         | 1          | D26/PCLKT1_5/MPI_DATA26 |
| D19         | PT66B         | 1          | A5/MPI_ADDR19           |
| E19         | PT66A         | 1          | A6/MPI_ADDR20           |
| H19         | PT63D         | 1          | D27/MPI_DATA27          |
| H20         | PT63C         | 1          | VREF1_1                 |
| A18         | PT63B         | 1          | A7/MPI_ADDR21           |
| B18         | PT63A         | 1          | A8/MPI_ADDR22           |
| H21         | PT61D         | 1          | D28/PCLKC1_6/MPI_DATA28 |
| J21         | PT61C         | 1          | D29/PCLKT1_6/MPI_DATA29 |
| A19         | PT61B         | 1          | A9/MPI_ADDR23           |
| B19         | PT61A         | 1          | A10/MPI_ADDR24          |
| H22         | PT58D         | 1          | D30/PCLKC1_7/MPI_DATA30 |
| J22         | PT58C         | 1          | D31/PCLKT1_7/MPI_DATA31 |
| F20         | PT58B         | 1          | A11/MPI_ADDR25          |
| G20         | PT58A         | 1          | A12/MPI_ADDR26          |
| K21         | PT57D         | 1          | D11/MPI_DATA11          |
| K22         | PT57C         | 1          | D12/MPI_DATA12          |
| A20         | PT57B         | 1          | A13/MPI_ADDR27          |
| B20         | PT57A         | 1          | A14/MPI_ADDR28          |

**LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA<sup>1, 2</sup> (Cont.)**

| Ball Number | LFSC/M80      |            |               | LFSC/M115     |            |               |
|-------------|---------------|------------|---------------|---------------|------------|---------------|
|             | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| BA19        | PB73A         | 4          |               | PB87A         | 4          |               |
| BA18        | PB73B         | 4          |               | PB87B         | 4          |               |
| AU19        | PB73C         | 4          |               | PB87C         | 4          |               |
| AU18        | PB73D         | 4          |               | PB87D         | 4          |               |
| AV19        | PB74A         | 4          | PCLKT4_2      | PB89A         | 4          | PCLKT4_2      |
| AV18        | PB74B         | 4          | PCLKC4_2      | PB89B         | 4          | PCLKC4_2      |
| AN19        | PB74C         | 4          | PCLKT4_7      | PB89C         | 4          | PCLKT4_7      |
| AP19        | PB74D         | 4          | PCLKC4_7      | PB89D         | 4          | PCLKC4_7      |
| BB17        | PB75A         | 4          | PCLKT4_1      | PB90A         | 4          | PCLKT4_1      |
| BB16        | PB75B         | 4          | PCLKC4_1      | PB90B         | 4          | PCLKC4_1      |
| AT19        | PB75C         | 4          | PCLKT4_6      | PB90C         | 4          | PCLKT4_6      |
| AT18        | PB75D         | 4          | PCLKC4_6      | PB90D         | 4          | PCLKC4_6      |
| BA17        | PB77A         | 4          | PCLKT4_0      | PB91A         | 4          | PCLKT4_0      |
| BA16        | PB77B         | 4          | PCLKC4_0      | PB91B         | 4          | PCLKC4_0      |
| AR19        | PB77C         | 4          | VREF2_4       | PB91C         | 4          | VREF2_4       |
| AR18        | PB77D         | 4          |               | PB91D         | 4          |               |
| AY17        | PB79A         | 4          | PCLKT4_5      | PB93A         | 4          | PCLKT4_5      |
| AY16        | PB79B         | 4          | PCLKC4_5      | PB93B         | 4          | PCLKC4_5      |
| AN18        | PB79C         | 4          |               | PB93C         | 4          |               |
| AP18        | PB79D         | 4          |               | PB93D         | 4          |               |
| AW17        | PB80A         | 4          | PCLKT4_3      | PB94A         | 4          | PCLKT4_3      |
| AW16        | PB80B         | 4          | PCLKC4_3      | PB94B         | 4          | PCLKC4_3      |
| AU17        | PB80C         | 4          | PCLKT4_4      | PB94C         | 4          | PCLKT4_4      |
| AU16        | PB80D         | 4          | PCLKC4_4      | PB94D         | 4          | PCLKC4_4      |
| AV17        | PB81A         | 4          |               | PB95A         | 4          |               |
| AV16        | PB81B         | 4          |               | PB95B         | 4          |               |
| AL18        | PB81C         | 4          |               | PB95C         | 4          |               |
| AM18        | PB81D         | 4          |               | PB95D         | 4          |               |
| BB15        | PB83A         | 4          |               | PB97A         | 4          |               |
| BB14        | PB83B         | 4          |               | PB97B         | 4          |               |
| AP17        | PB83C         | 4          |               | PB97C         | 4          |               |
| AN17        | PB83D         | 4          |               | PB97D         | 4          |               |
| BA15        | PB84A         | 4          |               | PB98A         | 4          |               |
| BA14        | PB84B         | 4          |               | PB98B         | 4          |               |
| AT16        | PB84C         | 4          |               | PB98C         | 4          |               |
| AT15        | PB84D         | 4          |               | PB98D         | 4          |               |
| AV15        | PB85A         | 4          |               | PB99A         | 4          |               |
| AV14        | PB85B         | 4          |               | PB99B         | 4          |               |
| AR16        | PB85C         | 4          |               | PB99C         | 4          |               |
| AR15        | PB85D         | 4          |               | PB99D         | 4          |               |
| AY14        | PB87A         | 4          |               | PB101A        | 4          |               |
| AY13        | PB87B         | 4          |               | PB101B        | 4          |               |
| AU15        | PB87C         | 4          |               | PB101C        | 4          |               |
| AU14        | PB87D         | 4          |               | PB101D        | 4          |               |
| BB13        | PB88A         | 4          |               | PB102A        | 4          |               |

**LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA<sup>1, 2</sup> (Cont.)**

| Ball Number | LFSC/M80      |            |               | LFSC/M115     |            |               |
|-------------|---------------|------------|---------------|---------------|------------|---------------|
|             | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AE1         | PR74A         | 3          |               | PR88A         | 3          |               |
| AF12        | PR73D         | 3          |               | PR87D         | 3          |               |
| AE12        | PR73C         | 3          |               | PR87C         | 3          |               |
| AF2         | PR73B         | 3          |               | PR87B         | 3          |               |
| AE2         | PR73A         | 3          |               | PR87A         | 3          |               |
| AF11        | PR72D         | 3          |               | PR86D         | 3          |               |
| AE11        | PR72C         | 3          |               | PR86C         | 3          |               |
| AF5         | PR72B         | 3          |               | PR86B         | 3          |               |
| AE5         | PR72A         | 3          |               | PR86A         | 3          |               |
| AF10        | PR69D         | 3          |               | PR83D         | 3          |               |
| AE10        | PR69C         | 3          |               | PR83C         | 3          |               |
| AD1         | PR69B         | 3          |               | PR83B         | 3          |               |
| AC1         | PR69A         | 3          |               | PR83A         | 3          |               |
| AF9         | PR68D         | 3          |               | PR82D         | 3          |               |
| AE9         | PR68C         | 3          |               | PR82C         | 3          |               |
| AD2         | PR68B         | 3          |               | PR82B         | 3          |               |
| AC2         | PR68A         | 3          |               | PR82A         | 3          |               |
| AF6         | PR67D         | 3          |               | PR81D         | 3          |               |
| AE6         | PR67C         | 3          |               | PR81C         | 3          |               |
| AD3         | PR67B         | 3          |               | PR81B         | 3          |               |
| AC3         | PR67A         | 3          |               | PR81A         | 3          |               |
| AE8         | PR65D         | 3          |               | PR79D         | 3          |               |
| AD8         | PR65C         | 3          |               | PR79C         | 3          |               |
| AD4         | PR65B         | 3          |               | PR79B         | 3          |               |
| AC4         | PR65A         | 3          |               | PR79A         | 3          |               |
| AE7         | PR64D         | 3          |               | PR78D         | 3          |               |
| AD7         | PR64C         | 3          |               | PR78C         | 3          |               |
| AD5         | PR64B         | 3          |               | PR78B         | 3          |               |
| AC5         | PR64A         | 3          |               | PR78A         | 3          |               |
| AD6         | PR63D         | 3          |               | PR77D         | 3          |               |
| AC6         | PR63C         | 3          |               | PR77C         | 3          |               |
| AB1         | PR63B         | 3          |               | PR77B         | 3          |               |
| AA1         | PR63A         | 3          |               | PR77A         | 3          |               |
| AD9         | PR61D         | 3          |               | PR75D         | 3          |               |
| AC9         | PR61C         | 3          |               | PR75C         | 3          |               |
| AB2         | PR61B         | 3          |               | PR75B         | 3          |               |
| AA2         | PR61A         | 3          |               | PR75A         | 3          |               |
| AD14        | PR60D         | 3          |               | PR74D         | 3          |               |
| AC14        | PR60C         | 3          |               | PR74C         | 3          |               |
| AB5         | PR60B         | 3          |               | PR74B         | 3          |               |
| AA5         | PR60A         | 3          |               | PR74A         | 3          |               |
| AD10        | PR59D         | 3          |               | PR73D         | 3          |               |
| AC10        | PR59C         | 3          |               | PR73C         | 3          |               |
| Y1          | PR59B         | 3          |               | PR73B         | 3          |               |
| W1          | PR59A         | 3          |               | PR73A         | 3          |               |

**LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA<sup>1, 2</sup> (Cont.)**

| Ball Number | LFSC/M80      |            |               | LFSC/M115     |            |               |
|-------------|---------------|------------|---------------|---------------|------------|---------------|
|             | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AB25        | VCC           | -          |               | VCC           | -          |               |
| AB26        | VCC           | -          |               | VCC           | -          |               |
| AC16        | VCC           | -          |               | VCC           | -          |               |
| AC18        | VCC           | -          |               | VCC           | -          |               |
| AC20        | VCC           | -          |               | VCC           | -          |               |
| AC23        | VCC           | -          |               | VCC           | -          |               |
| AC25        | VCC           | -          |               | VCC           | -          |               |
| AC27        | VCC           | -          |               | VCC           | -          |               |
| AD17        | VCC           | -          |               | VCC           | -          |               |
| AD19        | VCC           | -          |               | VCC           | -          |               |
| AD21        | VCC           | -          |               | VCC           | -          |               |
| AD22        | VCC           | -          |               | VCC           | -          |               |
| AD24        | VCC           | -          |               | VCC           | -          |               |
| AD26        | VCC           | -          |               | VCC           | -          |               |
| AE16        | VCC           | -          |               | VCC           | -          |               |
| AE18        | VCC           | -          |               | VCC           | -          |               |
| AE20        | VCC           | -          |               | VCC           | -          |               |
| AE21        | VCC           | -          |               | VCC           | -          |               |
| AE22        | VCC           | -          |               | VCC           | -          |               |
| AE23        | VCC           | -          |               | VCC           | -          |               |
| AE25        | VCC           | -          |               | VCC           | -          |               |
| AE27        | VCC           | -          |               | VCC           | -          |               |
| AF17        | VCC           | -          |               | VCC           | -          |               |
| AF19        | VCC           | -          |               | VCC           | -          |               |
| AF21        | VCC           | -          |               | VCC           | -          |               |
| AF22        | VCC           | -          |               | VCC           | -          |               |
| AF24        | VCC           | -          |               | VCC           | -          |               |
| AF26        | VCC           | -          |               | VCC           | -          |               |
| AG18        | VCC           | -          |               | VCC           | -          |               |
| AG20        | VCC           | -          |               | VCC           | -          |               |
| AG23        | VCC           | -          |               | VCC           | -          |               |
| AG25        | VCC           | -          |               | VCC           | -          |               |
| T18         | VCC           | -          |               | VCC           | -          |               |
| T20         | VCC           | -          |               | VCC           | -          |               |
| T23         | VCC           | -          |               | VCC           | -          |               |
| T25         | VCC           | -          |               | VCC           | -          |               |
| U17         | VCC           | -          |               | VCC           | -          |               |
| U19         | VCC           | -          |               | VCC           | -          |               |
| U21         | VCC           | -          |               | VCC           | -          |               |
| U22         | VCC           | -          |               | VCC           | -          |               |
| U24         | VCC           | -          |               | VCC           | -          |               |
| U26         | VCC           | -          |               | VCC           | -          |               |
| V16         | VCC           | -          |               | VCC           | -          |               |
| V18         | VCC           | -          |               | VCC           | -          |               |
| V20         | VCC           | -          |               | VCC           | -          |               |

**LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA<sup>1, 2</sup> (Cont.)**

| Ball Number | LFSC/M80      |            |               | LFSC/M115     |            |               |
|-------------|---------------|------------|---------------|---------------|------------|---------------|
|             | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AH22        | VTT_5         | 5          |               | VTT_5         | 5          |               |
| AJ22        | VTT_5         | 5          |               | VTT_5         | 5          |               |
| AJ23        | VTT_5         | 5          |               | VTT_5         | 5          |               |
| AJ24        | VTT_5         | 5          |               | VTT_5         | 5          |               |
| AJ25        | VTT_5         | 5          |               | VTT_5         | 5          |               |
| AB28        | VTT_6         | 6          |               | VTT_6         | 6          |               |
| AB29        | VTT_6         | 6          |               | VTT_6         | 6          |               |
| AE29        | VTT_6         | 6          |               | VTT_6         | 6          |               |
| AJ30        | VTT_6         | 6          |               | VTT_6         | 6          |               |
| AA28        | VTT_7         | 7          |               | VTT_7         | 7          |               |
| AA29        | VTT_7         | 7          |               | VTT_7         | 7          |               |
| R31         | VTT_7         | 7          |               | VTT_7         | 7          |               |
| V29         | VTT_7         | 7          |               | VTT_7         | 7          |               |
| Y24         | GND           | -          |               | GND           | -          |               |
| Y26         | GND           | -          |               | GND           | -          |               |
| Y8          | GND           | -          |               | GND           | -          |               |
| Y35         | GND           | -          |               | GND           | -          |               |
| AA16        | VCC12         | -          |               | VCC12         | -          |               |
| AA27        | VCC12         | -          |               | VCC12         | -          |               |
| AB16        | VCC12         | -          |               | VCC12         | -          |               |
| AB27        | VCC12         | -          |               | VCC12         | -          |               |
| AF16        | VCC12         | -          |               | VCC12         | -          |               |
| AF27        | VCC12         | -          |               | VCC12         | -          |               |
| AG17        | VCC12         | -          |               | VCC12         | -          |               |
| AG21        | VCC12         | -          |               | VCC12         | -          |               |
| G33         | NC            | -          |               | NC            | -          |               |
| G10         | NC            | -          |               | NC            | -          |               |
| M15         | NC            | -          |               | NC            | -          |               |
| L15         | NC            | -          |               | NC            | -          |               |
| K16         | NC            | -          |               | NC            | -          |               |
| J16         | NC            | -          |               | NC            | -          |               |
| M18         | NC            | -          |               | NC            | -          |               |
| L18         | NC            | -          |               | NC            | -          |               |
| M25         | NC            | -          |               | NC            | -          |               |
| L25         | NC            | -          |               | NC            | -          |               |
| J27         | NC            | -          |               | NC            | -          |               |
| K27         | NC            | -          |               | NC            | -          |               |
| L28         | NC            | -          |               | NC            | -          |               |
| M28         | NC            | -          |               | NC            | -          |               |

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).

2. The LatticeSC/M80 and LatticeSC/M115 in a 1704-pin package supports a 32-bit MPI interface.

## Industrial, Cont.

| Part Number                       | Grade | Package       | Balls | Temp. | LUTs (K) |
|-----------------------------------|-------|---------------|-------|-------|----------|
| LFSC3GA115E-6FC1152I <sup>1</sup> | -6    | Ceramic fcBGA | 1152  | IND   | 115.2    |
| LFSC3GA115E-5FC1152I <sup>1</sup> | -5    | Ceramic fcBGA | 1152  | IND   | 115.2    |
| LFSC3GA115E-6FF1152I              | -6    | Organic fcBGA | 1152  | IND   | 115.2    |
| LFSC3GA115E-5FF1152I              | -5    | Organic fcBGA | 1152  | IND   | 115.2    |
| LFSC3GA115E-6FC1704I <sup>1</sup> | -6    | Ceramic fcBGA | 1704  | IND   | 115.2    |
| LFSC3GA115E-5FC1704I <sup>1</sup> | -5    | Ceramic fcBGA | 1704  | IND   | 115.2    |
| LFSC3GA115E-6FF1704I              | -6    | Organic fcBGA | 1704  | IND   | 115.2    |
| LFSC3GA115E-5FF1704I              | -5    | Organic fcBGA | 1704  | IND   | 115.2    |

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

| Part Number                          | Grade | Package       | Balls | Temp. | LUTs (K) |
|--------------------------------------|-------|---------------|-------|-------|----------|
| LFSCM3GA115EP1-6FC1152I <sup>1</sup> | -6    | Ceramic fcBGA | 1152  | IND   | 115.2    |
| LFSCM3GA115EP1-5FC1152I <sup>1</sup> | -5    | Ceramic fcBGA | 1152  | IND   | 115.2    |
| LFSCM3GA115EP1-6FF1152I              | -6    | Organic fcBGA | 1152  | IND   | 115.2    |
| LFSCM3GA115EP1-5FF1152I              | -5    | Organic fcBGA | 1152  | IND   | 115.2    |
| LFSCM3GA115EP1-6FC1704I <sup>1</sup> | -6    | Ceramic fcBGA | 1704  | IND   | 115.2    |
| LFSCM3GA115EP1-5FC1704I <sup>1</sup> | -5    | Ceramic fcBGA | 1704  | IND   | 115.2    |
| LFSCM3GA115EP1-6FF1704I              | -6    | Organic fcBGA | 1704  | IND   | 115.2    |
| LFSCM3GA115EP1-5FF1704I              | -5    | Organic fcBGA | 1704  | IND   | 115.2    |

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).