# Lattice Semiconductor Corporation - LFSCM3GA40EP1-6FCN1152I Datasheet



**Welcome to E-XFL.COM**

### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 10000 |
| Number of Logic Elements/Cells | 40000 |
| Total RAM Bits | 4075520 |
| Number of I/O | 604 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 105°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga40ep1-6fcn1152i |

## Architecture Overview

The LatticeSC architecture contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM Embedded Block RAM (EBR). The upper left and upper right corners of the devices contain SERDES blocks and their associated PCS blocks, as show in Figure 2-1.

Top left and top right corner of the device contain blocks of SERDES. Each block of SERDES contains four channels (quad). Each channel contains a single serializer and de-serializer, synchronization and word alignment logic. The SERDES quad connects with the Physical Coding Sub-layer (PCS) blocks that contain logic to simultaneously perform alignment, coding, de-coding and other functions. The SERDES quad block has separate supply, ground and reference voltage pins.

The PICs contain logic to facilitate the conditioning of signals to and from the I/O before they leave or enter the FPGA fabric. The block provides DDR and shift register capabilities that act as a gearbox between high speed I/O and the FPGA fabric. The blocks also contain programmable Adaptive Input Logic that adjusts the delay applied to signals as they enter the device to optimize setup and hold times and ensure robust performance.

sysMEM EBRs are large dedicated fast memory blocks. They can be configured as RAM, ROM or FIFO. These blocks have dedicated logic to simplify the implementation of FIFOs.

The PFU, PIC and EBR blocks are arranged in a two-dimensional grid with rows and columns as shown in Figure 2-1. These blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

The corners contain the sysCLOCK Analog Phase Locked Loop (PLL) and Delay Locked Loop (DLL) Blocks. The PLLs have multiply, divide and phase shifting capability; they are used to manage the phase relationship of the clocks. The LatticeSC architecture provides eight analog PLLs per device and 12 DLLs. The DLLs provide a simple delay capability and can also be used to calibrate other delays within the device.

Every device in the family has a JTAG Port with internal Logic Analyzer (ispTRACY) capability. The sysCONFIG™ port which allows for serial or parallel device configuration. The system bus simplifies the connections of the external microprocessor to the device for tasks such as SERDES and PCS configuration or interface to the general FPGA logic. The LatticeSC devices use 1.2V as their core voltage operation with 1.0V operation also possible.

toggled. There are eight DCS blocks per device, located in pairs at the center of each side. Figure 2-9 illustrates the DCS Block diagram.

***Figure 2-9. DCS Block Diagram***

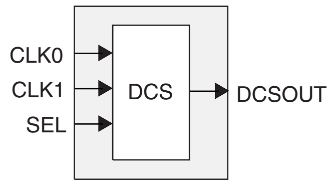
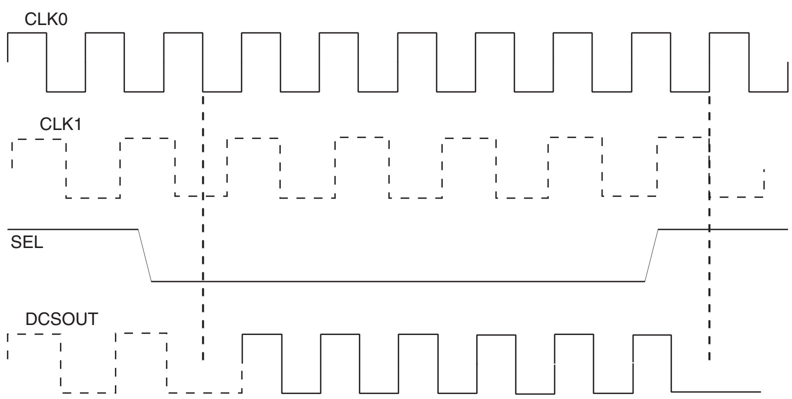



Figure 2-10 shows timing waveforms for one of the DCS operating modes. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

***Figure 2-10. DCS Waveforms***




### Clock Boosting

There are programmable delays available in the clock signal paths in the PFU, PIC and EBR blocks. These allow setup and clock-to-output times to be traded to meet critical timing without slowing the system clock. If this feature is enabled then the design tool automatically uses these delays to improve timing performance.

## Global Set/Reset

There is a global set/reset (GSR) network on the device that is distributed to all FFs, PLLs, DLLs and other blocks on the device. This GSR network can operate in two modes:

a) asynchronous - no clock is required to get into or out of the reset state.

b) synchronous - The global GSR net is synchronized to a user selected clock. In this mode it continues to be asynchronous to get into the reset state, but is synchronous to get out of the reset state. This allows all registers on the device to become operational in the same clock period. The synchronous GSR goes out of reset in two cycles from the clock edge where the setup time of the FF was met (not from the GSR being released).

## sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. Each PLL has four dividers associated with it: input clock divider, feedback divider and two clock output dividers. The input divider is used to divide the input clock signal, while the feedback divider is used to multiply the input clock signal.

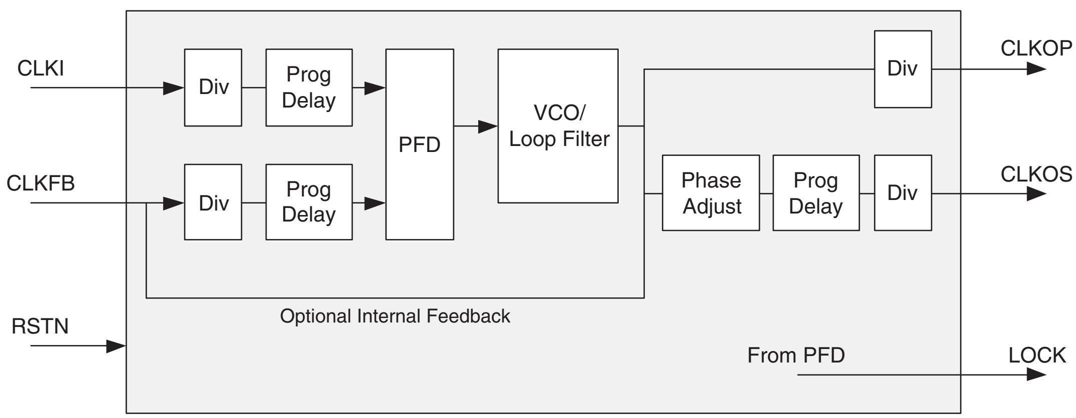
The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically.

The Phase Select block can modify the phase of the clock signal if desired. The Spread Spectrum block supports the modulation of the PLL output frequency. This reduces the peak energy in the fundamental and its harmonics providing for lower EMI (Electro Magnetic Interference).

The sysCLOCK PLL can be configured at power-up and then, if desired, reconfigured dynamically through the serial memory interface bus which connects with the on-chip system bus. For example, the user can select inputs, loop filters, divider setting, delay settings and phase shift settings. The user can also directly access the SMI bus through the routing.

The PLL clock input, from pin or routing, feeds into an input divider. There are four sources of feedback signal to the feedback divider: from the clock net, directly from the voltage controlled oscillator (VCO) output, from the routing or from an external pin. The signal from the input clock divider and the feedback divider are passed through the programmable delay before entering the phase frequency detector (PFD) unit. The output of this PFD is used to control the voltage controlled oscillator. There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

*Figure 2-11. PLL Diagram*




For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

## Spread Spectrum Clocking (SSC)

The PLL supports spread spectrum clocking to reduce peak EMI by using “down-spread” modulation. The spread spectrum operation will vary the output frequency (at 30KHz to 500KHz) in a range that is between its nominal value, down to a frequency that is a programmable 1%, 2%, or 3% lower than normal.

## Digital Locked Loop (DLLs)

In addition to PLLs, the LatticeSC devices have up to 12 DLLs per device. DLLs assist in the management of clocks and strobes. DLLs are well suited to applications where the clock may be stopped or transferring jitter from input to output is important, for example forward clocked interfaces. PLLs are good for applications requiring the lowest output jitter or jitter filtering. All DLL outputs are routed as primary/edge clock sources.

The DLL has two independent clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine phase shift and divider blocks to allow this output to be further modified, if required. The fine phase shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. LOCK output signal is asserted when the DLL is locked. The ALU HOLD signal setting allows users to freeze the DLL at its current delay setting.

## Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the PURESPEED I/O buffers. The block contains a register for SDR operation and a group of three registers for DDR and shift register operation. The output signal tri-state control signal (TO) can be derived directly from one of the inputs (bypass mode), the SDR shift register, the DDR registers or the data associated with the buffer (for open drain emulation). Figure 2-24 shows the diagram of the Tristate Register Block.

### Tristate SDR Register/Latch Block

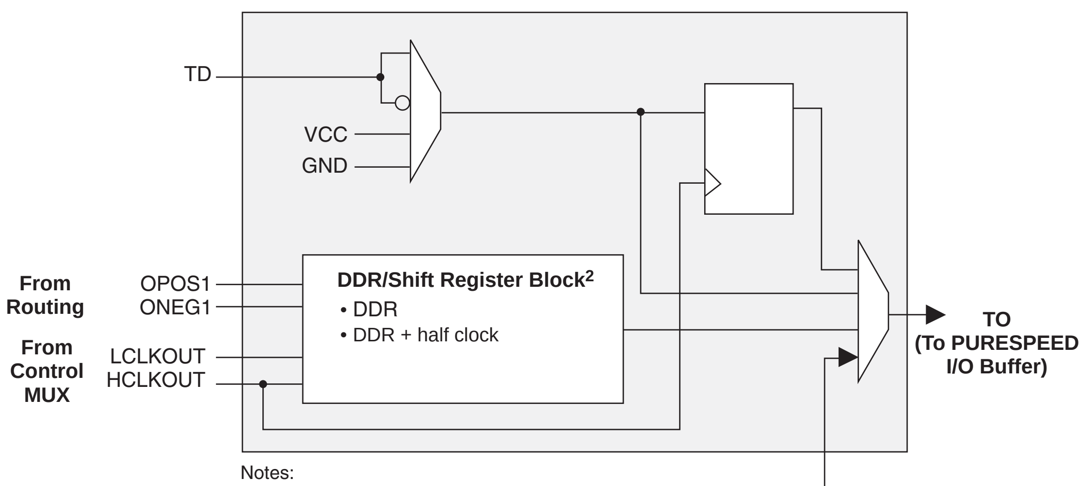
The SDR register operates on the positive edge of the high-speed clock. In it has a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR and Global Set Reset GSR enable or disable. The register LSR input is driven from LSRO, which is generated from the PIO control MUX. The GSR input is driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

### Tristate DDR/Shift Register Block

The DDR/Shift block is shared with the output block allowing DDR support using the high-speed clock and the associated transfer from the low-speed clock domain. It functions as a gearbox allowing low–speed parallel data from the FPGA fabric to provide a high-speed tri-state control stream.

There is a special mode for DDR-II memory interfaces where the termination is controlled by the output tristate signal. During WRITE cycle when the FPGA is driving the lines, the parallel terminations are turned off. During READ cycle when the FPGA is receiving data, the parallel terminations are turned on.

***Figure 2-24. Tristate Register Block[1]***




Notes:
1. CE, Update, Set and Reset not shown for clarity.
2. DDR/Shift Register Block shared with output register block.

## I/O Architecture Rules

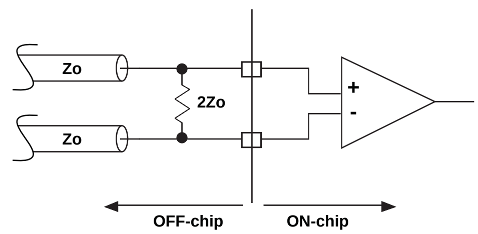
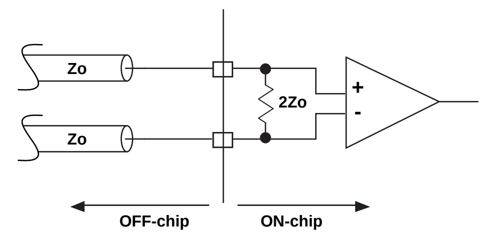
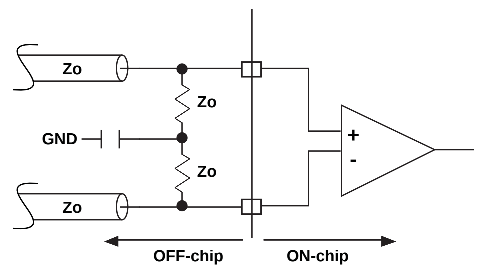
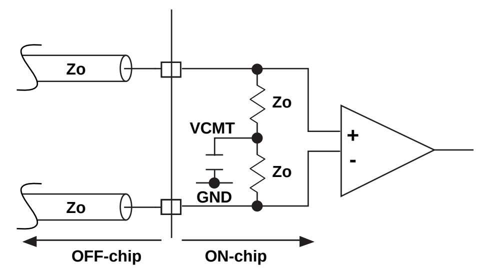
Table 2-6 shows the PIO usage for x1, x2, x4 gearing. The checkmarks in the columns show the specific PIOs that are used for each gearing mode. When using x2 or x4 gearing, any PIO which is not used for gearing can still be used as an output.

**Differential Input Termination**

The LatticeSC device allows two types of differential termination. The first is a single resistor across the differential inputs. The second is a center-tapped system where each input is terminated to the on-chip termination bus $V_{CMT}$. The $V_{CMT}$ bus is DC-coupled through an internal capacitor to ground.

Figure 2-29 shows the differential termination schemes and Table 2-9 shows the nominal values of the termination resistors.

***Figure 2-29. Differential Termination Scheme***

| Termination Type | Discrete Off-Chip Solution | Lattice On-Chip Solution |
|---|---|---|
| Differential termination |   |   |
| Differential and common mode termination |   |   |

**Calibration**

There are two calibration sources that are associated with the termination scheme used in the LatticeSC devices:

- DIFFR – This pin occurs in each bank that supports differential drivers and must be connected through a 1K+/-1% resistor to ground if differential outputs are used. Note that differential drivers are not supported in banks 1, 4 and 5.
- XRES – There is one of these pins per device. It is used for several functions including calibrating on-chip termination. This pin should always be connected through a 1K+/-1% resistor to ground.

The LatticeSC devices support two modes of calibration:

- Continuous – In this mode the SC devices continually calibrate the termination resistances. Calibration happens several times a second. Using this mode ensures that termination resistances remain calibrated as the silicon junction temperature changes.
- User Request – In this mode the calibration circuit operates continuously. However, the termination resistor values are only updated on the assertion of the calibration_update signal available to the core logic.

For more information on calibration, refer to the details of additional technical documentation at the end of this data sheet.

## Hot Socketing

The LatticeSC devices have been carefully designed to ensure predictable behavior during power-up and power-down. To ensure proper power sequencing, care must be taken during power-up and power-down as described below. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits, VDDAX25 needs to be connected independent of the use of the SERDES. This supply is used to control the SERDES CML I/O regardless of the SERDES being used in the design.

## Supported Source Synchronous Interfaces

The LatticeSC devices contain a variety of hardware, such as delay elements, DDR registers and PLLs, to simplify the implementation of Source Synchronous interfaces. Table 2-11 lists Source Synchronous and DDR/QDR standards supported in the LatticeSC. For additional detail refer to technical information at the end of the data sheet.

***Table 2-11. Source Synchronous Standards Table[1]***

| Source Synchronous Standard | Clocking | Speeds (MHz) | Data Rate (Mbps) |
|---|---|---|---|
| RapidIO | DDR | 500 | 1000 |
| SPI4.2 (POS-PHY4)/NPSI | DDR | 500 | 1000 |
| SFI4/XSBI | DDR<br>SDR | 334<br>667 | 667 |
| XGMII | DDR | 156.25 | 312 |
| CSIX | SDR | 250 | 250 |
| QDRII/QDRII+ memory interface | DDR | 300 | 600 |
| DDR memory interface | DDR | 240 | 480 |
| DDRII memory interface | DDR | 333 | 667 |
| RLDRAM memory interface | DDR | 400 | 800 |

1. Memory width is dependent on the system design and limited by the number of I/Os in the device.

# flexiPCS™ (Physical Coding Sublayer Block)

## flexiPCS Functionality

The LatticeSC family combines a high-performance FPGA fabric, high-performance I/Os and large embedded RAM in a single industry leading architecture. LatticeSC devices also feature up to 32 channels of embedded SERDES with associated Physical Coding Sublayer (PCS) logic. The flexiPCS logic can be configured to support numerous industry standard high-speed data transfer protocols.

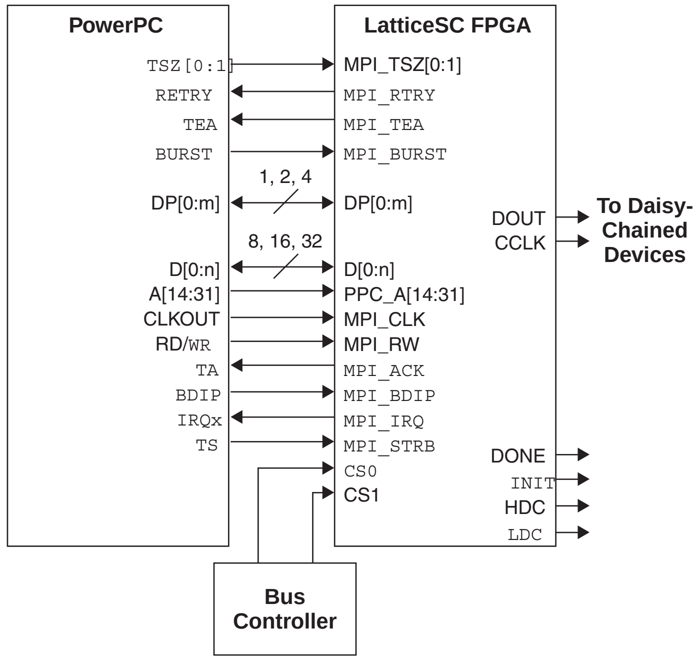
Each channel of flexiPCS logic contains dedicated transmit and receive SERDES for high-speed, full-duplex serial data transfers at data rates up to 3.8 Gbps. The PCS logic in each channel can be configured to support an array of popular data protocols including SONET (STS-12/STS-12c, STS-48/STS-48c, and TFI-5 support of 10 Gbps or above), Gigabit Ethernet (compliant to the IEEE 1000BASE-X specification), 1.02 or 2.04 Gbps Fibre Channel, PCI-Express, and Serial RapidIO. In addition, the protocol based logic can be fully or partially bypassed in a number of configurations to allow users flexibility in designing their own high-speed data interface.

Protocols requiring data rates above 3.8 Gbps can be accommodated by dedicating either one pair or all four channels in one flexiPCS quad block to one data link. One quad can support full-duplex serial data transfers at data rates up to 15.2 Gbps. A single flexiPCS quad can be configured to support 10Gb Ethernet (with a fully compliant XAUI interface), 10Gb Fibre Channel, and x4 PCI-Express and 4x RapidIO.

The flexiPCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic which can also be geared to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic. Each SERDES pin can be DC coupled independently and can allow for both high-speed and low-speed operation down to DC rates on the same SERDES pin, as required by some Serial Digital Video applications.

The ispLEVER design tools from Lattice support all modes of the flexiPCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow a user to define their own operation. With ispLEVER, the user can define the mode for each quad in a design. Nine modes are currently supported by the ispLEVER design flow:

*Figure 2-32. PowerPCI and MPI Schematic*




## Configuration and Testing

The following section describes the configuration and testing features of the LatticeSC family of devices.

### IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeSC devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage $V_{CCJ}$ and can operate with LVCMOS33, 25 and 18 standards. For additional detail refer to technical information at the end of the data sheet.

### Device Configuration

All LatticeSC devices contain three possible ports that can be used for device configuration. The serial port, which supports bit-wide configuration, and the sysCONFIG port that supports both byte-wide and serial configuration. The MPI port supports 8-bit, 16-bit or 32-bit configuration.

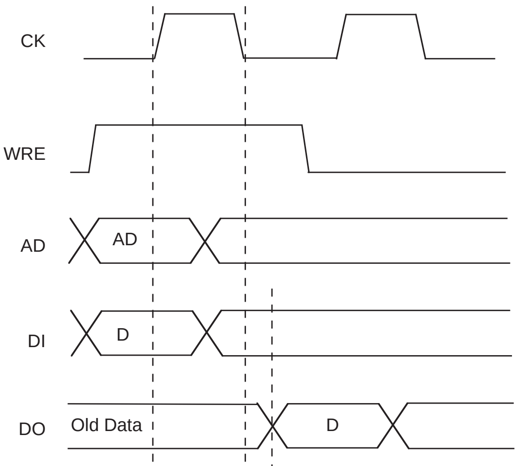
The serial port supports both the IEEE Std. 1149.1 Boundary Scan specification and the IEEE Std. 1532 In-System Configuration specification. The sysCONFIG port is a 20-pin interface with six of the I/Os used as dedicated pins and the rest being dual-use pins. When sysCONFIG mode is not used, these dual-use pins are available for general purpose I/O. All I/Os for the sysCONFIG and MPI ports are in I/O bank #1.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port. Once a configuration port is selected, that port is locked and another configuration port cannot be activated until the next re-initialization sequence. For additional detail refer to technical information at the end of the data sheet.

# Timing Diagrams

## PFU Timing Diagrams

***Figure 3-4. Slice Single/Dual Port Write Cycle Timing***




Notes:
- Rising Edge for latching WREN, WAD and DATAIN.
- WREN must continue past falling edge clock.
- Data output occurs on negative edge.

***Figure 3-5. Slice Single/Dual Port Read Cycle Timing***

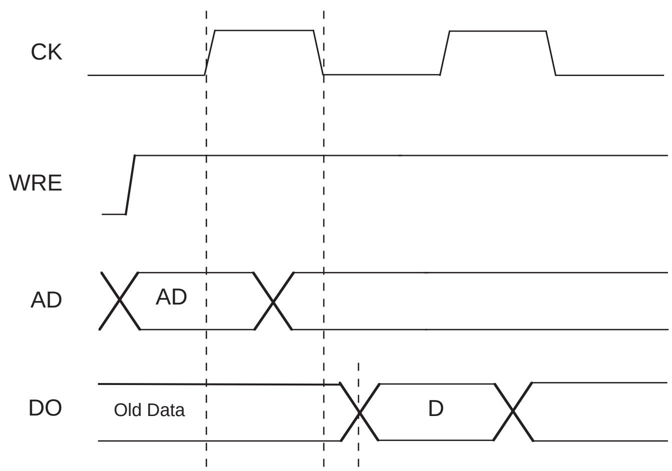
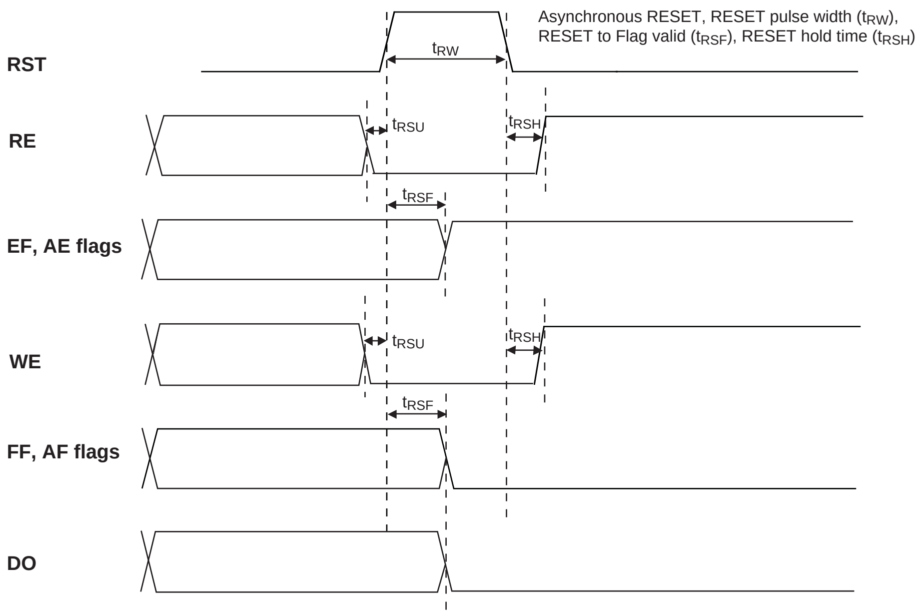
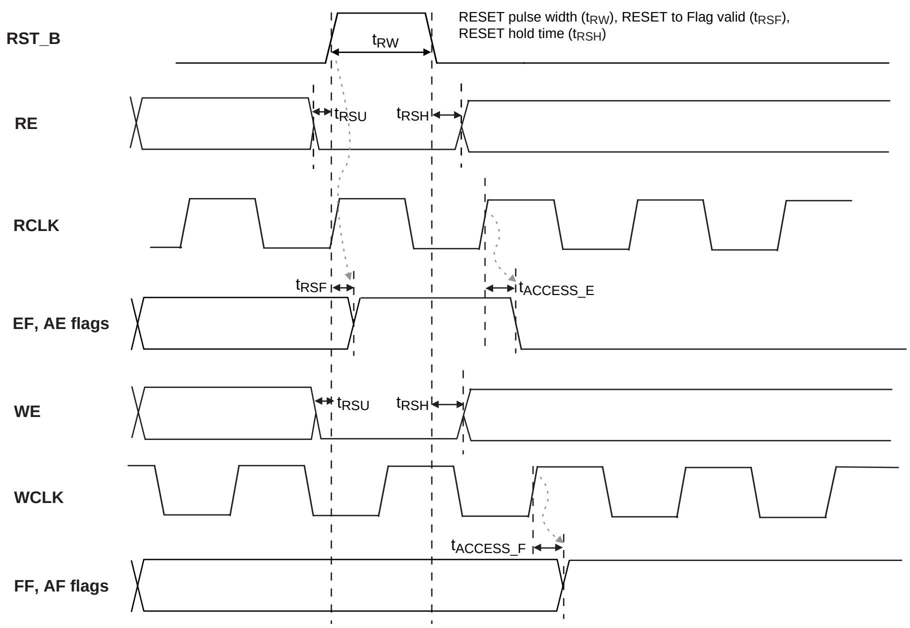


***Figure 3-10. FIFO Reset Waveform***




Note: RE and WE must be deactivated $t_{RSU}$ before the Positive FIFO reset edge and enabled $t_{RSH}$ after the FIFO reset negative edge.

***Figure 3-11. Read Pointer Reset Waveform***




Note: RE and WE must be deactivated $t_{RSU}$ before the Positive FIFO reset edge and enabled $t_{RSH}$ after the FIFO reset negative edge.

# LatticeSC/M sysCONFIG Port Timing (Continued)

**Over Recommended Operating Conditions**

| Parameter | Description | Min. | Max. | Units |
|---|---|---|---|---|
| **sysCONFIG Asynchronous Peripheral Configuration Mode** | | | | |
| $t_{WRAP}$ | WRN, CS0N and CS1 Pulse Width | 5 | - | ns |
| $t_{SAP}$ | D[7:0] Setup Time | 1.5 | - | ns |
| $t_{RDYAP}$ | RDY Delay | — | 8 | ns |
| $t_{BAP}$ | RDY Low | 1 | 8 | CCLK periods |
| $t_{WR2AP}$ | Earliest WRN After RDY Goes High | 0 | — | ns |
| $t_{DENAP}$ | RDN to D[7:0] Enable/Disable | — | 7.5 | ns |
| $t_{DAP}$ | CCLK to DOUT | — | 7.5 | ns |
| **sysCONFIG Slave Serial Configuration Mode** | | | | |
| $t_{SSS}$ | DIN Setup Time | 5.2 | — | ns |
| $t_{HSS}$ | DIN Hold Time | 0 | — | ns |
| $t_{CHSS}$ | CCLK High Time | 3.75 | — | ns |
| $t_{CLSS}$ | CCLK Low Time | 3.75 | — | ns |
| $f_{CSS}$ | CCLK Frequency | — | 150 | MHz |
| $t_{DSS}$ | CCLK to DOUT | — | 7.5 | ns |
| **sysCONFIG Slave Parallel Configuration Mode** | | | | |
| $t_{S1SP}$ | CS0N, CS1, WRN Setup Time | 5.2 | — | ns |
| $t_{H1SP}$ | CS0N, CS1, WRN Hold Time | 0 | — | ns |
| $t_{S2SP}$ | D[7:0] Setup Time | 5.2 | — | ns |
| $t_{H2SP}$ | D[7:0] Hold Time | 0 | — | ns |
| $t_{CHSP}$ | CCLK High Time | 3.75 | — | ns |
| $t_{CL}$ | CCLK Low Time | 3.75 | — | ns |
| $f_{CSP}$ | CCLK Frequency | — | 150 | MHz |

**sysCONFIG MPI Port**

| Parameter | Description | -7 | | -6 | | -5 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{MPICTRL\_SET}$ | MPI Control (MPCSTRBN, MPCWRN, MPCCLK, etc.) to MPCCLK Setup Time | 4.9 | — | 5.2 | — | 5.5 | — | ns |
| $t_{MPIADR\_SET}$ | MPI Address to MPCCLK Setup Time | 3.9 | — | 4.2 | — | 4.5 | — | ns |
| $t_{MPIDAT\_SET}$ | MPI Write Data to MPCCLK Setup Time | 4.9 | — | 5.2 | — | 5.5 | — | ns |
| $t_{MPIDPAR\_SET}$ | MPI Write Parity Data to MPCCLK Setup Time | 3.9 | — | 4.2 | — | 4.5 | — | ns |
| $t_{MPI\_HLD}$ | All Hold Times | 0 | — | 0 | — | 0 | — | ns |
| $t_{MPICTRL\_DEL}$ | MPCCLK to MPI Control (MPCTA, MPC-TEA, MPCRETRY) | — | 5.6 | — | 6.7 | — | 8.7 | ns |
| $t_{MPIDAT\_DEL}$ | MPCCLK to MPI Data | — | 5.6 | — | 6.7 | — | 8.7 | ns |
| $t_{MPIDPAR\_DEL}$ | MPCCLK to MPI Parity Data | — | 4.9 | — | 5.7 | — | 7.7 | ns |
| $f_{MPI\_CLK\_FRQ}$ | MPCCLK Frequency | — | 100 | — | 83 | — | 66 | MHz |

# LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

| | LFSC/M15 | | | LFSC/M25 | | |
|---|---|---|---|---|---|---|
| Ball Number | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| R29 | PR28B | 3 | | PR31B | 3 | |
| P29 | PR28A | 3 | | PR31A | 3 | |
| P27 | PR27C | 3 | PCLKT3_3 | PR30C | 3 | PCLKT3_3 |
| N29 | PR27B | 3 | | PR30B | 3 | |
| N28 | PR27A | 3 | | PR30A | 3 | |
| R25 | PR26D | 3 | PCLKC3_1 | PR29D | 3 | PCLKC3_1 |
| R26 | PR26C | 3 | PCLKT3_1 | PR29C | 3 | PCLKT3_1 |
| R28 | PR26B | 3 | PCLKC3_0 | PR29B | 3 | PCLKC3_0 |
| P28 | PR26A | 3 | PCLKT3_0 | PR29A | 3 | PCLKT3_0 |
| N27 | PR24D | 2 | PCLKC2_2 | PR27D | 2 | PCLKC2_2 |
| P26 | PR24C | 2 | PCLKT2_2 | PR27C | 2 | PCLKT2_2 |
| L30 | PR24B | 2 | PCLKC2_0 | PR27B | 2 | PCLKC2_0 |
| K30 | PR24A | 2 | PCLKT2_0 | PR27A | 2 | PCLKT2_0 |
| J30 | PR23B | 2 | PCLKC2_1 | PR26B | 2 | PCLKC2_1 |
| H30 | PR23A | 2 | PCLKT2_1 | PR26A | 2 | PCLKT2_1 |
| M26 | PR22D | 2 | DIFFR_2 | PR25D | 2 | DIFFR_2 |
| M25 | PR22C | 2 | VREF1_2 | PR25C | 2 | VREF1_2 |
| G29 | PR22B | 2 | | PR25B | 2 | |
| F29 | PR22A | 2 | | PR25A | 2 | |
| H28 | PR19D | 2 | | PR22D | 2 | |
| J28 | PR19C | 2 | | PR22C | 2 | |
| E30 | PR19B | 2 | | PR22B | 2 | |
| E29 | PR19A | 2 | | PR22A | 2 | |
| L26 | PR18D | 2 | VREF2_2 | PR18D | 2 | VREF2_2 |
| L25 | PR18C | 2 | | PR18C | 2 | |
| F28 | PR18B | 2 | URC_DLLC_IN_D/URC_DLLC_FB_C | PR18B | 2 | URC_DLLC_IN_D/URC_DLLC_FB_C |
| G28 | PR18A | 2 | URC_DLLT_IN_D/URC_DLLT_FB_C | PR18A | 2 | URC_DLLT_IN_D/URC_DLLT_FB_C |
| K26 | PR17D | 2 | URC_PLLC_IN_B/URC_PLLC_FB_A | PR17D | 2 | URC_PLLC_IN_B/URC_PLLC_FB_A |
| K25 | PR17C | 2 | URC_PLLT_IN_B/URC_PLLT_FB_A | PR17C | 2 | URC_PLLT_IN_B/URC_PLLT_FB_A |
| D30 | PR17B | 2 | URC_DLLC_IN_C/URC_DLLC_FB_D | PR17B | 2 | URC_DLLC_IN_C/URC_DLLC_FB_D |
| D29 | PR17A | 2 | URC_DLLT_IN_C/URC_DLLT_FB_D | PR17A | 2 | URC_DLLT_IN_C/URC_DLLT_FB_D |
| G26 | PR15D | 2 | | PR16D | 2 | |
| H26 | PR15C | 2 | | PR16C | 2 | |
| E28 | PR15B | 2 | URC_PLLC_IN_A/URC_PLLC_FB_B | PR16B | 2 | URC_PLLC_IN_A/URC_PLLC_FB_B |
| D28 | PR15A | 2 | URC_PLLT_IN_A/URC_PLLT_FB_B | PR16A | 2 | URC_PLLT_IN_A/URC_PLLT_FB_B |
| J25 | VCCJ | - | | VCCJ | - | |
| H25 | TDO | - | TDO | TDO | - | TDO |
| J26 | TMS | - | | TMS | - | |
| G25 | TCK | - | | TCK | - | |
| G24 | TDI | - | | TDI | - | |
| F26 | PROGRAMN | 1 | | PROGRAMN | 1 | |
| H24 | MPIIRQN | 1 | CFGIRQN/MPI_IRQ_N | MPIIRQN | 1 | CFGIRQN/MPI_IRQ_N |
| F25 | CCLK | 1 | | CCLK | 1 | |
| D27 | VCC12 | - | | VCC12 | - | |
| E26 | VCC12 | - | | VCC12 | - | |

# LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M25 | | | LFSC/M40 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AM21 | PB29A | 5 | | PB38A | 5 | |
| AM20 | PB29B | 5 | | PB38B | 5 | |
| AH21 | PB29C | 5 | | PB38C | 5 | |
| AH20 | PB29D | 5 | | PB38D | 5 | |
| AJ18 | PB31A | 5 | | PB39A | 5 | |
| AK18 | PB31B | 5 | | PB39B | 5 | |
| AH19 | PB31C | 5 | | PB39C | 5 | |
| AH18 | PB31D | 5 | | PB39D | 5 | |
| AL19 | PB32A | 5 | | PB41A | 5 | |
| AM19 | PB32B | 5 | | PB41B | 5 | |
| AH17 | PB32C | 5 | | PB41C | 5 | |
| AG17 | PB32D | 5 | | PB41D | 5 | |
| AL18 | PB33A | 5 | | PB42A | 5 | |
| AM18 | PB33B | 5 | | PB42B | 5 | |
| AC17 | PB33C | 5 | | PB42C | 5 | |
| AD17 | PB33D | 5 | | PB42D | 5 | |
| AL17 | PB35A | 5 | | PB43A | 5 | |
| AM17 | PB35B | 5 | | PB43B | 5 | |
| AE17 | PB35C | 5 | | PB43C | 5 | |
| AF17 | PB35D | 5 | | PB43D | 5 | |
| AM16 | PB37A | 4 | | PB45A | 4 | |
| AL16 | PB37B | 4 | | PB45B | 4 | |
| AF16 | PB37C | 4 | | PB45C | 4 | |
| AE16 | PB37D | 4 | | PB45D | 4 | |
| AM15 | PB38A | 4 | | PB46A | 4 | |
| AL15 | PB38B | 4 | | PB46B | 4 | |
| AD16 | PB38C | 4 | | PB46C | 4 | |
| AC16 | PB38D | 4 | | PB46D | 4 | |
| AM14 | PB39A | 4 | | PB47A | 4 | |
| AL14 | PB39B | 4 | | PB47B | 4 | |
| AG16 | PB39C | 4 | | PB47C | 4 | |
| AH16 | PB39D | 4 | | PB47D | 4 | |
| AK15 | PB41A | 4 | | PB49A | 4 | |
| AJ15 | PB41B | 4 | | PB49B | 4 | |
| AH15 | PB41C | 4 | | PB49C | 4 | |
| AH14 | PB41D | 4 | | PB49D | 4 | |
| AM13 | PB42A | 4 | | PB50A | 4 | |
| AM12 | PB42B | 4 | | PB50B | 4 | |
| AH13 | PB42C | 4 | | PB50C | 4 | |
| AH12 | PB42D | 4 | | PB50D | 4 | |
| AK14 | PB43A | 4 | | PB51A | 4 | |
| AJ14 | PB43B | 4 | | PB51B | 4 | |
| AE15 | PB43C | 4 | | PB51C | 4 | |
| AD15 | PB43D | 4 | | PB51D | 4 | |
| AL13 | PB46A | 4 | PCLKT4_2 | PB53A | 4 | PCLKT4_2 |
| AL12 | PB46B | 4 | PCLKC4_2 | PB53B | 4 | PCLKC4_2 |
| AG14 | PB46C | 4 | PCLKT4_7 | PB53C | 4 | PCLKT4_7 |
| AG13 | PB46D | 4 | PCLKC4_7 | PB53D | 4 | PCLKC4_7 |
| AM11 | PB47A | 4 | PCLKT4_1 | PB54A | 4 | PCLKT4_1 |
| AM10 | PB47B | 4 | PCLKC4_1 | PB54B | 4 | PCLKC4_1 |

# LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

| | LFSC/M40 | | | LFSC/M80 | | |
|---|---|---|---|---|---|---|
| Ball Number | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| L1 | PR31A | 2 | | PR43A | 2 | |
| T10 | PR30D | 2 | | PR42D | 2 | |
| U10 | PR30C | 2 | | PR42C | 2 | |
| N2 | PR30B | 2 | | PR42B | 2 | |
| M2 | PR30A | 2 | | PR42A | 2 | |
| R11 | PR29D | 2 | | PR37D | 2 | |
| P11 | PR29C | 2 | | PR37C | 2 | |
| N4 | PR29B | 2 | | PR37B | 2 | |
| M4 | PR29A | 2 | | PR37A | 2 | |
| N5 | PR27D | 2 | | PR35D | 2 | |
| M5 | PR27C | 2 | | PR35C | 2 | |
| L2 | PR27B | 2 | | PR35B | 2 | |
| K2 | PR27A | 2 | | PR35A | 2 | |
| P8 | PR26D | 2 | | PR33D | 2 | |
| N8 | PR26C | 2 | | PR33C | 2 | |
| J2 | PR26B | 2 | | PR33B | 2 | |
| H2 | PR26A | 2 | | PR33A | 2 | |
| M6 | PR25D | 2 | | PR31D | 2 | |
| L6 | PR25C | 2 | | PR31C | 2 | |
| K3 | PR25B | 2 | | PR31B | 2 | |
| J3 | PR25A | 2 | | PR31A | 2 | |
| M8 | PR23D | 2 | DIFFR_2 | PR29D | 2 | DIFFR_2 |
| L8 | PR23C | 2 | VREF1_2 | PR29C | 2 | VREF1_2 |
| K4 | PR23B | 2 | | PR29B | 2 | |
| J4 | PR23A | 2 | | PR29A | 2 | |
| M7 | PR22D | 2 | | PR21D | 2 | |
| L7 | PR22C | 2 | | PR21C | 2 | |
| J5 | PR22B | 2 | | PR21B | 2 | |
| H5 | PR22A | 2 | | PR21A | 2 | |
| N9 | PR21D | 2 | | PR20D | 2 | |
| P9 | PR21C | 2 | | PR20C | 2 | |
| G3 | PR21B | 2 | | PR20B | 2 | |
| F3 | PR21A | 2 | | PR20A | 2 | |
| J6 | PR18D | 2 | VREF2_2 | PR18D | 2 | VREF2_2 |
| H6 | PR18C | 2 | | PR18C | 2 | |
| E2 | PR18B | 2 | URC_DLLC_IN_D/URC_DLLC_FB_C | PR18B | 2 | URC_DLLC_IN_D/URC_DLLC_FB_C |
| D2 | PR18A | 2 | URC_DLLT_IN_D/URC_DLLT_FB_C | PR18A | 2 | URC_DLLT_IN_D/URC_DLLT_FB_C |
| P10 | PR17D | 2 | URC_PLLC_IN_B/URC_PLLC_FB_A | PR17D | 2 | URC_PLLC_IN_B/URC_PLLC_FB_A |
| N10 | PR17C | 2 | URC_PLLT_IN_B/URC_PLLT_FB_A | PR17C | 2 | URC_PLLT_IN_B/URC_PLLT_FB_A |
| G4 | PR17B | 2 | URC_DLLC_IN_C/URC_DLLC_FB_D | PR17B | 2 | URC_DLLC_IN_C/URC_DLLC_FB_D |
| F4 | PR17A | 2 | URC_DLLT_IN_C/URC_DLLT_FB_D | PR17A | 2 | URC_DLLT_IN_C/URC_DLLT_FB_D |
| J7 | PR16D | 2 | | PR16D | 2 | |
| H7 | PR16C | 2 | | PR16C | 2 | |
| G5 | PR16B | 2 | URC_PLLC_IN_A/URC_PLLC_FB_B | PR16B | 2 | URC_PLLC_IN_A/URC_PLLC_FB_B |
| F5 | PR16A | 2 | URC_PLLT_IN_A/URC_PLLT_FB_B | PR16A | 2 | URC_PLLT_IN_A/URC_PLLT_FB_B |

# LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

| | LFSC/M115 | | |
|---|---|---|---|
| Ball Number | Ball Function | VCCIO Bank | Dual Function |
| W7 | GND | - | |
| AA14 | VCC | - | |
| AA16 | VCC | - | |
| AA17 | VCC | - | |
| AA18 | VCC | - | |
| AA19 | VCC | - | |
| AA21 | VCC | - | |
| AB13 | VCC | - | |
| AB22 | VCC | - | |
| N13 | VCC | - | |
| N22 | VCC | - | |
| P14 | VCC | - | |
| P16 | VCC | - | |
| P17 | VCC | - | |
| P18 | VCC | - | |
| P19 | VCC | - | |
| P21 | VCC | - | |
| R15 | VCC | - | |
| R17 | VCC | - | |
| R18 | VCC | - | |
| R20 | VCC | - | |
| T14 | VCC | - | |
| T16 | VCC | - | |
| T19 | VCC | - | |
| T21 | VCC | - | |
| U14 | VCC | - | |
| U15 | VCC | - | |
| U17 | VCC | - | |
| U18 | VCC | - | |
| U20 | VCC | - | |
| U21 | VCC | - | |
| V14 | VCC | - | |
| V15 | VCC | - | |
| V17 | VCC | - | |
| V18 | VCC | - | |
| V20 | VCC | - | |
| V21 | VCC | - | |
| W14 | VCC | - | |
| W16 | VCC | - | |
| W19 | VCC | - | |
| W21 | VCC | - | |
| Y15 | VCC | - | |
| Y17 | VCC | - | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| Ball Number | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AP8 | PB117D | 4 | | PB131D | 4 | |
| AY3 | PB119A | 4 | | PB133A | 4 | |
| AW3 | PB119B | 4 | | PB133B | 4 | |
| AR6 | PB119C | 4 | | PB133C | 4 | |
| AR5 | PB119D | 4 | | PB133D | 4 | |
| AU5 | PB120A | 4 | | PB134A | 4 | |
| AV5 | PB120B | 4 | | PB134B | 4 | |
| AL12 | PB120C | 4 | | PB134C | 4 | |
| AL11 | PB120D | 4 | | PB134D | 4 | |
| AV3 | PB121A | 4 | | PB135A | 4 | |
| AV4 | PB121B | 4 | | PB135B | 4 | |
| AN9 | PB121C | 4 | | PB135C | 4 | |
| AN8 | PB121D | 4 | | PB135D | 4 | |
| AW1 | PB123A | 4 | | PB138A | 4 | |
| AY1 | PB123B | 4 | | PB138B | 4 | |
| AK14 | PB123C | 4 | VREF1_4 | PB138C | 4 | VREF1_4 |
| AK13 | PB123D | 4 | | PB138D | 4 | |
| AV2 | PB124A | 4 | LRC_DLLT_IN_C/LRC_DLLT_FB_D | PB139A | 4 | LRC_DLLT_IN_C/LRC_DLLT_FB_D |
| AW2 | PB124B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D | PB139B | 4 | LRC_DLLC_IN_C/LRC_DLLC_FB_D |
| AM10 | PB124C | 4 | | PB139C | 4 | |
| AM9 | PB124D | 4 | | PB139D | 4 | |
| AV1 | PB125A | 4 | LRC_PLLT_IN_A/LRC_PLLT_FB_B | PB141A | 4 | LRC_PLLT_IN_A/LRC_PLLT_FB_B |
| AU1 | PB125B | 4 | LRC_PLLC_IN_A/LRC_PLLC_FB_B | PB141B | 4 | LRC_PLLC_IN_A/LRC_PLLC_FB_B |
| AL10 | PB125C | 4 | LRC_DLLT_IN_D/LRC_DLLT_FB_C | PB141C | 4 | LRC_DLLT_IN_D/LRC_DLLT_FB_C |
| AL9 | PB125D | 4 | LRC_DLLC_IN_D/LRC_DLLC_FB_C | PB141D | 4 | LRC_DLLC_IN_D/LRC_DLLC_FB_C |
| AT3 | PROBE_VCC | - | | PROBE_VCC | - | |
| AU2 | PROBE_GND | - | | PROBE_GND | - | |
| AP7 | PR95D | 3 | LRC_PLLC_IN_B/LRC_PLLC_FB_A | PR117D | 3 | LRC_PLLC_IN_B/LRC_PLLC_FB_A |
| AN7 | PR95C | 3 | LRC_PLLT_IN_B/LRC_PLLT_FB_A | PR117C | 3 | LRC_PLLT_IN_B/LRC_PLLT_FB_A |
| AR3 | PR95B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E | PR117B | 3 | LRC_DLLC_IN_F/LRC_DLLC_FB_E |
| AR4 | PR95A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E | PR117A | 3 | LRC_DLLT_IN_F/LRC_DLLT_FB_E |
| AP6 | PR94D | 3 | | PR116D | 3 | |
| AN6 | PR94C | 3 | | PR116C | 3 | |
| AT2 | PR94B | 3 | | PR116B | 3 | |
| AR2 | PR94A | 3 | | PR116A | 3 | |
| AM6 | PR93D | 3 | LRC_DLLC_IN_E/LRC_DLLC_FB_F | PR115D | 3 | LRC_DLLC_IN_E/LRC_DLLC_FB_F |
| AL6 | PR93C | 3 | LRC_DLLT_IN_E/LRC_DLLT_FB_F | PR115C | 3 | LRC_DLLT_IN_E/LRC_DLLT_FB_F |
| AP5 | PR93B | 3 | | PR115B | 3 | |
| AN5 | PR93A | 3 | | PR115A | 3 | |
| AL8 | PR91D | 3 | | PR112D | 3 | |
| AK8 | PR91C | 3 | | PR112C | 3 | |
| AP2 | PR91B | 3 | | PR112B | 3 | |
| AN2 | PR91A | 3 | | PR112A | 3 | |
| AJ12 | PR90D | 3 | | PR109D | 3 | |
| AH12 | PR90C | 3 | | PR109C | 3 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AB6 | PR57D | 3 | | PR71D | 3 | |
| AA6 | PR57C | 3 | | PR71C | 3 | |
| Y2 | PR57B | 3 | | PR71B | 3 | |
| W2 | PR57A | 3 | | PR71A | 3 | |
| AB7 | PR56D | 3 | | PR70D | 3 | |
| AA7 | PR56C | 3 | | PR70C | 3 | |
| Y3 | PR56B | 3 | | PR70B | 3 | |
| W3 | PR56A | 3 | | PR70A | 3 | |
| AC11 | PR55D | 3 | | PR69D | 3 | |
| AB11 | PR55C | 3 | VREF1_3 | PR69C | 3 | VREF1_3 |
| Y4 | PR55B | 3 | | PR69B | 3 | |
| W4 | PR55A | 3 | | PR69A | 3 | |
| AB8 | PR52D | 3 | PCLKC3_2 | PR66D | 3 | PCLKC3_2 |
| AA8 | PR52C | 3 | PCLKT3_2 | PR66C | 3 | PCLKT3_2 |
| Y5 | PR52B | 3 | | PR66B | 3 | |
| W5 | PR52A | 3 | | PR66A | 3 | |
| AC12 | PR51D | 3 | PCLKC3_3 | PR65D | 3 | PCLKC3_3 |
| AB12 | PR51C | 3 | PCLKT3_3 | PR65C | 3 | PCLKT3_3 |
| V1 | PR51B | 3 | | PR65B | 3 | |
| U1 | PR51A | 3 | | PR65A | 3 | |
| W7 | PR50D | 3 | PCLKC3_1 | PR64D | 3 | PCLKC3_1 |
| V7 | PR50C | 3 | PCLKT3_1 | PR64C | 3 | PCLKT3_1 |
| V2 | PR50B | 3 | PCLKC3_0 | PR64B | 3 | PCLKC3_0 |
| U2 | PR50A | 3 | PCLKT3_0 | PR64A | 3 | PCLKT3_0 |
| AB9 | PR48D | 2 | PCLKC2_2 | PR62D | 2 | PCLKC2_2 |
| AA9 | PR48C | 2 | PCLKT2_2 | PR62C | 2 | PCLKT2_2 |
| T1 | PR48B | 2 | PCLKC2_0 | PR62B | 2 | PCLKC2_0 |
| R1 | PR48A | 2 | PCLKT2_0 | PR62A | 2 | PCLKT2_0 |
| AB10 | PR47D | 2 | PCLKC2_3 | PR61D | 2 | PCLKC2_3 |
| AA10 | PR47C | 2 | PCLKT2_3 | PR61C | 2 | PCLKT2_3 |
| U3 | PR47B | 2 | PCLKC2_1 | PR61B | 2 | PCLKC2_1 |
| T3 | PR47A | 2 | PCLKT2_1 | PR61A | 2 | PCLKT2_1 |
| Y9 | PR46D | 2 | | PR60D | 2 | |
| W9 | PR46C | 2 | | PR60C | 2 | |
| V5 | PR46B | 2 | | PR60B | 2 | |
| U5 | PR46A | 2 | | PR60A | 2 | |
| AA11 | PR43D | 2 | | PR57D | 2 | |
| Y11 | PR43C | 2 | | PR57C | 2 | |
| Y6 | PR43B | 2 | | PR57B | 2 | |
| W6 | PR43A | 2 | | PR57A | 2 | |
| Y10 | PR42D | 2 | | PR56D | 2 | |
| W10 | PR42C | 2 | | PR56C | 2 | |
| T2 | PR42B | 2 | | PR56B | 2 | |
| R2 | PR42A | 2 | | PR56A | 2 | |
| W8 | PR41D | 2 | | PR55D | 2 | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| Ball Number | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| B22 | PT61B | 1 | A3/MPI_ADDR17 | PT69B | 1 | A3/MPI_ADDR17 |
| B23 | PT61A | 1 | A4/MPI_ADDR18 | PT69A | 1 | A4/MPI_ADDR18 |
| K23 | PT60D | 1 | D25/PCLKC1_5/MPI_DATA25 | PT66D | 1 | D25/PCLKC1_5/MPI_DATA25 |
| J23 | PT60C | 1 | D26/PCLKT1_5/MPI_DATA26 | PT66C | 1 | D26/PCLKT1_5/MPI_DATA26 |
| D22 | PT60B | 1 | A5/MPI_ADDR19 | PT66B | 1 | A5/MPI_ADDR19 |
| E22 | PT60A | 1 | A6/MPI_ADDR20 | PT66A | 1 | A6/MPI_ADDR20 |
| K22 | PT59D | 1 | D27/MPI_DATA27 | PT63D | 1 | D27/MPI_DATA27 |
| J22 | PT59C | 1 | VREF1_1 | PT63C | 1 | VREF1_1 |
| D23 | PT59B | 1 | A7/MPI_ADDR21 | PT63B | 1 | A7/MPI_ADDR21 |
| C23 | PT59A | 1 | A8/MPI_ADDR22 | PT63A | 1 | A8/MPI_ADDR22 |
| L23 | PT57D | 1 | D28/PCLKC1_6/MPI_DATA28 | PT61D | 1 | D28/PCLKC1_6/MPI_DATA28 |
| M23 | PT57C | 1 | D29/PCLKT1_6/MPI_DATA29 | PT61C | 1 | D29/PCLKT1_6/MPI_DATA29 |
| A24 | PT57B | 1 | A9/MPI_ADDR23 | PT61B | 1 | A9/MPI_ADDR23 |
| B24 | PT57A | 1 | A10/MPI_ADDR24 | PT61A | 1 | A10/MPI_ADDR24 |
| K25 | PT56D | 1 | D30/PCLKC1_7/MPI_DATA30 | PT58D | 1 | D30/PCLKC1_7/MPI_DATA30 |
| J25 | PT56C | 1 | D31/PCLKT1_7/MPI_DATA31 | PT58C | 1 | D31/PCLKT1_7/MPI_DATA31 |
| F23 | PT56B | 1 | A11/MPI_ADDR25 | PT58B | 1 | A11/MPI_ADDR25 |
| F22 | PT56A | 1 | A12/MPI_ADDR26 | PT58A | 1 | A12/MPI_ADDR26 |
| J26 | PT55D | 1 | D11/MPI_DATA11 | PT57D | 1 | D11/MPI_DATA11 |
| K26 | PT55C | 1 | D12/MPI_DATA12 | PT57C | 1 | D12/MPI_DATA12 |
| E23 | PT55B | 1 | A13/MPI_ADDR27 | PT57B | 1 | A13/MPI_ADDR27 |
| E24 | PT55A | 1 | A14/MPI_ADDR28 | PT57A | 1 | A14/MPI_ADDR28 |
| G23 | PT53D | 1 | A16/MPI_ADDR30 | PT55D | 1 | A16/MPI_ADDR30 |
| G24 | PT53C | 1 | D13/MPI_DATA13 | PT55C | 1 | D13/MPI_DATA13 |
| F26 | PT53B | 1 | A15/MPI_ADDR29 | PT55B | 1 | A15/MPI_ADDR29 |
| F27 | PT53A | 1 | A17/MPI_ADDR31 | PT55A | 1 | A17/MPI_ADDR31 |
| H25 | PT52D | 1 | A19/MPI_TSIZ1 | PT54D | 1 | A19/MPI_TSIZ1 |
| H24 | PT52C | 1 | A20/MPI_BDIP | PT54C | 1 | A20/MPI_BDIP |
| C25 | PT52B | 1 | A18/MPI_TSIZ0 | PT54B | 1 | A18/MPI_TSIZ0 |
| C26 | PT52A | 1 | MPI_TEA | PT54A | 1 | MPI_TEA |
| K24 | PT51D | 1 | D14/MPI_DATA14 | PT51D | 1 | D14/MPI_DATA14 |
| J24 | PT51C | 1 | DP1/MPI_PAR1 | PT51C | 1 | DP1/MPI_PAR1 |
| F24 | PT51B | 1 | A21/MPI_BURST | PT51B | 1 | A21/MPI_BURST |
| F25 | PT51A | 1 | D15/MPI_DATA15 | PT51A | 1 | D15/MPI_DATA15 |
| L26 | D_REFCLKP_L | - | | D_REFCLKP_L | - | |
| M26 | D_REFCLKN_L | - | | D_REFCLKN_L | - | |
| G27 | VCC12 | - | | VCC12 | - | |
| C29 | D_VDDIB3_L | - | | D_VDDIB3_L | - | |
| F28 | VCC12 | - | | VCC12 | - | |
| D26 | D_HDINP3_L | - | PCS 363 CH 3 IN P | D_HDINP3_L | - | PCS 363 CH 3 IN P |
| E26 | D_HDINN3_L | - | PCS 363 CH 3 IN N | D_HDINN3_L | - | PCS 363 CH 3 IN N |
| B25 | D_HDOUTP3_L | - | PCS 363 CH 3 OUT P | D_HDOUTP3_L | - | PCS 363 CH 3 OUT P |
| D24 | VCC12 | - | | VCC12 | - | |
| A25 | D_HDOUTN3_L | - | PCS 363 CH 3 OUT N | D_HDOUTN3_L | - | PCS 363 CH 3 OUT N |
| E25 | D_VDDOB3_L | - | | D_VDDOB3_L | - | |

# LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

| | LFSC/M80 | | | LFSC/M115 | | |
|---|---|---|---|---|---|---|
| Ball Number | Ball Function | VCCIO Bank | Dual Function | Ball Function | VCCIO Bank | Dual Function |
| AH22 | VTT_5 | 5 | | VTT_5 | 5 | |
| AJ22 | VTT_5 | 5 | | VTT_5 | 5 | |
| AJ23 | VTT_5 | 5 | | VTT_5 | 5 | |
| AJ24 | VTT_5 | 5 | | VTT_5 | 5 | |
| AJ25 | VTT_5 | 5 | | VTT_5 | 5 | |
| AB28 | VTT_6 | 6 | | VTT_6 | 6 | |
| AB29 | VTT_6 | 6 | | VTT_6 | 6 | |
| AE29 | VTT_6 | 6 | | VTT_6 | 6 | |
| AJ30 | VTT_6 | 6 | | VTT_6 | 6 | |
| AA28 | VTT_7 | 7 | | VTT_7 | 7 | |
| AA29 | VTT_7 | 7 | | VTT_7 | 7 | |
| R31 | VTT_7 | 7 | | VTT_7 | 7 | |
| V29 | VTT_7 | 7 | | VTT_7 | 7 | |
| Y24 | GND | - | | GND | - | |
| Y26 | GND | - | | GND | - | |
| Y8 | GND | - | | GND | - | |
| Y35 | GND | - | | GND | - | |
| AA16 | VCC12 | - | | VCC12 | - | |
| AA27 | VCC12 | - | | VCC12 | - | |
| AB16 | VCC12 | - | | VCC12 | - | |
| AB27 | VCC12 | - | | VCC12 | - | |
| AF16 | VCC12 | - | | VCC12 | - | |
| AF27 | VCC12 | - | | VCC12 | - | |
| AG17 | VCC12 | - | | VCC12 | - | |
| AG21 | VCC12 | - | | VCC12 | - | |
| G33 | NC | - | | NC | - | |
| G10 | NC | - | | NC | - | |
| M15 | NC | - | | NC | - | |
| L15 | NC | - | | NC | - | |
| K16 | NC | - | | NC | - | |
| J16 | NC | - | | NC | - | |
| M18 | NC | - | | NC | - | |
| L18 | NC | - | | NC | - | |
| M25 | NC | - | | NC | - | |
| L25 | NC | - | | NC | - | |
| J27 | NC | - | | NC | - | |
| K27 | NC | - | | NC | - | |
| L28 | NC | - | | NC | - | |
| M28 | NC | - | | NC | - | |

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M80 and LatticeSC/M115 in a 1704-pin package supports a 32-bit MPI interface.

**Commercial, Cont.**

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA80E-7FC1152C[1] | -7 | Ceramic fcBGA | 1152 | COM | 80.1 |
| LFSC3GA80E-6FC1152C[1] | -6 | Ceramic fcBGA | 1152 | COM | 80.1 |
| LFSC3GA80E-5FC1152C[1] | -5 | Ceramic fcBGA | 1152 | COM | 80.1 |
| LFSC3GA80E-7FF1152C | -7 | Organic fcBGA | 1152 | COM | 80.1 |
| LFSC3GA80E-6FF1152C | -6 | Organic fcBGA | 1152 | COM | 80.1 |
| LFSC3GA80E-5FF1152C | -5 | Organic fcBGA | 1152 | COM | 80.1 |
| LFSC3GA80E-7FC1704C[1] | -7 | Ceramic fcBGA | 1704 | COM | 80.1 |
| LFSC3GA80E-6FC1704C[1] | -6 | Ceramic fcBGA | 1704 | COM | 80.1 |
| LFSC3GA80E-5FC1704C[1] | -5 | Ceramic fcBGA | 1704 | COM | 80.1 |
| LFSC3GA80E-7FF1704C | -7 | Organic fcBGA | 1704 | COM | 80.1 |
| LFSC3GA80E-6FF1704C | -6 | Organic fcBGA | 1704 | COM | 80.1 |
| LFSC3GA80E-5FF1704C | -5 | Organic fcBGA | 1704 | COM | 80.1 |

1. Converted to organic flip-chip BGA package per PCN #01A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSCM3GA80EP1-7FC1152C[1] | -7 | Ceramic fcBGA | 1152 | COM | 80.1 |
| LFSCM3GA80EP1-6FC1152C[1] | -6 | Ceramic fcBGA | 1152 | COM | 80.1 |
| LFSCM3GA80EP1-5FC1152C[1] | -5 | Ceramic fcBGA | 1152 | COM | 80.1 |
| LFSCM3GA80EP1-7FF1152C | -7 | Organic fcBGA | 1152 | COM | 80.1 |
| LFSCM3GA80EP1-6FF1152C | -6 | Organic fcBGA | 1152 | COM | 80.1 |
| LFSCM3GA80EP1-5FF1152C | -5 | Organic fcBGA | 1152 | COM | 80.1 |
| LFSCM3GA80EP1-7FC1704C[1] | -7 | Ceramic fcBGA | 1704 | COM | 80.1 |
| LFSCM3GA80EP1-6FC1704C[1] | -6 | Ceramic fcBGA | 1704 | COM | 80.1 |
| LFSCM3GA80EP1-5FC1704C[1] | -5 | Ceramic fcBGA | 1704 | COM | 80.1 |
| LFSCM3GA80EP1-7FF1704C | -7 | Organic fcBGA | 1704 | COM | 80.1 |
| LFSCM3GA80EP1-6FF1704C | -6 | Organic fcBGA | 1704 | COM | 80.1 |
| LFSCM3GA80EP1-5FF1704C | -5 | Organic fcBGA | 1704 | COM | 80.1 |

1. Converted to organic flip-chip BGA package per PCN #01A-10.

| Part Number | Grade | Package | Balls | Temp. | LUTs (K) |
|---|---|---|---|---|---|
| LFSC3GA115E-6FC1152C[1] | -6 | Ceramic fcBGA | 1152 | COM | 115.2 |
| LFSC3GA115E-5FC1152C[1] | -5 | Ceramic fcBGA | 1152 | COM | 115.2 |
| LFSC3GA115E-6FF1152C | -6 | Organic fcBGA | 1152 | COM | 115.2 |
| LFSC3GA115E-5FF1152C | -5 | Organic fcBGA | 1152 | COM | 115.2 |
| LFSC3GA115E-6FC1704C[1] | -6 | Ceramic fcBGA | 1704 | COM | 115.2 |
| LFSC3GA115E-5FC1704C[1] | -5 | Ceramic fcBGA | 1704 | COM | 115.2 |
| LFSC3GA115E-6FF1704C | -6 | Organic fcBGA | 1704 | COM | 115.2 |
| LFSC3GA115E-5FF1704C | -5 | Organic fcBGA | 1704 | COM | 115.2 |

1. Converted to organic flip-chip BGA package per PCN #01A-10.

| Date | Version | Section | Change Summary |
|---|---|---|---|
| March 2007 (cont.) | 01.5 (cont.) | DC and Switching Characteristics (cont.) | Updated LatticeSC Internal Timing Parameters with ispLEVER 6.1 SP1 results. |
| | | | Updated $t_{FDEL}$ and $t_{CDEL}$ specifications. |
| | | | Updated LatticeSC Family Timing Adders with ispLEVER 6.1 SP1 results. |
| | | | Updated PLL specifications to expand frequency range down to 2 MHz and break out jitter for the different ranges. |
| | | | Added footnote to sysCLOCK PLL Timing table specifying the conditions for the jitter measurements. |
| | | | Added $t_{DLL}$ specification to sysCLOCK DLL Timing table. |
| | | | Added footnote to sysCLOCK DLL Timing table specifying the conditions for the jitter measurements. |
| | | | Added sysCONFIG Master Parallel Configuration Mode and sysCONFIG SPI Port to LatticeSC sysCONFIG Port Timing table. |
| | | Pin Information | Updated Pin Information Summary with SC40 information. |
| | | | Updated LFSC25 Logic Signal Connections: FF1020 with SC40 information. |
| | | | Updated LFSC80 Logic Signal Connections: FC1152 with SC40 information. |
| August 2007 | 01.6 | General | Changed references of "HDC" to "HDC/SI". |
| | | | Changed references of "LDCN" to "LDCN/SCS". |
| | | | Changed references of "BUSYN/RCLK" to "BUSYN/RCLK/SCK". |
| | | | Changed references of "RDCFGN" to "TSALLN". |
| | | | Changed references of "TDO/RDDATA" to "TDO". |
| | | Architecture | Updated text in Ripple Mode section. |
| | | | Added information to Global Set/Reset. |
| | | | Added information for Spread Spectrum Clocking |
| | | | Modified information for PLL/DLL Cascading. DLL to PLL is now supported. |
| | | | Modified AIL Block text and figure. |
| | | | Modified Figure 2-20 DDR/Shift Register Block. |
| | | | Added Information to Hot Socketing. |
| | | | Added new information for I/O Architecture Rules. |
| | | | Added information to SERDES Power Supply Sequencing Requirements. |
| | | DC and Switching Characteristics | Added footnote to Hot Socketing Specifications table. |
| | | | Modified Initialization and Standby Supply Current table. |
| | | | Modified GSR Timing table. |
| | | | Modified sysCLOCK DLL Timing table to include $I_{DUTY}$. |
| | | | Deleted Readback Timing information from sysCONFIG Port Timing table. |
| | | | Modified data in External Switching Characteristics table. |
| | | Pin Information | Added information to the Signal Descriptions table for HDC/SI, LDCN/SCS. |
| | | | Added footnote to Signal Descriptions table. |
| | | | Modified Description for signal BUSYN/RCLK/SCK. |
| | | | Modified data in Pin Information Summary and device-specific Pinout Information tables. |