Lattice Semiconductor Corporation - LFSCM3GA40EP1-6FF1152I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	604
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga40ep1-6ff1152i

DLLs and dynamic glitch free clock MUXs which are required in today's high end system designs. High-speed, high-bandwidth I/O make this family ideal for high-throughput systems.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeSC family of FPGA devices. Synthesis library support for LatticeSC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeSC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeSC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

Innovative high-performance FPGA architecture, high-speed SERDES with PCS support, sysMEM embedded memory and high performance I/O are combined in the LatticeSC to provide excellent performance for today's leading edge systems designs. Table 1-3 details the performance of several common functions implemented within the LatticeSC.

Table1-3. Speed Performance for Typical Functions[1]

Functions	Performance (MHz)[2]
32-bit Address Decoder	539
64-bit Address Decoder	517
32:1 Multiplexer	779
64-bit Adder (ripple)	353
32x8 Distributed Single Port (SP) RAM	768
64-bit Counter (up or down counter, non-loadable)	369
True Dual-Port 1024x18 bits	372
FIFO Port A: x36 bits, B: x9 bits	375

1. For additional information, see Typical Building BLock Function Performance table in this data sheet.
2. Advance information (-7 speed grade).

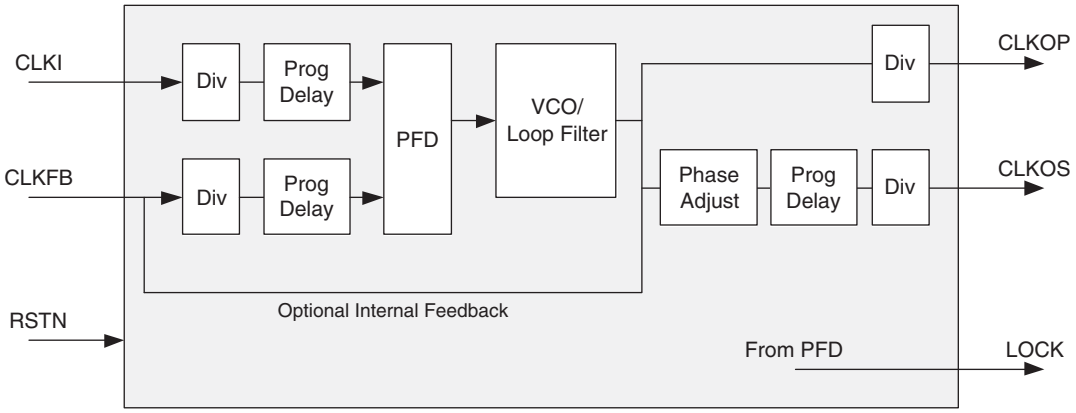
The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically.

The Phase Select block can modify the phase of the clock signal if desired. The Spread Spectrum block supports the modulation of the PLL output frequency. This reduces the peak energy in the fundamental and its harmonics providing for lower EMI (Electro Magnetic Interference).

The sysCLOCK PLL can be configured at power-up and then, if desired, reconfigured dynamically through the serial memory interface bus which connects with the on-chip system bus. For example, the user can select inputs, loop filters, divider setting, delay settings and phase shift settings. The user can also directly access the SMI bus through the routing.

The PLL clock input, from pin or routing, feeds into an input divider. There are four sources of feedback signal to the feedback divider: from the clock net, directly from the voltage controlled oscillator (VCO) output, from the routing or from an external pin. The signal from the input clock divider and the feedback divider are passed through the programmable delay before entering the phase frequency detector (PFD) unit. The output of this PFD is used to control the voltage controlled oscillator. There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

Figure 2-11. PLL Diagram



For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

Spread Spectrum Clocking (SSC)

The PLL supports spread spectrum clocking to reduce peak EMI by using “down-spread” modulation. The spread spectrum operation will vary the output frequency (at 30KHz to 500KHz) in a range that is between its nominal value, down to a frequency that is a programmable 1%, 2%, or 3% lower than normal.

Digital Locked Loop (DLLs)

In addition to PLLs, the LatticeSC devices have up to 12 DLLs per device. DLLs assist in the management of clocks and strobes. DLLs are well suited to applications where the clock may be stopped or transferring jitter from input to output is important, for example forward clocked interfaces. PLLs are good for applications requiring the lowest output jitter or jitter filtering. All DLL outputs are routed as primary/edge clock sources.

The DLL has two independent clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine phase shift and divider blocks to allow this output to be further modified, if required. The fine phase shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. LOCK output signal is asserted when the DLL is locked. The ALU HOLD signal setting allows users to freeze the DLL at its current delay setting.

Figure 2-13. DLL to PLL

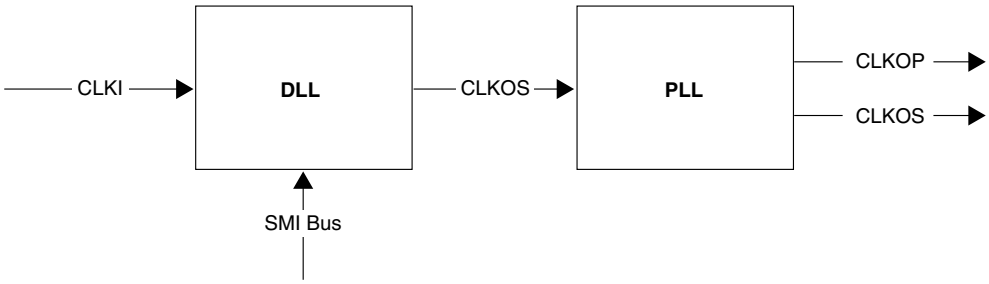


Figure 2-14 shows a shift of only CLKOP out in time.

Figure 2-14. PLL to DLL

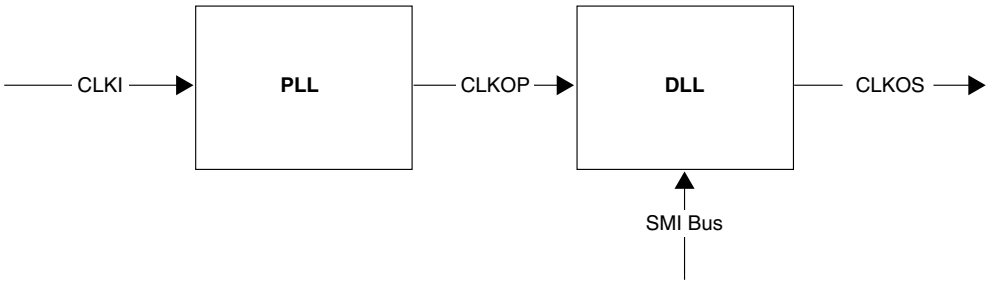
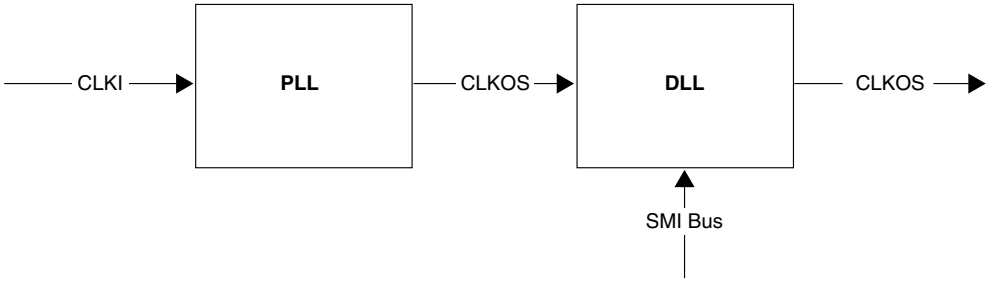


Figure 2-15 shows a shift of only CLKOS out in time.

Figure 2-15. PLL to DLL



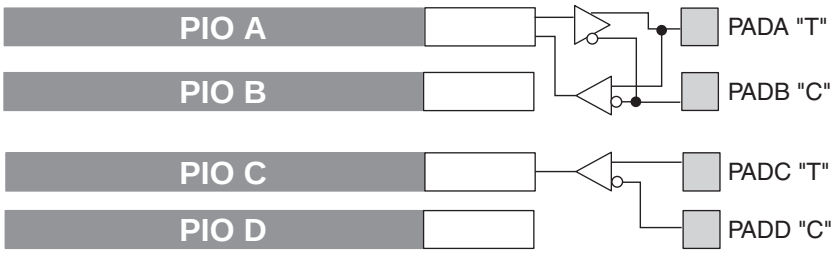
For further information on the DLL, please see details of additional technical documentation at the end of this data sheet.

sysMEM Memory Block

The sysMEM block can implement single port, true dual port, pseudo dual port or FIFO memories. Dedicated FIFO support logic allows the LatticeSC devices to efficiently implement FIFOs without consuming LUTs or routing resources for flag generation. Each block can be used in a variety of depths and widths as shown in Table 2-5. Memory with ranges from x1 to x18 in all modes: single port, pseudo-dual port and FIFO also providing x36.

high-speed interfaces in the LatticeSC devices. Figure 2-18 shows how differential receivers and drivers are arranged between PIOs.

Figure 2-18. Differential Drivers and Receivers



*Differential Driver only available on right and left of the device.

PIO

The PIO contains five blocks: an input register block, output register block, tristate register block, update block, and a control logic block. These blocks contain registers for both single data rate (SDR), double data rate (DDR), and shift register operation along with the necessary clock and selection logic.

Input Register Block

The input register block contains delay elements and registers that can be used to condition signals before they are passed to the device core. Figure 2-20 show the diagram of the input register block. The signal from the PURESPEED I/O buffer (DI) enters the input register block and can be used for three purposes, as a source for the combinatorial (INDD) and clock outputs (INCK), the input into the SDR register/latch block and the input to the delay block. The output of the delay block can be used as combinatorial (INDD) and clock (INCK) outputs, an input to the DDR/Shift Register Block or an input into the SDR register block.

Input SDR Register/Latch Block

The SDR register/latch block has a latch and a register/latch that can be used in a variety of combinations to provide a registered or latched output (INFF). The latch operates off high-speed input clocks and latches data on the positive going edge. The register/latch operates off the low-speed input clock and registers/latches data on the positive going edge. Both the latch and the register/latch have a clock enable input that is driven by the input clock enable. In addition both have a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR (LSR has precedence over CE) and Global Set Reset GSR enable or disable. The register and latch LSR inputs are driven from LSRI, which is generated from the PIO control MUX. The GSR inputs are driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

Input Delay Block

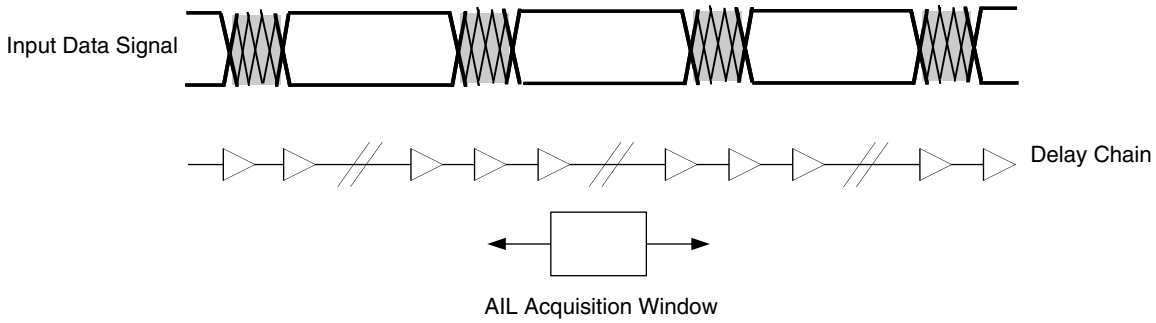
The delay block uses 144 tapped delay lines to obtain coarse and fine delay resolution. These delays can be adjusted during configuration or automatically via DLL or AIL blocks. The Adaptive Input Logic (AIL) uses this delay block to adjust automatically the delay in the data path to ensure that it has sufficient setup and hold time.

The delay line in this block matches the delay line that is used in the 12 on-chip DLLs. The delay line can be set via configuration bits or driven from a calibration bus that allows the setting to be controlled either from one of the on-chip DLLs or user logic. Controlling the delay from one of the on-chip DLLs allow the delay to be calibrated to the DLL clock and hence compensated for the variations in process, voltage and temperature.

Adaptive Input Logic (AIL) Overview

The Adaptive Input Logic (AIL) provides the ability of the input logic to dynamically find a solution by monitoring multiple samples of the input data. The input data signal from the input buffer is run through a delay chain. Data, transitions, jitter, noise are all contained inside of the delay chain. The AIL will then search the delay chain for a clean sampling point for data. Once found the AIL will monitor and walk with the data dynamically. This novel approach of using a delay chain to create multiple copies of the data provides a lower power solution than oversampling data with a higher speed clock. Figure 2-19 provides a high level view of the AIL methodology.

Figure 2-19. LatticeSC AIL Delay of Input Data Waveform



The AIL slides the acquisition window through the delay chain searching for stable data based solely on data transitions. A specific training pattern is not required to perform this bit alignment, simply data transitions. The size of the acquisition window is user-selectable allowing the AIL to operate over the full range of the PURESPEED I/O range. Based on dynamic user control the AIL can either continuously adjust the window location based on data edge detection or it can be locked to a specific delay.

The AIL operates on single data and double data rate interfaces and is available on most FPGA input pins on the LatticeSC device and all buffer types. The AIL block is low power using only 0.003 mW/MHz typical (6 mW @ 2 Gbps) for PRBS 2^7 data. Multiple AIL inputs can be used to create a bus with a FPGA circuit to realign the bus to a common clock cycle. The FPGA circuit to realign the bus is required and is provided by Lattice as a reference design.

For more information on the LatticeSC AIL please refer to TN1158 LatticeSC PURESPEED I/O Adaptive Input Logic User's Guide.

Input DDR/Shift Block

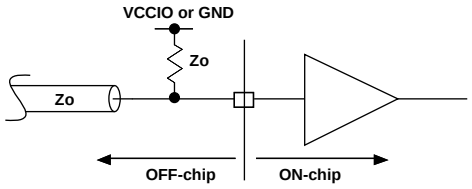
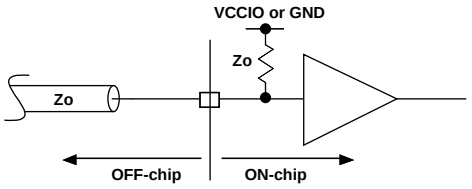
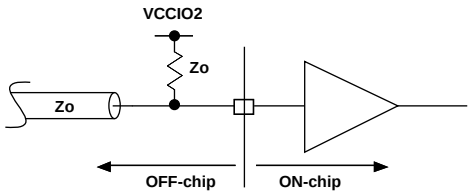
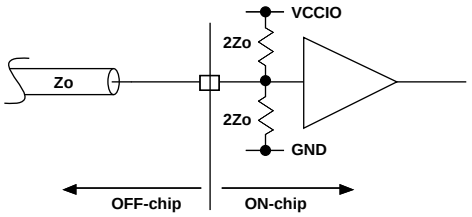
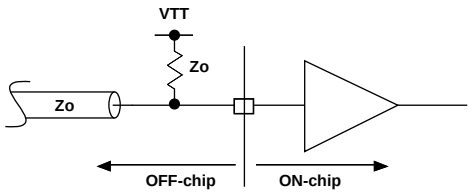
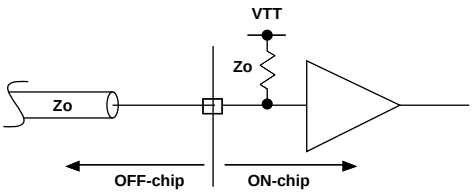
The DDR/Shift block contains registers and associated logic that support DDR and shift register functions using the high-speed clock and the associated transfer to the low-speed clock domain. It functions as a gearbox allowing high-speed incoming data to be passed into the FPGA fabric. Each PIO supports DDR and x2 shift functions. If desired PIOs A and B or C and D can be combined to form x4 shift functions. The PIOs A and C on the left, right and bottom of the device also contain an optional Adaptive Input Logic (AIL) element. This logic automatically aligns incoming data with the clock allowing for easy design of high-speed interfaces. Figure 2-21 shows a simplified block diagram of the shift register block. The shift block in conjunction with the update and clock divider blocks automatically handles the hand off between the low-speed and high-speed clock domains.

Single Ended Inputs: The SC devices support a number of different termination schemes for single ended inputs:

- Parallel to V_{CCIO} or GND
- Parallel to $V_{CCIO}/2$
- Parallel to V_{TT}

Figure 2-28 shows the single ended input schemes that are supported. The nominal values of the termination resistors are shown in Table 2-9.

Figure 2-28. Input Termination Schemes

Termination Type	Discrete Off-Chip Solution	Lattice On-Chip Solution
Parallel termination to to V_{CCIO}, or parallel to GND receiving end		
Parallel termination to $V_{CCIO}/2$ receiving end		
Parallel termination to V_{TT} at receiving end		

In many situations designers can chose whether to use Thevenin or parallel to V_{TT} termination. The Thevenin approach has the benefit of not requiring a termination voltage to be applied to the device. The parallel to V_{TT} approach consumes less power.

VTT Termination Resources

Each I/O bank, except bank 1, has a number of V_{TT} pins that must be connected if V_{TT} is used. Note V_{TT} pins can sink or source current and the power supply they are connected to must be able to handle the relatively high currents associated with the termination circuits. Note: V_{TT} is not available in all package styles.

On-chip parallel termination to V_{TT} is supported at the receiving end only. On-chip parallel output termination to V_{TT} is not supported.

The V_{TT} internal bus is also connected to the internal V_{CMT} node. Thus in one bank designers can implement either V_{TT} termination or V_{CMT} termination for differential inputs.

DDRII/RLDRAMII Termination Support

The DDR II memory and RLDRAMII (in Bidirection Data mode) standards require that the on-chip termination to V_{TT} be turned on when a pin is an input and off when the pin is an output. The LatticeSC devices contain the required circuitry to support this behavior. For additional detail refer to technical information at the end of the data sheet.

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

MLVDS

The LatticeSC devices support the MLVDS standard. This industry standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. MLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-1 is one possible solution for bi-directional multi-point differential signals.

Figure 3-1. MLVDS Multi-Point Output Example

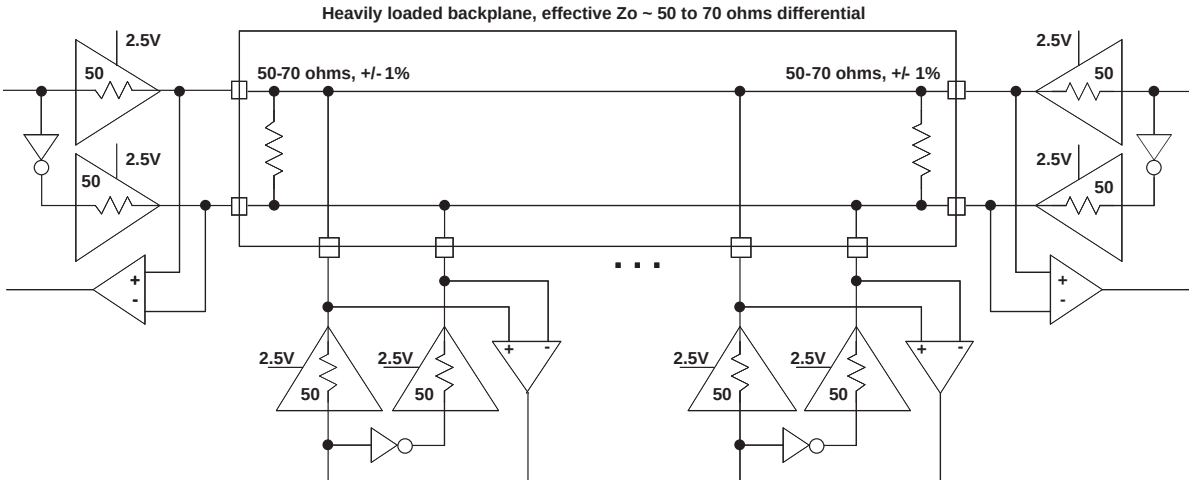


Table 3-1. MLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 50	Zo = 70	
Z_{OUT}	Output impedance	50	50	ohm
R_{TLEFT}	Left end termination	50	70	ohm
R_{TRIGHT}	Right end termination	50	70	ohm
V_{OH}	Output high voltage	1.50	1.575	V
V_{OL}	Output low voltage	1.00	0.925	V
V_{OD}	Output differential voltage	0.50	0.65	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	20.0	18.5	mA

1. For input buffer, see LVDS table.

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PIC row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
VREF1_x, VREF2_x	—	The reference supply pins for I/O bank x. Any I/O pin in a bank can be assigned as a reference supply pin, but software defaults use designated pin.
NC	—	No connect. NC pins should not be connected to any active signals, VCC or GND.
Non-SERDES Power Supplies		
VCCIOx	—	VCCIO - The power supply pins for I/O bank x. Dedicated pins.
VCC12[1]	—	1.2V supply for configuration logic, PLLs and SERDES Rx, Tx and PLL. All VCC12 pins must be connected. As VCC12 supplies power for analog circuitry, VCC12 should be quiet and isolated from noisy digital board supplies.
VTT_x	—	Termination voltage for bank x. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. VCMT function is not used in the bank. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.
GND	—	GND - Ground. Dedicated pins. All grounds must be electrically connected at the board level.
VCC	—	VCC - The power supply pins for core logic. Dedicated pins (1.2V/ 1.0V).
VCCAUX	—	VCCAUX - Auxiliary power supply pin - powers all differential and referenced input buffers. Dedicated pins (2.5V).
VCCJ	—	VCCJ - The power supply pin for JTAG Test Access Port.
PROBE_VCC	—	VCC signal - Connected to internal VCC node. Can be used for feedback to control an external board power converter. Can be unconnected if not used.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AF4	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AE5	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AG3	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AH2	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AD6	PB4C	5		PB4C	5	
AJ2	PB5A	5		PB5A	5	
AK2	PB5B	5		PB5B	5	
AD7	PB5C	5		PB5C	5	
AD8	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AH3	PB7A	5		PB11A	5	
AJ3	PB7B	5		PB11B	5	
AF9	PB7C	5		PB11C	5	
AE10	PB7D	5		PB11D	5	
AK3	PB8A	5		PB12A	5	
AJ4	PB8B	5		PB12B	5	
AE11	PB9A	5		PB13A	5	
AF10	PB9B	5		PB13B	5	
AK4	PB11A	5		PB16A	5	
AK5	PB11B	5		PB16B	5	
AH10	PB12A	5	PCLKT5_3	PB20A	5	PCLKT5_3
AH11	PB12B	5	PCLKC5_3	PB20B	5	PCLKC5_3
AF13	PB12C	5	PCLKT5_4	PB20C	5	PCLKT5_4
AE14	PB12D	5	PCLKC5_4	PB20D	5	PCLKC5_4
AK6	PB13A	5	PCLKT5_5	PB21A	5	PCLKT5_5
AK7	PB13B	5	PCLKC5_5	PB21B	5	PCLKC5_5
AF14	PB13C	5		PB21C	5	
AJ11	PB15A	5	PCLKT5_0	PB23A	5	PCLKT5_0
AJ12	PB15B	5	PCLKC5_0	PB23B	5	PCLKC5_0
AH13	PB15D	5	VREF2_5	PB23D	5	VREF2_5
AK8	PB16A	5	PCLKT5_1	PB24A	5	PCLKT5_1
AK9	PB16B	5	PCLKC5_1	PB24B	5	PCLKC5_1
AH14	PB17A	5	PCLKT5_2	PB25A	5	PCLKT5_2
AG14	PB17B	5	PCLKC5_2	PB25B	5	PCLKC5_2
AK10	PB19A	5		PB28A	5	
AK11	PB19B	5		PB28B	5	
AH15	PB20A	5		PB29A	5	
AG15	PB20B	5		PB29B	5	
AH12	PB21A	5		PB31A	5	
AJ13	PB21B	5		PB31B	5	
AD15	PB21C	5		PB31C	5	
AE15	PB21D	5		PB31D	5	
AK12	PB23A	5		PB32A	5	
AK13	PB23B	5		PB32B	5	
AJ14	PB24A	5		PB33A	5	
AJ15	PB24B	5		PB33B	5	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ27	GND	-		GND	-	
AF23	GND	-		GND	-	
AF22	GND	-		GND	-	
AE27	GND	-		GND	-	
AA27	GND	-		GND	-	
AB29	GND	-		GND	-	
Y26	GND	-		GND	-	
AC30	GND	-		GND	-	
Y29	GND	-		GND	-	
F30	GND	-		GND	-	
E27	GND	-		GND	-	
F27	GND	-		GND	-	
P25	GND	-		GND	-	
H29	GND	-		GND	-	
K29	GND	-		GND	-	
R24	GND	-		GND	-	
M28	GND	-		GND	-	
J27	GND	-		GND	-	
N26	GND	-		GND	-	
E20	GND	-		GND	-	
E21	GND	-		GND	-	
F21	GND	-		GND	-	
F23	GND	-		GND	-	
G23	GND	-		GND	-	
D21	GND	-		GND	-	
D20	GND	-		GND	-	
E18	GND	-		GND	-	
C20	GND	-		GND	-	
C11	GND	-		GND	-	
A12	GND	-		GND	-	
E11	GND	-		GND	-	
F8	GND	-		GND	-	
G8	GND	-		GND	-	
D11	GND	-		GND	-	
D10	GND	-		GND	-	
H7	GND	-		GND	-	
F10	GND	-		GND	-	
E10	GND	-		GND	-	
AC16	NC	-		NC	-	
J22	VCC	-		VCC	-	
J9	VCC	-		VCC	-	
B2	NC	-		NC	-	
C2	RESPN_ULC	-		RESPN_ULC	-	
C29	RESPN_URC	-		RESPN_URC	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
B30	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
D30	A_VDDOB0_L	-		A_VDDOB0_L	-	
A30	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
C31	A_HDINN0_L	-	PCS 360 CH 0 IN N	A_HDINN0_L	-	PCS 360 CH 0 IN N
C32	A_HDINP0_L	-	PCS 360 CH 0 IN P	A_HDINP0_L	-	PCS 360 CH 0 IN P
B31	A_VDDIB0_L	-		A_VDDIB0_L	-	
AL25	NC	-		PB26A	5	
AL24	NC	-		PB26B	5	
AG27	NC	-		PB26C	5	
AH27	NC	-		PB26D	5	
AM25	NC	-		PB27A	5	
AM24	NC	-		PB27B	5	
AL9	NC	-		PB62A	4	
AL8	NC	-		PB62B	4	
AK9	NC	-		PB63A	4	
AJ9	NC	-		PB63B	4	
AG10	NC	-		PB63C	4	
AG11	NC	-		PB63D	4	
J30	NC	-		PL26A	7	
H30	NC	-		PL26B	7	
M28	NC	-		PL26C	7	
N28	NC	-		PL26D	7	
J32	NC	-		PL27A	7	
J31	NC	-		PL27B	7	
N26	NC	-		PL27C	7	
N27	NC	-		PL27D	7	
K31	NC	-		PL29A	7	
K32	NC	-		PL29B	7	
P25	NC	-		PL29C	7	
P26	NC	-		PL29D	7	
L27	NC	-		PL22C	7	
L28	NC	-		PL22D	7	
M29	NC	-		PL30A	7	
L29	NC	-		PL30B	7	
M30	NC	-		PL31A	7	
L30	NC	-		PL31B	7	
L31	NC	-		PL34A	7	
M31	NC	-		PL34B	7	
AA29	NC	-		PL56A	6	
AA30	NC	-		PL56B	6	
AB31	NC	-		PL57A	6	
AA31	NC	-		PL57B	6	
AG30	NC	-		PL57C	6	
AG29	NC	-		PL57D	6	
AB29	NC	-		PL58A	6	
AB30	NC	-		PL58B	6	
Y25	NC	-		PL58C	6	
AA25	NC	-		PL58D	6	
AA8	NC	-		PR58D	3	
Y8	NC	-		PR58C	3	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ9	PB78C	4		PB117C	4	
AJ8	PB78D	4		PB117D	4	
AP3	PB79A	4		PB119A	4	
AN3	PB79B	4		PB119B	4	
AF10	PB79C	4		PB119C	4	
AE10	PB79D	4		PB119D	4	
AL7	PB81A	4		PB121A	4	
AL6	PB81B	4		PB121B	4	
AK7	PB81C	4		PB121C	4	
AK6	PB81D	4		PB121D	4	
AN5	PB82A	4		PB123A	4	
AN4	PB82B	4		PB123B	4	
AH9	PB82C	4	VREF1_4	PB123C	4	VREF1_4
AH8	PB82D	4		PB123D	4	
AM3	PB83A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB124A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AM4	PB83B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB124B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AG9	PB83C	4		PB124C	4	
AG8	PB83D	4		PB124D	4	
AN2	PB85A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB125A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AM2	PB85B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB125B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ6	PB85C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB125C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH6	PB85D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB125D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF7	PROBE_VCC	-		PROBE_VCC	-	
AF8	PROBE_GND	-		PROBE_GND	-	
AG7	PR71D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR95D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AG6	PR71C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR95C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AL4	PR71B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR95B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AL3	PR71A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR95A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD10	PR70D	3		PR94D	3	
AD9	PR70C	3		PR94C	3	
AH4	PR70B	3		PR94B	3	
AJ4	PR70A	3		PR94A	3	
AK5	PR69D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR93D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AJ5	PR69C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR93C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AM1	PR69B	3		PR93B	3	
AL1	PR69A	3		PR93A	3	
AH5	PR67D	3		PR91D	3	
AG5	PR67C	3		PR91C	3	
AL2	PR67B	3		PR91B	3	
AK2	PR67A	3		PR91A	3	
AB9	PR66D	3		PR90D	3	
AC9	PR66C	3		PR90C	3	
AH1	PR66B	3		PR90B	3	
AG1	PR66A	3		PR90A	3	
AE8	PR65D	3	VREF2_3	PR89D	3	VREF2_3

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
BA19	PB73A	4		PB87A	4	
BA18	PB73B	4		PB87B	4	
AU19	PB73C	4		PB87C	4	
AU18	PB73D	4		PB87D	4	
AV19	PB74A	4	PCLKT4_2	PB89A	4	PCLKT4_2
AV18	PB74B	4	PCLKC4_2	PB89B	4	PCLKC4_2
AN19	PB74C	4	PCLKT4_7	PB89C	4	PCLKT4_7
AP19	PB74D	4	PCLKC4_7	PB89D	4	PCLKC4_7
BB17	PB75A	4	PCLKT4_1	PB90A	4	PCLKT4_1
BB16	PB75B	4	PCLKC4_1	PB90B	4	PCLKC4_1
AT19	PB75C	4	PCLKT4_6	PB90C	4	PCLKT4_6
AT18	PB75D	4	PCLKC4_6	PB90D	4	PCLKC4_6
BA17	PB77A	4	PCLKT4_0	PB91A	4	PCLKT4_0
BA16	PB77B	4	PCLKC4_0	PB91B	4	PCLKC4_0
AR19	PB77C	4	VREF2_4	PB91C	4	VREF2_4
AR18	PB77D	4		PB91D	4	
AY17	PB79A	4	PCLKT4_5	PB93A	4	PCLKT4_5
AY16	PB79B	4	PCLKC4_5	PB93B	4	PCLKC4_5
AN18	PB79C	4		PB93C	4	
AP18	PB79D	4		PB93D	4	
AW17	PB80A	4	PCLKT4_3	PB94A	4	PCLKT4_3
AW16	PB80B	4	PCLKC4_3	PB94B	4	PCLKC4_3
AU17	PB80C	4	PCLKT4_4	PB94C	4	PCLKT4_4
AU16	PB80D	4	PCLKC4_4	PB94D	4	PCLKC4_4
AV17	PB81A	4		PB95A	4	
AV16	PB81B	4		PB95B	4	
AL18	PB81C	4		PB95C	4	
AM18	PB81D	4		PB95D	4	
BB15	PB83A	4		PB97A	4	
BB14	PB83B	4		PB97B	4	
AP17	PB83C	4		PB97C	4	
AN17	PB83D	4		PB97D	4	
BA15	PB84A	4		PB98A	4	
BA14	PB84B	4		PB98B	4	
AT16	PB84C	4		PB98C	4	
AT15	PB84D	4		PB98D	4	
AV15	PB85A	4		PB99A	4	
AV14	PB85B	4		PB99B	4	
AR16	PB85C	4		PB99C	4	
AR15	PB85D	4		PB99D	4	
AY14	PB87A	4		PB101A	4	
AY13	PB87B	4		PB101B	4	
AU15	PB87C	4		PB101C	4	
AU14	PB87D	4		PB101D	4	
BB13	PB88A	4		PB102A	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AP1	PR90B	3		PR109B	3	
AN1	PR90A	3		PR109A	3	
AK10	PR89D	3	VREF2_3	PR107D	3	VREF2_3
AJ10	PR89C	3		PR107C	3	
AM5	PR89B	3		PR107B	3	
AL5	PR89A	3		PR107A	3	
AL7	PR86D	3		PR104D	3	
AK7	PR86C	3		PR104C	3	
AM1	PR86B	3		PR104B	3	
AL1	PR86A	3		PR104A	3	
AJ11	PR85D	3		PR103D	3	
AH11	PR85C	3		PR103C	3	
AK5	PR85B	3		PR103B	3	
AJ5	PR85A	3		PR103A	3	
AK9	PR84D	3		PR99D	3	
AJ9	PR84C	3		PR99C	3	
AK3	PR84B	3		PR99B	3	
AJ3	PR84A	3		PR99A	3	
AK6	PR82D	3		PR98D	3	
AJ6	PR82C	3		PR98C	3	
AK2	PR82B	3		PR98B	3	
AJ2	PR82A	3		PR98A	3	
AH10	PR81D	3		PR96D	3	
AG10	PR81C	3		PR96C	3	
AK1	PR81B	3		PR96B	3	
AJ1	PR81A	3		PR96A	3	
AH9	PR80D	3		PR94D	3	
AG9	PR80C	3		PR94C	3	
AH2	PR80B	3		PR94B	3	
AG2	PR80A	3		PR94A	3	
AH8	PR78D	3		PR92D	3	
AG8	PR78C	3		PR92C	3	
AG1	PR78B	3		PR92B	3	
AH1	PR78A	3		PR92A	3	
AG14	PR77D	3		PR91D	3	
AF14	PR77C	3		PR91C	3	
AG4	PR77B	3		PR91B	3	
AF4	PR77A	3		PR91A	3	
AH7	PR76D	3	DIFFR_3	PR90D	3	DIFFR_3
AG7	PR76C	3		PR90C	3	
AG3	PR76B	3		PR90B	3	
AF3	PR76A	3		PR90A	3	
AH6	PR74D	3		PR88D	3	
AG6	PR74C	3		PR88C	3	
AF1	PR74B	3		PR88B	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AE1	PR74A	3		PR88A	3	
AF12	PR73D	3		PR87D	3	
AE12	PR73C	3		PR87C	3	
AF2	PR73B	3		PR87B	3	
AE2	PR73A	3		PR87A	3	
AF11	PR72D	3		PR86D	3	
AE11	PR72C	3		PR86C	3	
AF5	PR72B	3		PR86B	3	
AE5	PR72A	3		PR86A	3	
AF10	PR69D	3		PR83D	3	
AE10	PR69C	3		PR83C	3	
AD1	PR69B	3		PR83B	3	
AC1	PR69A	3		PR83A	3	
AF9	PR68D	3		PR82D	3	
AE9	PR68C	3		PR82C	3	
AD2	PR68B	3		PR82B	3	
AC2	PR68A	3		PR82A	3	
AF6	PR67D	3		PR81D	3	
AE6	PR67C	3		PR81C	3	
AD3	PR67B	3		PR81B	3	
AC3	PR67A	3		PR81A	3	
AE8	PR65D	3		PR79D	3	
AD8	PR65C	3		PR79C	3	
AD4	PR65B	3		PR79B	3	
AC4	PR65A	3		PR79A	3	
AE7	PR64D	3		PR78D	3	
AD7	PR64C	3		PR78C	3	
AD5	PR64B	3		PR78B	3	
AC5	PR64A	3		PR78A	3	
AD6	PR63D	3		PR77D	3	
AC6	PR63C	3		PR77C	3	
AB1	PR63B	3		PR77B	3	
AA1	PR63A	3		PR77A	3	
AD9	PR61D	3		PR75D	3	
AC9	PR61C	3		PR75C	3	
AB2	PR61B	3		PR75B	3	
AA2	PR61A	3		PR75A	3	
AD14	PR60D	3		PR74D	3	
AC14	PR60C	3		PR74C	3	
AB5	PR60B	3		PR74B	3	
AA5	PR60A	3		PR74A	3	
AD10	PR59D	3		PR73D	3	
AC10	PR59C	3		PR73C	3	
Y1	PR59B	3		PR73B	3	
W1	PR59A	3		PR73A	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
K14	VCC12	-		VCC12	-	
H11	B_VDDIB2_R	-		B_VDDIB2_R	-	
D8	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
E8	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
G5	VCC12	-		VCC12	-	
B9	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
L12	B_VDDOB2_R	-		B_VDDOB2_R	-	
A9	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
C5	B_VDDOB3_R	-		B_VDDOB3_R	-	
A10	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
H5	VCC12	-		VCC12	-	
B10	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
E9	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
D9	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
J13	VCC12	-		VCC12	-	
H12	B_VDDIB3_R	-		B_VDDIB3_R	-	
J12	VCC12	-		VCC12	-	
M14	B_REFCLKN_R	-		B_REFCLKN_R	-	
L14	B_REFCLKP_R	-		B_REFCLKP_R	-	
J14	VCC12	-		VCC12	-	
G12	C_VDDIB0_R	-		C_VDDIB0_R	-	
D10	C_HDINP0_R	-	PCS 3E2 CH 0 IN P	C_HDINP0_R	-	PCS 3E2 CH 0 IN P
E10	C_HDINN0_R	-	PCS 3E2 CH 0 IN N	C_HDINN0_R	-	PCS 3E2 CH 0 IN N
H6	VCC12	-		VCC12	-	
B11	C_HDOUTP0_R	-	PCS 3E2 CH 0 OUT P	C_HDOUTP0_R	-	PCS 3E2 CH 0 OUT P
M12	C_VDDOB0_R	-		C_VDDOB0_R	-	
A11	C_HDOUTN0_R	-	PCS 3E2 CH 0 OUT N	C_HDOUTN0_R	-	PCS 3E2 CH 0 OUT N
L11	C_VDDOB1_R	-		C_VDDOB1_R	-	
A12	C_HDOUTN1_R	-	PCS 3E2 CH 1 OUT N	C_HDOUTN1_R	-	PCS 3E2 CH 1 OUT N
K11	VCC12	-		VCC12	-	
B12	C_HDOUTP1_R	-	PCS 3E2 CH 1 OUT P	C_HDOUTP1_R	-	PCS 3E2 CH 1 OUT P
E11	C_HDINN1_R	-	PCS 3E2 CH 1 IN N	C_HDINN1_R	-	PCS 3E2 CH 1 IN N
D11	C_HDINP1_R	-	PCS 3E2 CH 1 IN P	C_HDINP1_R	-	PCS 3E2 CH 1 IN P
H13	VCC12	-		VCC12	-	
C6	C_VDDIB1_R	-		C_VDDIB1_R	-	
H15	VCC12	-		VCC12	-	
G13	C_VDDIB2_R	-		C_VDDIB2_R	-	
D12	C_HDINP2_R	-	PCS 3E2 CH 2 IN P	C_HDINP2_R	-	PCS 3E2 CH 2 IN P
E12	C_HDINN2_R	-	PCS 3E2 CH 2 IN N	C_HDINN2_R	-	PCS 3E2 CH 2 IN N
J9	VCC12	-		VCC12	-	
B13	C_HDOUTP2_R	-	PCS 3E2 CH 2 OUT P	C_HDOUTP2_R	-	PCS 3E2 CH 2 OUT P
K10	C_VDDOB2_R	-		C_VDDOB2_R	-	
A13	C_HDOUTN2_R	-	PCS 3E2 CH 2 OUT N	C_HDOUTN2_R	-	PCS 3E2 CH 2 OUT N
J10	C_VDDOB3_R	-		C_VDDOB3_R	-	
A14	C_HDOUTN3_R	-	PCS 3E2 CH 3 OUT N	C_HDOUTN3_R	-	PCS 3E2 CH 3 OUT N

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH27	VCCAUX	-		VCCAUX	-	
AH29	VCCAUX	-		VCCAUX	-	
AJ14	VCCAUX	-		VCCAUX	-	
AJ15	VCCAUX	-		VCCAUX	-	
AJ28	VCCAUX	-		VCCAUX	-	
AJ29	VCCAUX	-		VCCAUX	-	
P14	VCCAUX	-		VCCAUX	-	
P15	VCCAUX	-		VCCAUX	-	
P28	VCCAUX	-		VCCAUX	-	
P29	VCCAUX	-		VCCAUX	-	
R14	VCCAUX	-		VCCAUX	-	
R16	VCCAUX	-		VCCAUX	-	
R17	VCCAUX	-		VCCAUX	-	
R18	VCCAUX	-		VCCAUX	-	
R19	VCCAUX	-		VCCAUX	-	
R20	VCCAUX	-		VCCAUX	-	
R23	VCCAUX	-		VCCAUX	-	
R24	VCCAUX	-		VCCAUX	-	
R25	VCCAUX	-		VCCAUX	-	
R26	VCCAUX	-		VCCAUX	-	
R27	VCCAUX	-		VCCAUX	-	
R29	VCCAUX	-		VCCAUX	-	
T15	VCCAUX	-		VCCAUX	-	
T28	VCCAUX	-		VCCAUX	-	
U15	VCCAUX	-		VCCAUX	-	
U28	VCCAUX	-		VCCAUX	-	
V15	VCCAUX	-		VCCAUX	-	
V28	VCCAUX	-		VCCAUX	-	
W15	VCCAUX	-		VCCAUX	-	
W28	VCCAUX	-		VCCAUX	-	
Y15	VCCAUX	-		VCCAUX	-	
Y28	VCCAUX	-		VCCAUX	-	
F3	VCCIO1	-		VCCIO1	-	
F39	VCCIO1	-		VCCIO1	-	
G35	VCCIO1	-		VCCIO1	-	
G8	VCCIO1	-		VCCIO1	-	
L19	VCCIO1	-		VCCIO1	-	
L24	VCCIO1	-		VCCIO1	-	
M16	VCCIO1	-		VCCIO1	-	
M27	VCCIO1	-		VCCIO1	-	
N11	VCCIO1	-		VCCIO1	-	
N32	VCCIO1	-		VCCIO1	-	
AA4	VCCIO2	-		VCCIO2	-	
H7	VCCIO2	-		VCCIO2	-	
J4	VCCIO2	-		VCCIO2	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L8	VCCIO2	-		VCCIO2	-	
M3	VCCIO2	-		VCCIO2	-	
P7	VCCIO2	-		VCCIO2	-	
R4	VCCIO2	-		VCCIO2	-	
T12	VCCIO2	-		VCCIO2	-	
U8	VCCIO2	-		VCCIO2	-	
V3	VCCIO2	-		VCCIO2	-	
W11	VCCIO2	-		VCCIO2	-	
Y7	VCCIO2	-		VCCIO2	-	
AB3	VCCIO3	-		VCCIO3	-	
AC7	VCCIO3	-		VCCIO3	-	
AD11	VCCIO3	-		VCCIO3	-	
AE4	VCCIO3	-		VCCIO3	-	
AF8	VCCIO3	-		VCCIO3	-	
AG12	VCCIO3	-		VCCIO3	-	
AH3	VCCIO3	-		VCCIO3	-	
AJ7	VCCIO3	-		VCCIO3	-	
AK11	VCCIO3	-		VCCIO3	-	
AL4	VCCIO3	-		VCCIO3	-	
AM8	VCCIO3	-		VCCIO3	-	
AP3	VCCIO3	-		VCCIO3	-	
AR7	VCCIO3	-		VCCIO3	-	
AU4	VCCIO3	-		VCCIO3	-	
AL16	VCCIO4	-		VCCIO4	-	
AM13	VCCIO4	-		VCCIO4	-	
AM19	VCCIO4	-		VCCIO4	-	
AR11	VCCIO4	-		VCCIO4	-	
AR17	VCCIO4	-		VCCIO4	-	
AT14	VCCIO4	-		VCCIO4	-	
AT20	VCCIO4	-		VCCIO4	-	
AT8	VCCIO4	-		VCCIO4	-	
AW15	VCCIO4	-		VCCIO4	-	
AW21	VCCIO4	-		VCCIO4	-	
AW9	VCCIO4	-		VCCIO4	-	
AY12	VCCIO4	-		VCCIO4	-	
AY18	VCCIO4	-		VCCIO4	-	
AY6	VCCIO4	-		VCCIO4	-	
AL27	VCCIO5	-		VCCIO5	-	
AM24	VCCIO5	-		VCCIO5	-	
AM30	VCCIO5	-		VCCIO5	-	
AR26	VCCIO5	-		VCCIO5	-	
AR32	VCCIO5	-		VCCIO5	-	
AT23	VCCIO5	-		VCCIO5	-	
AT29	VCCIO5	-		VCCIO5	-	
AT35	VCCIO5	-		VCCIO5	-	

Lead-Free Packaging

Commercial

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-7FN256C	-7	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-6FN256C	-6	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-5FN256C	-5	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-7FN900C	-7	Lead-Free fpBGA	900	COM	15.2
LFSC3GA15E-6FN900C	-6	Lead-Free fpBGA	900	COM	15.2
LFSC3GA15E-5FN900C	-5	Lead-Free fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-7FN256C	-7	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-6FN256C	-6	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-5FN256C	-5	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-7FN900C	-7	Lead-Free fpBGA	900	COM	15.2
LFSCM3GA15EP1-6FN900C	-6	Lead-Free fpBGA	900	COM	15.2
LFSCM3GA15EP1-5FN900C	-5	Lead-Free fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-7FN900C	-7	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-6FN900C	-6	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-5FN900C	-5	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-7FFN1020C[1]	-7	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-6FFN1020C[1]	-6	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-5FFN1020C[1]	-5	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-7FN900C	-7	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-6FN900C	-6	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-5FN900C	-5	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-7FFN1020C[1]	-7	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-6FFN1020C[1]	-6	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-5FFN1020C[1]	-5	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Date	Version	Section	Change Summary
August 2006 (cont.)	01.3 (cont.)	DC and Switching Characteristics (cont.)	Updated LatticeSC Family Timing Adders with ispLEVER 6.0 SP1 results
			Updated PLL Timing Parameters based on PDE testing results
			Removed RDDATA parameter from sysCONFIG readback timing table
		Multiple	Changed TDO/RDDATA to TDO
		Pinout Information	Removed all MPI signals from SC15 256 pin package Dual Function Column
			Added note to SC15, SC25 900 pin package that the package supports a 16 bit MPI
			Added note that pin D3 in an SC15 and SC25 900 pin package should not be used for single-ended outputs
			Added note that pin D28 in an SC15 and SC25 900 pin package should not be used for single-ended outputs
			Added note to SC25 1020 pin package that the package supports a 16 bit MPI
			Added note to SC80 1152 pin package that the package supports a 32 bit MPI
			Added note to SC80 1704 pin package that the package supports a 32 bit MPI
		Ordering Information	Changed “fcBGA” for the 1020 packages to “ffBGA”
November 2006	01.4	Introduction	LatticeSC Family Selection Guide table – I/O count for SC80 device, 1704 fcBGA package changed to 904/32. I/O count for SC115 device, 1704 fcBGA package changed to 942/32.
		DC and Switching Characteristics	DC Electrical Characteristics table – Updated the initialization and standby supply current values.
			DC Electrical Characteristics table – Updated the sysCONFIG Master Parallel mode RCLK low and RCLK high time specifications.
			DC Electrical Characteristics table – Updated VCCIO values for LVPECL33 I/Os.
		Pin Information	Pin Information Summary table - Changed number of single ended user I/Os from 906 to 904 for 1704 fcBGA.
			Removed the single-ended only output restriction on pins D3 and D28 in an SC15 and SC25 900 pin package.
		Ordering Information	Ordering Information tables - Changed number of I/Os from 906 to 904 for 1704 fcBGA.
			Added ordering part numbers for LatticeSC/SCM 40K and 115K LUT devices.
			Added lead-free ordering part numbers.
		Multiple	Changed number of available SC80 I/O from 906 to 904.
			Changed number of available SC115 I/O from 944 to 942.
January 2007	01.4a	Architecture	Added EBR Asynchronous Reset section.
February 2007	01.4b	Architecture	Updated EBR Asynchronous Reset section.
March 2007	01.5	Architecture	Added EBR asynchronous reset clarification
			Clarified that differential drivers are not supported in banks 1, 4 and 5
		DC and Switching Characteristics	Added clarification for the description of the junction temperature specification in the Absolute Maximum Ratings section.
			Updated Initialization and Standby Current table.
			Updated LatticeSC External Switching Characteristics with ispLEVER 6.1 SP1 results.