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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

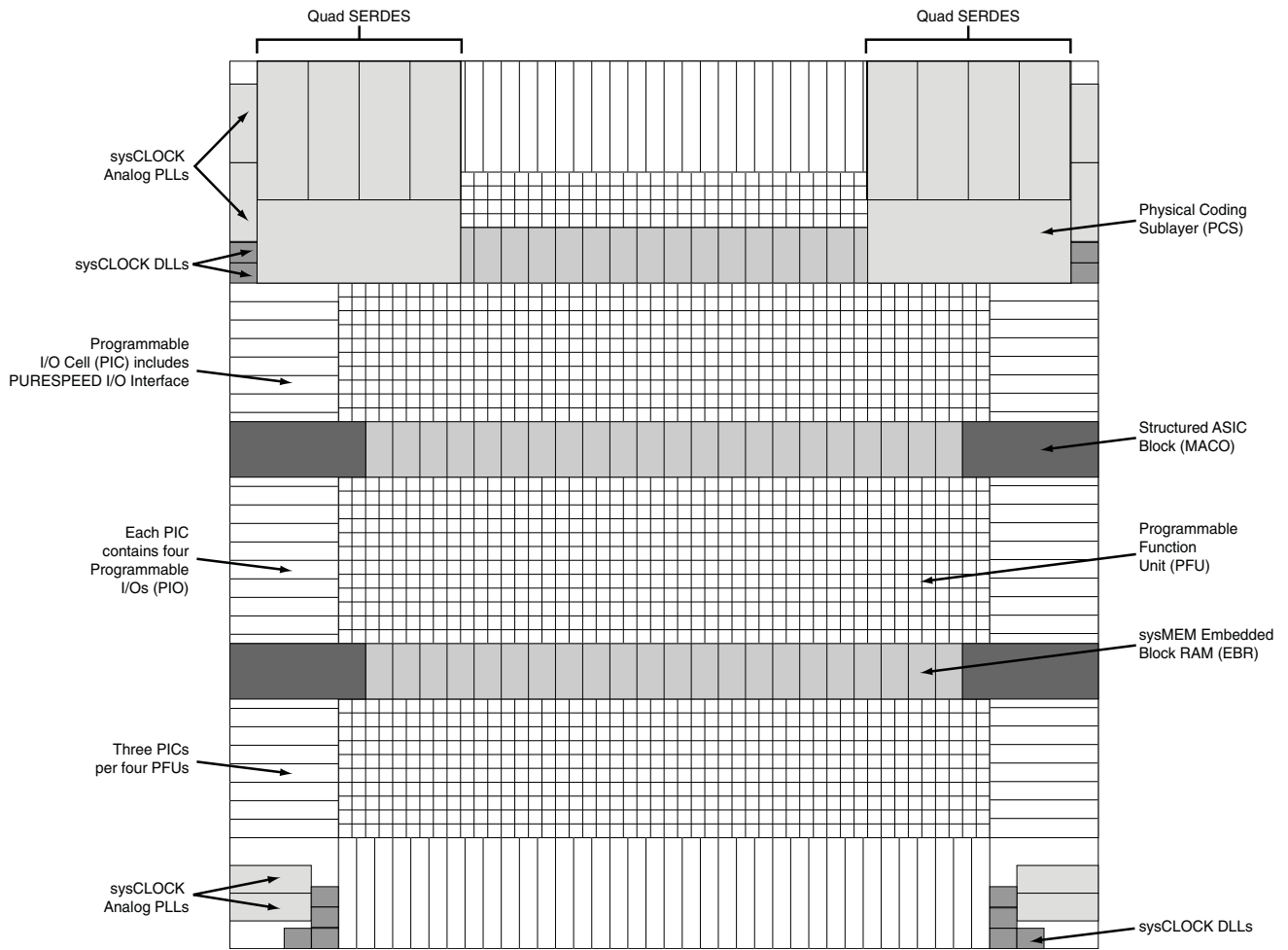
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	562
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-OFCBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga40ep1-6ffn1020i

Figure 2-1. Simplified Block Diagram (Top Level)



PFU Modes of Operation

Slices can be combined within a PFU to form larger functions. Table 2-4 tabulates these modes and documents the functionality possible at the PFU level.

Table 2-4. PFU Modes of Operation

Logic	Ripple	RAM	ROM
LUT 4x8 or MUX 2x1 x 8	2-bit Add x 4	SPR 16x2 x 4 DPR 16x2 x 2	ROM 16x1 x 8
LUT 5x4 or MUX 4x1 x 4	2-bit Sub x 4	SPR 16x4 x 2 DPR 16x4 x 1	ROM 16x2 x 4
LUT 6x2 or MUX 8x1 x 2	2-bit Counter x 4	SPR 16x8 x 1	ROM 16x4 x 2
LUT 7x1 or MUX 16x1 x 1	2-bit Comp x 4		ROM 16x8 x1

Routing

There are many resources provided in the LatticeSC devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

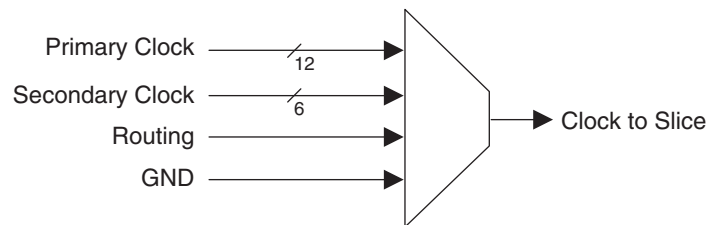
The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU) resources. The x1 and x2 connections provide fast and efficient connections in horizontal, vertical and diagonal directions. All connections are buffered to ensure high-speed operation even with long high-fanout connections.

The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Network

The LatticeSC devices have three distinct clock networks for use in distributing high-performance clocks within the device: primary clocks, secondary clocks and edge clocks. In addition to these dedicated clock networks, users are free to route clocks within the device using the general purpose routing. Figure 2-4 shows the clock resources available to each slice.

Figure 2-4. Slice Clock Selection



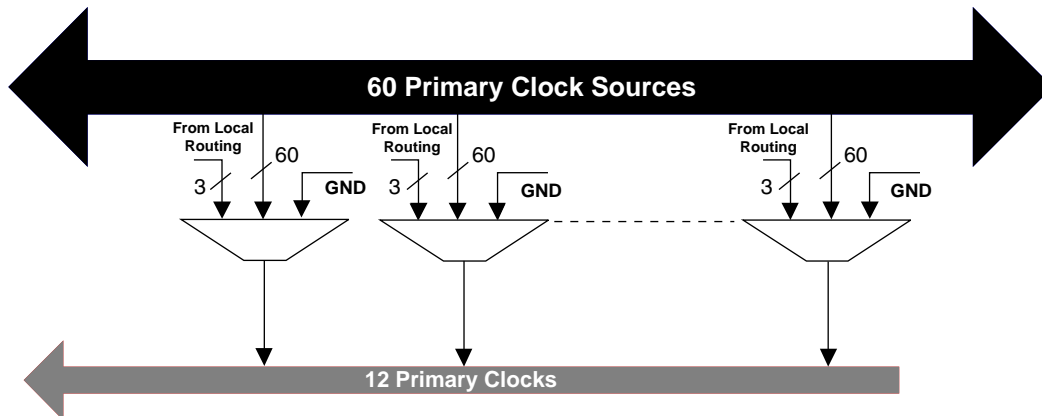
Note: GND is available to switch off the network.

Primary Clock Sources

LatticeSC devices have a wide variety of primary clock sources available. Primary clocks sources consists of the following:

- Primary clock input pins
- Edge clock input pins
- Two outputs per DLL

Figure 2-6. Per Quadrant Clock Selection



Note: GND is available to switch off the network.

Secondary Clocks

In addition to the primary clock network and edge clocks the LatticeSC devices also contain a secondary clock network. Built of X6 style routing elements this secondary clock network is ideal for routing slower speed clock and control signals throughout the device preserving high-speed clock networks for the most timing critical signals.

Edge Clocks

LatticeSC devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are eight edge clocks per bank for the top and bottom of the device. The left and right sides have eight edge clocks per side for both banks located on that side. Figure 2-7 shows the arrangement of edge clocks.

Edge clock resources can be driven from a variety of sources. Edge clock resources can be driven from:

- Edge clock PIOs in the same bank
- Primary clock PIOs in the same bank
- Routing
- Adjacent PLLs and DLLs
- ELSR output from the clock divider

Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the PURESPEED I/O buffers. The block contains a register for SDR operation and a group of three registers for DDR and shift register operation. The output signal tri-state control signal (TO) can be derived directly from one of the inputs (bypass mode), the SDR shift register, the DDR registers or the data associated with the buffer (for open drain emulation). Figure 2-24 shows the diagram of the Tristate Register Block.

Tristate SDR Register/Latch Block

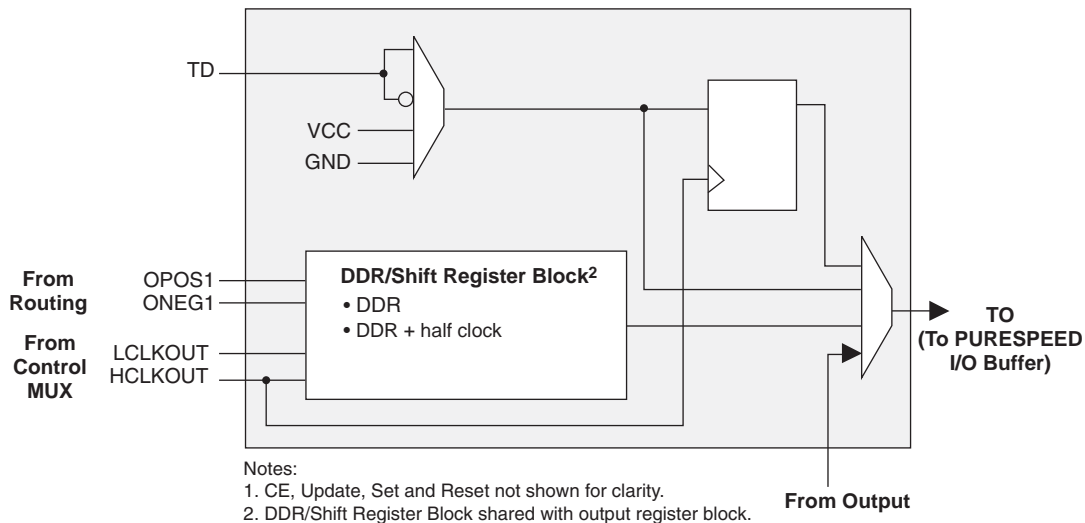
The SDR register operates on the positive edge of the high-speed clock. In it has a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR and Global Set Reset GSR enable or disable. The register LSR input is driven from LSRO, which is generated from the PIO control MUX. The GSR input is driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

Tristate DDR/Shift Register Block

The DDR/Shift block is shared with the output block allowing DDR support using the high-speed clock and the associated transfer from the low-speed clock domain. It functions as a gearbox allowing low-speed parallel data from the FPGA fabric to provide a high-speed tri-state control stream.

There is a special mode for DDR-II memory interfaces where the termination is controlled by the output tristate signal. During WRITE cycle when the FPGA is driving the lines, the parallel terminations are turned off. During READ cycle when the FPGA is receiving data, the parallel terminations are turned on.

Figure 2-24. Tristate Register Block¹



I/O Architecture Rules

Table 2-6 shows the PIO usage for x1, x2, x4 gearing. The checkmarks in the columns show the specific PIOs that are used for each gearing mode. When using x2 or x4 gearing, any PIO which is not used for gearing can still be used as an output.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
D[n:0]	I/O	In parallel configuration modes, D[7:0] receives configuration data, and each pin is pull-up enabled. For slave serial mode, D0 is the data input. D[7:3] is the output internal status for peripheral mode when RDN is low. D[7:0] is also the first byte of MPI data pins. In MPI configuration mode, MPI selectable data bus width from 8 and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction.
DP[m:0]	I/O	MPI selectable parity data bus width from 1, 2, and 3-bit DP[0] for D[7:0], DP[1] for D[15:8], and DP[2] for D[23:16].
BUSYN/RCLK/SCK	O	During configuration in peripheral mode, high on BUSYN indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D[7] in asynchronous peripheral mode. During configuration in slave parallel mode, low on BUSYN inhibits the external host from sending new data. The output is used by slave parallel and master serial modes only for decompression. During configuration in master parallel and master byte modes, RCLK is a read clock output signal to an external memory. The RCLK frequency is the same as CCLK when used with uncompressed bit-streams. RCLK will be 1/8 the frequency of CCLK when the bitstream is compressed. During configuration in SPI modes, SCK is generated by the device and connected to the CLK input of the FLASH memory.
MPI Interface (Dedicated pin)		
MPI_IRQ_N	O	MPI Interrupt request active low signal is controlled by system bus interrupt controller and may be sourced from any bus error or MPI configuration error. It can be connected to one of MPC860 IRQ pins.
MPI Interface (User I/O if MPI is not used.)		
MPI_CS0N MPI_CS1	I	MPI chip select pins, active low on MPI_CS0N while active high on MPI_CS1. Both have to be active during the whole transfer data phase. During transfer address phase, both can be inactive so that the decoding for them from address can be slow. If they are active during address phase, one cycle can be saved for sync read.
MPI_CLK	I	This is the PowerPC bus clock. It can be a source of the clock for embedded system bus. If MPI_CLK is used as system bus clock, MPI will be set into sync mode by default. All of the operation on PowerPC side of MPI are synchronized to the rising edge of this clock.
MPI_TSIZE[1:0]	I	Driven by a bus master to indicate the data transfer size for the transaction. 01 for byte, 10 for half-word, and 00 for word.
MPI_WR_N	I	Driven high indicates that a read access is in progress. Driven low indicates that a write access is in process.
MPI_BURST	I	Driven active low indicates that a burst transfer is in progress. Driven high indicates that the current transfer is not a burst.
MPI_BDIP	I	Active low "Burst Data in Process" is driven by a PowerPC processor. Asserted indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
N3	PL27A	6		PL30A	6	
P3	PL27B	6		PL30B	6	
P4	PL27C	6	PCLKT6_3	PL30C	6	PCLKT6_3
P2	PL28A	6		PL31A	6	
R2	PL28B	6		PL31B	6	
T3	PL28C	6	PCLKT6_2	PL31C	6	PCLKT6_2
R3	PL28D	6	PCLKC6_2	PL31D	6	PCLKC6_2
P1	PL31A	6		PL34A	6	
R1	PL31B	6		PL34B	6	
R5	PL31C	6	VREF1_6	PL34C	6	VREF1_6
R4	PL31D	6		PL34D	6	
T2	PL32A	6		PL35A	6	
U2	PL32B	6		PL35B	6	
T1	PL33A	6		PL38A	6	
U1	PL33B	6		PL38B	6	
V1	PL35A	6		PL42A	6	
W1	PL35B	6		PL42B	6	
V6	PL35D	6	DIFFR_6	PL42D	6	DIFFR_6
V2	PL36A	6		PL43A	6	
W2	PL36B	6		PL43B	6	
Y1	PL37A	6		PL44A	6	
AA1	PL37B	6		PL44B	6	
AB1	PL39A	6		PL48A	6	
AC1	PL39B	6		PL48B	6	
Y5	PL40A	6		PL49A	6	
Y6	PL40B	6		PL49B	6	
AD2	PL41A	6		PL51A	6	
AE2	PL41B	6		PL51B	6	
AB5	PL41D	6	VREF2_6	PL51D	6	VREF2_6
AC3	PL43A	6		PL52A	6	
AD3	PL43B	6		PL52B	6	
AF1	PL44A	6		PL55A	6	
AG1	PL44B	6		PL55B	6	
AB6	PL44C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL55C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AC5	PL44D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL55D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AF2	PL45A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL57A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AG2	PL45B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL57B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AC6	PL45C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL57C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AC7	PL45D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL57D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AE4	XRES	-		XRES	-	
AG4	VCC12	-		VCC12	-	
AD5	TEMP	6		TEMP	6	
AF5	VCC12	-		VCC12	-	
AH1	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AJ1	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AF4	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AE5	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AG3	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AH2	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AD6	PB4C	5		PB4C	5	
AJ2	PB5A	5		PB5A	5	
AK2	PB5B	5		PB5B	5	
AD7	PB5C	5		PB5C	5	
AD8	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AH3	PB7A	5		PB11A	5	
AJ3	PB7B	5		PB11B	5	
AF9	PB7C	5		PB11C	5	
AE10	PB7D	5		PB11D	5	
AK3	PB8A	5		PB12A	5	
AJ4	PB8B	5		PB12B	5	
AE11	PB9A	5		PB13A	5	
AF10	PB9B	5		PB13B	5	
AK4	PB11A	5		PB16A	5	
AK5	PB11B	5		PB16B	5	
AH10	PB12A	5	PCLKT5_3	PB20A	5	PCLKT5_3
AH11	PB12B	5	PCLKC5_3	PB20B	5	PCLKC5_3
AF13	PB12C	5	PCLKT5_4	PB20C	5	PCLKT5_4
AE14	PB12D	5	PCLKC5_4	PB20D	5	PCLKC5_4
AK6	PB13A	5	PCLKT5_5	PB21A	5	PCLKT5_5
AK7	PB13B	5	PCLKC5_5	PB21B	5	PCLKC5_5
AF14	PB13C	5		PB21C	5	
AJ11	PB15A	5	PCLKT5_0	PB23A	5	PCLKT5_0
AJ12	PB15B	5	PCLKC5_0	PB23B	5	PCLKC5_0
AH13	PB15D	5	VREF2_5	PB23D	5	VREF2_5
AK8	PB16A	5	PCLKT5_1	PB24A	5	PCLKT5_1
AK9	PB16B	5	PCLKC5_1	PB24B	5	PCLKC5_1
AH14	PB17A	5	PCLKT5_2	PB25A	5	PCLKT5_2
AG14	PB17B	5	PCLKC5_2	PB25B	5	PCLKC5_2
AK10	PB19A	5		PB28A	5	
AK11	PB19B	5		PB28B	5	
AH15	PB20A	5		PB29A	5	
AG15	PB20B	5		PB29B	5	
AH12	PB21A	5		PB31A	5	
AJ13	PB21B	5		PB31B	5	
AD15	PB21C	5		PB31C	5	
AE15	PB21D	5		PB31D	5	
AK12	PB23A	5		PB32A	5	
AK13	PB23B	5		PB32B	5	
AJ14	PB24A	5		PB33A	5	
AJ15	PB24B	5		PB33B	5	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P32	PL30A	6		PL39A	6	
P31	PL30B	6		PL39B	6	
R28	PL30C	6	PCLKT6_3	PL39C	6	PCLKT6_3
T28	PL30D	6	PCLKC6_3	PL39D	6	PCLKC6_3
R30	PL31A	6		PL40A	6	
R29	PL31B	6		PL40B	6	
T25	PL31C	6	PCLKT6_2	PL40C	6	PCLKT6_2
T26	PL31D	6	PCLKC6_2	PL40D	6	PCLKC6_2
R31	PL34A	6		PL43A	6	
R32	PL34B	6		PL43B	6	
U23	PL34C	6	VREF1_6	PL43C	6	VREF1_6
U24	PL34D	6		PL43D	6	
T31	PL35A	6		PL44A	6	
T32	PL35B	6		PL44B	6	
T27	PL35C	6		PL44C	6	
U28	PL35D	6		PL44D	6	
U32	PL36A	6		PL45A	6	
U31	PL36B	6		PL45B	6	
U26	PL36C	6		PL45C	6	
U25	PL36D	6		PL45D	6	
V32	PL38A	6		PL47A	6	
V31	PL38B	6		PL47B	6	
V24	PL38C	6		PL47C	6	
V23	PL38D	6		PL47D	6	
V29	PL39A	6		PL48A	6	
V30	PL39B	6		PL48B	6	
U27	PL39C	6		PL48C	6	
V28	PL39D	6		PL48D	6	
W30	PL40A	6		PL49A	6	
W29	PL40B	6		PL49B	6	
V25	PL40C	6		PL49C	6	
W26	PL40D	6		PL49D	6	
W31	PL42A	6		PL51A	6	
Y31	PL42B	6		PL51B	6	
W27	PL42C	6		PL51C	6	
Y27	PL42D	6	DIFFR_6	PL51D	6	DIFFR_6
W28	PL43A	6		PL52A	6	
Y28	PL43B	6		PL52B	6	
Y26	PL43C	6		PL52C	6	
W25	PL43D	6		PL52D	6	
W32	PL44A	6		PL53A	6	
Y32	PL44B	6		PL53B	6	
AB28	PL44C	6		PL53C	6	
AA28	PL44D	6		PL53D	6	
AB32	PL47A	6		PL60A	6	
AA32	PL47B	6		PL60B	6	
AB27	PL47C	6		PL60C	6	
AC27	PL47D	6		PL60D	6	
AD31	PL48A	6		PL61A	6	
AC31	PL48B	6		PL61B	6	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD8	PR65C	3		PR89C	3	
AJ3	PR65B	3		PR89B	3	
AH3	PR65A	3		PR89A	3	
AD7	PR62D	3		PR86D	3	
AC7	PR62C	3		PR86C	3	
AJ2	PR62B	3		PR86B	3	
AH2	PR62A	3		PR86A	3	
AF6	PR61D	3		PR85D	3	
AF5	PR61C	3		PR85C	3	
AF4	PR61B	3		PR85B	3	
AE4	PR61A	3		PR85A	3	
AD6	PR60D	3		PR84D	3	
AC6	PR60C	3		PR84C	3	
AG2	PR60B	3		PR84B	3	
AF2	PR60A	3		PR84A	3	
AC8	PR58D	3		PR82D	3	
AB8	PR58C	3		PR82C	3	
AK1	PR58B	3		PR82B	3	
AJ1	PR58A	3		PR82A	3	
AB10	PR57D	3		PR81D	3	
AA10	PR57C	3		PR81C	3	
AF3	PR57B	3		PR81B	3	
AE3	PR57A	3		PR81A	3	
AE5	PR56D	3		PR80D	3	
AD5	PR56C	3		PR80C	3	
AE2	PR56B	3		PR80B	3	
AD2	PR56A	3		PR80A	3	
AC5	PR53D	3		PR78D	3	
AB5	PR53C	3		PR78C	3	
AF1	PR53B	3		PR78B	3	
AE1	PR53A	3		PR78A	3	
AA11	PR52D	3		PR77D	3	
Y11	PR52C	3		PR77C	3	
AC4	PR52B	3		PR77B	3	
AB4	PR52A	3		PR77A	3	
AA8	PR51D	3	DIFFR_3	PR76D	3	DIFFR_3
AA9	PR51C	3		PR76C	3	
AC3	PR51B	3		PR76B	3	
AB3	PR51A	3		PR76A	3	
AA7	PR49D	3		PR65D	3	
Y7	PR49C	3		PR65C	3	
AA2	PR49B	3		PR65B	3	
Y2	PR49A	3		PR65A	3	
AA6	PR48D	3		PR63D	3	
Y6	PR48C	3		PR63C	3	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
D7	B_VDDIB0_R	-		B_VDDIB0_R	-	
E10	B_HDINP0_R	-	PCS 3E1 CH 0 IN P	B_HDINP0_R	-	PCS 3E1 CH 0 IN P
F10	B_HDINN0_R	-	PCS 3E1 CH 0 IN N	B_HDINN0_R	-	PCS 3E1 CH 0 IN N
K10	VCC12	-		VCC12	-	
A11	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P
D10	B_VDDOB0_R	-		B_VDDOB0_R	-	
B11	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N
D11	B_VDDOB1_R	-		B_VDDOB1_R	-	
B12	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N
L10	VCC12	-		VCC12	-	
A12	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P
F11	B_HDINN1_R	-	PCS 3E1 CH 1 IN N	B_HDINN1_R	-	PCS 3E1 CH 1 IN N
E11	B_HDINP1_R	-	PCS 3E1 CH 1 IN P	B_HDINP1_R	-	PCS 3E1 CH 1 IN P
G11	VCC12	-		VCC12	-	
D8	B_VDDIB1_R	-		B_VDDIB1_R	-	
G12	VCC12	-		VCC12	-	
D9	B_VDDIB2_R	-		B_VDDIB2_R	-	
E12	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
F12	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
K11	VCC12	-		VCC12	-	
A13	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D12	B_VDDOB2_R	-		B_VDDOB2_R	-	
B13	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D13	B_VDDOB3_R	-		B_VDDOB3_R	-	
B14	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
L11	VCC12	-		VCC12	-	
A14	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
F13	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
E13	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
G13	VCC12	-		VCC12	-	
E9	B_VDDIB3_R	-		B_VDDIB3_R	-	
L13	VCC12	-		VCC12	-	
J11	B_REFCLKN_R	-		B_REFCLKN_R	-	
H11	B_REFCLKP_R	-		B_REFCLKP_R	-	
M15	PT61D	1	HDC/SI	PT77D	1	HDC/SI
M16	PT61C	1	LDCN/SCS	PT77C	1	LDCN/SCS
F14	PT59B	1	D8/MPI_DATA8	PT77B	1	D8/MPI_DATA8
G14	PT59A	1	CS1/MPI_CS1	PT77A	1	CS1/MPI_CS1
L15	PT58D	1	D9/MPI_DATA9	PT75D	1	D9/MPI_DATA9
L14	PT58C	1	D10/MPI_DATA10	PT75C	1	D10/MPI_DATA10
D14	PT57B	1	CS0N/MPI_CS0N	PT75B	1	CS0N/MPI_CS0N
E14	PT57A	1	RDN/MPI_STRB_N	PT75A	1	RDN/MPI_STRB_N
L16	PT55D	1	WRN/MPI_WR_N	PT74D	1	WRN/MPI_WR_N
K16	PT55C	1	D7/MPI_DATA7	PT74C	1	D7/MPI_DATA7
G15	PT55B	1	D6/MPI_DATA6	PT74B	1	D6/MPI_DATA6

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1,2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
G27	A_REFCLKP_L	-	
H27	A_REFCLKN_L	-	
H25	VCC12	-	
H26	RESP_ULC	-	
B33	RESETN	1	
C34	TSALLN	1	
D34	DONE	1	
C33	INITN	1	
J27	M0	1	
K27	M1	1	
M26	M2	1	
L26	M3	1	
F30	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
G30	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
H28	PL15C	7	
J28	PL15D	7	
F31	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
G31	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N25	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P25	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
D33	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
E33	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
H29	PL18C	7	
J29	PL18D	7	VREF2_7
F32	PL19A	7	
G32	PL19B	7	
P26	PL19C	7	
N26	PL19D	7	
H30	PL26A	7	
J30	PL26B	7	
L28	PL26C	7	
M28	PL26D	7	
J31	PL43A	7	
K31	PL43B	7	
L27	PL43C	7	VREF1_7
M27	PL43D	7	DIFFR_7
J32	PL45A	7	
K32	PL45B	7	
L29	PL45C	7	
M29	PL45D	7	
H33	PL47A	7	
J33	PL47B	7	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1,2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
D9	B_VDDIB2_R	-	
E12	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
F12	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
K11	VCC12	-	
A13	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D12	B_VDDOB2_R	-	
B13	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D13	B_VDDOB3_R	-	
B14	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
L11	VCC12	-	
A14	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
F13	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
E13	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
G13	VCC12	-	
E9	B_VDDIB3_R	-	
L13	VCC12	-	
J11	B_REFCLKN_R	-	
H11	B_REFCLKP_R	-	
M15	PT93D	1	HDC/SI
M16	PT93C	1	LDCN/SCS
F14	PT93B	1	D8/MPI_DATA8
G14	PT93A	1	CS1/MPI_CS1
L15	PT90D	1	D9/MPI_DATA9
L14	PT90C	1	D10/MPI_DATA10
D14	PT90B	1	CS0N/MPI_CS0N
E14	PT90A	1	RDN/MPI_STRB_N
L16	PT89D	1	WRN/MPI_WR_N
K16	PT89C	1	D7/MPI_DATA7
G15	PT89B	1	D6/MPI_DATA6
F15	PT89A	1	D5/MPI_DATA5
K14	PT87D	1	D4/MPI_DATA4
K13	PT87C	1	D3/MPI_DATA3
B15	PT87B	1	D2/MPI_DATA2
A15	PT87A	1	D1/MPI_DATA1
J14	PT86D	1	D16/PCLKC1_3/MPI_DATA16
H14	PT86C	1	D17/PCLKT1_3/MPI_DATA17
A16	PT86B	1	D0/MPI_DATA0
B16	PT86A	1	QOUT/CEON
J13	PT83D	1	VREF2_1
H13	PT83C	1	D18/MPI_DATA18
D15	PT83B	1	DOUT
E15	PT83A	1	MCA_DONE_IN
J16	PT81D	1	D19/PCLKC1_2/MPI_DATA19

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
J17	PT81C	1	D20/PCLKT1_2/MPI_DATA20
D16	PT81B	1	MCA_CLK_P1_OUT
E16	PT81A	1	MCA_CLK_P1_IN
H15	PT78D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT78C	1	D22/PCLKT1_1/MPI_DATA22
C15	PT78B	1	MCA_CLK_P2_OUT
C16	PT78A	1	MCA_CLK_P2_IN
L17	PT75D	1	MCA_DONE_OUT
K17	PT75C	1	BUSYN/RCLK/SCK
E17	PT75B	1	DP0/MPI_PAR0
F17	PT75A	1	MPI_TA
G17	PT73D	1	D23/MPI_DATA23
H17	PT73C	1	DP2/MPI_PAR2
A17	PT73B	1	PCLKC1_0
B17	PT73A	1	PCLKT1_0/MPI_CLK
G18	PT71D	1	DP3/PCLKC1_4/MPI_PAR3
H18	PT71C	1	D24/PCLKT1_4/MPI_DATA24
E18	PT71B	1	MPI_RETRY
F18	PT71A	1	A0/MPI_ADDR14
J18	PT69D	1	A1/MPI_ADDR15
J19	PT69C	1	A2/MPI_ADDR16
C20	PT69B	1	A3/MPI_ADDR17
C19	PT69A	1	A4/MPI_ADDR18
K18	PT66D	1	D25/PCLKC1_5/MPI_DATA25
L18	PT66C	1	D26/PCLKT1_5/MPI_DATA26
D19	PT66B	1	A5/MPI_ADDR19
E19	PT66A	1	A6/MPI_ADDR20
H19	PT63D	1	D27/MPI_DATA27
H20	PT63C	1	VREF1_1
A18	PT63B	1	A7/MPI_ADDR21
B18	PT63A	1	A8/MPI_ADDR22
H21	PT61D	1	D28/PCLKC1_6/MPI_DATA28
J21	PT61C	1	D29/PCLKT1_6/MPI_DATA29
A19	PT61B	1	A9/MPI_ADDR23
B19	PT61A	1	A10/MPI_ADDR24
H22	PT58D	1	D30/PCLKC1_7/MPI_DATA30
J22	PT58C	1	D31/PCLKT1_7/MPI_DATA31
F20	PT58B	1	A11/MPI_ADDR25
G20	PT58A	1	A12/MPI_ADDR26
K21	PT57D	1	D11/MPI_DATA11
K22	PT57C	1	D12/MPI_DATA12
A20	PT57B	1	A13/MPI_ADDR27
B20	PT57A	1	A14/MPI_ADDR28

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AL5	GND	-	
AM14	GND	-	
AM18	GND	-	
AM24	GND	-	
AM30	GND	-	
AM8	GND	-	
AN1	GND	-	
AN34	GND	-	
AP2	GND	-	
AP33	GND	-	
B1	GND	-	
B34	GND	-	
C11	GND	-	
C12	GND	-	
C13	GND	-	
C14	GND	-	
C17	GND	-	
C21	GND	-	
C22	GND	-	
C23	GND	-	
C24	GND	-	
C26	GND	-	
C27	GND	-	
C30	GND	-	
C31	GND	-	
C4	GND	-	
C5	GND	-	
C8	GND	-	
C9	GND	-	
D18	GND	-	
E32	GND	-	
E4	GND	-	
F19	GND	-	
G16	GND	-	
G29	GND	-	
G7	GND	-	
H3	GND	-	
H31	GND	-	
J10	GND	-	
J15	GND	-	
J26	GND	-	
K20	GND	-	
K23	GND	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
R12	VTT_2	2	
T12	VTT_2	2	
AB11	VTT_3	3	
W12	VTT_3	3	
Y12	VTT_3	3	
AC15	VTT_4	4	
AC16	VTT_4	4	
AD13	VTT_4	4	
AC19	VTT_5	5	
AC20	VTT_5	5	
AD22	VTT_5	5	
AB24	VTT_6	6	
W23	VTT_6	6	
Y23	VTT_6	6	
N24	VTT_7	7	
R23	VTT_7	7	
T23	VTT_7	7	
M12	VDDAX25_R	-	
M23	VDDAX25_L	-	
Y16	GND	-	
Y14	GND	-	
N21	VCC12	-	
P22	VCC12	-	
AA22	VCC12	-	
AB21	VCC12	-	
AB14	VCC12	-	
AA13	VCC12	-	
P13	VCC12	-	
N14	VCC12	-	
G26	NC	-	
G9	NC	-	
J12	NC	-	
H12	NC	-	
H23	NC	-	
J23	NC	-	

1. Differential pair grouping within a PCI is A (True) and B (complement) and C (True) and D (Complement).
 2. The LatticeSC/M115 in an 1152-pin package supports a 32-bit MPI interface.

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
V8	PR41C	2		PR55C	2	
T4	PR41B	2		PR55B	2	
U4	PR41A	2		PR55A	2	
V9	PR39D	2		PR53D	2	
U9	PR39C	2		PR53C	2	
V6	PR39B	2		PR53B	2	
U6	PR39A	2		PR53A	2	
AA12	PR38D	2		PR52D	2	
Y12	PR38C	2		PR52C	2	
P1	PR38B	2		PR52B	2	
N1	PR38A	2		PR52A	2	
T7	PR37D	2		PR51D	2	
R7	PR37C	2		PR51C	2	
T5	PR37B	2		PR51B	2	
R5	PR37A	2		PR51A	2	
U10	PR35D	2		PR49D	2	
V10	PR35C	2		PR49C	2	
P2	PR35B	2		PR49B	2	
N2	PR35A	2		PR49A	2	
T8	PR34D	2		PR48D	2	
R8	PR34C	2		PR48C	2	
N3	PR34B	2		PR48B	2	
P3	PR34A	2		PR48A	2	
M6	PR33D	2		PR47D	2	
M7	PR33C	2		PR47C	2	
T6	PR33B	2		PR47B	2	
R6	PR33A	2		PR47A	2	
V11	PR31D	2		PR45D	2	
U11	PR31C	2		PR45C	2	
M1	PR31B	2		PR45B	2	
L1	PR31A	2		PR45A	2	
Y14	PR30D	2		PR44D	2	
W14	PR30C	2		PR44C	2	
M2	PR30B	2		PR44B	2	
L2	PR30A	2		PR44A	2	
T9	PR29D	2	DIFFR_2	PR43D	2	DIFFR_2
R9	PR29C	2	VREF1_2	PR43C	2	VREF1_2
P4	PR29B	2		PR43B	2	
N4	PR29A	2		PR43A	2	
N7	PR26D	2		PR40D	2	
N8	PR26C	2		PR40C	2	
P5	PR26B	2		PR40B	2	
N5	PR26A	2		PR40A	2	
K7	PR25D	2		PR38D	2	
J7	PR25C	2		PR38C	2	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
J1	PR25B	2		PR38B	2	
K1	PR25A	2		PR38A	2	
V12	PR24D	2		PR34D	2	
U12	PR24C	2		PR34C	2	
K2	PR24B	2		PR34B	2	
J2	PR24A	2		PR34A	2	
R10	PR22D	2		PR30D	2	
T10	PR22C	2		PR30C	2	
L5	PR22B	2		PR30B	2	
K5	PR22A	2		PR30A	2	
P9	PR21D	2		PR26D	2	
N9	PR21C	2		PR26C	2	
L6	PR21B	2		PR26B	2	
K6	PR21A	2		PR26A	2	
M8	PR20D	2		PR19D	2	
M9	PR20C	2		PR19C	2	
H1	PR20B	2		PR19B	2	
G1	PR20A	2		PR19A	2	
U14	PR18D	2	VREF2_2	PR18D	2	VREF2_2
T14	PR18C	2		PR18C	2	
H2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
G2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
H3	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
G3	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
R11	PR16D	2		PR15D	2	
P11	PR16C	2		PR15C	2	
J5	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
J6	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
P18	VCCJ	-		VCCJ	-	
P19	TDO	-	TDO	TDO	-	TDO
R21	TMS	-		TMS	-	
P20	TCK	-		TCK	-	
P12	TDI	-		TDI	-	
P17	PROGRAMN	1		PROGRAMN	1	
P21	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
P13	CCLK	1		CCLK	1	
H10	RESP_URC	-		RESP_URC	-	
N13	VCC12	-		VCC12	-	
H9	A_REFCLKN_R	-		A_REFCLKN_R	-	
G9	A_REFCLKP_R	-		A_REFCLKP_R	-	
F2	VCC12	-		VCC12	-	
H4	A_VDDIB0_R	-		A_VDDIB0_R	-	
C1	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
H18	PT77C	1	LDCN/SCS	PT93C	1	LDCN/SCS
F18	PT77B	1	D8/MPI_DATA8	PT93B	1	D8/MPI_DATA8
E18	PT77A	1	CS1/MPI_CS1	PT93A	1	CS1/MPI_CS1
H19	PT75D	1	D9/MPI_DATA9	PT90D	1	D9/MPI_DATA9
G19	PT75C	1	D10/MPI_DATA10	PT90C	1	D10/MPI_DATA10
D19	PT75B	1	CS0N/MPI_CS0N	PT90B	1	CS0N/MPI_CS0N
D18	PT75A	1	RDN/MPI_STRB_N	PT90A	1	RDN/MPI_STRB_N
J20	PT74D	1	WRN/MPI_WR_N	PT89D	1	WRN/MPI_WR_N
K20	PT74C	1	D7/MPI_DATA7	PT89C	1	D7/MPI_DATA7
E19	PT74B	1	D6/MPI_DATA6	PT89B	1	D6/MPI_DATA6
F19	PT74A	1	D5/MPI_DATA5	PT89A	1	D5/MPI_DATA5
K18	PT73D	1	D4/MPI_DATA4	PT87D	1	D4/MPI_DATA4
J18	PT73C	1	D3/MPI_DATA3	PT87C	1	D3/MPI_DATA3
A19	PT73B	1	D2/MPI_DATA2	PT87B	1	D2/MPI_DATA2
B19	PT73A	1	D1/MPI_DATA1	PT87A	1	D1/MPI_DATA1
H17	PT71D	1	D16/PCLKC1_3/MPI_DATA16	PT86D	1	D16/PCLKC1_3/MPI_DATA16
J17	PT71C	1	D17/PCLKT1_3/MPI_DATA17	PT86C	1	D17/PCLKT1_3/MPI_DATA17
B20	PT71B	1	D0/MPI_DATA0	PT86B	1	D0/MPI_DATA0
C20	PT71A	1	QOUT/CEON	PT86A	1	QOUT/CEON
M20	PT70D	1	VREF2_1	PT83D	1	VREF2_1
L20	PT70C	1	D18/MPI_DATA18	PT83C	1	D18/MPI_DATA18
F20	PT70B	1	DOUT	PT83B	1	DOUT
G20	PT70A	1	MCA_DONE_IN	PT83A	1	MCA_DONE_IN
K19	PT69D	1	D19/PCLKC1_2/MPI_DATA19	PT81D	1	D19/PCLKC1_2/MPI_DATA19
J19	PT69C	1	D20/PCLKT1_2/MPI_DATA20	PT81C	1	D20/PCLKT1_2/MPI_DATA20
D20	PT69B	1	MCA_CLK_P1_OUT	PT81B	1	MCA_CLK_P1_OUT
E20	PT69A	1	MCA_CLK_P1_IN	PT81A	1	MCA_CLK_P1_IN
H21	PT67D	1	D21/PCLKC1_1/MPI_DATA21	PT78D	1	D21/PCLKC1_1/MPI_DATA21
G21	PT67C	1	D22/PCLKT1_1/MPI_DATA22	PT78C	1	D22/PCLKT1_1/MPI_DATA22
B21	PT67B	1	MCA_CLK_P2_OUT	PT78B	1	MCA_CLK_P2_OUT
C21	PT67A	1	MCA_CLK_P2_IN	PT78A	1	MCA_CLK_P2_IN
M21	PT66D	1	MCA_DONE_OUT	PT75D	1	MCA_DONE_OUT
L21	PT66C	1	BUSYN/RCLK/SCK	PT75C	1	BUSYN/RCLK/SCK
A21	PT66B	1	DP0/MPI_PAR0	PT75B	1	DP0/MPI_PAR0
A20	PT66A	1	MPI_TA	PT75A	1	MPI_TA
J21	PT65D	1	D23/MPI_DATA23	PT73D	1	D23/MPI_DATA23
K21	PT65C	1	DP2/MPI_PAR2	PT73C	1	DP2/MPI_PAR2
E21	PT65B	1	PCLKC1_0	PT73B	1	PCLKC1_0
F21	PT65A	1	PCLKT1_0/MPI_CLK	PT73A	1	PCLKT1_0/MPI_CLK
G22	PT63D	1	DP3/PCLKC1_4/MPI_PAR3	PT71D	1	DP3/PCLKC1_4/MPI_PAR3
H22	PT63C	1	D24/PCLKT1_4/MPI_DATA24	PT71C	1	D24/PCLKT1_4/MPI_DATA24
A23	PT63B	1	MPI_RETRY	PT71B	1	MPI_RETRY
A22	PT63A	1	A0/MPI_ADDR14	PT71A	1	A0/MPI_ADDR14
L22	PT61D	1	A1/MPI_ADDR15	PT69D	1	A1/MPI_ADDR15
M22	PT61C	1	A2/MPI_ADDR16	PT69C	1	A2/MPI_ADDR16

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FF1152C	-6	Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FF1152C	-5	Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FF1704C	-6	Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FF1704C	-5	Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Date	Version	Section	Change Summary
March 2007 (cont.)	01.5 (cont.)	DC and Switching Characteristics (cont.)	Updated LatticeSC Internal Timing Parameters with ispLEVER 6.1 SP1 results.
			Updated t_{FDEL} and t_{CDEL} specifications.
			Updated LatticeSC Family Timing Adders with ispLEVER 6.1 SP1 results.
			Updated PLL specifications to expand frequency range down to 2 MHz and break out jitter for the different ranges.
			Added footnote to sysCLOCK PLL Timing table specifying the conditions for the jitter measurements.
			Added t_{DLL} specification to sysCLOCK DLL Timing table.
			Added footnote to sysCLOCK DLL Timing table specifying the conditions for the jitter measurements.
			Added sysCONFIG Master Parallel Configuration Mode and sysCONFIG SPI Port to LatticeSC sysCONFIG Port Timing table.
		Pin Information	Updated Pin Information Summary with SC40 information.
			Updated LFSC25 Logic Signal Connections: FF1020 with SC40 information.
Updated LFSC80 Logic Signal Connections: FC1152 with SC40 information.			
August 2007	01.6	General	Changed references of "HDC" to "HDC/SI".
			Changed references of "LDCN" to "LDCN/SCS".
			Changed references of "BUSYN/RCLK" to "BUSYN/RCLK/SCK".
			Changed references of "RDCFGN" to "TSALLN".
			Changed references of "TDO/RDDATA" to "TDO".
		Architecture	Updated text in Ripple Mode section.
			Added information to Global Set/Reset.
			Added information for Spread Spectrum Clocking
			Modified information for PLL/DLL Cascading. DLL to PLL is now supported.
			Modified AIL Block text and figure.
			Modified Figure 2-20 DDR/Shift Register Block.
			Added Information to Hot Socketing.
			Added new information for I/O Architecture Rules.
			Added information to SERDES Power Supply Sequencing Requirements.
		DC and Switching Characteristics	Added footnote to Hot Socketing Specifications table.
			Modified Initialization and Standby Supply Current table.
			Modified GSR Timing table.
			Modified sysCLOCK DLL Timing table to include I_{DUTY} .
			Deleted Readback Timing information from sysCONFIG Port Timing table.
			Modified data in External Switching Characteristics table.
		Pin Information	Added information to the Signal Descriptions table for HDC/SI, LDCN/SCS.
			Added footnote to Signal Descriptions table.
			Modified Description for signal BUSYN/RCLK/SCK.
			Modified data in Pin Information Summary and device-specific Pinout Information tables.