Lattice Semiconductor Corporation - LFSCM3GA40EP1-6FFN1152C Datasheet

Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	604
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga40ep1-6ffn1152c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

Logic Mode

In this mode, the LUTs in each Slice are configured as combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices in the PFU.

Ripple Mode

Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Up counter 2-bit
- Down counter 2-bit
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the Slice. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information on RAM mode, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

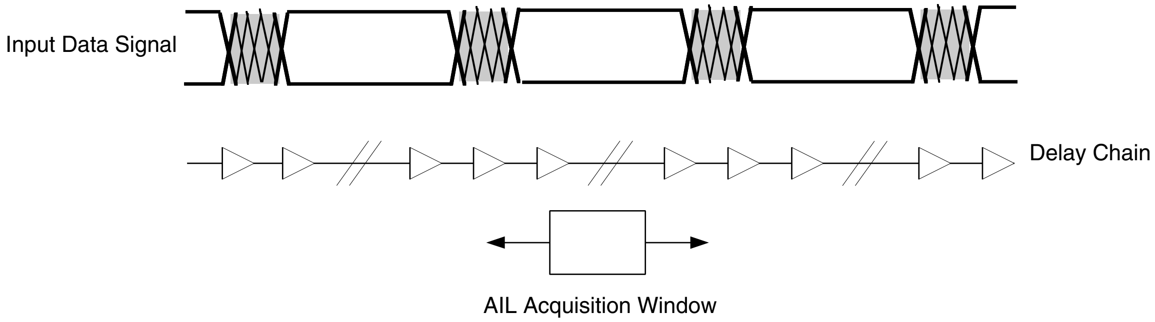
ROM Mode

The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accom-

Adaptive Input Logic (AIL) Overview

The Adaptive Input Logic (AIL) provides the ability of the input logic to dynamically find a solution by monitoring multiple samples of the input data. The input data signal from the input buffer is run through a delay chain. Data, transitions, jitter, noise are all contained inside of the delay chain. The AIL will then search the delay chain for a clean sampling point for data. Once found the AIL will monitor and walk with the data dynamically. This novel approach of using a delay chain to create multiple copies of the data provides a lower power solution than oversampling data with a higher speed clock. Figure 2-19 provides a high level view of the AIL methodology.

Figure 2-19. LatticeSC AIL Delay of Input Data Waveform



The AIL slides the acquisition window through the delay chain searching for stable data based solely on data transitions. A specific training pattern is not required to perform this bit alignment, simply data transitions. The size of the acquisition window is user-selectable allowing the AIL to operate over the full range of the PURESPEED I/O range. Based on dynamic user control the AIL can either continuously adjust the window location based on data edge detection or it can be locked to a specific delay.

The AIL operates on single data and double data rate interfaces and is available on most FPGA input pins on the LatticeSC device and all buffer types. The AIL block is low power using only 0.003 mW/MHz typical (6 mW @ 2 Gbps) for PRBS 2^7 data. Multiple AIL inputs can be used to create a bus with a FPGA circuit to realign the bus to a common clock cycle. The FPGA circuit to realign the bus is required and is provided by Lattice as a reference design.

For more information on the LatticeSC AIL please refer to TN1158 LatticeSC PURESPEED I/O Adaptive Input Logic User's Guide.

Input DDR/Shift Block

The DDR/Shift block contains registers and associated logic that support DDR and shift register functions using the high-speed clock and the associated transfer to the low-speed clock domain. It functions as a gearbox allowing high-speed incoming data to be passed into the FPGA fabric. Each PIO supports DDR and x2 shift functions. If desired PIOs A and B or C and D can be combined to form x4 shift functions. The PIOs A and C on the left, right and bottom of the device also contain an optional Adaptive Input Logic (AIL) element. This logic automatically aligns incoming data with the clock allowing for easy design of high-speed interfaces. Figure 2-21 shows a simplified block diagram of the shift register block. The shift block in conjunction with the update and clock divider blocks automatically handles the hand off between the low-speed and high-speed clock domains.

BLVDS

The LatticeSC devices support BLVDS standard. This standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

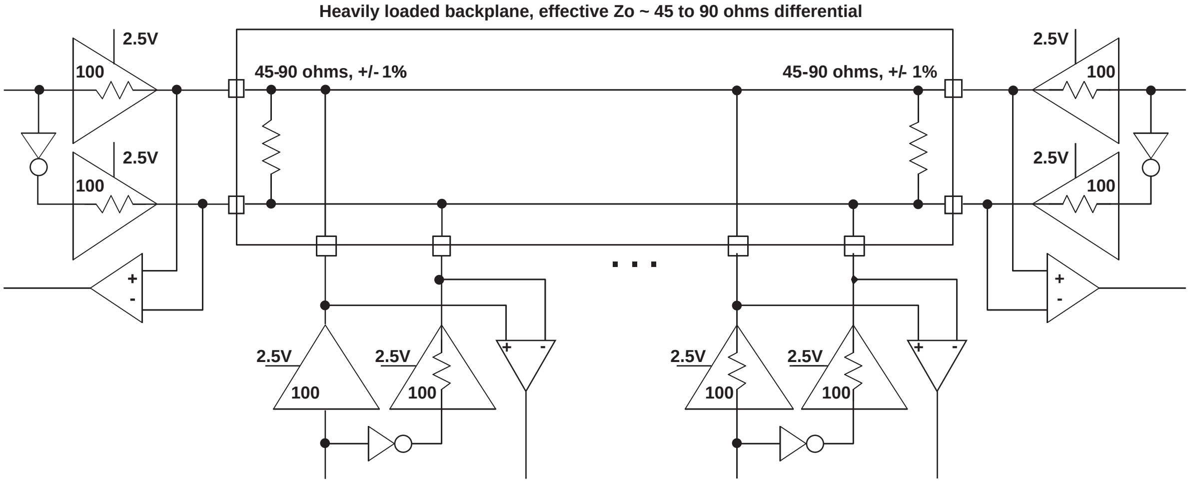


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	100	100	ohm
R_{TLEFT}	Left end termination	45	90	ohm
R_{TRIGHT}	Right end termination	45	90	ohm
V_{OH}	Output high voltage	1.375	1.48	V
V_{OL}	Output low voltage	1.125	1.02	V
V_{OD}	Output differential voltage	0.25	0.46	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-6FF1020I[1]	-6	Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-5FF1020I[1]	-5	Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-6FFA1020I	-6	Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-5FFA1020I	-5	Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-6FC1152I[2]	-6	Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FC1152I[2]	-5	Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-6FF1152I	-6	Organic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FF1152I	-5	Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-6FC1152I[1]	-6	Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-5FC1152I[1]	-5	Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-6FF1152I	-6	Organic fcBGA	1152	IND	80.1
LFSC3GA80E-5FF1152I	-5	Organic fcBGA	1152	IND	80.1
LFSC3GA80E-6FC1704I[1]	-6	Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-5FC1704I[1]	-5	Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-6FF1704I	-6	Organic fcBGA	1704	IND	80.1
LFSC3GA80E-5FF1704I	-5	Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-6FC1152I[1]	-6	Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FC1152I[1]	-5	Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FF1152I	-6	Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FF1152I	-5	Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FC1704I[1]	-6	Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FC1704I[1]	-5	Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-6FF1704I	-6	Organic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FF1704I	-5	Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per PCN #01A-10.