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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	604
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga40ep1-6ffn1152i

Table 1-1. LatticeSC Family Selection Guide¹

Device	SC15	SC25	SC40	SC80	SC115
LUT4s (K)	15	25	40	80	115
sysMEM Blocks (18Kb)	56	104	216	308	424
Embedded Memory (Mbits)	1.03	1.92	3.98	5.68	7.8
Max. Distributed Memory (Mbits)	0.24	0.41	0.65	1.28	1.84
Number of 3.8Gbps SERDES (Max.)	8	16	16	32	32
DLLs	12	12	12	12	12
Analog PLLs	8	8	8	8	8
MACO Blocks	4	6	10	10	12
Package I/O/SERDES Combinations (1mm ball pitch)					
256-ball fpBGA (17 x 17mm)	139/4				
900-ball fpBGA (31 x 31mm)	300/8	378/8			
1020-ball fcBGA (33 x 33mm) ²		476/16	562/16		
1152-ball fcBGA (35 x 35mm) ³			604/16	660/16	660/16
1704-ball fcBGA (42.5 x 42.5mm) ³				904/32	942/32

1. The information in this preliminary data sheet is by definition not final and subject to change. Please consult the Lattice web site and your local Lattice sales office to ensure you have the latest information regarding the specifications for these products as you make critical design decisions.
2. Organic fcBGA converted to organic fcBGA revision 2 per [PCN #02A-10](#).
3. Ceramic fcBGA converted to organic fcBGA per [PCN #01A-10](#).

The LatticeSCM devices add MACO-enabled IP functionality to the base LatticeSC devices. Table 1-2 shows the type and number of each pre-engineered IP core.

Table 1-2. LatticeSCM Family

Device	SCM15	SCM25	SCM40	SCM80	SCM115
flexiMAC Blocks • 1GbE Mode • 10GbE Mode • PCI Express Mode	1	2	2	2	4
SPI4.2 Blocks	1	2	2	2	2
Memory Controller Blocks • DDR/DDR2 DRAM Mode • QDR II/II+ SRAM Mode • RLDRAM I • RLDRAM II CIO/SIO	1	2	2	2	2
Low-Speed CDR Blocks	0	0	2	2	2
PCI Express LTSSM (PHY) Blocks	1	0	2	2	2

Note: See each IP core user's guide for more information about support for specific LatticeSCM devices.

Introduction

The LatticeSC family of FPGAs combines a high-performance FPGA fabric, high-speed SERDES, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated in a state of the art technology to provide one of the highest performing FPGAs in the industry.

This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding sub-layer), up to 7.8 Mbits of sysMEM embedded block RAM, dedicated logic to support system level standards such as RAPIDIO, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. The devices in this family feature clock multiply, divide and phase shift PLLs, numerous

Differential Input Termination

The LatticeSC device allows two types of differential termination. The first is a single resistor across the differential inputs. The second is a center-tapped system where each input is terminated to the on-chip termination bus V_{CMT} . The V_{CMT} bus is DC-coupled through an internal capacitor to ground.

Figure 2-29 shows the differential termination schemes and Table 2-9 shows the nominal values of the termination resistors.

Figure 2-29. Differential Termination Scheme

Termination Type	Discrete Off-Chip Solution	Lattice On-Chip Solution
Differential termination		
Differential and common mode termination		

Calibration

There are two calibration sources that are associated with the termination scheme used in the LatticeSC devices:

- DIFFR – This pin occurs in each bank that supports differential drivers and must be connected through a 1K+/-1% resistor to ground if differential outputs are used. Note that differential drivers are not supported in banks 1, 4 and 5.
- XRES – There is one of these pins per device. It is used for several functions including calibrating on-chip termination. This pin should always be connected through a 1K+/-1% resistor to ground.

The LatticeSC devices support two modes of calibration:

- Continuous – In this mode the SC devices continually calibrate the termination resistances. Calibration happens several times a second. Using this mode ensures that termination resistances remain calibrated as the silicon junction temperature changes.
- User Request – In this mode the calibration circuit operates continuously. However, the termination resistor values are only updated on the assertion of the calibration_update signal available to the core logic.

For more information on calibration, refer to the details of additional technical documentation at the end of this data sheet.

Hot Socketing

The LatticeSC devices have been carefully designed to ensure predictable behavior during power-up and power-down. To ensure proper power sequencing, care must be taken during power-up and power-down as described below. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits,

Internal Logic Analyzer Capability (ispTRACY)

All LatticeSC devices support an internal logic analyzer diagnostic feature. The diagnostic features provide capabilities similar to an external logic analyzer, such as programmable event and trigger condition and deep trace memory. This feature is enabled by Lattice's ispTRACY. The ispTRACY utility is added into the user design at compile time. For additional detail refer to technical information at the end of the data sheet.

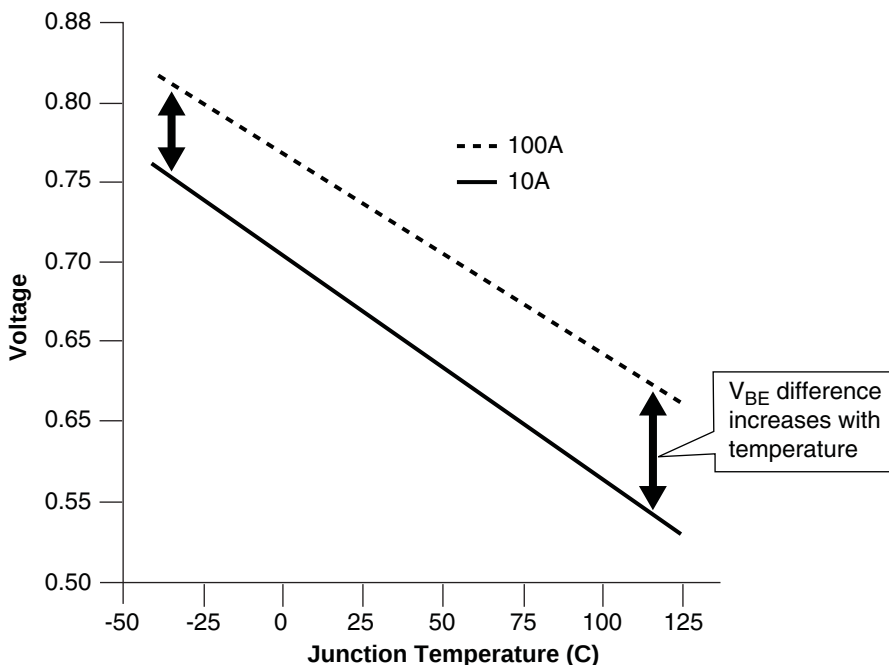
Temperature Sensing

Lattice provides a way to monitor the die temperature by using a temperature-sensing diode that is designed into every LatticeSC device. The difference in V_{BE} of the diode at two different forward currents varies with temperature. This relationship is shown in Figure 2-33. The accuracy of the temperature-sensing diode is typically $\pm 10^{\circ}\text{C}$.

On packages that include PROBE_GND, the most accurate measurements will occur between the TEMP pin and the PROBE_GND pin. On packages that do not include PROBE_GND, measurements should be made between the TEMP pin and board ground.

This temperature-sensing diode is designed to work with an external temperature sensor such as the Maxim 1617A. The Maxim 1617A is configured to measure difference in V_{BE} (of the temperature-sensing diode) at $10\mu\text{A}$ and at $100\mu\text{A}$. This difference in V_{BE} voltage varies with temperature at approximately $1.64\text{ mV}/^{\circ}\text{C}$. A typical device with a 85°C junction temperature will measure approximately 593mV . For additional detail refer to TN1115, [Temperature Sensing Diode in LatticeSC Devices](#).

Figure 2-33. Sensing Diode Typical Characteristics



Oscillator

Every LatticeSC device has an internal CMOS oscillator, which is used as a master serial clock for configuration and is also available as a potential general purpose clock (MCK) for the FPGA core. There is a K divider (divide by 2/4/8/16/32/64/128) available with this oscillator to get lower MCK frequencies. This clock is available as a general purpose clock signal to the software routing tool. For additional detail refer to technical information at the end of the data sheet.

LatticeSC/M Family Timing Adders (Continued)

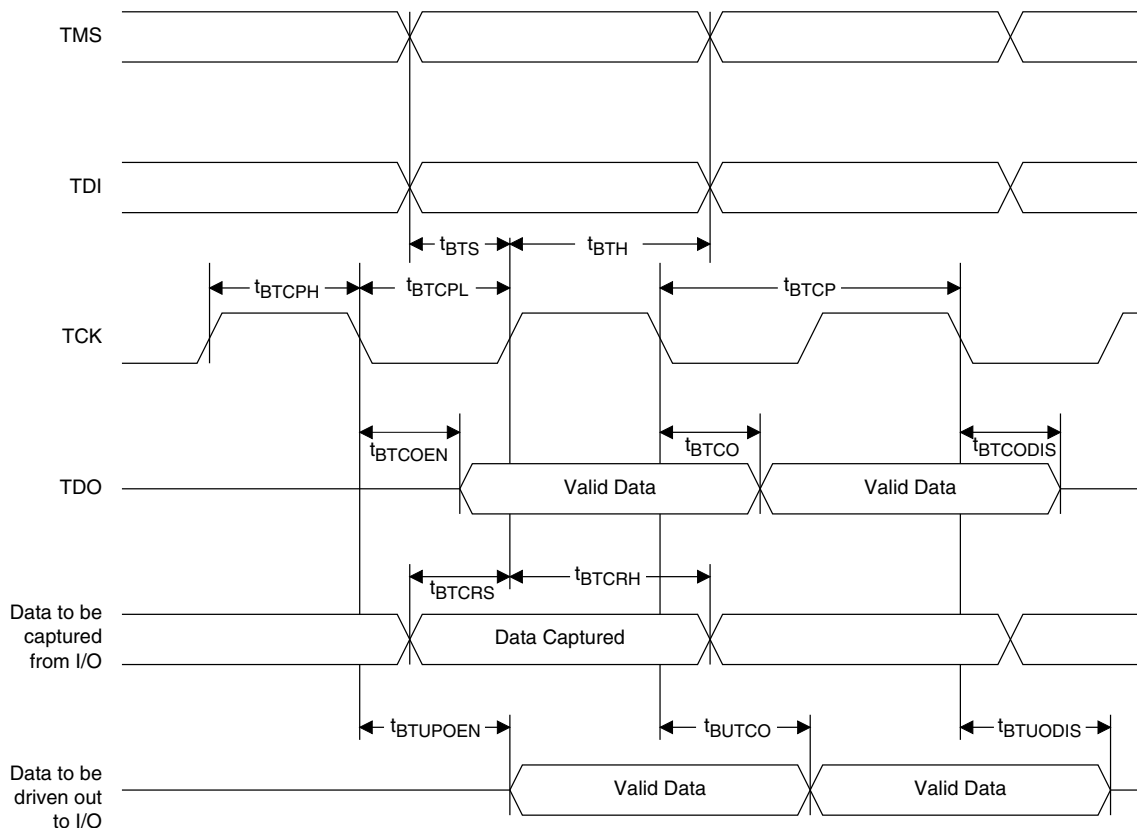
Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVC MOS18_12mA	LVC MOS 1.8 12mA drive	0.024	-0.106	0.019	-0.004	0.016	0.099	ns
LVC MOS18_16mA	LVC MOS 1.8 16mA drive	0.074	-0.134	0.08	-0.022	0.088	0.089	ns
LVC MOS18_OD	LVC MOS 1.8 open drain	0.002	-0.206	0	-0.196	-0.002	-0.221	ns
LVC MOS15_4mA	LVC MOS 1.5 4mA drive	-0.344	-0.164	-0.379	-0.186	-0.412	-0.209	ns
LVC MOS15_8mA	LVC MOS 1.5 8mA drive	-0.125	-0.137	-0.145	-0.157	-0.164	-0.176	ns
LVC MOS15_12mA	LVC MOS 1.5 12mA drive	-0.027	-0.166	-0.043	-0.07	-0.059	0.026	ns
LVC MOS15_16mA	LVC MOS 1.5 16mA drive	0.025	-0.195	0.013	-0.089	0.003	0.017	ns
LVC MOS15_OD	LVC MOS 1.5 open drain	-0.047	-0.267	-0.067	-0.267	-0.087	-0.299	ns
LVC MOS12_2mA	LVC MOS 1.2 2mA drive	-0.473	-0.293	-0.505	-0.317	-0.537	-0.34	ns
LVC MOS12_4mA	LVC MOS 1.2 4mA drive	-0.218	-0.239	-0.25	-0.271	-0.28	-0.303	ns
LVC MOS12_8mA	LVC MOS 1.2 8mA drive	-0.109	-0.269	-0.143	-0.181	-0.176	-0.093	ns
LVC MOS12_12mA	LVC MOS 1.2 12mA drive	-0.054	-0.3	-0.085	-0.203	-0.114	-0.106	ns
LVC MOS12_OD	LVC MOS 1.2 open drain	-0.126	-0.371	-0.166	-0.398	-0.204	-0.43	ns
PCI33	PCI	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX33	PCI-X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX15	PCI-X 1.5	0.208	0.227	0.233	0.312	0.259	0.398	ns
AGP1X33	AGP-1X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
AGP2X33	AGP-2X	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns

JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}		—	25	MHz
t_{BTCP}	TCK [BSCAN] Clock Pulse Width	40	—	ns
t_{BTCPH}	TCK [BSCAN] Clock Pulse Width High	20	—	ns
t_{BTCPL}	TCK [BSCAN] Clock Pulse Width Low	20	—	ns
t_{BTS}	TCK [BSCAN] Setup Time	8	—	ns
t_{BTH}	TCK [BSCAN] Hold Time	10	—	ns
t_{BTRF}	TCK [BSCAN] Rise/Fall Time	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
t_{BTCODIS}	TAP Controller Falling Edge of Clock to Valid Disable	—	10	ns
t_{BTCOEN}	TAP Controller Falling Edge of Clock to Valid Enable	—	10	ns
t_{BTCRS}	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCRH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BUTCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
t_{BTUODIS}	BSCAN Test Update Register, Falling Edge of Clock to Valid Disable	—	25	ns
t_{BTUPOEN}	BSCAN Test Update Register, Falling Edge of Clock to Valid Enable	—	25	ns

Figure 3-14. JTAG Port Timing Waveforms

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AF4	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AE5	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AG3	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AH2	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AD6	PB4C	5		PB4C	5	
AJ2	PB5A	5		PB5A	5	
AK2	PB5B	5		PB5B	5	
AD7	PB5C	5		PB5C	5	
AD8	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AH3	PB7A	5		PB11A	5	
AJ3	PB7B	5		PB11B	5	
AF9	PB7C	5		PB11C	5	
AE10	PB7D	5		PB11D	5	
AK3	PB8A	5		PB12A	5	
AJ4	PB8B	5		PB12B	5	
AE11	PB9A	5		PB13A	5	
AF10	PB9B	5		PB13B	5	
AK4	PB11A	5		PB16A	5	
AK5	PB11B	5		PB16B	5	
AH10	PB12A	5	PCLKT5_3	PB20A	5	PCLKT5_3
AH11	PB12B	5	PCLKC5_3	PB20B	5	PCLKC5_3
AF13	PB12C	5	PCLKT5_4	PB20C	5	PCLKT5_4
AE14	PB12D	5	PCLKC5_4	PB20D	5	PCLKC5_4
AK6	PB13A	5	PCLKT5_5	PB21A	5	PCLKT5_5
AK7	PB13B	5	PCLKC5_5	PB21B	5	PCLKC5_5
AF14	PB13C	5		PB21C	5	
AJ11	PB15A	5	PCLKT5_0	PB23A	5	PCLKT5_0
AJ12	PB15B	5	PCLKC5_0	PB23B	5	PCLKC5_0
AH13	PB15D	5	VREF2_5	PB23D	5	VREF2_5
AK8	PB16A	5	PCLKT5_1	PB24A	5	PCLKT5_1
AK9	PB16B	5	PCLKC5_1	PB24B	5	PCLKC5_1
AH14	PB17A	5	PCLKT5_2	PB25A	5	PCLKT5_2
AG14	PB17B	5	PCLKC5_2	PB25B	5	PCLKC5_2
AK10	PB19A	5		PB28A	5	
AK11	PB19B	5		PB28B	5	
AH15	PB20A	5		PB29A	5	
AG15	PB20B	5		PB29B	5	
AH12	PB21A	5		PB31A	5	
AJ13	PB21B	5		PB31B	5	
AD15	PB21C	5		PB31C	5	
AE15	PB21D	5		PB31D	5	
AK12	PB23A	5		PB32A	5	
AK13	PB23B	5		PB32B	5	
AJ14	PB24A	5		PB33A	5	
AJ15	PB24B	5		PB33B	5	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F19	PT37D	1	WRN/MPI_WR_N	PT46D	1	WRN/MPI_WR_N
F18	PT37C	1	D7/MPI_DATA7	PT46C	1	D7/MPI_DATA7
C18	PT37B	1	D6/MPI_DATA6	PT46B	1	D6/MPI_DATA6
C17	PT37A	1	D5/MPI_DATA5	PT46A	1	D5/MPI_DATA5
E17	PT36D	1	D4/MPI_DATA4	PT45D	1	D4/MPI_DATA4
E16	PT36C	1	D3/MPI_DATA3	PT45C	1	D3/MPI_DATA3
G18	PT35B	1	D2/MPI_DATA2	PT45B	1	D2/MPI_DATA2
G17	PT35A	1	D1/MPI_DATA1	PT45A	1	D1/MPI_DATA1
B18	PT33B	1	D0/MPI_DATA0	PT43B	1	D0/MPI_DATA0
B17	PT33A	1	QOUT/CEON	PT43A	1	QOUT/CEON
G16	PT32D	1	VREF2_1	PT42D	1	VREF2_1
A18	PT32B	1	DOUT	PT42B	1	DOUT
A17	PT32A	1	MCA_DONE_IN	PT42A	1	MCA_DONE_IN
H18	PT31B	1	MCA_CLK_P1_OUT	PT41B	1	MCA_CLK_P1_OUT
H17	PT31A	1	MCA_CLK_P1_IN	PT41A	1	MCA_CLK_P1_IN
D17	PT29B	1	MCA_CLK_P2_OUT	PT39B	1	MCA_CLK_P2_OUT
D16	PT29A	1	MCA_CLK_P2_IN	PT39A	1	MCA_CLK_P2_IN
F17	PT28D	1	MCA_DONE_OUT	PT38D	1	MCA_DONE_OUT
F16	PT28C	1	BUSYN/RCLK/SCK	PT38C	1	BUSYN/RCLK/SCK
C16	PT28B	1	DP0/MPI_PAR0	PT38B	1	DP0/MPI_PAR0
C15	PT28A	1	MPI_TA	PT38A	1	MPI_TA
B16	PT27B	1	PCLKC1_0	PT37B	1	PCLKC1_0
B15	PT27A	1	PCLKT1_0/MPI_CLK	PT37A	1	PCLKT1_0/MPI_CLK
H16	PT25D	1	DP3/PCLKC1_4/MPI_PAR3	PT35D	1	DP3/PCLKC1_4/MPI_PAR3
A16	PT25B	1	MPI_RETRY	PT35B	1	MPI_RETRY
A15	PT25A	1	A0/MPI_ADDR14	PT35A	1	A0/MPI_ADDR14
G15	PT24D	1	A1/MPI_ADDR15	PT33D	1	A1/MPI_ADDR15
F15	PT24C	1	A2/MPI_ADDR16	PT33C	1	A2/MPI_ADDR16
E15	PT24B	1	A3/MPI_ADDR17	PT33B	1	A3/MPI_ADDR17
D15	PT24A	1	A4/MPI_ADDR18	PT33A	1	A4/MPI_ADDR18
C14	PT23B	1	A5/MPI_ADDR19	PT32B	1	A5/MPI_ADDR19
C13	PT23A	1	A6/MPI_ADDR20	PT32A	1	A6/MPI_ADDR20
H14	PT21C	1	VREF1_1	PT31C	1	VREF1_1
B14	PT21B	1	A7/MPI_ADDR21	PT31B	1	A7/MPI_ADDR21
B13	PT21A	1	A8/MPI_ADDR22	PT31A	1	A8/MPI_ADDR22
G14	PT20B	1	A9/MPI_ADDR23	PT29B	1	A9/MPI_ADDR23
F14	PT20A	1	A10/MPI_ADDR24	PT29A	1	A10/MPI_ADDR24
A14	PT19B	1	A11/MPI_ADDR25	PT28B	1	A11/MPI_ADDR25
A13	PT19A	1	A12/MPI_ADDR26	PT28A	1	A12/MPI_ADDR26
G13	PT17D	1	D11/MPI_DATA11	PT27D	1	D11/MPI_DATA11
H13	PT17C	1	D12/MPI_DATA12	PT27C	1	D12/MPI_DATA12
E14	PT17B	1	A13/MPI_ADDR27	PT27B	1	A13/MPI_ADDR27
E13	PT17A	1	A14/MPI_ADDR28	PT27A	1	A14/MPI_ADDR28
G12	PT15D	1	A16/MPI_ADDR30	PT25D	1	A16/MPI_ADDR30
G11	PT15C	1	D13/MPI_DATA13	PT25C	1	D13/MPI_DATA13

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
E16	PT45C	1	D3/MPI_DATA3	PT54C	1	D3/MPI_DATA3
C13	PT45B	1	D2/MPI_DATA2	PT53B	1	D2/MPI_DATA2
C14	PT45A	1	D1/MPI_DATA1	PT53A	1	D1/MPI_DATA1
B14	PT43B	1	D0/MPI_DATA0	PT51B	1	D0/MPI_DATA0
B13	PT43A	1	QOUT/CEON	PT51A	1	QOUT/CEON
L13	PT42D	1	VREF2_1	PT50D	1	VREF2_1
C15	PT42B	1	DOUT	PT50B	1	DOUT
D15	PT42A	1	MCA_DONE_IN	PT50A	1	MCA_DONE_IN
J16	PT41B	1	MCA_CLK_P1_OUT	PT49B	1	MCA_CLK_P1_OUT
K16	PT41A	1	MCA_CLK_P1_IN	PT49A	1	MCA_CLK_P1_IN
H15	PT39D	1	D21/PCLKC1_1/MPI_DATA21	PT47D	1	D21/PCLKC1_1/MPI_DATA21
H16	PT39C	1	D22/PCLKT1_1/MPI_DATA22	PT47C	1	D22/PCLKT1_1/MPI_DATA22
A14	PT39B	1	MCA_CLK_P2_OUT	PT47B	1	MCA_CLK_P2_OUT
A13	PT39A	1	MCA_CLK_P2_IN	PT47A	1	MCA_CLK_P2_IN
G16	PT38D	1	MCA_DONE_OUT	PT46D	1	MCA_DONE_OUT
F16	PT38C	1	BUSYN/RCLK/SCK	PT46C	1	BUSYN/RCLK/SCK
B16	PT38B	1	DP0/MPI_PAR0	PT46B	1	DP0/MPI_PAR0
B15	PT38A	1	MPI_TA	PT46A	1	MPI_TA
L16	PT37C	1	DP2/MPI_PAR2	PT45C	1	DP2/MPI_PAR2
A16	PT37B	1	PCLKC1_0	PT45B	1	PCLKC1_0
A15	PT37A	1	PCLKT1_0/MPI_CLK	PT45A	1	PCLKT1_0/MPI_CLK
L17	PT35C	1	D24/PCLKT1_4/MPI_DATA24	PT43C	1	D24/PCLKT1_4/MPI_DATA24
A17	PT35B	1	MPI_RETRY	PT43B	1	MPI_RETRY
A18	PT35A	1	A0/MPI_ADDR14	PT43A	1	A0/MPI_ADDR14
F17	PT33D	1	A1/MPI_ADDR15	PT42D	1	A1/MPI_ADDR15
G17	PT33C	1	A2/MPI_ADDR16	PT42C	1	A2/MPI_ADDR16
B17	PT33B	1	A3/MPI_ADDR17	PT42B	1	A3/MPI_ADDR17
B18	PT33A	1	A4/MPI_ADDR18	PT42A	1	A4/MPI_ADDR18
H17	PT32D	1	D25/PCLKC1_5/MPI_DATA25	PT41D	1	D25/PCLKC1_5/MPI_DATA25
H18	PT32C	1	D26/PCLKT1_5/MPI_DATA26	PT41C	1	D26/PCLKT1_5/MPI_DATA26
A19	PT32B	1	A5/MPI_ADDR19	PT41B	1	A5/MPI_ADDR19
A20	PT32A	1	A6/MPI_ADDR20	PT41A	1	A6/MPI_ADDR20
L20	PT31C	1	VREF1_1	PT39C	1	VREF1_1
J17	PT31B	1	A7/MPI_ADDR21	PT39B	1	A7/MPI_ADDR21
K17	PT31A	1	A8/MPI_ADDR22	PT39A	1	A8/MPI_ADDR22
C18	PT29B	1	A9/MPI_ADDR23	PT38B	1	A9/MPI_ADDR23
D18	PT29A	1	A10/MPI_ADDR24	PT38A	1	A10/MPI_ADDR24
B19	PT28B	1	A11/MPI_ADDR25	PT37B	1	A11/MPI_ADDR25
B20	PT28A	1	A12/MPI_ADDR26	PT37A	1	A12/MPI_ADDR26
E17	PT27D	1	D11/MPI_DATA11	PT35D	1	D11/MPI_DATA11
E18	PT27C	1	D12/MPI_DATA12	PT35C	1	D12/MPI_DATA12
C20	PT27B	1	A13/MPI_ADDR27	PT35B	1	A13/MPI_ADDR27
C19	PT27A	1	A14/MPI_ADDR28	PT35A	1	A14/MPI_ADDR28
H19	PT25D	1	A16/MPI_ADDR30	PT33D	1	A16/MPI_ADDR30
G19	PT25C	1	D13/MPI_DATA13	PT33C	1	D13/MPI_DATA13
D20	PT25B	1	A15/MPI_ADDR29	PT33B	1	A15/MPI_ADDR29
D19	PT25A	1	A17/MPI_ADDR31	PT33A	1	A17/MPI_ADDR31
H20	PT24D	1	A19/MPI_TSI21	PT30D	1	A19/MPI_TSI21
G20	PT24C	1	A20/MPI_BDIP	PT30C	1	A20/MPI_BDIP
E19	PT24B	1	A18/MPI_TSI20	PT30B	1	A18/MPI_TSI20

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P10	GND	-		GND	-	
P13	GND	-		GND	-	
P15	GND	-		GND	-	
P18	GND	-		GND	-	
P20	GND	-		GND	-	
P24	GND	-		GND	-	
R12	GND	-		GND	-	
R14	GND	-		GND	-	
R16	GND	-		GND	-	
R17	GND	-		GND	-	
R19	GND	-		GND	-	
R21	GND	-		GND	-	
R26	GND	-		GND	-	
R6	GND	-		GND	-	
T15	GND	-		GND	-	
T18	GND	-		GND	-	
T30	GND	-		GND	-	
T4	GND	-		GND	-	
U15	GND	-		GND	-	
U18	GND	-		GND	-	
U29	GND	-		GND	-	
U3	GND	-		GND	-	
V12	GND	-		GND	-	
V14	GND	-		GND	-	
V16	GND	-		GND	-	
V17	GND	-		GND	-	
V19	GND	-		GND	-	
V21	GND	-		GND	-	
V27	GND	-		GND	-	
V7	GND	-		GND	-	
W13	GND	-		GND	-	
W15	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W23	GND	-		GND	-	
W9	GND	-		GND	-	
Y12	GND	-		GND	-	
Y14	GND	-		GND	-	
Y19	GND	-		GND	-	
Y21	GND	-		GND	-	
Y30	GND	-		GND	-	
Y4	GND	-		GND	-	
N13	VCC	-		VCC	-	
N15	VCC	-		VCC	-	
N16	VCC	-		VCC	-	
N17	VCC	-		VCC	-	
N18	VCC	-		VCC	-	
N20	VCC	-		VCC	-	
P14	VCC	-		VCC	-	
P16	VCC	-		VCC	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ9	PB78C	4		PB117C	4	
AJ8	PB78D	4		PB117D	4	
AP3	PB79A	4		PB119A	4	
AN3	PB79B	4		PB119B	4	
AF10	PB79C	4		PB119C	4	
AE10	PB79D	4		PB119D	4	
AL7	PB81A	4		PB121A	4	
AL6	PB81B	4		PB121B	4	
AK7	PB81C	4		PB121C	4	
AK6	PB81D	4		PB121D	4	
AN5	PB82A	4		PB123A	4	
AN4	PB82B	4		PB123B	4	
AH9	PB82C	4	VREF1_4	PB123C	4	VREF1_4
AH8	PB82D	4		PB123D	4	
AM3	PB83A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB124A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AM4	PB83B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB124B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AG9	PB83C	4		PB124C	4	
AG8	PB83D	4		PB124D	4	
AN2	PB85A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB125A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AM2	PB85B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB125B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ6	PB85C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB125C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH6	PB85D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB125D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF7	PROBE_VCC	-		PROBE_VCC	-	
AF8	PROBE_GND	-		PROBE_GND	-	
AG7	PR71D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR95D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AG6	PR71C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR95C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AL4	PR71B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR95B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AL3	PR71A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR95A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD10	PR70D	3		PR94D	3	
AD9	PR70C	3		PR94C	3	
AH4	PR70B	3		PR94B	3	
AJ4	PR70A	3		PR94A	3	
AK5	PR69D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR93D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AJ5	PR69C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR93C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AM1	PR69B	3		PR93B	3	
AL1	PR69A	3		PR93A	3	
AH5	PR67D	3		PR91D	3	
AG5	PR67C	3		PR91C	3	
AL2	PR67B	3		PR91B	3	
AK2	PR67A	3		PR91A	3	
AB9	PR66D	3		PR90D	3	
AC9	PR66C	3		PR90C	3	
AH1	PR66B	3		PR90B	3	
AG1	PR66A	3		PR90A	3	
AE8	PR65D	3	VREF2_3	PR89D	3	VREF2_3

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP20	PB61B	5	
AH21	PB61C	5	
AH20	PB61D	5	
AM20	PB63A	5	
AM19	PB63B	5	
AJ21	PB63C	5	
AJ20	PB63D	5	
AK19	PB66A	5	
AK18	PB66B	5	
AE18	PB66C	5	
AD18	PB66D	5	
AN19	PB69A	5	
AN18	PB69B	5	
AG18	PB69C	5	
AF18	PB69D	5	
AP19	PB71A	5	
AP18	PB71B	5	
AJ18	PB71C	5	
AH18	PB71D	5	
AP17	PB73A	4	
AP16	PB73B	4	
AJ17	PB73C	4	
AH17	PB73D	4	
AN17	PB75A	4	
AN16	PB75B	4	
AE17	PB75C	4	
AD17	PB75D	4	
AK17	PB78A	4	
AK16	PB78B	4	
AG17	PB78C	4	
AF17	PB78D	4	
AM16	PB81A	4	
AM15	PB81B	4	
AJ15	PB81C	4	
AJ14	PB81D	4	
AL16	PB83A	4	
AL15	PB83B	4	
AG16	PB83C	4	
AF16	PB83D	4	
AP15	PB86A	4	
AP14	PB86B	4	
AH15	PB86C	4	
AH14	PB86D	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AD5	PR94C	3	
AE2	PR94B	3	
AD2	PR94A	3	
AC5	PR92D	3	
AB5	PR92C	3	
AF1	PR92B	3	
AE1	PR92A	3	
AA11	PR91D	3	
Y11	PR91C	3	
AC4	PR91B	3	
AB4	PR91A	3	
AA8	PR90D	3	DIFFR_3
AA9	PR90C	3	
AC3	PR90B	3	
AB3	PR90A	3	
AA7	PR79D	3	
Y7	PR79C	3	
AA2	PR79B	3	
Y2	PR79A	3	
AA6	PR77D	3	
Y6	PR77C	3	
Y4	PR77B	3	
W4	PR77A	3	
W11	PR74D	3	
V11	PR74C	3	
W2	PR74B	3	
V2	PR74A	3	
W9	PR71D	3	
V9	PR71C	3	
V1	PR71B	3	
U1	PR71A	3	
W10	PR70D	3	
V10	PR70C	3	
U2	PR70B	3	
T2	PR70A	3	
Y8	PR69D	3	
W8	PR69C	3	VREF1_3
W5	PR69B	3	
V5	PR69A	3	
V7	PR66D	3	PCLKC3_2
U7	PR66C	3	PCLKT3_2
T1	PR66B	3	
R1	PR66A	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
V8	PR65D	3	PCLKC3_3
U8	PR65C	3	PCLKT3_3
U5	PR65B	3	
T5	PR65A	3	
V6	PR64D	3	PCLKC3_1
U6	PR64C	3	PCLKT3_1
T4	PR64B	3	PCLKC3_0
T3	PR64A	3	PCLKT3_0
U9	PR62D	2	PCLKC2_2
T9	PR62C	2	PCLKT2_2
R2	PR62B	2	PCLKC2_0
P2	PR62A	2	PCLKT2_0
T11	PR61D	2	PCLKC2_3
U11	PR61C	2	PCLKT2_3
R4	PR61B	2	PCLKC2_1
R3	PR61A	2	PCLKT2_1
T8	PR60D	2	
R8	PR60C	2	
P1	PR60B	2	
N1	PR60A	2	
R6	PR57D	2	
P6	PR57C	2	
M1	PR57B	2	
L1	PR57A	2	
T10	PR56D	2	
U10	PR56C	2	
N2	PR56B	2	
M2	PR56A	2	
R11	PR51D	2	
P11	PR51C	2	
N4	PR51B	2	
M4	PR51A	2	
N5	PR49D	2	
M5	PR49C	2	
L2	PR49B	2	
K2	PR49A	2	
P8	PR47D	2	
N8	PR47C	2	
J2	PR47B	2	
H2	PR47A	2	
M6	PR45D	2	
L6	PR45C	2	
K3	PR45B	2	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD33	PL59D	6		PL73D	6	
AA38	PL60A	6		PL74A	6	
AB38	PL60B	6		PL74B	6	
AC29	PL60C	6		PL74C	6	
AD29	PL60D	6		PL74D	6	
AA41	PL61A	6		PL75A	6	
AB41	PL61B	6		PL75B	6	
AC34	PL61C	6		PL75C	6	
AD34	PL61D	6		PL75D	6	
AA42	PL63A	6		PL77A	6	
AB42	PL63B	6		PL77B	6	
AC37	PL63C	6		PL77C	6	
AD37	PL63D	6		PL77D	6	
AC38	PL64A	6		PL78A	6	
AD38	PL64B	6		PL78B	6	
AD36	PL64C	6		PL78C	6	
AE36	PL64D	6		PL78D	6	
AC39	PL65A	6		PL79A	6	
AD39	PL65B	6		PL79B	6	
AD35	PL65C	6		PL79C	6	
AE35	PL65D	6		PL79D	6	
AC40	PL67A	6		PL81A	6	
AD40	PL67B	6		PL81B	6	
AE37	PL67C	6		PL81C	6	
AF37	PL67D	6		PL81D	6	
AC41	PL68A	6		PL82A	6	
AD41	PL68B	6		PL82B	6	
AE34	PL68C	6		PL82C	6	
AF34	PL68D	6		PL82D	6	
AC42	PL69A	6		PL83A	6	
AD42	PL69B	6		PL83B	6	
AE33	PL69C	6		PL83C	6	
AF33	PL69D	6		PL83D	6	
AE38	PL72A	6		PL86A	6	
AF38	PL72B	6		PL86B	6	
AE32	PL72C	6		PL86C	6	
AF32	PL72D	6		PL86D	6	
AE41	PL73A	6		PL87A	6	
AF41	PL73B	6		PL87B	6	
AE31	PL73C	6		PL87C	6	
AF31	PL73D	6		PL87D	6	
AE42	PL74A	6		PL88A	6	
AF42	PL74B	6		PL88B	6	
AG37	PL74C	6		PL88C	6	
AH37	PL74D	6		PL88D	6	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AP41	PL91B	6		PL112B	6	
AK35	PL91C	6		PL112C	6	
AL35	PL91D	6		PL112D	6	
AN38	PL93A	6		PL115A	6	
AP38	PL93B	6		PL115B	6	
AL37	PL93C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL115C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AM37	PL93D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL115D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AR41	PL94A	6		PL116A	6	
AT41	PL94B	6		PL116B	6	
AN37	PL94C	6		PL116C	6	
AP37	PL94D	6		PL116D	6	
AR39	PL95A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL117A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AR40	PL95B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL117B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AN36	PL95C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL117C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AP36	PL95D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL117D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AT40	XRES	-		XRES	-	
AU41	TEMP	6		TEMP	6	
AU42	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AV42	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
AL33	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AL34	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AU38	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AV38	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AM34	PB4C	5		PB4C	5	
AM33	PB4D	5		PB4D	5	
AV41	PB5A	5		PB5A	5	
AW41	PB5B	5		PB5B	5	
AK30	PB5C	5		PB5C	5	
AK29	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AW42	PB7A	5		PB7A	5	
AY42	PB7B	5		PB7B	5	
AR37	PB7C	5		PB7C	5	
AR38	PB7D	5		PB7D	5	
AV40	PB8A	5		PB9A	5	
AV39	PB8B	5		PB9B	5	
AN35	PB8C	5		PB9C	5	
AN34	PB8D	5		PB9D	5	
AW40	PB9A	5		PB11A	5	
AY40	PB9B	5		PB11B	5	
AP34	PB9C	5		PB11C	5	
AP35	PB9D	5		PB11D	5	
AW39	PB11A	5		PB12A	5	
AW38	PB11B	5		PB12B	5	
AL32	PB11C	5		PB12C	5	
AL31	PB11D	5		PB12D	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AV32	PB27B	5		PB29B	5	
AU36	PB27C	5		PB29C	5	
AU37	PB27D	5		PB29D	5	
BA35	PB28A	5		PB30A	5	
BA34	PB28B	5		PB30B	5	
AJ26	PB28C	5		PB30C	5	
AJ27	PB28D	5		PB30D	5	
AW33	PB29A	5		PB31A	5	
AW32	PB29B	5		PB31B	5	
AU35	PB29C	5		PB31C	5	
AU34	PB29D	5		PB31D	5	
BB35	PB31A	5		PB33A	5	
BB34	PB31B	5		PB33B	5	
AN29	PB31C	5		PB33C	5	
AP29	PB31D	5		PB33D	5	
AY33	PB32A	5		PB34A	5	
AY32	PB32B	5		PB34B	5	
AR31	PB32C	5		PB34C	5	
AR30	PB32D	5		PB34D	5	
AV31	PB33A	5		PB35A	5	
AV30	PB33B	5		PB35B	5	
AN28	PB33C	5		PB35C	5	
AP28	PB33D	5		PB35D	5	
BA33	PB35A	5		PB37A	5	
BA32	PB35B	5		PB37B	5	
AT30	PB35C	5		PB37C	5	
AT31	PB35D	5		PB37D	5	
BB33	PB36A	5		PB38A	5	
BB32	PB36B	5		PB38B	5	
AM26	PB36C	5		PB38C	5	
AL26	PB36D	5		PB38D	5	
AW30	PB37A	5		PB39A	5	
AW29	PB37B	5		PB39B	5	
AP27	PB37C	5		PB39C	5	
AN27	PB37D	5		PB39D	5	
BA31	PB39A	5		PB41A	5	
BA30	PB39B	5		PB41B	5	
AU32	PB39C	5		PB41C	5	
AU33	PB39D	5		PB41D	5	
BB31	PB40A	5		PB42A	5	
BB30	PB40B	5		PB42B	5	
AR28	PB40C	5		PB42C	5	
AR27	PB40D	5		PB42D	5	
AV29	PB41A	5		PB43A	5	
AV28	PB41B	5		PB43B	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
J1	PR25B	2		PR38B	2	
K1	PR25A	2		PR38A	2	
V12	PR24D	2		PR34D	2	
U12	PR24C	2		PR34C	2	
K2	PR24B	2		PR34B	2	
J2	PR24A	2		PR34A	2	
R10	PR22D	2		PR30D	2	
T10	PR22C	2		PR30C	2	
L5	PR22B	2		PR30B	2	
K5	PR22A	2		PR30A	2	
P9	PR21D	2		PR26D	2	
N9	PR21C	2		PR26C	2	
L6	PR21B	2		PR26B	2	
K6	PR21A	2		PR26A	2	
M8	PR20D	2		PR19D	2	
M9	PR20C	2		PR19C	2	
H1	PR20B	2		PR19B	2	
G1	PR20A	2		PR19A	2	
U14	PR18D	2	VREF2_2	PR18D	2	VREF2_2
T14	PR18C	2		PR18C	2	
H2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
G2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
H3	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
G3	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
R11	PR16D	2		PR15D	2	
P11	PR16C	2		PR15C	2	
J5	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
J6	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
P18	VCCJ	-		VCCJ	-	
P19	TDO	-	TDO	TDO	-	TDO
R21	TMS	-		TMS	-	
P20	TCK	-		TCK	-	
P12	TDI	-		TDI	-	
P17	PROGRAMN	1		PROGRAMN	1	
P21	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
P13	CCLK	1		CCLK	1	
H10	RESP_URC	-		RESP_URC	-	
N13	VCC12	-		VCC12	-	
H9	A_REFCLKN_R	-		A_REFCLKN_R	-	
G9	A_REFCLKP_R	-		A_REFCLKP_R	-	
F2	VCC12	-		VCC12	-	
H4	A_VDDIB0_R	-		A_VDDIB0_R	-	
C1	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C3	GND	-		GND	-	
C30	GND	-		GND	-	
C33	GND	-		GND	-	
C35	GND	-		GND	-	
C36	GND	-		GND	-	
C39	GND	-		GND	-	
C4	GND	-		GND	-	
C40	GND	-		GND	-	
C7	GND	-		GND	-	
C8	GND	-		GND	-	
D15	GND	-		GND	-	
D21	GND	-		GND	-	
D25	GND	-		GND	-	
D31	GND	-		GND	-	
F4	GND	-		GND	-	
F40	GND	-		GND	-	
G11	GND	-		GND	-	
G17	GND	-		GND	-	
G26	GND	-		GND	-	
G32	GND	-		GND	-	
H14	GND	-		GND	-	
H20	GND	-		GND	-	
H23	GND	-		GND	-	
H29	GND	-		GND	-	
H35	GND	-		GND	-	
H8	GND	-		GND	-	
J3	GND	-		GND	-	
J39	GND	-		GND	-	
L16	GND	-		GND	-	
L27	GND	-		GND	-	
L36	GND	-		GND	-	
L7	GND	-		GND	-	
M19	GND	-		GND	-	
M24	GND	-		GND	-	
M4	GND	-		GND	-	
M40	GND	-		GND	-	
N12	GND	-		GND	-	
N31	GND	-		GND	-	
P35	GND	-		GND	-	
P8	GND	-		GND	-	
R15	GND	-		GND	-	
R28	GND	-		GND	-	
R3	GND	-		GND	-	
R39	GND	-		GND	-	
T11	GND	-		GND	-	

Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Thermal Management document to find the device/package specific thermal values.

For Further Information

For further information regarding Thermal Management, refer to the following located on the Lattice website at www.latticesemi.com.

- Thermal Management document
- Technical Note TN1101 - Power Estimation and Management for LatticeSC Devices
- Power Calculator tool included with Lattice's ispLEVER design tool, or as a standalone download from www.latticesemi.com/software

Lead-Free Packaging**Commercial**

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-7FN256C	-7	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-6FN256C	-6	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-5FN256C	-5	Lead-Free fpBGA	256	COM	15.2
LFSC3GA15E-7FN900C	-7	Lead-Free fpBGA	900	COM	15.2
LFSC3GA15E-6FN900C	-6	Lead-Free fpBGA	900	COM	15.2
LFSC3GA15E-5FN900C	-5	Lead-Free fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-7FN256C	-7	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-6FN256C	-6	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-5FN256C	-5	Lead-Free fpBGA	256	COM	15.2
LFSCM3GA15EP1-7FN900C	-7	Lead-Free fpBGA	900	COM	15.2
LFSCM3GA15EP1-6FN900C	-6	Lead-Free fpBGA	900	COM	15.2
LFSCM3GA15EP1-5FN900C	-5	Lead-Free fpBGA	900	COM	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-7FN900C	-7	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-6FN900C	-6	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-5FN900C	-5	Lead-Free fpBGA	900	COM	25.4
LFSC3GA25E-7FFN1020C ¹	-7	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-6FFN1020C ¹	-6	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-5FFN1020C ¹	-5	Lead-Free Organic fcBGA	1020	COM	25.4
LFSC3GA25E-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSC3GA25E-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-7FN900C	-7	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-6FN900C	-6	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-5FN900C	-5	Lead-Free fpBGA	900	COM	25.4
LFSCM3GA25EP1-7FFN1020C ¹	-7	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-6FFN1020C ¹	-6	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-5FFN1020C ¹	-5	Lead-Free Organic fcBGA	1020	COM	25.4
LFSCM3GA25EP1-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4
LFSCM3GA25EP1-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	25.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).