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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	604
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BCBGA, FCBGA
Supplier Device Package	1152-CFCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga40ep1-7fc1152c

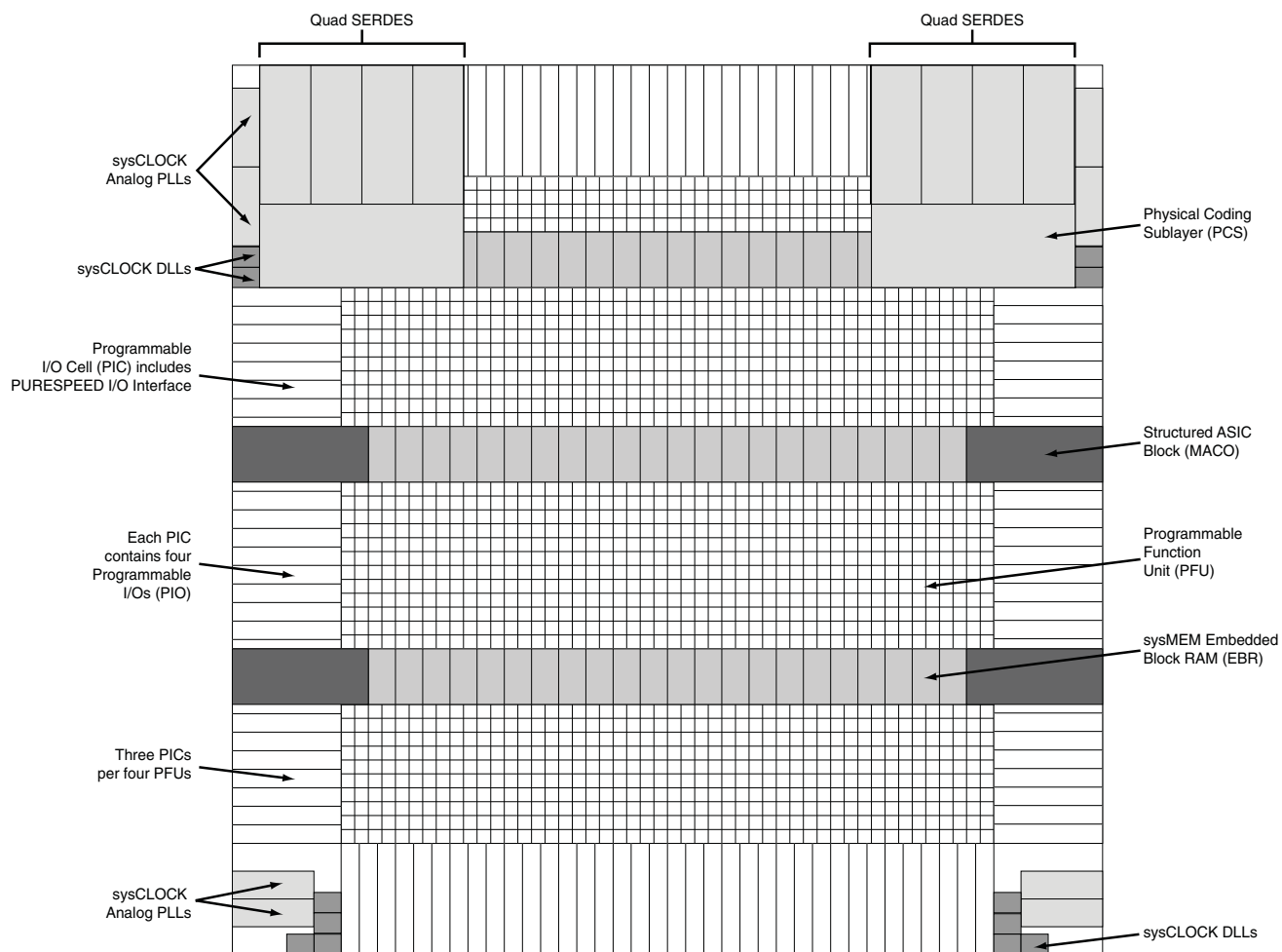
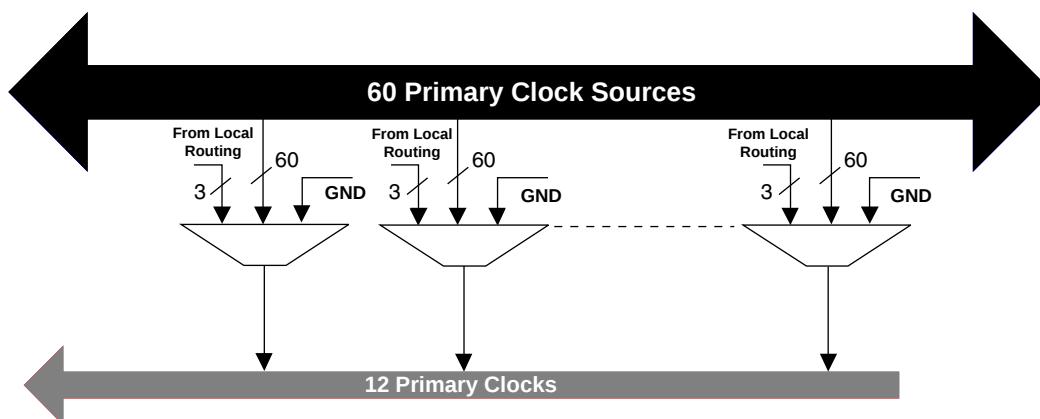
Figure 2-1. Simplified Block Diagram (Top Level)

Figure 2-6. Per Quadrant Clock Selection

Note: GND is available to switch off the network.

Secondary Clocks

In addition to the primary clock network and edge clocks the LatticeSC devices also contain a secondary clock network. Built of X6 style routing elements this secondary clock network is ideal for routing slower speed clock and control signals throughout the device preserving high-speed clock networks for the most timing critical signals.

Edge Clocks

LatticeSC devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are eight edge clocks per bank for the top and bottom of the device. The left and right sides have eight edge clocks per side for both banks located on that side. Figure 2-7 shows the arrangement of edge clocks.

Edge clock resources can be driven from a variety of sources. Edge clock resources can be driven from:

- Edge clock PIOs in the same bank
- Primary clock PIOs in the same bank
- Routing
- Adjacent PLLs and DLLs
- ELSR output from the clock divider

RSDS**Over Recommended Operating Conditions**

Parameter Symbol	Description	Min.	Typ.	Max.	Units
V_{OD}	Output voltage, differential, $R_T = 100$ ohms	100	200	600	mV
V_{OS}	Output voltage, common mode	0.5	1.2	1.5	V
I_{RSDS}	Differential driver output current	1	2	6	mA
V_{THD}	Input voltage differential	100	—	—	mV
V_{CM}	Input common mode voltage	0.3	—	1.5	V
T_R, T_F	Output rise and fall times, 20% to 80%	—	500	—	ps
T_{ODUTY}	Output clock duty cycle	45	50	55	%

Note: Data is for 2mA drive. Other differential driver current options are available.

Input Delay Block/AIL Timing

Parameter	Description	Min.	Typ.	Max.	Units
t_{FDEL}	Fine delay time	35	45	80	ps
t_{CDEL}	Coarse delay time	1120	1440	2560	ps
j_{AIL}	AIL jitter tolerance	$1 - ((N + 1) * t_{FDEL}) / (\text{Clock Period})$			UI

1. N = number of fine delays used in a particular AIL setting

GSR Timing

Parameter	Description	VCC	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{SYNC_GSR_MAX}$	Maximum operating frequency for synchronous GSR	1.14V	—	438	—	417	—	398	MHz
		0.95V	—	378	—	355	—	337	MHz
$t_{ASYNC_GSR_MPW}$	Minimum pulse width of asynchronous input	—	—	—	—	—	3.3	—	ns

Note: Synchronous GSR goes out of reset in two cycles from the clock edge where the setup time of the FF was met.

Internal System Bus Timing

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{HCLK}	Maximum operating frequency for internal system bus HCLK.	—	200	—	200	—	200	MHz

Note: There is no minimum frequency. If HCLK is sourced from the embedded oscillator, the minimum frequency limitation of the oscillator/divider is about 0.3 MHz. Refer to the oscillator data for missing configuration modes.

Figure 3-8. Read Mode with Input and Output Registers

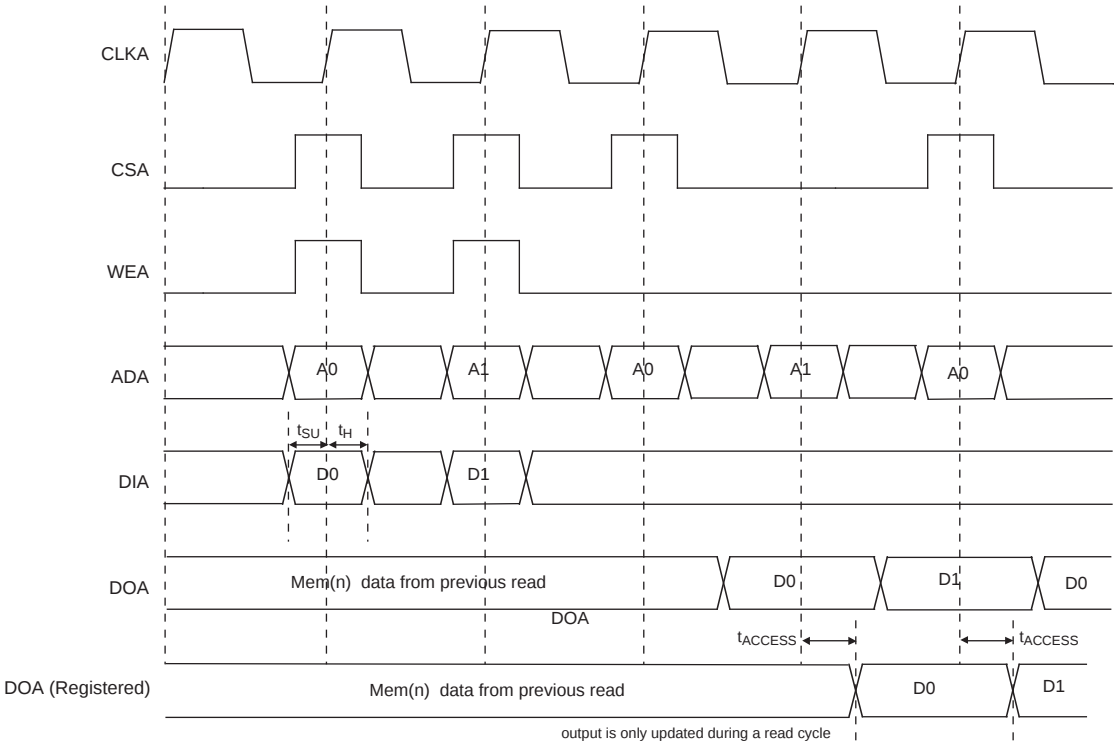
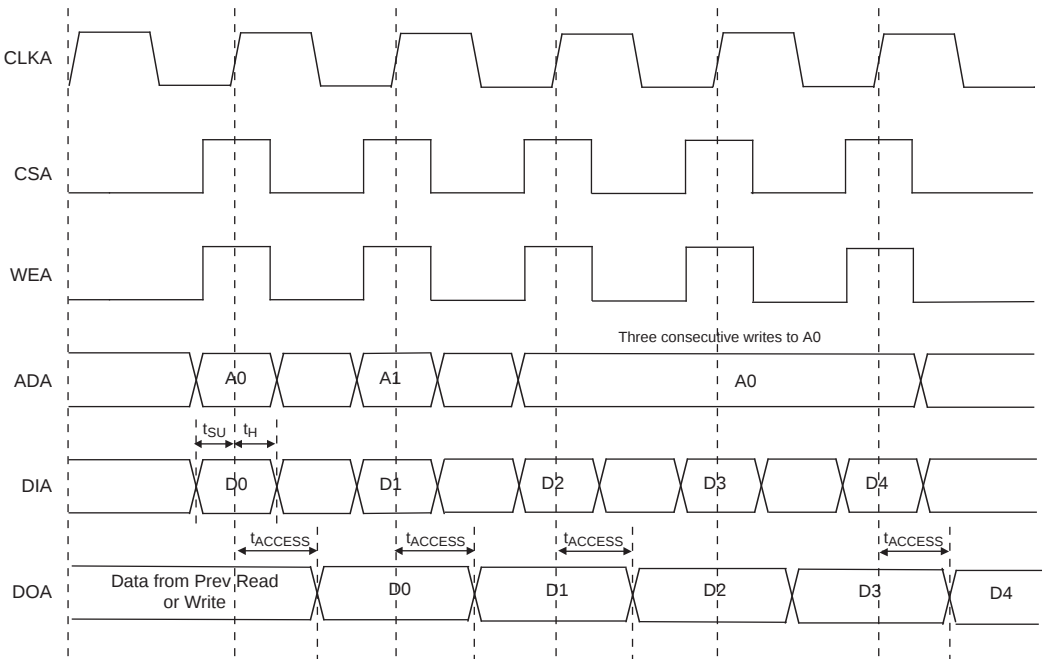


Figure 3-9. Write Through (SP Read/Write On Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive of the clock.

LatticeSC/M sysCONFIG Port Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
General Configuration Timing				
t_{SMODE}	M[3:0] Setup Time to INITN High	0	—	ns
t_{HMODE}	M[3:0] Hold Time from INITN High	600	—	ns
t_{RW}	RESETN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
t_{PGW}	PROGRAMN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
$f_{ESB_CLK_FRQ}$	System Bus ESB_CLK Frequency (No Wait States)	—	133	MHz
sysCONFIG Master Parallel Configuration Mode				
t_{SMB}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMB}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMB}	RCLK Low Time (Non-compressed Bitstreams)	0.5	0.5	CCLK periods
	RCLK Low Time (Compressed Bitstreams)	0.5	7.5	CCLK periods
t_{CHMB}	RCLK High Time	0.5	0.5	CCLK periods
sysCONFIG SPI Port				
t_{CFGX}	INITN High to CSCK Low	—	80	ns
t_{CSSPI}	INITN High to CSSPIN Low	0	2	μ s
t_{SCK}	CSCK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CSCK Low to Output Valid	—	15	ns
t_{CSPID}	CSSPIN Low to CSCK high Setup Time	—	15	ns
f_{MAXSPI}	Max CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN=0)	—	50	MHz
t_{SUSPI}	SOSPI/D0 Data Setup Time Before CSCK	7	—	ns
t_{HSPI}	SOSPI/D0 Data Hold Time After CSCK	2	—	ns
	Master Clock Frequency	Selected value - 30%	Selected value + 30%	MHz
	Duty Cycle	40	60	%
sysCONFIG Master Serial Configuration Mode				
t_{SMS}	DIN Setup Time	4.4	—	ns
t_{HMS}	DIN Hold Time	0	—	ns
f_{CMS}	CCLK Frequency (No Divider)	90	190	MHz
f_{C_DIV}	CCLK Frequency (Div 128)	0.70	1.48	MHz
t_D	CCLK to DOUT Delay	—	7.5	ns
sysCONFIG Master Parallel Configuration Mode				
t_{AVMP}	RCLK to Address Valid	—	10	ns
t_{SMP}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMP}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMP}	RCLK Low Time (Non-compressed Bitstream)	7.5	7.5	CCLK periods
	RCLK Low Time (Compressed Bitstream)	0.5	63.5	CCLK periods
t_{CHMP}	RCLK High Time	0.5	0.5	CCLK periods
t_{DMP}	CCLK to DOUT	—	7.5	ns

LFSC/M15 Logic Signal Connections: 256 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
N12	PB39C	4	
T15	PB40A	4	PCLKT4_3
R16	PB40B	4	PCLKC4_3
L12	PB43A	4	
M12	PB43B	4	
P16	PB44A	4	
N16	PB44B	4	
R14	PB47C	4	VREF1_4
P15	PB48A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
M13	PB48B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
N13	PB49A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
P14	PB49B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
M16	PR45B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
L16	PR45A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
M14	PR43B	3	
M15	PR43A	3	
K16	PR41D	3	VREF2_3
J16	PR37B	3	
H16	PR37A	3	
L13	PR35D	3	DIFFR_3
L14	PR35B	3	
L15	PR35A	3	
K12	PR31C	3	VREF1_3
J13	PR28D	3	PCLKC3_2
K13	PR28C	3	PCLKT3_2
H15	PR28B	3	
F16	PR28A	3	
J11	PR26D	3	PCLKC3_1
J12	PR26C	3	PCLKT3_1
J15	PR26B	3	PCLKC3_0
J14	PR26A	3	PCLKT3_0
E16	PR24D	2	PCLKC2_2
D16	PR24C	2	PCLKT2_2
H11	PR24B	2	PCLKC2_0
H12	PR24A	2	PCLKT2_0
H13	PR23B	2	PCLKC2_1
H14	PR23A	2	PCLKT2_1
G12	PR22D	2	DIFFR_2
G13	PR22C	2	VREF1_2
F8	PR22B	2	
F9	PR22A	2	
G16	PR18D	2	VREF2_2
F15	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
R29	PR28B	3		PR31B	3	
P29	PR28A	3		PR31A	3	
P27	PR27C	3	PCLKT3_3	PR30C	3	PCLKT3_3
N29	PR27B	3		PR30B	3	
N28	PR27A	3		PR30A	3	
R25	PR26D	3	PCLKC3_1	PR29D	3	PCLKC3_1
R26	PR26C	3	PCLKT3_1	PR29C	3	PCLKT3_1
R28	PR26B	3	PCLKC3_0	PR29B	3	PCLKC3_0
P28	PR26A	3	PCLKT3_0	PR29A	3	PCLKT3_0
N27	PR24D	2	PCLKC2_2	PR27D	2	PCLKC2_2
P26	PR24C	2	PCLKT2_2	PR27C	2	PCLKT2_2
L30	PR24B	2	PCLKC2_0	PR27B	2	PCLKC2_0
K30	PR24A	2	PCLKT2_0	PR27A	2	PCLKT2_0
J30	PR23B	2	PCLKC2_1	PR26B	2	PCLKC2_1
H30	PR23A	2	PCLKT2_1	PR26A	2	PCLKT2_1
M26	PR22D	2	DIFFR_2	PR25D	2	DIFFR_2
M25	PR22C	2	VREF1_2	PR25C	2	VREF1_2
G29	PR22B	2		PR25B	2	
F29	PR22A	2		PR25A	2	
H28	PR19D	2		PR22D	2	
J28	PR19C	2		PR22C	2	
E30	PR19B	2		PR22B	2	
E29	PR19A	2		PR22A	2	
L26	PR18D	2	VREF2_2	PR18D	2	VREF2_2
L25	PR18C	2		PR18C	2	
F28	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
G28	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
K26	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
K25	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
D30	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
D29	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
G26	PR15D	2		PR16D	2	
H26	PR15C	2		PR16C	2	
E28	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
D28	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
J25	VCCJ	-		VCCJ	-	
H25	TDO	-	TDO	TDO	-	TDO
J26	TMS	-		TMS	-	
G25	TCK	-		TCK	-	
G24	TDI	-		TDI	-	
F26	PROGRAMN	1		PROGRAMN	1	
H24	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
F25	CCLK	1		CCLK	1	
D27	VCC12	-		VCC12	-	
E26	VCC12	-		VCC12	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ27	GND	-		GND	-	
AF23	GND	-		GND	-	
AF22	GND	-		GND	-	
AE27	GND	-		GND	-	
AA27	GND	-		GND	-	
AB29	GND	-		GND	-	
Y26	GND	-		GND	-	
AC30	GND	-		GND	-	
Y29	GND	-		GND	-	
F30	GND	-		GND	-	
E27	GND	-		GND	-	
F27	GND	-		GND	-	
P25	GND	-		GND	-	
H29	GND	-		GND	-	
K29	GND	-		GND	-	
R24	GND	-		GND	-	
M28	GND	-		GND	-	
J27	GND	-		GND	-	
N26	GND	-		GND	-	
E20	GND	-		GND	-	
E21	GND	-		GND	-	
F21	GND	-		GND	-	
F23	GND	-		GND	-	
G23	GND	-		GND	-	
D21	GND	-		GND	-	
D20	GND	-		GND	-	
E18	GND	-		GND	-	
C20	GND	-		GND	-	
C11	GND	-		GND	-	
A12	GND	-		GND	-	
E11	GND	-		GND	-	
F8	GND	-		GND	-	
G8	GND	-		GND	-	
D11	GND	-		GND	-	
D10	GND	-		GND	-	
H7	GND	-		GND	-	
F10	GND	-		GND	-	
E10	GND	-		GND	-	
AC16	NC	-		NC	-	
J22	VCC	-		VCC	-	
J9	VCC	-		VCC	-	
B2	NC	-		NC	-	
C2	RESPN_ULC	-		RESPN_ULC	-	
C29	RESPN_URC	-		RESPN_URC	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G6	A_HDINN2_R	-	PCS 3E0 CH 2 IN N	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
A6	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
D6	A_VDDOB2_R	-		A_VDDOB2_R	-	
B6	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
D7	A_VDDOB3_R	-		A_VDDOB3_R	-	
B7	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
A7	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
G7	A_HDINN3_R	-	PCS 3E0 CH 3 IN N	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
F7	A_HDINP3_R	-	PCS 3E0 CH 3 IN P	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
H7	A_VDDIB3_R	-		A_VDDIB3_R	-	
H8	B_VDDIB0_R	-		B_VDDIB0_R	-	
F8	B_HDINP0_R	-	PCS 3E1 CH 0 IN P	B_HDINP0_R	-	PCS 3E1 CH 0 IN P
G8	B_HDINN0_R	-	PCS 3E1 CH 0 IN N	B_HDINN0_R	-	PCS 3E1 CH 0 IN N
A8	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P
D8	B_VDDOB0_R	-		B_VDDOB0_R	-	
B8	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N
D9	B_VDDOB1_R	-		B_VDDOB1_R	-	
B9	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N
A9	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P
H10	B_HDINN1_R	-	PCS 3E1 CH 1 IN N	B_HDINN1_R	-	PCS 3E1 CH 1 IN N
G10	B_HDINP1_R	-	PCS 3E1 CH 1 IN P	B_HDINP1_R	-	PCS 3E1 CH 1 IN P
H9	B_VDDIB1_R	-		B_VDDIB1_R	-	
H11	B_VDDIB2_R	-		B_VDDIB2_R	-	
F11	B_HDINP2_R	-	PCS 3E1 CH 2 IN P	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
G11	B_HDINN2_R	-	PCS 3E1 CH 2 IN N	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
A11	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D11	B_VDDOB2_R	-		B_VDDOB2_R	-	
B11	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D12	B_VDDOB3_R	-		B_VDDOB3_R	-	
B12	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
A12	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
G12	B_HDINN3_R	-	PCS 3E1 CH 3 IN N	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
F12	B_HDINP3_R	-	PCS 3E1 CH 3 IN P	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
H12	B_VDDIB3_R	-		B_VDDIB3_R	-	
B10	VCC12	-		VCC12	-	
D10	B_REFCLKN_R	-		B_REFCLKN_R	-	
C10	B_REFCLKP_R	-		B_REFCLKP_R	-	
J15	PT49D	1	HDC/SI	PT61D	1	HDC/SI
K15	PT49C	1	LDCN/SCS	PT61C	1	LDCN/SCS
E13	PT49B	1	D8/MPI_DATA8	PT59B	1	D8/MPI_DATA8
F13	PT49A	1	CS1/MPI_CS1	PT59A	1	CS1/MPI_CS1
H13	PT47D	1	D9/MPI_DATA9	PT58D	1	D9/MPI_DATA9
G13	PT47C	1	D10/MPI_DATA10	PT58C	1	D10/MPI_DATA10
E14	PT47B	1	CS0N/MPI_CS0N	PT57B	1	CS0N/MPI_CS0N
F14	PT47A	1	RDN/MPI_STRB_N	PT57A	1	RDN/MPI_STRB_N
H14	PT46D	1	WRN/MPI_WR_N	PT55D	1	WRN/MPI_WR_N
G14	PT46C	1	D7/MPI_DATA7	PT55C	1	D7/MPI_DATA7
D13	PT46B	1	D6/MPI_DATA6	PT55B	1	D6/MPI_DATA6
D14	PT46A	1	D5/MPI_DATA5	PT55A	1	D5/MPI_DATA5
E15	PT45D	1	D4/MPI_DATA4	PT54D	1	D4/MPI_DATA4

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ9	PB78C	4		PB117C	4	
AJ8	PB78D	4		PB117D	4	
AP3	PB79A	4		PB119A	4	
AN3	PB79B	4		PB119B	4	
AF10	PB79C	4		PB119C	4	
AE10	PB79D	4		PB119D	4	
AL7	PB81A	4		PB121A	4	
AL6	PB81B	4		PB121B	4	
AK7	PB81C	4		PB121C	4	
AK6	PB81D	4		PB121D	4	
AN5	PB82A	4		PB123A	4	
AN4	PB82B	4		PB123B	4	
AH9	PB82C	4	VREF1_4	PB123C	4	VREF1_4
AH8	PB82D	4		PB123D	4	
AM3	PB83A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB124A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AM4	PB83B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB124B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AG9	PB83C	4		PB124C	4	
AG8	PB83D	4		PB124D	4	
AN2	PB85A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB125A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AM2	PB85B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB125B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ6	PB85C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB125C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH6	PB85D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB125D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF7	PROBE_VCC	-		PROBE_VCC	-	
AF8	PROBE_GND	-		PROBE_GND	-	
AG7	PR71D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR95D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AG6	PR71C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR95C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AL4	PR71B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR95B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AL3	PR71A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR95A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD10	PR70D	3		PR94D	3	
AD9	PR70C	3		PR94C	3	
AH4	PR70B	3		PR94B	3	
AJ4	PR70A	3		PR94A	3	
AK5	PR69D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR93D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AJ5	PR69C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR93C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AM1	PR69B	3		PR93B	3	
AL1	PR69A	3		PR93A	3	
AH5	PR67D	3		PR91D	3	
AG5	PR67C	3		PR91C	3	
AL2	PR67B	3		PR91B	3	
AK2	PR67A	3		PR91A	3	
AB9	PR66D	3		PR90D	3	
AC9	PR66C	3		PR90C	3	
AH1	PR66B	3		PR90B	3	
AG1	PR66A	3		PR90A	3	
AE8	PR65D	3	VREF2_3	PR89D	3	VREF2_3

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
G27	A_REFCLKP_L	-	
H27	A_REFCLKN_L	-	
H25	VCC12	-	
H26	RESP_ULC	-	
B33	RESETN	1	
C34	TSALLN	1	
D34	DONE	1	
C33	INITN	1	
J27	M0	1	
K27	M1	1	
M26	M2	1	
L26	M3	1	
F30	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
G30	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
H28	PL15C	7	
J28	PL15D	7	
F31	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
G31	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N25	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P25	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
D33	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
E33	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
H29	PL18C	7	
J29	PL18D	7	VREF2_7
F32	PL19A	7	
G32	PL19B	7	
P26	PL19C	7	
N26	PL19D	7	
H30	PL26A	7	
J30	PL26B	7	
L28	PL26C	7	
M28	PL26D	7	
J31	PL43A	7	
K31	PL43B	7	
L27	PL43C	7	VREF1_7
M27	PL43D	7	DIFFR_7
J32	PL45A	7	
K32	PL45B	7	
L29	PL45C	7	
M29	PL45D	7	
H33	PL47A	7	
J33	PL47B	7	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AJ34	PL98A	6	
AK34	PL98B	6	
AB27	PL98C	6	
AC27	PL98D	6	
AF33	PL99A	6	
AG33	PL99B	6	
AC29	PL99C	6	
AD29	PL99D	6	
AE31	PL103A	6	
AF31	PL103B	6	
AF30	PL103C	6	
AF29	PL103D	6	
AH33	PL104A	6	
AJ33	PL104B	6	
AC28	PL104C	6	
AD28	PL104D	6	
AH32	PL107A	6	
AJ32	PL107B	6	
AD27	PL107C	6	
AE27	PL107D	6	VREF2_6
AG34	PL109A	6	
AH34	PL109B	6	
AC26	PL109C	6	
AB26	PL109D	6	
AK33	PL112A	6	
AL33	PL112B	6	
AG30	PL112C	6	
AH30	PL112D	6	
AL34	PL115A	6	
AM34	PL115B	6	
AJ30	PL115C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AK30	PL115D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AJ31	PL116A	6	
AH31	PL116B	6	
AD26	PL116C	6	
AD25	PL116D	6	
AL32	PL117A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AL31	PL117B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AG29	PL117C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AG28	PL117D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AF28	XRES	-	
AF27	TEMP	6	
AM33	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AN15	PB89A	4	PCLKT4_2
AN14	PB89B	4	PCLKC4_2
AE16	PB89C	4	PCLKT4_7
AD16	PB89D	4	PCLKC4_7
AK15	PB90A	4	PCLKT4_1
AK14	PB90B	4	PCLKC4_1
AG15	PB90C	4	PCLKT4_6
AG14	PB90D	4	PCLKC4_6
AM13	PB91A	4	PCLKT4_0
AM12	PB91B	4	PCLKC4_0
AJ12	PB91C	4	VREF2_4
AJ11	PB91D	4	
AL13	PB93A	4	PCLKT4_5
AL12	PB93B	4	PCLKC4_5
AH12	PB93C	4	
AH11	PB93D	4	
AN13	PB94A	4	PCLKT4_3
AN12	PB94B	4	PCLKC4_3
AD14	PB94C	4	PCLKT4_4
AD15	PB94D	4	PCLKC4_4
AP13	PB87A	4	
AP12	PB87B	4	
AK13	PB87C	4	
AK12	PB87D	4	
AP11	PB97A	4	
AP10	PB97B	4	
AN11	PB113A	4	
AN10	PB113B	4	
AF14	PB113C	4	
AF13	PB113D	4	
AM10	PB115A	4	
AM9	PB115B	4	
AE14	PB115C	4	
AE13	PB115D	4	
AP9	PB118A	4	
AP8	PB118B	4	
AK11	PB118C	4	
AK10	PB118D	4	
AL10	PB121A	4	
AL9	PB121B	4	
AF12	PB121C	4	
AF11	PB121D	4	
AN9	PB123A	4	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
J3	PR45A	2	
M8	PR43D	2	DIFFR_2
L8	PR43C	2	VREF1_2
K4	PR43B	2	
J4	PR43A	2	
M7	PR26D	2	
L7	PR26C	2	
J5	PR26B	2	
H5	PR26A	2	
N9	PR19D	2	
P9	PR19C	2	
G3	PR19B	2	
F3	PR19A	2	
J6	PR18D	2	VREF2_2
H6	PR18C	2	
E2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
D2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
G4	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
F4	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
J7	PR15D	2	
H7	PR15C	2	
G5	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
F5	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
C2	VCCJ	-	
M9	TDO	-	TDO
L9	TMS	-	
D1	TCK	-	
C1	TDI	-	
J8	PROGRAMN	1	
K8	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
B2	CCLK	1	
H9	RESP_URC	-	
H10	VCC12	-	
H8	A_REFCLKN_R	-	
G8	A_REFCLKP_R	-	
C3	VCC12	-	
D3	A_VDDIB0_R	-	
A3	A_HDINP0_R	-	PCS 3E0 CH 0 IN P
B3	A_HDINN0_R	-	PCS 3E0 CH 0 IN N
E5	VCC12	-	
A4	A_HDOUPT0_R	-	PCS 3E0 CH 0 OUT P

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AV32	PB27B	5		PB29B	5	
AU36	PB27C	5		PB29C	5	
AU37	PB27D	5		PB29D	5	
BA35	PB28A	5		PB30A	5	
BA34	PB28B	5		PB30B	5	
AJ26	PB28C	5		PB30C	5	
AJ27	PB28D	5		PB30D	5	
AW33	PB29A	5		PB31A	5	
AW32	PB29B	5		PB31B	5	
AU35	PB29C	5		PB31C	5	
AU34	PB29D	5		PB31D	5	
BB35	PB31A	5		PB33A	5	
BB34	PB31B	5		PB33B	5	
AN29	PB31C	5		PB33C	5	
AP29	PB31D	5		PB33D	5	
AY33	PB32A	5		PB34A	5	
AY32	PB32B	5		PB34B	5	
AR31	PB32C	5		PB34C	5	
AR30	PB32D	5		PB34D	5	
AV31	PB33A	5		PB35A	5	
AV30	PB33B	5		PB35B	5	
AN28	PB33C	5		PB35C	5	
AP28	PB33D	5		PB35D	5	
BA33	PB35A	5		PB37A	5	
BA32	PB35B	5		PB37B	5	
AT30	PB35C	5		PB37C	5	
AT31	PB35D	5		PB37D	5	
BB33	PB36A	5		PB38A	5	
BB32	PB36B	5		PB38B	5	
AM26	PB36C	5		PB38C	5	
AL26	PB36D	5		PB38D	5	
AW30	PB37A	5		PB39A	5	
AW29	PB37B	5		PB39B	5	
AP27	PB37C	5		PB39C	5	
AN27	PB37D	5		PB39D	5	
BA31	PB39A	5		PB41A	5	
BA30	PB39B	5		PB41B	5	
AU32	PB39C	5		PB41C	5	
AU33	PB39D	5		PB41D	5	
BB31	PB40A	5		PB42A	5	
BB30	PB40B	5		PB42B	5	
AR28	PB40C	5		PB42C	5	
AR27	PB40D	5		PB42D	5	
AV29	PB41A	5		PB43A	5	
AV28	PB41B	5		PB43B	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
BB12	PB88B	4		PB102B	4	
AM17	PB88C	4		PB102C	4	
AL17	PB88D	4		PB102D	4	
AW14	PB89A	4		PB103A	4	
AW13	PB89B	4		PB103B	4	
AP16	PB89C	4		PB103C	4	
AN16	PB89D	4		PB103D	4	
BA13	PB91A	4		PB105A	4	
BA12	PB91B	4		PB105B	4	
AU13	PB91C	4		PB105C	4	
AU12	PB91D	4		PB105D	4	
BB11	PB92A	4		PB106A	4	
BB10	PB92B	4		PB106B	4	
AP15	PB92C	4		PB106C	4	
AN15	PB92D	4		PB106D	4	
AV13	PB93A	4		PB107A	4	
AV12	PB93B	4		PB107B	4	
AT13	PB93C	4		PB107C	4	
AT12	PB93D	4		PB107D	4	
BA11	PB95A	4		PB109A	4	
BA10	PB95B	4		PB109B	4	
AR13	PB95C	4		PB109C	4	
AR12	PB95D	4		PB109D	4	
AY11	PB96A	4		PB110A	4	
AY10	PB96B	4		PB110B	4	
AP14	PB96C	4		PB110C	4	
AN14	PB96D	4		PB110D	4	
BB9	PB97A	4		PB111A	4	
BB8	PB97B	4		PB111B	4	
AU11	PB97C	4		PB111C	4	
AU10	PB97D	4		PB111D	4	
AW11	PB99A	4		PB113A	4	
AW10	PB99B	4		PB113B	4	
AJ16	PB99C	4		PB113C	4	
AJ17	PB99D	4		PB113D	4	
BA9	PB100A	4		PB114A	4	
BA8	PB100B	4		PB114B	4	
AM15	PB100C	4		PB114C	4	
AL15	PB100D	4		PB114D	4	
AV11	PB101A	4		PB115A	4	
AV10	PB101B	4		PB115B	4	
AP13	PB101C	4		PB115C	4	
AP12	PB101D	4		PB115D	4	
BB7	PB103A	4		PB117A	4	
BB6	PB103B	4		PB117B	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AU9	PB103C	4		PB117C	4	
AU8	PB103D	4		PB117D	4	
AY8	PB104A	4		PB118A	4	
AY7	PB104B	4		PB118B	4	
AU7	PB104C	4		PB118C	4	
AU6	PB104D	4		PB118D	4	
BA7	PB105A	4		PB119A	4	
BA6	PB105B	4		PB119B	4	
AN13	PB105C	4		PB119C	4	
AN12	PB105D	4		PB119D	4	
AV9	PB107A	4		PB121A	4	
AV8	PB107B	4		PB121B	4	
AT10	PB107C	4		PB121C	4	
AT9	PB107D	4		PB121D	4	
AW8	PB108A	4		PB122A	4	
AW7	PB108B	4		PB122B	4	
AP11	PB108C	4		PB122C	4	
AP10	PB108D	4		PB122D	4	
BB5	PB109A	4		PB123A	4	
BB4	PB109B	4		PB123B	4	
AR10	PB109C	4		PB123C	4	
AR9	PB109D	4		PB123D	4	
BA5	PB111A	4		PB125A	4	
BA4	PB111B	4		PB125B	4	
AT7	PB111C	4		PB125C	4	
AT6	PB111D	4		PB125D	4	
BB3	PB112A	4		PB126A	4	
BA3	PB112B	4		PB126B	4	
AM14	PB112C	4		PB126C	4	
AL14	PB112D	4		PB126D	4	
AY5	PB113A	4		PB127A	4	
AY4	PB113B	4		PB127B	4	
AN11	PB113C	4		PB127C	4	
AN10	PB113D	4		PB127D	4	
AV7	PB115A	4		PB129A	4	
AV6	PB115B	4		PB129B	4	
AM12	PB115C	4		PB129C	4	
AM11	PB115D	4		PB129D	4	
AW5	PB116A	4		PB130A	4	
AW4	PB116B	4		PB130B	4	
AT5	PB116C	4		PB130C	4	
AT4	PB116D	4		PB130D	4	
AY2	PB117A	4		PB131A	4	
BA2	PB117B	4		PB131B	4	
AP9	PB117C	4		PB131C	4	

Date	Version	Section	Change Summary
September 2007	01.7	Pinout Information	Added Thermal Management text section.
		Supplemental Information	Updated title list.
November 2007	01.8	Ordering Information	Removed -7 speed grade information for 115K LUT devices in the Ordering Information tables.
January 2008	01.9	Introduction	Corrections/Additions to memory controller list (Tables 1-2).
		Architecture	AIL Overview – Modified power used by AIL block.
			PURESPEED I/O Buffer Banks – Modified VTT termination info. Added info about complimentary drivers for all banks.
			Supported Source Synchronous Interfaces – Modified data for DDRII in Table 2-11.
		DC and Switching Characteristics	Recommended Operating Conditions – Changed footnote 3.
			Initialization and Standby Supply Current – Inserted a paragraph with info regarding the table. Also updated the table.
			Typical Building Block Function Performance – Added VCC=1.2V=1.2V+/-5% above Pin to Pin Performance table.
			LatticeSC External Switching Characteristics – Added VCC=1.2V=1.2V+/-5% above table. Reworded footnote 3.
			LatticeSC Family Timing Adders – Added VCC=1.2V=1.2V+/-5% above table.
			LatticeSC Internal Timing Parameters – Added VCC=1.2V=1.2V+/-5% above table. Reworded footnote 1.
			GSR Timing – Added a new table for Internal System Bus Timing after GSR Timing.
			LatticeSC sysCONFIG Port Timing – Corrected sysCONFIG SPI Port information.
		Pinout Information	Signal Descriptions – Modified info for VTT_x, PROBE_VCC, and PROBE_GND. Modified info for [LOC]_DLL[T,C]_IN[C,D,E,F].
		Supplemental Information	Updated list of technical notes, added reference to LatticeSC/M flexiPCS Data Sheet.
March 2008	02.0	DC and Switching Characteristics	Updated Internal Timing Parameters table.
			Updated Read Mode timing diagram.
			Updated Read Mode with Input Registers Only timing diagram.
June 2008	02.1	—	Data sheet status changed from preliminary to final.
		Architecture	Removed Read-Before-Write sysMEM EBR mode.
		DC and Switching Characteristics	Updated LatticeSC/M External Switching Characteristics table.
			Updated LatticeSC/M Internal Timing Parameters table.
December 2008	02.2	Architecture	Removed Read-Before-Write sysMEM EBR mode.
			Output/Tristate DDR/Shift Register Block Diagram - corrected connection to POS.
		DC and Switching Characteristics	DC and Switching Characteristics table - updated data for t_{SUI_PIO} .
			Added T_R , T_F parameter to PURESPEED I/O Differential Electrical Characteristics (LVDS) table.
January 2010	02.3	Multiple	Removed references to HyperTransport throughout the data sheet.
		Introduction	Updated per PCN #01A-10 (ceramic fcBGA conversion to organic fcBGA for the 1152-ball and 1704-ball fcBGA packages) and PCN #02A-10 (1020-ball organic fcBGA conversion to 1020-ball organic fcBGA revision 2 package).
		Ordering Information	

Date	Version	Section	Change Summary
December 2011	02.4	DC and Switching Characteristics	Updated JTAG Port Timing Specifications table.