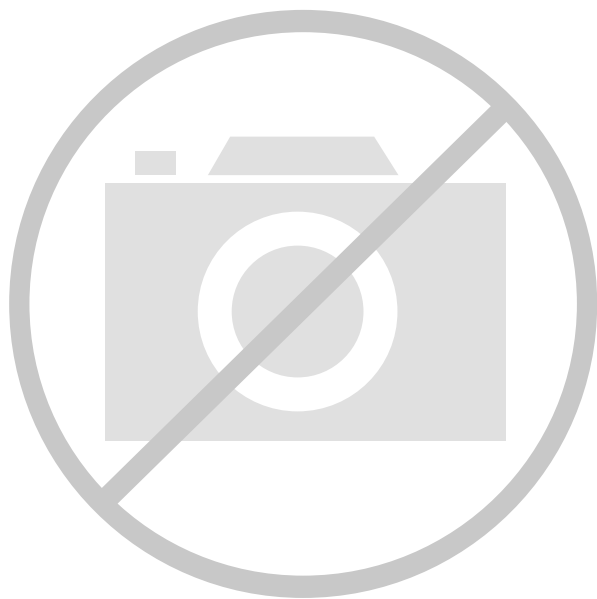




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	604
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga40ep1-7ff1152c

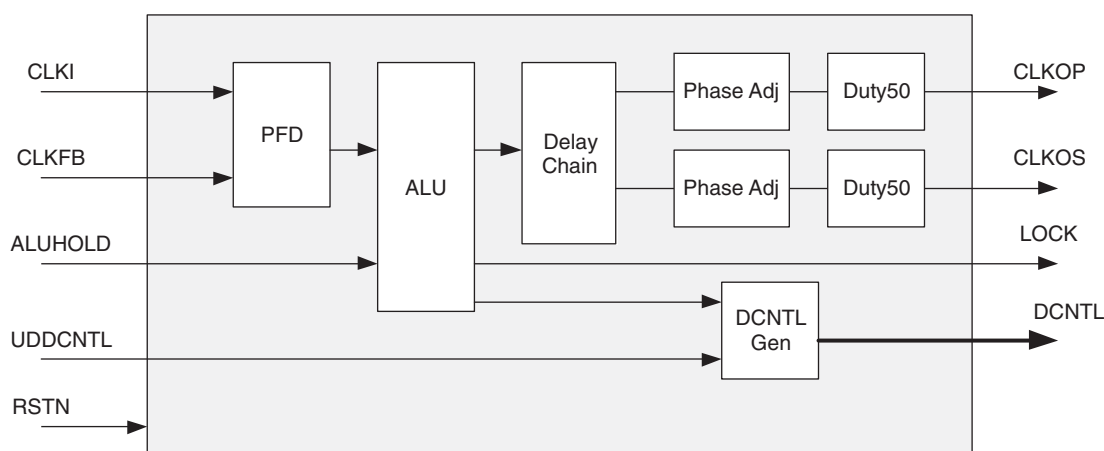
There is a Digital Control (DCNTL) bus available from the DLL block. This Digital Control bus is available to the delay lines in the PIC blocks in the adjacent banks. The UDDCNTL signal allows the user to latch the current value on the digital control bus.

Figure 2-12 shows the DLL block diagram of the DLL inputs and outputs. The output of the phase frequency detector controls an arithmetic logic unit (ALU) to add or subtract one delay tap. The digital output of this ALU is used to control the delay value of the delay chain and this digital code is transmitted via the DCNTL bus.

The sysCLOCK DLL can be configured at power-up, then, if desired, reconfigured dynamically through the Serial Memory Interface bus which interfaces with the on-chip Microprocessor Interface (MPI) bus. In addition, users can drive the SMI interface from routing if desired.

The user can configure the DLL for many common functions such as clock injection match and single delay cell. Lattice provides primitives in its design for time reference delay (DDR memory) and clock injection delay removal.

Figure 2-12. DLL Diagram



PLL/DLL Cascading

The LatticeSC devices have been designed to allow certain combinations of PLL and DLL cascading. The allowable combinations are as follows:

- PLL to PLL
- PLL to DLL
- DLL to DLL
- DLL to PLL

DLLs are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLL and PLLs.

When cascading the DLL to the PLL, the DLL can be used to drive the PLL to create fine phase shifts of an input clock signal. Figure 2-13 shows a shift of all outputs for CLKOP and CLKOS out in time.

Table 2-10. Supported Output Standards⁴

Output Standard	Drive	V _{CCIO} (Nom)	On-chip Output Termination
Single-ended Interfaces			
LVTTL/D ¹	8mA, 16mA, 24mA	3.3	None.
LVC MOS33/D ¹	8mA, 16mA, 24mA	3.3	None
LVC MOS25/D ^{1,2}	4mA, 8mA, 12mA, 16mA,	2.5	None, series: 25, 33, 50, 100
LVC MOS18/D ^{1,2}	4mA, 8mA, 12mA, 16mA,	1.8	None, series: 25, 33, 50, 100
LVC MOS15/D ^{1,2}	4mA, 8mA, 12mA, 16mA,	1.5	None, series: 25, 33, 50, 100
LVC MOS12/D ^{1,2}	2mA, 4mA, 8mA, 12mA	1.2	None, series: 25, 33, 50, 100
PCIX15	N/A	1.5	None
PCI33, PCIX33, AGP1X33, AGP2X33	N/A	3.3	None
HSTL18_I	N/A	1.8	None, series: 50
HSTL18_II	N/A	1.8	None, series: 25, series + parallel to V _{CCIO} /2: 25 + 60
HSTL15_I	N/A	1.5	None, series: 50
HSTL15_II	N/A	1.5	None, series: 25, series + parallel to V _{CCIO} /2: 25 + 60
SSTL33_I	N/A	3.3	None
SSTL33_II	N/A	3.3	None
SSTL25_I	N/A	2.5	None, series: 50
SSTL25_II	N/A	2.5	None, series: 33, series + parallel to V _{CCIO} /2: 33+ 60
SSTL18_I	N/A	1.8	None, series: 33
SSTL18_II	N/A	1.8	None, series: 33, series + parallel to V _{CCIO} /2: 33+ 60
Differential Interfaces			
SSTL18D_I	N/A	1.8	None, series: 33
SSTL25D_I	N/A	2.5	None, series: 50
SSTL18D_II, SSTL25D_II	N/A	1.2/2.5/3.3	None, series: 33, series + parallel to V _{CCIO} /2: 33+ 60
SSTL33D_I, II	N/A	3.3	None
HSTL15D_I, HSTL18D_I	N/A	1.5/1.8	None, series: 50
HST15D_II, HSTL18D_II	N/A	1.5/1.8	None, series: 25, series + parallel to V _{CCIO} /2: 25 + 60
LVDS	2mA, 3.5mA, 4mA, 6mA	N/A	None
Mini-LVDS	3.5mA, 4mA, 6mA	N/A	None
BLVDS25	N/A	N/A	None
MLVDS25	N/A	N/A	None
LVPECL33 ³	N/A	3.3	None
RSDS	2mA, 3.5mA, 4mA, 6mA	N/A	None

1. D refers to open drain capability.

2. User can select either drive current or driver impedances but not both.

3. Emulated with external resistors.

4. No GTL or GTL+ support.

PCI Clamp

A programmable PCI clamp is available on the top and bottom banks of the device. The PCI clamp can be turned “ON” or “OFF” on each pin independently. The PCI clamp is used when implementing a 3.3V PCI interface. The

Initialization and Standby Supply Current

The table below indicates initialization and standby supply current while operating at 85°C junction temperature (T_J), which is the high end of the commercial temperature range, and 105°C, which is the high end of the industrial temperature range. This data assumes all outputs are tri-stated and all inputs are configured as LVCMOS and held at V_{CCIO} or GND. The remaining SERDES supply current for V_{DDIB} and V_{DDOB} is detailed in the SERDES section of this data sheet. For power at your design temperature, it is recommended to use the Power Calculator tool which is accessible in ispLEVER or can be used as a standalone tool. For more information on supply current, see the reference to additional technical documentation available at the end of this data sheet.

Over Recommended Operating Conditions

Symbol	Condition	Parameter	Device	25°C Typ. ¹	85°C Max. ²		105°C Max. ²	Units
				All	-5, -6	-7	-5, -6	
I_{CC}	(VCC = 1.2V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	65	449	678	755	mA
			LFSC/M25	113	798	1255	1343	mA
			LFSC/M40	159	1178	2006	1981	mA
			LFSC/M80	276	2122	3827	3569	mA
			LFSC/M115	454	3376	—	5679	mA
	(VCC = 1.0V +/- 5%)	Core Operating Power Supply Current	LFSC/M15	45	312	471	524	mA
			LFSC/M25	79	554	872	933	mA
			LFSC/M40	110	818	1393	1375	mA
			LFSC/M80	191	1473	2658	2478	mA
			LFSC/M115	315	2344	—	3943	mA
I_{CC12}		1.2V Power Supply Current for Configuration Logic, FPGA PLL, SERDES PLL and SERDES Analog Supplies	LFSC/M15	23	39	59	35	mA
			LFSC/M25	25	50	78	56	mA
			LFSC/M40	31	78	133	89	mA
			LFSC/M80	50	108	195	123	mA
			LFSC/M115	65	131	—	154	mA
I_{CCAUX}		Auxiliary Operating Power Supply Current	LFSC/M15	7	12	19	14	mA
			LFSC/M25	9	16	25	18	mA
			LFSC/M40	12	23	39	25	mA
			LFSC/M80	13	25	45	23	mA
			LFSC/M115	16	27	—	26	mA
I_{CCIO} and I_{CCJ}		Bank Power Supply Current (per bank)	LFSC/M15	0.1	0.2	0.3	0.2	mA
			LFSC/M25	0.3	0.6	1.0	0.7	mA
			LFSC/M40	0.4	0.9	1.5	1.0	mA
			LFSC/M80	0.5	1.1	2.1	1.3	mA
			LFSC/M115	0.7	1.5	—	1.8	mA

1. I_{CC} is specified at $T_J = 25^\circ\text{C}$ and typical V_{CC} .

2. I_{CC} is specified at the respective commercial and industrial maximum T_J and V_{CC} limits.

Switching Characteristics

All devices are 100% functionally tested. Listed below are representative values of internal and external timing parameters. For more specific, more precise, and worst-case guaranteed data at a particular temperature and voltage, use the values reported by the static timing analyzer in the ispLEVER design tool from Lattice and back-annotate to the simulation net list.

LatticeSC/M Internal Timing Parameters¹ (Continued)

Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

Parameter	Symbol	Description	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
EBR Timing									
t _{CO_EBR}	CK_Q_DEL	Clock (Read) to output from Address or Data	—	1.900	—	2.116	—	2.335	ns
t _{COO_EBR}	CK_Q_DEL	Clock (Write) to output from EBR output Register	0.390	—	0.444	—	0.498	—	ns
t _{SUDATA_EBR}	D_CK_SET	Setup Data to EBR Memory (Write clk)	-0.173	—	-0.192	—	-0.210	—	ns
t _{HDATA_EBR}	D_CK_HLD	Hold Data to EBR Memory (Write clk)	0.276	—	0.305	—	0.335	—	ns
t _{SUADDR_EBR}	A_CK_SET	Setup Address to EBR Memory (Write clk)	-0.165	—	-0.182	—	-0.200	—	ns
t _{HADDR_EBR}	A_CK_HLD	Hold Address to EBR Memory (Write clk)	0.269	—	0.298	—	0.327	—	ns
t _{SUWREN_EBR}	CE_CK_SET	Setup Write/Read Enable to EBR Memory (Write/Read clk)	0.225	—	0.226	—	0.226	—	ns
t _{HWREN_EBR}	CE_CK_HLD	Hold Write/Read Enable to EBR Memory (write/read clk)	0.073	—	0.095	—	0.116	—	ns
t _{SUCE_EBR}	CS_CK_SET	Clock Enable Setup Time to EBR Output Register (Read clk)	0.261	—	0.269	—	0.276	—	ns
t _{HCE_EBR}	CS_CK_HLD	Clock Enable Hold Time to EBR Out-put Register (Read clk)	0.023	—	0.039	—	0.055	—	ns
t _{RSTO_EBR}	RESET_Q_DEL	Reset To Output Delay Time from EBR Output Register (asynchronous)	—	0.589	—	0.673	—	0.757	ns
Cycle Boosting Timing									
t _{DEL1}	DEL1	Cycle boosting delay 1 applies to PIO, PFU, EBR	—	0.480	—	0.524	—	0.570	ns
t _{DEL2}	DEL2	Cycle boosting delay 2 applies to PIO, PFU, EBR	—	0.922	—	1.005	—	1.090	ns
t _{DEL3}	DEL3	Cycle boosting delay 3 applies to PIO, PFU, EBR	—	1.366	—	1.488	—	1.612	ns

1. Complete timing parameters for a user design will be incorporated when running ispLEVER. This is a sampling of the key timing parameters.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
D[n:0]	I/O	In parallel configuration modes, D[7:0] receives configuration data, and each pin is pull-up enabled. For slave serial mode, D0 is the data input. D[7:3] is the output internal status for peripheral mode when RDN is low. D[7:0] is also the first byte of MPI data pins. In MPI configuration mode, MPI selectable data bus width from 8 and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction.
DP[m:0]	I/O	MPI selectable parity data bus width from 1, 2, and 3-bit DP[0] for D[7:0], DP[1] for D[15:8], and DP[2] for D[23:16].
BUSYN/RCLK/SCK	O	During configuration in peripheral mode, high on BUSYN indicates another byte can be written to the FPGA. If a read operation is done when the device is selected, the same status is also available on D[7] in asynchronous peripheral mode. During configuration in slave parallel mode, low on BUSYN inhibits the external host from sending new data. The output is used by slave parallel and master serial modes only for decompression. During configuration in master parallel and master byte modes, RCLK is a read clock output signal to an external memory. The RCLK frequency is the same as CCLK when used with uncompressed bit-streams. RCLK will be 1/8 the frequency of CCLK when the bitstream is compressed. During configuration in SPI modes, SCK is generated by the device and connected to the CLK input of the FLASH memory.
MPI Interface (Dedicated pin)		
MPI_IRQ_N	O	MPI Interrupt request active low signal is controlled by system bus interrupt controller and may be sourced from any bus error or MPI configuration error. It can be connected to one of MPC860 IRQ pins.
MPI Interface (User I/O if MPI is not used.)		
MPI_CS0N MPI_CS1	I	MPI chip select pins, active low on MPI_CS0N while active high on MPI_CS1. Both have to be active during the whole transfer data phase. During transfer address phase, both can be inactive so that the decoding for them from address can be slow. If they are active during address phase, one cycle can be saved for sync read.
MPI_CLK	I	This is the PowerPC bus clock. It can be a source of the clock for embedded system bus. If MPI_CLK is used as system bus clock, MPI will be set into sync mode by default. All of the operation on PowerPC side of MPI are synchronized to the rising edge of this clock.
MPI_TSIZE[1:0]	I	Driven by a bus master to indicate the data transfer size for the transaction. 01 for byte, 10 for half-word, and 00 for word.
MPI_WR_N	I	Driven high indicates that a read access is in progress. Driven low indicates that a write access is in process.
MPI_BURST	I	Driven active low indicates that a burst transfer is in progress. Driven high indicates that the current transfer is not a burst.
MPI_BDIP	I	Active low "Burst Data in Process" is driven by a PowerPC processor. Asserted indicates that the second beat in front of the current one is requested by the master. Negated before the burst transfer ends to abort the burst data phase.

LFSC/M15 Logic Signal Connections: 256 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
C5	A_VDDIB1_L	-	
A5	A_HDINP1_L	-	PCS 360 CH 1 IN P
B5	A_HDINN1_L	-	PCS 360 CH 1 IN N
A4	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
B4	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
C4	A_VDDOB1_L	-	
B3	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
C3	A_VDDOB0_L	-	
A3	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
B2	A_HDINN0_L	-	PCS 360 CH 0 IN N
A2	A_HDINP0_L	-	PCS 360 CH 0 IN P
C2	A_VDDIB0_L	-	
A1	GND	-	
A16	GND	-	
B10	GND	-	
C13	GND	-	
D15	GND	-	
D3	GND	-	
E11	GND	-	
F13	GND	-	
G14	GND	-	
G2	GND	-	
G8	GND	-	
H10	GND	-	
J7	GND	-	
K15	GND	-	
K3	GND	-	
K9	GND	-	
M6	GND	-	
N11	GND	-	
N14	GND	-	
N2	GND	-	
P10	GND	-	
P4	GND	-	
R13	GND	-	
R7	GND	-	
G10	VCC	-	
G7	VCC	-	
G9	VCC	-	
H7	VCC	-	
H8	VCC	-	
H9	VCC	-	
J10	VCC	-	
J8	VCC	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
F19	PT37D	1	WRN/MPI_WR_N	PT46D	1	WRN/MPI_WR_N
F18	PT37C	1	D7/MPI_DATA7	PT46C	1	D7/MPI_DATA7
C18	PT37B	1	D6/MPI_DATA6	PT46B	1	D6/MPI_DATA6
C17	PT37A	1	D5/MPI_DATA5	PT46A	1	D5/MPI_DATA5
E17	PT36D	1	D4/MPI_DATA4	PT45D	1	D4/MPI_DATA4
E16	PT36C	1	D3/MPI_DATA3	PT45C	1	D3/MPI_DATA3
G18	PT35B	1	D2/MPI_DATA2	PT45B	1	D2/MPI_DATA2
G17	PT35A	1	D1/MPI_DATA1	PT45A	1	D1/MPI_DATA1
B18	PT33B	1	D0/MPI_DATA0	PT43B	1	D0/MPI_DATA0
B17	PT33A	1	QOUT/CEON	PT43A	1	QOUT/CEON
G16	PT32D	1	VREF2_1	PT42D	1	VREF2_1
A18	PT32B	1	DOUT	PT42B	1	DOUT
A17	PT32A	1	MCA_DONE_IN	PT42A	1	MCA_DONE_IN
H18	PT31B	1	MCA_CLK_P1_OUT	PT41B	1	MCA_CLK_P1_OUT
H17	PT31A	1	MCA_CLK_P1_IN	PT41A	1	MCA_CLK_P1_IN
D17	PT29B	1	MCA_CLK_P2_OUT	PT39B	1	MCA_CLK_P2_OUT
D16	PT29A	1	MCA_CLK_P2_IN	PT39A	1	MCA_CLK_P2_IN
F17	PT28D	1	MCA_DONE_OUT	PT38D	1	MCA_DONE_OUT
F16	PT28C	1	BUSYN/RCLK/SCK	PT38C	1	BUSYN/RCLK/SCK
C16	PT28B	1	DP0/MPI_PAR0	PT38B	1	DP0/MPI_PAR0
C15	PT28A	1	MPI_TA	PT38A	1	MPI_TA
B16	PT27B	1	PCLKC1_0	PT37B	1	PCLKC1_0
B15	PT27A	1	PCLKT1_0/MPI_CLK	PT37A	1	PCLKT1_0/MPI_CLK
H16	PT25D	1	DP3/PCLKC1_4/MPI_PAR3	PT35D	1	DP3/PCLKC1_4/MPI_PAR3
A16	PT25B	1	MPI_RETRY	PT35B	1	MPI_RETRY
A15	PT25A	1	A0/MPI_ADDR14	PT35A	1	A0/MPI_ADDR14
G15	PT24D	1	A1/MPI_ADDR15	PT33D	1	A1/MPI_ADDR15
F15	PT24C	1	A2/MPI_ADDR16	PT33C	1	A2/MPI_ADDR16
E15	PT24B	1	A3/MPI_ADDR17	PT33B	1	A3/MPI_ADDR17
D15	PT24A	1	A4/MPI_ADDR18	PT33A	1	A4/MPI_ADDR18
C14	PT23B	1	A5/MPI_ADDR19	PT32B	1	A5/MPI_ADDR19
C13	PT23A	1	A6/MPI_ADDR20	PT32A	1	A6/MPI_ADDR20
H14	PT21C	1	VREF1_1	PT31C	1	VREF1_1
B14	PT21B	1	A7/MPI_ADDR21	PT31B	1	A7/MPI_ADDR21
B13	PT21A	1	A8/MPI_ADDR22	PT31A	1	A8/MPI_ADDR22
G14	PT20B	1	A9/MPI_ADDR23	PT29B	1	A9/MPI_ADDR23
F14	PT20A	1	A10/MPI_ADDR24	PT29A	1	A10/MPI_ADDR24
A14	PT19B	1	A11/MPI_ADDR25	PT28B	1	A11/MPI_ADDR25
A13	PT19A	1	A12/MPI_ADDR26	PT28A	1	A12/MPI_ADDR26
G13	PT17D	1	D11/MPI_DATA11	PT27D	1	D11/MPI_DATA11
H13	PT17C	1	D12/MPI_DATA12	PT27C	1	D12/MPI_DATA12
E14	PT17B	1	A13/MPI_ADDR27	PT27B	1	A13/MPI_ADDR27
E13	PT17A	1	A14/MPI_ADDR28	PT27A	1	A14/MPI_ADDR28
G12	PT15D	1	A16/MPI_ADDR30	PT25D	1	A16/MPI_ADDR30
G11	PT15C	1	D13/MPI_DATA13	PT25C	1	D13/MPI_DATA13

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W24	VCCAUX	-		VCCAUX	-	
AC17	VCCAUX	-		VCCAUX	-	
AC18	VCCAUX	-		VCCAUX	-	
AC19	VCCAUX	-		VCCAUX	-	
AD17	VCCAUX	-		VCCAUX	-	
AD18	VCCAUX	-		VCCAUX	-	
AD19	VCCAUX	-		VCCAUX	-	
AC12	VCCAUX	-		VCCAUX	-	
AC13	VCCAUX	-		VCCAUX	-	
AC14	VCCAUX	-		VCCAUX	-	
AD12	VCCAUX	-		VCCAUX	-	
AD13	VCCAUX	-		VCCAUX	-	
AD14	VCCAUX	-		VCCAUX	-	
U7	VCCAUX	-		VCCAUX	-	
U8	VCCAUX	-		VCCAUX	-	
V7	VCCAUX	-		VCCAUX	-	
V8	VCCAUX	-		VCCAUX	-	
W7	VCCAUX	-		VCCAUX	-	
W8	VCCAUX	-		VCCAUX	-	
M7	VCCAUX	-		VCCAUX	-	
M8	VCCAUX	-		VCCAUX	-	
N7	VCCAUX	-		VCCAUX	-	
N8	VCCAUX	-		VCCAUX	-	
H10	VCCIO1	-		VCCIO1	-	
H21	VCCIO1	-		VCCIO1	-	
H22	VCCIO1	-		VCCIO1	-	
H9	VCCIO1	-		VCCIO1	-	
J11	VCCIO1	-		VCCIO1	-	
J12	VCCIO1	-		VCCIO1	-	
J13	VCCIO1	-		VCCIO1	-	
J14	VCCIO1	-		VCCIO1	-	
J15	VCCIO1	-		VCCIO1	-	
J16	VCCIO1	-		VCCIO1	-	
J17	VCCIO1	-		VCCIO1	-	
J18	VCCIO1	-		VCCIO1	-	
J19	VCCIO1	-		VCCIO1	-	
J20	VCCIO1	-		VCCIO1	-	
J23	VCCIO2	-		VCCIO2	-	
J24	VCCIO2	-		VCCIO2	-	
K23	VCCIO2	-		VCCIO2	-	
K24	VCCIO2	-		VCCIO2	-	
L22	VCCIO2	-		VCCIO2	-	
L23	VCCIO2	-		VCCIO2	-	
M22	VCCIO2	-		VCCIO2	-	
N22	VCCIO2	-		VCCIO2	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH11	PB47C	4	PCLKT4_6	PB54C	4	PCLKT4_6
AH10	PB47D	4	PCLKC4_6	PB54D	4	PCLKC4_6
AK12	PB49A	4	PCLKT4_0	PB55A	4	PCLKT4_0
AJ12	PB49B	4	PCLKC4_0	PB55B	4	PCLKC4_0
AF14	PB49C	4	VREF2_4	PB55C	4	VREF2_4
AE14	PB49D	4		PB55D	4	
AL11	PB51A	4	PCLKT4_5	PB57A	4	PCLKT4_5
AL10	PB51B	4	PCLKC4_5	PB57B	4	PCLKC4_5
AH9	PB51C	4		PB57C	4	
AH8	PB51D	4		PB57D	4	
AK11	PB52A	4	PCLKT4_3	PB58A	4	PCLKT4_3
AJ11	PB52B	4	PCLKC4_3	PB58B	4	PCLKC4_3
AH7	PB52C	4	PCLKT4_4	PB58C	4	PCLKT4_4
AH6	PB52D	4	PCLKC4_4	PB58D	4	PCLKC4_4
AK8	PB53A	4		PB67A	4	
AJ8	PB53B	4		PB67B	4	
AF11	PB53C	4		PB67C	4	
AD12	PB55A	4		PB69A	4	
AE12	PB55B	4		PB69B	4	
AM6	PB56A	4		PB70A	4	
AM5	PB56B	4		PB70B	4	
AC12	PB56C	4		PB70C	4	
AL6	PB57A	4		PB73A	4	
AL5	PB57B	4		PB73B	4	
AG7	PB59A	4		PB74A	4	
AG8	PB59B	4		PB74B	4	
AK6	PB60A	4		PB75A	4	
AJ6	PB60B	4		PB75B	4	
AF10	PB60C	4		PB75C	4	
AE11	PB60D	4		PB75D	4	
AM4	PB61A	4		PB77A	4	
AM3	PB61B	4		PB77B	4	
AH5	PB63A	4		PB78A	4	
AH4	PB63B	4		PB78B	4	
AK5	PB64A	4		PB79A	4	
AJ5	PB64B	4		PB79B	4	
AF8	PB64C	4		PB79C	4	
AF7	PB64D	4		PB79D	4	
AL4	PB65A	4		PB81A	4	
AL3	PB65B	4		PB81B	4	
AG5	PB65C	4		PB81C	4	
AF6	PB65D	4		PB81D	4	
AK3	PB67A	4		PB82A	4	
AJ3	PB67B	4		PB82B	4	
AE10	PB67C	4	VREF1_4	PB82C	4	VREF1_4
AD10	PB67D	4		PB82D	4	
AL2	PB68A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB83A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AK2	PB68B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB83B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AE9	PB68C	4		PB83C	4	
AE8	PB68D	4		PB83D	4	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ1	PB69A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB85A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AK1	PB69B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB85B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ2	PB69C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB85C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH3	PB69D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB85D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AH1	PROBE_VCC	-		PROBE_VCC	-	
AH2	PROBE_GND	-		PROBE_GND	-	
AD9	PR57D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR71D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AC10	PR57C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR71C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AG2	PR57B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR71B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AG1	PR57A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR71A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AD8	PR56D	3		PR70D	3	
AC9	PR56C	3		PR70C	3	
AF2	PR56B	3		PR70B	3	
AF1	PR56A	3		PR70A	3	
AE6	PR55D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR69D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AE7	PR55C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR69C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AE1	PR55B	3		PR69B	3	
AE2	PR55A	3		PR69A	3	
AB8	PR53D	3		PR67D	3	
AC8	PR53C	3		PR67C	3	
AE4	PR53B	3		PR67B	3	
AE3	PR53A	3		PR67A	3	
AA10	PR52D	3		PR66D	3	
AA9	PR52C	3		PR66C	3	
AD1	PR52B	3		PR66B	3	
AC1	PR52A	3		PR66A	3	
AC7	PR51D	3	VREF2_3	PR65D	3	VREF2_3
AB7	PR51C	3		PR65C	3	
AD5	PR51B	3		PR65B	3	
AC5	PR51A	3		PR65A	3	
AE5	PR49D	3		PR62D	3	
AF5	PR49C	3		PR62C	3	
AD3	PR49B	3		PR62B	3	
AD4	PR49A	3		PR62A	3	
Y10	PR48D	3		PR61D	3	
Y9	PR48C	3		PR61C	3	
AC2	PR48B	3		PR61B	3	
AD2	PR48A	3		PR61A	3	
AC6	PR47D	3		PR60D	3	
AB6	PR47C	3		PR60C	3	
AA1	PR47B	3		PR60B	3	
AB1	PR47A	3		PR60A	3	
AA5	PR44D	3		PR53D	3	
AB5	PR44C	3		PR53C	3	
Y1	PR44B	3		PR53B	3	
W1	PR44A	3		PR53A	3	
W8	PR43D	3		PR52D	3	
Y7	PR43C	3		PR52C	3	
Y5	PR43B	3		PR52B	3	
W5	PR43A	3		PR52A	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AN8	PB123B	4	
AG11	PB123C	4	
AG10	PB123D	4	
AP7	PB125A	4	
AP6	PB125B	4	
AG13	PB125C	4	
AG12	PB125D	4	
AN7	PB127A	4	
AN6	PB127B	4	
AK9	PB127C	4	
AK8	PB127D	4	
AP5	PB129A	4	
AP4	PB129B	4	
AD11	PB129C	4	
AE11	PB129D	4	
AM7	PB131A	4	
AM6	PB131B	4	
AJ9	PB131C	4	
AJ8	PB131D	4	
AP3	PB133A	4	
AN3	PB133B	4	
AF10	PB133C	4	
AE10	PB133D	4	
AL7	PB135A	4	
AL6	PB135B	4	
AK7	PB135C	4	
AK6	PB135D	4	
AN5	PB138A	4	
AN4	PB138B	4	
AH9	PB138C	4	VREF1_4
AH8	PB138D	4	
AM3	PB139A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AM4	PB139B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AG9	PB139C	4	
AG8	PB139D	4	
AN2	PB141A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AM2	PB141B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AJ6	PB141C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AH6	PB141D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF7	PROBE_VCC	-	
AF8	PROBE_GND	-	
AG7	PR117D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AG6	PR117C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AD5	PR94C	3	
AE2	PR94B	3	
AD2	PR94A	3	
AC5	PR92D	3	
AB5	PR92C	3	
AF1	PR92B	3	
AE1	PR92A	3	
AA11	PR91D	3	
Y11	PR91C	3	
AC4	PR91B	3	
AB4	PR91A	3	
AA8	PR90D	3	DIFFR_3
AA9	PR90C	3	
AC3	PR90B	3	
AB3	PR90A	3	
AA7	PR79D	3	
Y7	PR79C	3	
AA2	PR79B	3	
Y2	PR79A	3	
AA6	PR77D	3	
Y6	PR77C	3	
Y4	PR77B	3	
W4	PR77A	3	
W11	PR74D	3	
V11	PR74C	3	
W2	PR74B	3	
V2	PR74A	3	
W9	PR71D	3	
V9	PR71C	3	
V1	PR71B	3	
U1	PR71A	3	
W10	PR70D	3	
V10	PR70C	3	
U2	PR70B	3	
T2	PR70A	3	
Y8	PR69D	3	
W8	PR69C	3	VREF1_3
W5	PR69B	3	
V5	PR69A	3	
V7	PR66D	3	PCLKC3_2
U7	PR66C	3	PCLKT3_2
T1	PR66B	3	
R1	PR66A	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
D9	B_VDDIB2_R	-	
E12	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
F12	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
K11	VCC12	-	
A13	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D12	B_VDDOB2_R	-	
B13	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D13	B_VDDOB3_R	-	
B14	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
L11	VCC12	-	
A14	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
F13	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
E13	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
G13	VCC12	-	
E9	B_VDDIB3_R	-	
L13	VCC12	-	
J11	B_REFCLKN_R	-	
H11	B_REFCLKP_R	-	
M15	PT93D	1	HDC/SI
M16	PT93C	1	LDCN/SCS
F14	PT93B	1	D8/MPI_DATA8
G14	PT93A	1	CS1/MPI_CS1
L15	PT90D	1	D9/MPI_DATA9
L14	PT90C	1	D10/MPI_DATA10
D14	PT90B	1	CS0N/MPI_CS0N
E14	PT90A	1	RDN/MPI_STRB_N
L16	PT89D	1	WRN/MPI_WR_N
K16	PT89C	1	D7/MPI_DATA7
G15	PT89B	1	D6/MPI_DATA6
F15	PT89A	1	D5/MPI_DATA5
K14	PT87D	1	D4/MPI_DATA4
K13	PT87C	1	D3/MPI_DATA3
B15	PT87B	1	D2/MPI_DATA2
A15	PT87A	1	D1/MPI_DATA1
J14	PT86D	1	D16/PCLKC1_3/MPI_DATA16
H14	PT86C	1	D17/PCLKT1_3/MPI_DATA17
A16	PT86B	1	D0/MPI_DATA0
B16	PT86A	1	QOUT/CEON
J13	PT83D	1	VREF2_1
H13	PT83C	1	D18/MPI_DATA18
D15	PT83B	1	DOUT
E15	PT83A	1	MCA_DONE_IN
J16	PT81D	1	D19/PCLKC1_2/MPI_DATA19

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
L21	PT55D	1	A16/MPI_ADDR30
L20	PT55C	1	D13/MPI_DATA13
D20	PT55B	1	A15/MPI_ADDR29
E20	PT55A	1	A17/MPI_ADDR31
L19	PT54D	1	A19/MPI_TSI21
K19	PT54C	1	A20/MPI_BDIP
D21	PT54B	1	A18/MPI_TSI20
E21	PT54A	1	MPI_TEA
M20	PT51D	1	D14/MPI_DATA14
M19	PT51C	1	DP1/MPI_PAR1
F21	PT51B	1	A21/MPI_BURST
G21	PT51A	1	D15/MPI_DATA15
H24	B_REFCLKP_L	-	
J24	B_REFCLKN_L	-	
L22	VCC12	-	
E26	B_VDDIB3_L	-	
G22	VCC12	-	
E22	B_HDINP3_L	-	PCS 361 CH 3 IN P
F22	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
L24	VCC12	-	
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D22	B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D23	B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
K24	VCC12	-	
F23	B_HDINN2_L	-	PCS 361 CH 2 IN N
E23	B_HDINP2_L	-	PCS 361 CH 2 IN P
D26	B_VDDIB2_L	-	
G23	VCC12	-	
D27	B_VDDIB1_L	-	
G24	VCC12	-	
E24	B_HDINP1_L	-	PCS 361 CH 1 IN P
F24	B_HDINN1_L	-	PCS 361 CH 1 IN N
A23	B_HDOUTP1_L	-	PCS 361 CH 1 OUT P
L25	VCC12	-	
B23	B_HDOUTN1_L	-	PCS 361 CH 1 OUT N
D24	B_VDDOB1_L	-	
B24	B_HDOUTN0_L	-	PCS 361 CH 0 OUT N
D25	B_VDDOB0_L	-	
A24	B_HDOUTP0_L	-	PCS 361 CH 0 OUT P
K25	VCC12	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCI/O Bank	Dual Function	Ball Function	VCCI/O Bank	Dual Function
AY41	PB12A	5		PB13A	5	
BA41	PB12B	5		PB13B	5	
AT39	PB12C	5		PB13C	5	
AT38	PB12D	5		PB13D	5	
AV37	PB13A	5		PB15A	5	
AV36	PB13B	5		PB15B	5	
AM31	PB13C	5		PB15C	5	
AM32	PB13D	5		PB15D	5	
BA40	PB15A	5		PB16A	5	
BB40	PB15B	5		PB16B	5	
AM29	PB15C	5		PB16C	5	
AL29	PB15D	5		PB16D	5	
AY39	PB16A	5		PB17A	5	
AY38	PB16B	5		PB17B	5	
AN33	PB16C	5		PB17C	5	
AN32	PB16D	5		PB17D	5	
BA39	PB17A	5		PB19A	5	
BA38	PB17B	5		PB19B	5	
AT37	PB17C	5		PB19C	5	
AT36	PB17D	5		PB19D	5	
AW36	PB19A	5		PB20A	5	
AW35	PB19B	5		PB20B	5	
AM28	PB19C	5		PB20C	5	
AL28	PB19D	5		PB20D	5	
BB38	PB20A	5		PB21A	5	
BB39	PB20B	5		PB21B	5	
AR34	PB20C	5		PB21C	5	
AR33	PB20D	5		PB21D	5	
AV35	PB21A	5		PB23A	5	
AV34	PB21B	5		PB23B	5	
AT33	PB21C	5		PB23C	5	
AT34	PB21D	5		PB23D	5	
BA37	PB23A	5		PB25A	5	
BA36	PB23B	5		PB25B	5	
AP33	PB23C	5		PB25C	5	
AP32	PB23D	5		PB25D	5	
AY36	PB24A	5		PB26A	5	
AY35	PB24B	5		PB26B	5	
AN31	PB24C	5		PB26C	5	
AN30	PB24D	5		PB26D	5	
BB37	PB25A	5		PB27A	5	
BB36	PB25B	5		PB27B	5	
AP31	PB25C	5		PB27C	5	
AP30	PB25D	5		PB27D	5	
AV33	PB27A	5		PB29A	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
J1	PR25B	2		PR38B	2	
K1	PR25A	2		PR38A	2	
V12	PR24D	2		PR34D	2	
U12	PR24C	2		PR34C	2	
K2	PR24B	2		PR34B	2	
J2	PR24A	2		PR34A	2	
R10	PR22D	2		PR30D	2	
T10	PR22C	2		PR30C	2	
L5	PR22B	2		PR30B	2	
K5	PR22A	2		PR30A	2	
P9	PR21D	2		PR26D	2	
N9	PR21C	2		PR26C	2	
L6	PR21B	2		PR26B	2	
K6	PR21A	2		PR26A	2	
M8	PR20D	2		PR19D	2	
M9	PR20C	2		PR19C	2	
H1	PR20B	2		PR19B	2	
G1	PR20A	2		PR19A	2	
U14	PR18D	2	VREF2_2	PR18D	2	VREF2_2
T14	PR18C	2		PR18C	2	
H2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
G2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
H3	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
G3	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
R11	PR16D	2		PR15D	2	
P11	PR16C	2		PR15C	2	
J5	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
J6	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
P18	VCCJ	-		VCCJ	-	
P19	TDO	-	TDO	TDO	-	TDO
R21	TMS	-		TMS	-	
P20	TCK	-		TCK	-	
P12	TDI	-		TDI	-	
P17	PROGRAMN	1		PROGRAMN	1	
P21	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
P13	CCLK	1		CCLK	1	
H10	RESP_URC	-		RESP_URC	-	
N13	VCC12	-		VCC12	-	
H9	A_REFCLKN_R	-		A_REFCLKN_R	-	
G9	A_REFCLKP_R	-		A_REFCLKP_R	-	
F2	VCC12	-		VCC12	-	
H4	A_VDDIB0_R	-		A_VDDIB0_R	-	
C1	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-7FC1152C ¹	-7	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-7FC1704C ¹	-7	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-7FC1152C ¹	-7	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FC1704C ¹	-7	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FC1152C ¹	-6	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-5FC1152C ¹	-5	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-6FF1152C	-6	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-5FF1152C	-5	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-6FC1704C ¹	-6	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-5FC1704C ¹	-5	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-6FF1704C	-6	Organic fcBGA	1704	COM	115.2
LFSC3GA115E-5FF1704C	-5	Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA40E-7FFN1020C ¹	-7	Lead-Free Organic fcBGA	1020	COM	40.4
LFSC3GA40E-6FFN1020C ¹	-6	Lead-Free Organic fcBGA	1020	COM	40.4
LFSC3GA40E-5FFN1020C ¹	-5	Lead-Free Organic fcBGA	1020	COM	40.4
LFSC3GA40E-7FFAN1020C	-7	Lead-Free Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-6FFAN1020C	-6	Lead-Free Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-5FFAN1020C	-5	Lead-Free Organic fcBGA Revision 2	1020	COM	40.4
LFSC3GA40E-7FCN1152C ²	-7	Lead-Free Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-6FCN1152C ²	-6	Lead-Free Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-5FCN1152C ²	-5	Lead-Free Ceramic fcBGA	1152	COM	40.4
LFSC3GA40E-7FFN1152C	-7	Lead-Free Organic fcBGA	1152	COM	40.4
LFSC3GA40E-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	40.4
LFSC3GA40E-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

2. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-7FFN1020C ¹	-7	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-6FFN1020C ¹	-6	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-5FFN1020C ¹	-5	Organic fcBGA	1020	COM	40.4
LFSCM3GA40EP1-7FFAN1020C	-7	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-6FFAN1020C	-6	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-5FFAN1020C	-5	Organic fcBGA Revision 2	1020	COM	40.4
LFSCM3GA40EP1-7FCN1152C ²	-7	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FCN1152C ²	-6	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FCN1152C ²	-5	Ceramic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-7FFN1152C	-7	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-6FFN1152C	-6	Organic fcBGA	1152	COM	40.4
LFSCM3GA40EP1-5FFN1152C	-5	Organic fcBGA	1152	COM	40.4

1. Converted to organic flip-chip BGA package revision 2 per [PCN #02A-10](#).

2. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FCN1152I ¹	-6	Lead-Free Ceramic fcBGA	1152	IND	115.2
LFSC3GA115E-5FCN1152I ¹	-5	Lead-Free Ceramic fcBGA	1152	IND	115.2
LFSC3GA115E-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	115.2
LFSC3GA115E-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	115.2
LFSC3GA115E-6FCN1704I ¹	-6	Lead-Free Ceramic fcBGA	1704	IND	115.2
LFSC3GA115E-5FCN1704I ¹	-5	Lead-Free Ceramic fcBGA	1704	IND	115.2
LFSC3GA115E-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	115.2
LFSC3GA115E-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FCN1152I ¹	-6	Lead-Free Ceramic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-5FCN1152I ¹	-5	Lead-Free Ceramic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-6FCN1704I ¹	-6	Lead-Free Ceramic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-5FCN1704I ¹	-5	Lead-Free Ceramic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).