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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	10000
Number of Logic Elements/Cells	40000
Total RAM Bits	4075520
Number of I/O	562
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1020-BBGA, FCBGA
Supplier Device Package	1020-OFcBGA Rev 2 (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga40ep1-7ffa1020c

PURESPEED I/O Buffer Banks

LatticeSC devices have seven PURESPEED I/O buffer banks; each is capable of supporting multiple I/O standards. Each PURESPEED I/O bank has its own I/O supply voltage (V_{CCIO}), and two voltage references V_{REF1} and V_{REF2} resources allowing each bank to be completely independent from each other. Figure 2-26 shows the seven banks and their associated supplies. Table 2-7 lists the maximum number of I/Os per bank for the whole LatticeSC family.

In the LatticeSC devices, single-ended output buffers and ratioed input buffers (LVTTTL, LVCMOS, PCI33 and PCIX33) are powered using V_{CCIO} . In addition to the bank V_{CCIO} supplies, the LatticeSC devices have a V_{CC} core logic power supply, and a V_{CCAUX} supply that power all differential and referenced buffers. V_{CCAUX} also powers a predriver of single-ended output buffers to enhance buffer performance.

Each bank can support up to two separate VREF voltages, VREF1 and VREF2 that set the threshold for the referenced input buffers. In the LatticeSC devices any I/O pin in a bank can be configured to be a dedicated reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Differential drivers have user selectable internal or external bias. External bias is brought in by the VREF1 pin in the bank. External bias for differential buffers is needed for applications that requires tighter than standard output common mode range.

Since a bank can have only one external bias circuit for differential drivers, LVDS and RSDS differential outputs can be mixed in a bank.

If a differential driver is configured in a bank, one pin in that bank becomes a DIFFR pin. This DIFFR pin must be connected to ground via an external 1K +/-1% ohm resistor. Note that differential drivers are not supported in banks 1, 4 and 5.

In addition, there are dedicated Terminating Supply (V_{TT}) pins to be used as terminating voltage for one of the two ways to perform parallel terminations. These V_{TT} pins are available in banks 2-7, these pins are not available in some packages. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.

There are further restrictions on the use of V_{TT} pins, for additional details refer to technical information at the end of this data sheet.

PCI Specification, Revision 2.2 requires the use of clamping diodes for 3.3V operation. For more information on the PCI interface, please refer to the PCI Specification, Revision 2.2.

Programmable Slew Rate Control

All output and bidirectional buffers have an optional programmable output slew rate control that can be configured for either low noise or high-speed performance. Each I/O pin has an individual slew rate control. This allows designers to specify slew rate control on a pin-by-pin basis. This slew rate control affects both the rising and falling edges.

Programmable Termination

Many of the I/O standards supported by the LatticeSC devices require termination at the transmitter, receiver or both. The SC devices provide the capability to implement many kinds of termination on-chip, minimizing stub lengths and hence improving performance. Utilizing this feature also has the benefit of reducing the number of discrete components required on the circuit board. The termination schemes can be split into two categories single-ended and differential.

Single Ended Termination

Single Ended Outputs: The SC devices support a number of different terminations for single ended outputs:

- Series
- Parallel to V_{CCIO} or GND
- Parallel to $V_{CCIO}/2$
- Parallel to $V_{CCIO}/2$ combined with series

Figure 2-27 shows the single ended output schemes that are supported. The nominal values of the termination resistors are shown in Table 2-10.

Density Shifting

The LatticeSC family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

PURESPEED I/O Differential Electrical Characteristics**LVDS****Over Recommended Operating Conditions**

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input voltage		0	—	2.4	V
V_{THD}	Differential input threshold (Q- \bar{Q})		+/-100	—	—	mV
V_{CM}	Input common mode voltage		0.05	1.2	2.35	V
I_{IN}	Input current	Power on or power off	—	—	+/-10	μ A
V_{OH}	Output high voltage for V_{OP} or V_{OM}	$R_T = 100$ Ohm	—	1.38	1.60	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	$R_T = 100$ Ohm	0.9V	1.03	—	V
V_{OD}	Output voltage differential	$(V_{OP} - V_{OM}), R_T = 100$ Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	$(V_{OP} - V_{OM})/2, R_T = 100$ Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{SAB}	Output short circuit current	$V_{OD} = 0V$ Driver outputs shorted	—	—	12	mA
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	500	ps	T_R, T_F

Notes:

1. Data is for 3.5mA differential current drive. Other differential driver current options are available.
2. If the low power mode of the input buffer is used, the minimum V_{CM} is 600 mV.

Mini-LVDS**Over Recommended Operating Conditions**

Parameter Symbol	Description	Min.	Typ.	Max.	Units
Z_O	Single-ended PCB trace impedance	30	50	75	ohms
R_T	Differential termination resistance	60	100	150	ohms
V_{OD}	Output voltage, differential, $ V_{OP} - V_{OM} $	300	—	600	mV
V_{OS}	Output voltage, common mode, $ V_{OP} + V_{OM} /2$	1	1.2	1.4	V
ΔV_{OD}	Change in V_{OD} , between H and L	—	—	50	mV
ΔV_{ID}	Change in V_{OS} , between H and L	—	—	50	mV
V_{THD}	Input voltage, differential, $ V_{INP} - V_{INM} $	200	—	600	mV
V_{CM}	Input voltage, common mode, $ V_{INP} + V_{INM} /2$	$0.3+(V_{THD}/2)$	—	$2.1-(V_{THD}/2)$	
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	500	ps
T_{ODUTY}	Output clock duty cycle	45	—	55	%
T_{IDUTY}	Input clock duty cycle	40	—	60	%

Note: Data is for 6mA differential current drive. Other differential driver current options are available.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
MPI_STRBN	I	Driven active low indicates the start of a transaction on the PowerPC bus. MPI will strobe the address bus at next rising edge of clock.
MPI_ADDR[31:14]	I	Address bus driven by a PowerPC bus master. Only 18-bit width is needed. It has to be the least significant bit of the PowerPC 32-bit address A[31:14].
MPI_DAT[n:0]	I/O	Selectable data bus width from 8, and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction.
MPI_PAR[m:0]	I/O	Selectable parity bus width from 1, 2, and 3-bit. MPI_DP[0] for MPI_D[7:0], MPI_DP[1] for MPI_D[15:8] and MPI_DP[2] for MPI_D[23:16].
MPI_TA	O	Transfer acknowledge. Driven active low indicates that MPI received the data on the write cycle or returned data on the read cycle.
MPI_TEA	O	Transfer Error Acknowledge. Driven active low indicates that MPI detects a bus error on the internal system bus for current transaction.
MPI_RETRY	O	Active low MPI Retry requests the MPC860 to relinquish the bus and retry the cycle.
Multi-chip Alignment (User I/O if not used.)		
MCA_DONE_OUT	O	Multi-chip alignment done output (to second MCA chip)
MCA_DONE_IN	I	Multi-chip alignment done input (from second MCA chip)
MCA_CLK_P[1:2]_OUT	O	Multi-chip alignment clock [1:2] output (sourced by MCA master chip)
MCA_CLK_P[1:2]_IN	I	Multi-chip alignment clock [1:2] input (from MCA master chip)
TEMP	—	Temperature sensing diode pin. Dedicated pin. Accuracy is typically +/- 10°C.
Miscellaneous Dedicated Pins		
XRES	—	External reference resistor between this pin and ground. The reference resistor is used to calibrate the programmable terminating resistors used in the I/Os. Dedicated pin. Value: 1K ± 1% ohm.
DIFFRx	—	Only used if a differential driver is used in a bank. This DIFFRx must be connected to ground via an external 1K ±1% ohm resistor for all banks that have a differential driver.
SERDES Block (Dedicated Pins)		
[A:D]_HDINPx_[L/R]	I	High-speed input (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDINNx_[L/R]	I	High-speed input (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTPx_[L/R]	O	High-speed output (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTNx_[L/R]	O	High-speed output (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_REFCLKP_[L/R]	I	Ref clock input (positive), aux channel on left [L] or right [R] side of device.
[A:D]_REFCLKN_[L/R]	I	Ref clock input (negative), aux channel on left [L] or right [R] side of device.

LFSC/M15 Logic Signal Connections: 256 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
J9	VCC	-	
K8	VCC	-	
F6	VCC12	-	
F11	VCC12	-	
L11	VCC12	-	
L6	VCC12	-	
K7	VCC12	-	
K10	VCC12	-	
F10	VCCAUX	-	
F7	VCCAUX	-	
T1	GND	-	
G11	VCCAUX	-	
K11	VCCAUX	-	
L10	VCCAUX	-	
L9	VCCAUX	-	
L7	VCCAUX	-	
L8	VCCAUX	-	
T16	GND	-	
G6	VCCAUX	-	
K6	VCCAUX	-	
B13	VCCIO1	-	
D11	VCCIO1	-	
D14	VCCIO1	-	
F12	VCCIO2	-	
G15	VCCIO2	-	
K14	VCCIO3	-	
N15	VCCIO3	-	
M11	VCCIO4	-	
P13	VCCIO4	-	
R10	VCCIO4	-	
N6	VCCIO5	-	
P7	VCCIO5	-	
R4	VCCIO5	-	
K2	VCCIO6	-	
N3	VCCIO6	-	
F4	VCCIO7	-	
G3	VCCIO7	-	
D4	VCC12	-	
D7	VCC12	-	
D5	VCC12	-	
D6	VCC12	-	

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
 2. The LatticeSC/M15 in a 256-pin package does not support an MPI interface.

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH20	NC	-		PB51D	4	
AK27	NC	-		NC	-	
AJ24	NC	-		NC	-	
AF17	NC	-		PB42C	4	
AH27	NC	-		PB61B	4	
AD23	NC	-		PB57A	4	
AE23	NC	-		PB57B	4	
AH24	NC	-		PB59A	4	
AH25	NC	-		PB59B	4	
AH26	NC	-		PB61A	4	
AF24	NC	-		PB63A	4	
AG24	NC	-		PB63B	4	
AG25	NC	-		PB64A	4	
AF25	NC	-		PB64B	4	
AG26	NC	-		PB65A	4	
AF27	NC	-		PB65B	4	
AD28	NC	-		PR56B	3	
AC27	NC	-		PR56A	3	
AE29	NC	-		PR53B	3	
AD29	NC	-		PR53A	3	
AB30	NC	-		NC	-	
AA28	NC	-		NC	-	
Y27	NC	-		PR47C	3	
W27	NC	-		PR47D	3	
V30	NC	-		PR47A	3	
W30	NC	-		PR47B	3	
W26	NC	-		PR43D	3	
V26	NC	-		PR43C	3	
U25	NC	-		PR42C	3	
T27	NC	-		PR40B	3	
R27	NC	-		PR40A	3	
V27	NC	-		PR39B	3	
U27	NC	-		PR39A	3	
U29	NC	-		PR36B	3	
T29	NC	-		PR36A	3	
T24	NC	-		PR35C	3	
Y25	NC	-		PR48C	3	
P24	NC	-		NC	-	
K28	NC	-		NC	-	
P23	NC	-		NC	-	
L28	NC	-		NC	-	
M27	NC	-		PR21B	2	
L27	NC	-		PR21A	2	
H27	NC	-		PR20B	2	
G27	NC	-		PR20A	2	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
Y6	PR42D	3	DIFFR_3	PR51D	3	DIFFR_3
W6	PR42C	3		PR51C	3	
Y2	PR42B	3		PR51B	3	
W2	PR42A	3		PR51A	3	
W7	PR40D	3		PR49D	3	
V8	PR40C	3		PR49C	3	
W4	PR40B	3		PR49B	3	
W3	PR40A	3		PR49A	3	
V5	PR39D	3		PR48D	3	
U6	PR39C	3		PR48C	3	
V3	PR39B	3		PR48B	3	
V4	PR39A	3		PR48A	3	
V10	PR38D	3		PR47D	3	
V9	PR38C	3		PR47C	3	
V2	PR38B	3		PR47B	3	
V1	PR38A	3		PR47A	3	
U8	PR36D	3		PR45D	3	
U7	PR36C	3		PR45C	3	
U2	PR36B	3		PR45B	3	
U1	PR36A	3		PR45A	3	
U5	PR35D	3		PR44D	3	
T6	PR35C	3		PR44C	3	
T1	PR35B	3		PR44B	3	
T2	PR35A	3		PR44A	3	
U9	PR34D	3		PR43D	3	
U10	PR34C	3	VREF1_3	PR43C	3	VREF1_3
R1	PR34B	3		PR43B	3	
R2	PR34A	3		PR43A	3	
T7	PR31D	3	PCLKC3_2	PR40D	3	PCLKC3_2
T8	PR31C	3	PCLKT3_2	PR40C	3	PCLKT3_2
R4	PR31B	3		PR40B	3	
R3	PR31A	3		PR40A	3	
T5	PR30D	3	PCLKC3_3	PR39D	3	PCLKC3_3
R5	PR30C	3	PCLKT3_3	PR39C	3	PCLKT3_3
P2	PR30B	3		PR39B	3	
P1	PR30A	3		PR39A	3	
T9	PR29D	3	PCLKC3_1	PR38D	3	PCLKC3_1
T10	PR29C	3	PCLKT3_1	PR38C	3	PCLKT3_1
P4	PR29B	3	PCLKC3_0	PR38B	3	PCLKC3_0
P3	PR29A	3	PCLKT3_0	PR38A	3	PCLKT3_0
P5	PR27D	2	PCLKC2_2	PR36D	2	PCLKC2_2
P6	PR27C	2	PCLKT2_2	PR36C	2	PCLKT2_2
N1	PR27B	2	PCLKC2_0	PR36B	2	PCLKC2_0
N2	PR27A	2	PCLKT2_0	PR36A	2	PCLKT2_0
R9	PR26D	2	PCLKC2_3	PR35D	2	PCLKC2_3
R8	PR26C	2	PCLKT2_3	PR35C	2	PCLKT2_3
M1	PR26B	2	PCLKC2_1	PR35B	2	PCLKC2_1
L1	PR26A	2	PCLKT2_1	PR35A	2	PCLKT2_1
N9	PR25D	2	DIFFR_2	PR23D	2	DIFFR_2
M9	PR25C	2	VREF1_2	PR23C	2	VREF1_2

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH11	PB57D	4		PB79D	4	
AN13	PB58A	4	PCLKT4_3	PB80A	4	PCLKT4_3
AN12	PB58B	4	PCLKC4_3	PB80B	4	PCLKC4_3
AD14	PB58C	4	PCLKT4_4	PB80C	4	PCLKT4_4
AD15	PB58D	4	PCLKC4_4	PB80D	4	PCLKC4_4
AP13	PB61A	4		PB73A	4	
AP12	PB61B	4		PB73B	4	
AK13	PB61C	4		PB73C	4	
AK12	PB61D	4		PB73D	4	
AP11	PB62A	4		PB83A	4	
AP10	PB62B	4		PB83B	4	
AN11	PB63A	4		PB99A	4	
AN10	PB63B	4		PB99B	4	
AF14	PB63C	4		PB99C	4	
AF13	PB63D	4		PB99D	4	
AM10	PB67A	4		PB101A	4	
AM9	PB67B	4		PB101B	4	
AE14	PB67C	4		PB101C	4	
AE13	PB67D	4		PB101D	4	
AP9	PB69A	4		PB104A	4	
AP8	PB69B	4		PB104B	4	
AK11	PB69C	4		PB104C	4	
AK10	PB69D	4		PB104D	4	
AL10	PB70A	4		PB107A	4	
AL9	PB70B	4		PB107B	4	
AF12	PB70C	4		PB107C	4	
AF11	PB70D	4		PB107D	4	
AN9	PB73A	4		PB109A	4	
AN8	PB73B	4		PB109B	4	
AG11	PB73C	4		PB109C	4	
AG10	PB73D	4		PB109D	4	
AP7	PB74A	4		PB111A	4	
AP6	PB74B	4		PB111B	4	
AG13	PB74C	4		PB111C	4	
AG12	PB74D	4		PB111D	4	
AN7	PB75A	4		PB113A	4	
AN6	PB75B	4		PB113B	4	
AK9	PB75C	4		PB113C	4	
AK8	PB75D	4		PB113D	4	
AP5	PB77A	4		PB115A	4	
AP4	PB77B	4		PB115B	4	
AD11	PB77C	4		PB115C	4	
AE11	PB77D	4		PB115D	4	
AM7	PB78A	4		PB117A	4	
AM6	PB78B	4		PB117B	4	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
H21	PT38D	1	D28/PCLKC1_6/MPI_DATA28	PT57D	1	D28/PCLKC1_6/MPI_DATA28
J21	PT38C	1	D29/PCLKT1_6/MPI_DATA29	PT57C	1	D29/PCLKT1_6/MPI_DATA29
A19	PT38B	1	A9/MPI_ADDR23	PT57B	1	A9/MPI_ADDR23
B19	PT38A	1	A10/MPI_ADDR24	PT57A	1	A10/MPI_ADDR24
H22	PT37D	1	D30/PCLKC1_7/MPI_DATA30	PT56D	1	D30/PCLKC1_7/MPI_DATA30
J22	PT37C	1	D31/PCLKT1_7/MPI_DATA31	PT56C	1	D31/PCLKT1_7/MPI_DATA31
F20	PT37B	1	A11/MPI_ADDR25	PT56B	1	A11/MPI_ADDR25
G20	PT37A	1	A12/MPI_ADDR26	PT56A	1	A12/MPI_ADDR26
K21	PT35D	1	D11/MPI_DATA11	PT55D	1	D11/MPI_DATA11
K22	PT35C	1	D12/MPI_DATA12	PT55C	1	D12/MPI_DATA12
A20	PT35B	1	A13/MPI_ADDR27	PT55B	1	A13/MPI_ADDR27
B20	PT35A	1	A14/MPI_ADDR28	PT55A	1	A14/MPI_ADDR28
L21	PT33D	1	A16/MPI_ADDR30	PT53D	1	A16/MPI_ADDR30
L20	PT33C	1	D13/MPI_DATA13	PT53C	1	D13/MPI_DATA13
D20	PT33B	1	A15/MPI_ADDR29	PT53B	1	A15/MPI_ADDR29
E20	PT33A	1	A17/MPI_ADDR31	PT53A	1	A17/MPI_ADDR31
L19	PT30D	1	A19/MPI_TSIZ1	PT52D	1	A19/MPI_TSIZ1
K19	PT30C	1	A20/MPI_BDIP	PT52C	1	A20/MPI_BDIP
D21	PT30B	1	A18/MPI_TSIZ0	PT52B	1	A18/MPI_TSIZ0
E21	PT30A	1	MPI_TEA	PT52A	1	MPI_TEA
M20	PT28D	1	D14/MPI_DATA14	PT51D	1	D14/MPI_DATA14
M19	PT28C	1	DP1/MPI_PAR1	PT51C	1	DP1/MPI_PAR1
F21	PT27B	1	A21/MPI_BURST	PT51B	1	A21/MPI_BURST
G21	PT27A	1	D15/MPI_DATA15	PT51A	1	D15/MPI_DATA15
H24	B_REFCLKP_L	-		B_REFCLKP_L	-	
J24	B_REFCLKN_L	-		B_REFCLKN_L	-	
L22	VCC12	-		VCC12	-	
E26	B_VDDIB3_L	-		B_VDDIB3_L	-	
G22	VCC12	-		VCC12	-	
E22	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
F22	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
L24	VCC12	-		VCC12	-	
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D22	B_VDDOB3_L	-		B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D23	B_VDDOB2_L	-		B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
K24	VCC12	-		VCC12	-	
F23	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
E23	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
D26	B_VDDIB2_L	-		B_VDDIB2_L	-	
G23	VCC12	-		VCC12	-	
D27	B_VDDIB1_L	-		B_VDDIB1_L	-	
G24	VCC12	-		VCC12	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1,2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
G27	A_REFCLKP_L	-	
H27	A_REFCLKN_L	-	
H25	VCC12	-	
H26	RESP_ULC	-	
B33	RESETN	1	
C34	TSALLN	1	
D34	DONE	1	
C33	INITN	1	
J27	M0	1	
K27	M1	1	
M26	M2	1	
L26	M3	1	
F30	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
G30	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
H28	PL15C	7	
J28	PL15D	7	
F31	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
G31	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N25	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P25	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
D33	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
E33	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
H29	PL18C	7	
J29	PL18D	7	VREF2_7
F32	PL19A	7	
G32	PL19B	7	
P26	PL19C	7	
N26	PL19D	7	
H30	PL26A	7	
J30	PL26B	7	
L28	PL26C	7	
M28	PL26D	7	
J31	PL43A	7	
K31	PL43B	7	
L27	PL43C	7	VREF1_7
M27	PL43D	7	DIFFR_7
J32	PL45A	7	
K32	PL45B	7	
L29	PL45C	7	
M29	PL45D	7	
H33	PL47A	7	
J33	PL47B	7	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AP27	PB26A	5	
AP26	PB26B	5	
AK25	PB26C	5	
AK24	PB26D	5	
AN25	PB29A	5	
AN24	PB29B	5	
AE22	PB29C	5	
AE21	PB29D	5	
AM26	PB31A	5	
AM25	PB31B	5	
AF22	PB31C	5	
AF21	PB31D	5	
AN23	PB47A	5	
AN22	PB47B	5	
AP23	PB57A	5	
AP22	PB57B	5	
AG21	PB57C	5	
AG20	PB57D	5	
AP25	PB50A	5	PCLKT5_3
AP24	PB50B	5	PCLKC5_3
AD21	PB50C	5	PCLKT5_4
AD20	PB50D	5	PCLKC5_4
AL23	PB51A	5	PCLKT5_5
AL22	PB51B	5	PCLKC5_5
AH24	PB51C	5	
AH23	PB51D	5	
AM23	PB53A	5	PCLKT5_0
AM22	PB53B	5	PCLKC5_0
AJ24	PB53C	5	
AJ23	PB53D	5	VREF2_5
AN21	PB54A	5	PCLKT5_1
AN20	PB54B	5	PCLKC5_1
AE19	PB54C	5	PCLKT5_6
AD19	PB54D	5	PCLKC5_6
AK21	PB55A	5	PCLKT5_2
AK20	PB55B	5	PCLKC5_2
AK23	PB55C	5	PCLKT5_7
AK22	PB55D	5	PCLKC5_7
AL20	PB58A	5	
AL19	PB58B	5	
AG19	PB58C	5	
AF19	PB58D	5	
AP21	PB61A	5	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1,2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
V8	PR65D	3	PCLKC3_3
U8	PR65C	3	PCLKT3_3
U5	PR65B	3	
T5	PR65A	3	
V6	PR64D	3	PCLKC3_1
U6	PR64C	3	PCLKT3_1
T4	PR64B	3	PCLKC3_0
T3	PR64A	3	PCLKT3_0
U9	PR62D	2	PCLKC2_2
T9	PR62C	2	PCLKT2_2
R2	PR62B	2	PCLKC2_0
P2	PR62A	2	PCLKT2_0
T11	PR61D	2	PCLKC2_3
U11	PR61C	2	PCLKT2_3
R4	PR61B	2	PCLKC2_1
R3	PR61A	2	PCLKT2_1
T8	PR60D	2	
R8	PR60C	2	
P1	PR60B	2	
N1	PR60A	2	
R6	PR57D	2	
P6	PR57C	2	
M1	PR57B	2	
L1	PR57A	2	
T10	PR56D	2	
U10	PR56C	2	
N2	PR56B	2	
M2	PR56A	2	
R11	PR51D	2	
P11	PR51C	2	
N4	PR51B	2	
M4	PR51A	2	
N5	PR49D	2	
M5	PR49C	2	
L2	PR49B	2	
K2	PR49A	2	
P8	PR47D	2	
N8	PR47C	2	
J2	PR47B	2	
H2	PR47A	2	
M6	PR45D	2	
L6	PR45C	2	
K3	PR45B	2	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
F25	B_HDINN0_L	-	PCS 361 CH 0 IN N
E25	B_HDINP0_L	-	PCS 361 CH 0 IN P
D28	B_VDDIB0_L	-	
G25	VCC12	-	
D29	A_VDDIB3_L	-	
C25	VCC12	-	
A25	A_HDINP3_L	-	PCS 360 CH 3 IN P
B25	A_HDINN3_L	-	PCS 360 CH 3 IN N
A26	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
E27	VCC12	-	
B26	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
F26	A_VDDOB3_L	-	
B27	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
F27	A_VDDOB2_L	-	
A27	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
E28	VCC12	-	
B28	A_HDINN2_L	-	PCS 360 CH 2 IN N
A28	A_HDINP2_L	-	PCS 360 CH 2 IN P
D30	A_VDDIB2_L	-	
C28	VCC12	-	
D31	A_VDDIB1_L	-	
C29	VCC12	-	
A29	A_HDINP1_L	-	PCS 360 CH 1 IN P
B29	A_HDINN1_L	-	PCS 360 CH 1 IN N
A30	A_HDOUTP1_L	-	PCS 360 CH 1 OUT P
E29	VCC12	-	
B30	A_HDOUTN1_L	-	PCS 360 CH 1 OUT N
F28	A_VDDOB1_L	-	
B31	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
F29	A_VDDOB0_L	-	
A31	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
E30	VCC12	-	
B32	A_HDINN0_L	-	PCS 360 CH 0 IN N
A32	A_HDINP0_L	-	PCS 360 CH 0 IN P
D32	A_VDDIB0_L	-	
C32	VCC12	-	
E34	PL30A	7	
F34	PL30B	7	
F33	PL34A	7	
G33	PL34B	7	
K30	PL38A	7	
L30	PL38B	7	
G34	PL40A	7	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
Y18	VCC	-	
Y20	VCC	-	
AB15	VCC12	-	
AB20	VCC12	-	
N15	VCC12	-	
N20	VCC12	-	
R13	VCC12	-	
R22	VCC12	-	
Y13	VCC12	-	
Y22	VCC12	-	
AA12	VCCAUX	-	
AA23	VCCAUX	-	
AB12	VCCAUX	-	
AB16	VCCAUX	-	
AB17	VCCAUX	-	
AB18	VCCAUX	-	
AB19	VCCAUX	-	
AB23	VCCAUX	-	
AC12	VCCAUX	-	
AC13	VCCAUX	-	
Y19	GND	-	
AC14	VCCAUX	-	
AC17	VCCAUX	-	
AC21	VCCAUX	-	
AC22	VCCAUX	-	
AC23	VCCAUX	-	
M13	VCCAUX	-	
M14	VCCAUX	-	
M18	VCCAUX	-	
M21	VCCAUX	-	
M22	VCCAUX	-	
N12	VCCAUX	-	
N16	VCCAUX	-	
N17	VCCAUX	-	
N18	VCCAUX	-	
N19	VCCAUX	-	
N23	VCCAUX	-	
P12	VCCAUX	-	
P23	VCCAUX	-	
T13	VCCAUX	-	
T22	VCCAUX	-	
U12	VCCAUX	-	
U13	VCCAUX	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AF40	PL76A	6		PL90A	6	
AG40	PL76B	6		PL90B	6	
AG36	PL76C	6		PL90C	6	
AH36	PL76D	6	DIFFR_6	PL90D	6	DIFFR_6
AF39	PL77A	6		PL91A	6	
AG39	PL77B	6		PL91B	6	
AF29	PL77C	6		PL91C	6	
AG29	PL77D	6		PL91D	6	
AH42	PL78A	6		PL92A	6	
AG42	PL78B	6		PL92B	6	
AG35	PL78C	6		PL92C	6	
AH35	PL78D	6		PL92D	6	
AG41	PL80A	6		PL94A	6	
AH41	PL80B	6		PL94B	6	
AG34	PL80C	6		PL94C	6	
AH34	PL80D	6		PL94D	6	
AJ42	PL81A	6		PL96A	6	
AK42	PL81B	6		PL96B	6	
AG33	PL81C	6		PL96C	6	
AH33	PL81D	6		PL96D	6	
AJ41	PL82A	6		PL98A	6	
AK41	PL82B	6		PL98B	6	
AJ37	PL82C	6		PL98C	6	
AK37	PL82D	6		PL98D	6	
AJ40	PL84A	6		PL99A	6	
AK40	PL84B	6		PL99B	6	
AJ34	PL84C	6		PL99C	6	
AK34	PL84D	6		PL99D	6	
AJ38	PL85A	6		PL103A	6	
AK38	PL85B	6		PL103B	6	
AH32	PL85C	6		PL103C	6	
AJ32	PL85D	6		PL103D	6	
AL42	PL86A	6		PL104A	6	
AM42	PL86B	6		PL104B	6	
AK36	PL86C	6		PL104C	6	
AL36	PL86D	6		PL104D	6	
AL38	PL89A	6		PL107A	6	
AM38	PL89B	6		PL107B	6	
AJ33	PL89C	6		PL107C	6	
AK33	PL89D	6	VREF2_6	PL107D	6	VREF2_6
AN42	PL90A	6		PL109A	6	
AP42	PL90B	6		PL109B	6	
AH31	PL90C	6		PL109C	6	
AJ31	PL90D	6		PL109D	6	
AN41	PL91A	6		PL112A	6	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AP26	PB41C	5		PB43C	5	
AN26	PB41D	5		PB43D	5	
AY30	PB43A	5		PB45A	5	
AY29	PB43B	5		PB45B	5	
AU30	PB43C	5		PB45C	5	
AU31	PB43D	5		PB45D	5	
AV27	PB44A	5		PB46A	5	
AV26	PB44B	5		PB46B	5	
AT28	PB44C	5		PB46C	5	
AT27	PB44D	5		PB46D	5	
BA29	PB45A	5		PB47A	5	
BA28	PB45B	5		PB47B	5	
AL25	PB45C	5		PB47C	5	
AM25	PB45D	5		PB47D	5	
BB29	PB47A	5		PB49A	5	
BB28	PB47B	5		PB49B	5	
AN25	PB47C	5		PB49C	5	
AP25	PB47D	5		PB49D	5	
AY27	PB48A	5	PCLKT5_3	PB50A	5	PCLKT5_3
AY26	PB48B	5	PCLKC5_3	PB50B	5	PCLKC5_3
AT25	PB48C	5	PCLKT5_4	PB50C	5	PCLKT5_4
AT24	PB48D	5	PCLKC5_4	PB50D	5	PCLKC5_4
AW27	PB49A	5	PCLKT5_5	PB51A	5	PCLKT5_5
AW26	PB49B	5	PCLKC5_5	PB51B	5	PCLKC5_5
AU29	PB49C	5		PB51C	5	
AU28	PB49D	5		PB51D	5	
BB27	PB51A	5	PCLKT5_0	PB53A	5	PCLKT5_0
BB26	PB51B	5	PCLKC5_0	PB53B	5	PCLKC5_0
AR25	PB51C	5		PB53C	5	
AR24	PB51D	5	VREF2_5	PB53D	5	VREF2_5
BA27	PB52A	5	PCLKT5_1	PB54A	5	PCLKT5_1
BA26	PB52B	5	PCLKC5_1	PB54B	5	PCLKC5_1
AP24	PB52C	5	PCLKT5_6	PB54C	5	PCLKT5_6
AN24	PB52D	5	PCLKC5_6	PB54D	5	PCLKC5_6
AV25	PB53A	5	PCLKT5_2	PB55A	5	PCLKT5_2
AV24	PB53B	5	PCLKC5_2	PB55B	5	PCLKC5_2
AU27	PB53C	5	PCLKT5_7	PB55C	5	PCLKT5_7
AU26	PB53D	5	PCLKC5_7	PB55D	5	PCLKC5_7
BA25	PB55A	5		PB57A	5	
BA24	PB55B	5		PB57B	5	
AU24	PB55C	5		PB57C	5	
AU25	PB55D	5		PB57D	5	
BB24	PB56A	5		PB58A	5	
BB25	PB56B	5		PB58B	5	
AM23	PB56C	5		PB58C	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1,2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB25	VCC	-		VCC	-	
AB26	VCC	-		VCC	-	
AC16	VCC	-		VCC	-	
AC18	VCC	-		VCC	-	
AC20	VCC	-		VCC	-	
AC23	VCC	-		VCC	-	
AC25	VCC	-		VCC	-	
AC27	VCC	-		VCC	-	
AD17	VCC	-		VCC	-	
AD19	VCC	-		VCC	-	
AD21	VCC	-		VCC	-	
AD22	VCC	-		VCC	-	
AD24	VCC	-		VCC	-	
AD26	VCC	-		VCC	-	
AE16	VCC	-		VCC	-	
AE18	VCC	-		VCC	-	
AE20	VCC	-		VCC	-	
AE21	VCC	-		VCC	-	
AE22	VCC	-		VCC	-	
AE23	VCC	-		VCC	-	
AE25	VCC	-		VCC	-	
AE27	VCC	-		VCC	-	
AF17	VCC	-		VCC	-	
AF19	VCC	-		VCC	-	
AF21	VCC	-		VCC	-	
AF22	VCC	-		VCC	-	
AF24	VCC	-		VCC	-	
AF26	VCC	-		VCC	-	
AG18	VCC	-		VCC	-	
AG20	VCC	-		VCC	-	
AG23	VCC	-		VCC	-	
AG25	VCC	-		VCC	-	
T18	VCC	-		VCC	-	
T20	VCC	-		VCC	-	
T23	VCC	-		VCC	-	
T25	VCC	-		VCC	-	
U17	VCC	-		VCC	-	
U19	VCC	-		VCC	-	
U21	VCC	-		VCC	-	
U22	VCC	-		VCC	-	
U24	VCC	-		VCC	-	
U26	VCC	-		VCC	-	
V16	VCC	-		VCC	-	
V18	VCC	-		VCC	-	
V20	VCC	-		VCC	-	

Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FC1152I ¹	-6	Ceramic fcBGA	1152	IND	115.2
LFSC3GA115E-5FC1152I ¹	-5	Ceramic fcBGA	1152	IND	115.2
LFSC3GA115E-6FF1152I	-6	Organic fcBGA	1152	IND	115.2
LFSC3GA115E-5FF1152I	-5	Organic fcBGA	1152	IND	115.2
LFSC3GA115E-6FC1704I ¹	-6	Ceramic fcBGA	1704	IND	115.2
LFSC3GA115E-5FC1704I ¹	-5	Ceramic fcBGA	1704	IND	115.2
LFSC3GA115E-6FF1704I	-6	Organic fcBGA	1704	IND	115.2
LFSC3GA115E-5FF1704I	-5	Organic fcBGA	1704	IND	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FC1152I ¹	-6	Ceramic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-5FC1152I ¹	-5	Ceramic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-6FF1152I	-6	Organic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-5FF1152I	-5	Organic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-6FC1704I ¹	-6	Ceramic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-5FC1704I ¹	-5	Ceramic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-6FF1704I	-6	Organic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-5FF1704I	-5	Organic fcBGA	1704	IND	115.2

1. Converted to organic flip-chip BGA package per [PCN #01A-10](#).

Date	Version	Section	Change Summary
December 2011	02.4	DC and Switching Characteristics	Updated JTAG Port Timing Specifications table.