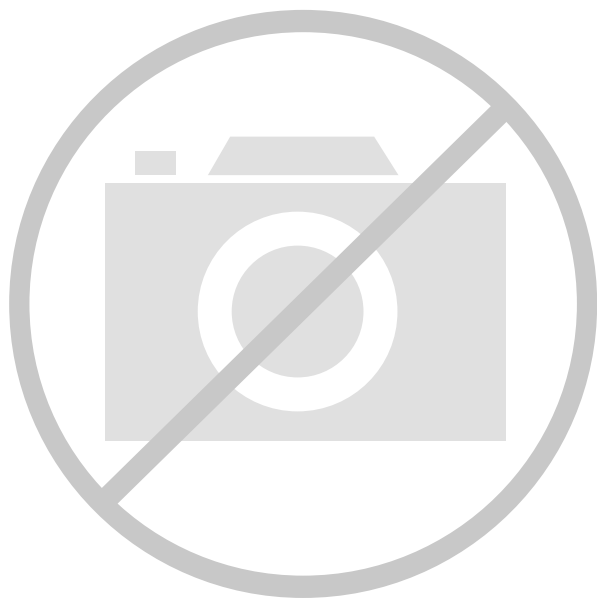




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

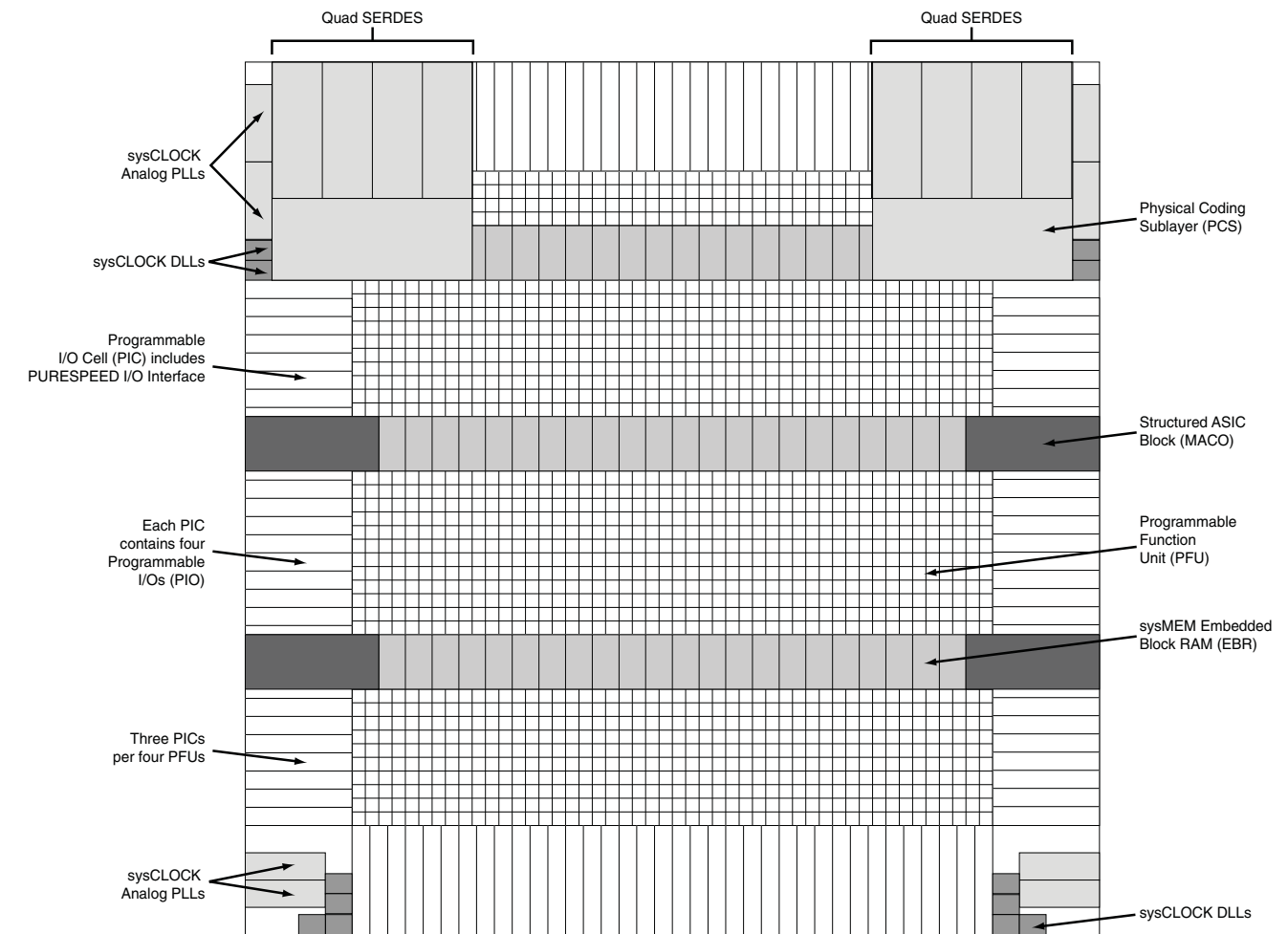
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	20000
Number of Logic Elements/Cells	80000
Total RAM Bits	5816320
Number of I/O	904
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1704-BCBGA, FCBGA
Supplier Device Package	1704-CFCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga80ep1-5fcn1704i

Figure 2-1. Simplified Block Diagram (Top Level)



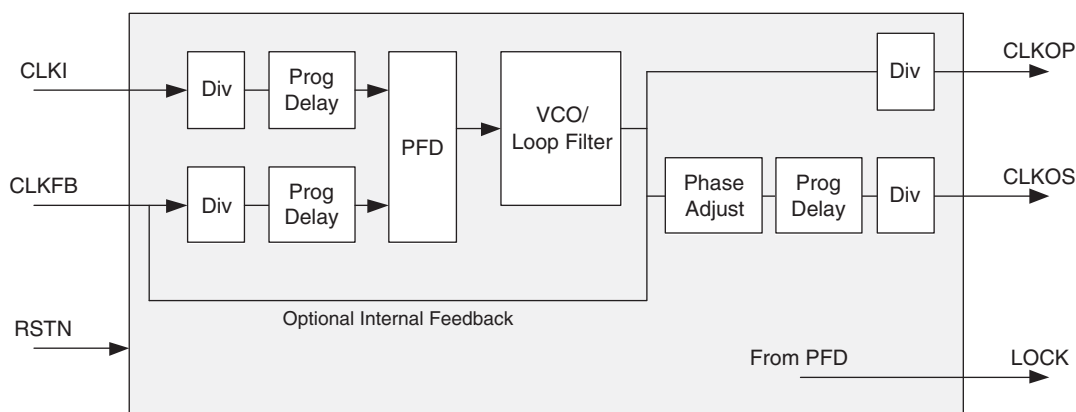
The setup and hold times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock. This delay can be either programmed during configuration or can be adjusted dynamically.

The Phase Select block can modify the phase of the clock signal if desired. The Spread Spectrum block supports the modulation of the PLL output frequency. This reduces the peak energy in the fundamental and its harmonics providing for lower EMI (Electro Magnetic Interference).

The sysCLOCK PLL can be configured at power-up and then, if desired, reconfigured dynamically through the serial memory interface bus which connects with the on-chip system bus. For example, the user can select inputs, loop filters, divider setting, delay settings and phase shift settings. The user can also directly access the SMI bus through the routing.

The PLL clock input, from pin or routing, feeds into an input divider. There are four sources of feedback signal to the feedback divider: from the clock net, directly from the voltage controlled oscillator (VCO) output, from the routing or from an external pin. The signal from the input clock divider and the feedback divider are passed through the programmable delay before entering the phase frequency detector (PFD) unit. The output of this PFD is used to control the voltage controlled oscillator. There is a PLL_LOCK signal to indicate that VCO has locked on to the input clock signal. Figure 2-11 shows the sysCLOCK PLL diagram.

Figure 2-11. PLL Diagram



For more information on the PLL, please see details of additional technical documentation at the end of this data sheet.

Spread Spectrum Clocking (SSC)

The PLL supports spread spectrum clocking to reduce peak EMI by using “down-spread” modulation. The spread spectrum operation will vary the output frequency (at 30KHz to 500KHz) in a range that is between its nominal value, down to a frequency that is a programmable 1%, 2%, or 3% lower than normal.

Digital Locked Loop (DLLs)

In addition to PLLs, the LatticeSC devices have up to 12 DLLs per device. DLLs assist in the management of clocks and strobes. DLLs are well suited to applications where the clock may be stopped or transferring jitter from input to output is important, for example forward clocked interfaces. PLLs are good for applications requiring the lowest output jitter or jitter filtering. All DLL outputs are routed as primary/edge clock sources.

The DLL has two independent clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine phase shift and divider blocks to allow this output to be further modified, if required. The fine phase shift block allows the CLKOS output to be phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. LOCK output signal is asserted when the DLL is locked. The ALU HOLD signal setting allows users to freeze the DLL at its current delay setting.

VDDAX25 needs to be connected independent of the use of the SERDES. This supply is used to control the SERDES CML I/O regardless of the SERDES being used in the design.

Supported Source Synchronous Interfaces

The LatticeSC devices contain a variety of hardware, such as delay elements, DDR registers and PLLs, to simplify the implementation of Source Synchronous interfaces. Table 2-11 lists Source Synchronous and DDR/QDR standards supported in the LatticeSC. For additional detail refer to technical information at the end of the data sheet.

Table 2-11. Source Synchronous Standards Table¹

Source Synchronous Standard	Clocking	Speeds (MHz)	Data Rate (Mbps)
RapidIO	DDR	500	1000
SPI4.2 (POS-PHY4)/NPSI	DDR	500	1000
SFI4/XSBI	DDR SDR	334 667	667
XGMII	DDR	156.25	312
CSIX	SDR	250	250
QDRII/QDRII+ memory interface	DDR	300	600
DDR memory interface	DDR	240	480
DDRII memory interface	DDR	333	667
RLDRAM memory interface	DDR	400	800

1. Memory width is dependent on the system design and limited by the number of I/Os in the device.

flexiPCS™ (Physical Coding Sublayer Block)

flexiPCS Functionality

The LatticeSC family combines a high-performance FPGA fabric, high-performance I/Os and large embedded RAM in a single industry leading architecture. LatticeSC devices also feature up to 32 channels of embedded SERDES with associated Physical Coding Sublayer (PCS) logic. The flexiPCS logic can be configured to support numerous industry standard high-speed data transfer protocols.

Each channel of flexiPCS logic contains dedicated transmit and receive SERDES for high-speed, full-duplex serial data transfers at data rates up to 3.8 Gbps. The PCS logic in each channel can be configured to support an array of popular data protocols including SONET (STS-12/STS-12c, STS-48/STS-48c, and TFI-5 support of 10 Gbps or above), Gigabit Ethernet (compliant to the IEEE 100BASE-X specification), 1.02 or 2.04 Gbps Fibre Channel, PCI-Express, and Serial RapidIO. In addition, the protocol based logic can be fully or partially bypassed in a number of configurations to allow users flexibility in designing their own high-speed data interface.

Protocols requiring data rates above 3.8 Gbps can be accommodated by dedicating either one pair or all four channels in one flexiPCS quad block to one data link. One quad can support full-duplex serial data transfers at data rates up to 15.2 Gbps. A single flexiPCS quad can be configured to support 10Gb Ethernet (with a fully compliant XAUI interface), 10Gb Fibre Channel, and x4 PCI-Express and 4x RapidIO.

The flexiPCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic which can also be geared to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic. Each SERDES pin can be DC coupled independently and can allow for both high-speed and low-speed operation down to DC rates on the same SERDES pin, as required by some Serial Digital Video applications.

The ispLEVER design tools from Lattice support all modes of the flexiPCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow a user to define their own operation. With ispLEVER, the user can define the mode for each quad in a design. Nine modes are currently supported by the ispLEVER design flow:

Internal Logic Analyzer Capability (ispTRACY)

All LatticeSC devices support an internal logic analyzer diagnostic feature. The diagnostic features provide capabilities similar to an external logic analyzer, such as programmable event and trigger condition and deep trace memory. This feature is enabled by Lattice's ispTRACY. The ispTRACY utility is added into the user design at compile time. For additional detail refer to technical information at the end of the data sheet.

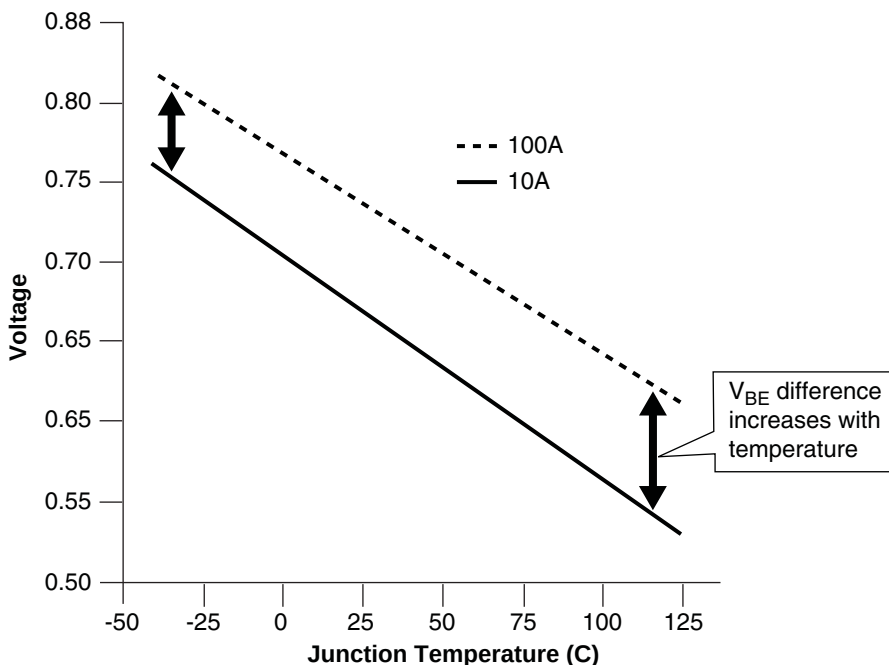
Temperature Sensing

Lattice provides a way to monitor the die temperature by using a temperature-sensing diode that is designed into every LatticeSC device. The difference in V_{BE} of the diode at two different forward currents varies with temperature. This relationship is shown in Figure 2-33. The accuracy of the temperature-sensing diode is typically $\pm 10^{\circ}\text{C}$.

On packages that include PROBE_GND, the most accurate measurements will occur between the TEMP pin and the PROBE_GND pin. On packages that do not include PROBE_GND, measurements should be made between the TEMP pin and board ground.

This temperature-sensing diode is designed to work with an external temperature sensor such as the Maxim 1617A. The Maxim 1617A is configured to measure difference in V_{BE} (of the temperature-sensing diode) at $10\mu\text{A}$ and at $100\mu\text{A}$. This difference in V_{BE} voltage varies with temperature at approximately $1.64\text{ mV}/^{\circ}\text{C}$. A typical device with a 85°C junction temperature will measure approximately 593mV . For additional detail refer to TN1115, [Temperature Sensing Diode in LatticeSC Devices](#).

Figure 2-33. Sensing Diode Typical Characteristics



Oscillator

Every LatticeSC device has an internal CMOS oscillator, which is used as a master serial clock for configuration and is also available as a potential general purpose clock (MCK) for the FPGA core. There is a K divider (divide by 2/4/8/16/32/64/128) available with this oscillator to get lower MCK frequencies. This clock is available as a general purpose clock signal to the software routing tool. For additional detail refer to technical information at the end of the data sheet.

Switching Characteristics

All devices are 100% functionally tested. Listed below are representative values of internal and external timing parameters. For more specific, more precise, and worst-case guaranteed data at a particular temperature and voltage, use the values reported by the static timing analyzer in the ispLEVER design tool from Lattice and back-annotate to the simulation net list.

Figure 3-12. Waveforms First Read after Full Flag

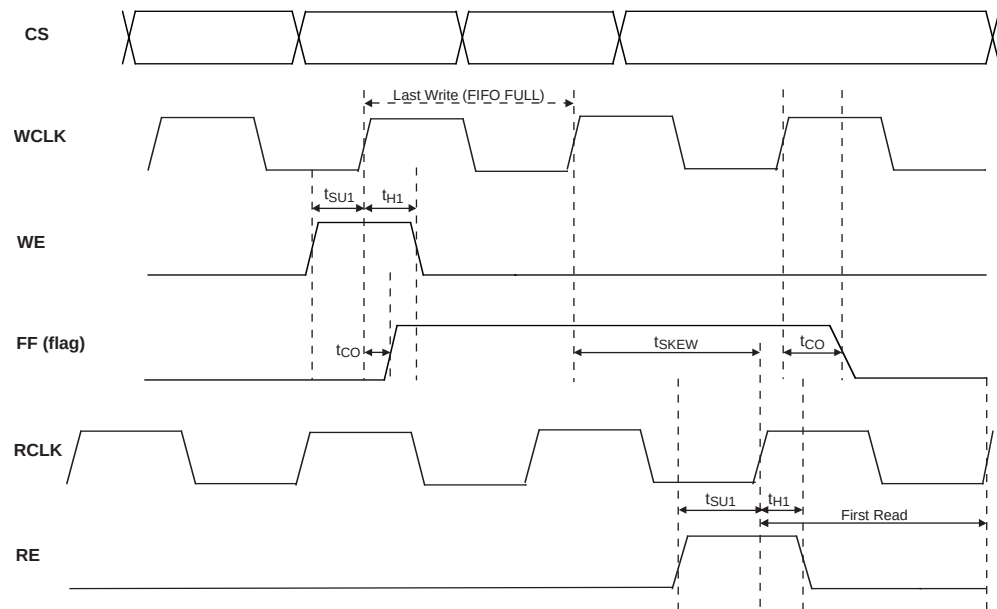
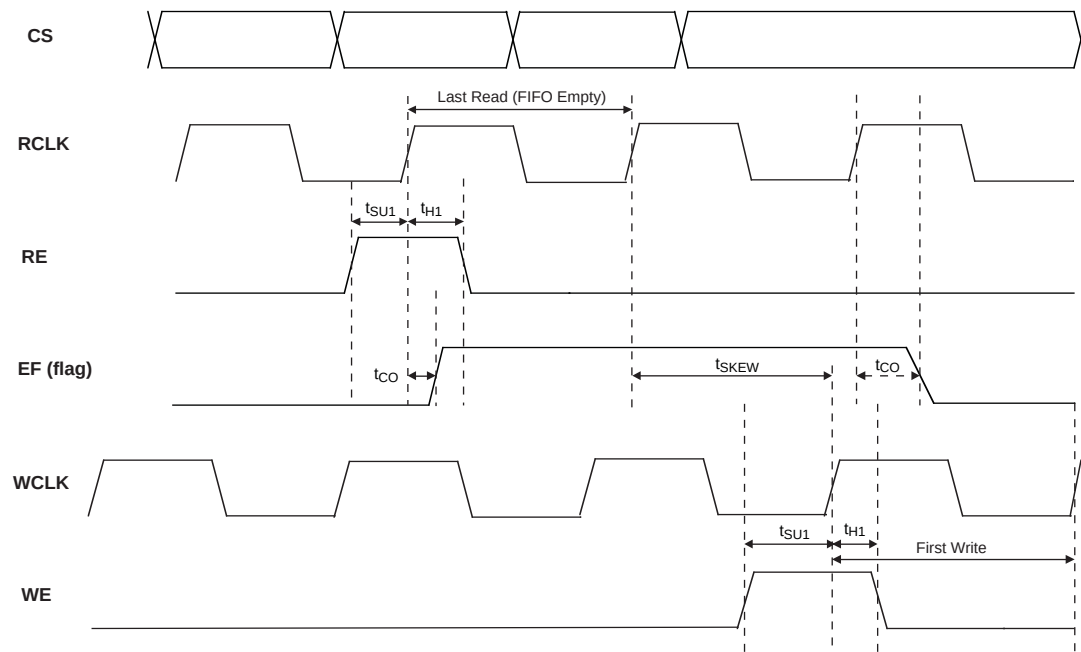


Figure 3-13. Waveform First Write after Empty Flag



LFSC/M15 Logic Signal Connections: 256 fpBGA^{1,2} (Cont.)

Ball Number	LFSC/M15		
	Ball Function	VCCIO Bank	Dual Function
F14	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
E15	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
E14	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
D9	VCCJ	-	
C16	TDO	-	TDO
B15	TMS	-	
B16	TCK	-	
E13	TDI	-	
C14	PROGRAMN	1	
C15	CCLK	1	
A15	PT43D	1	HDC/SI
A14	PT43C	1	LDCN/SCS
B14	PT41A	1	CS1
E12	PT39B	1	CS0N
D13	PT39A	1	RDN
D12	PT37D	1	WRN
E10	PT37C	1	D7
C11	PT37B	1	D6
D10	PT37A	1	D5
A13	PT36D	1	D4
B12	PT36C	1	D3
A12	PT35B	1	D2
C12	PT35A	1	D1
A11	PT33B	1	D0
B11	PT33A	1	QOUT/CEON
E9	PT32D	1	VREF2_1
E8	PT32B	1	DOUT
D8	PT28C	1	BUSYN/RCLK/SCK
A10	PT27B	1	PCLKC1_0
C10	PT27A	1	PCLKT1_0
E7	PT21C	1	VREF1_1
C9	A_VDDIB3_L	-	
A9	A_HDINP3_L	-	PCS 360 CH 3 IN P
B9	A_HDINN3_L	-	PCS 360 CH 3 IN N
A8	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
B8	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
C8	A_VDDOB3_L	-	
B7	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
C7	A_VDDOB2_L	-	
A7	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
B6	A_HDINN2_L	-	PCS 360 CH 2 IN N
A6	A_HDINP2_L	-	PCS 360 CH 2 IN P
C6	A_VDDIB2_L	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
N3	PL27A	6		PL30A	6	
P3	PL27B	6		PL30B	6	
P4	PL27C	6	PCLKT6_3	PL30C	6	PCLKT6_3
P2	PL28A	6		PL31A	6	
R2	PL28B	6		PL31B	6	
T3	PL28C	6	PCLKT6_2	PL31C	6	PCLKT6_2
R3	PL28D	6	PCLKC6_2	PL31D	6	PCLKC6_2
P1	PL31A	6		PL34A	6	
R1	PL31B	6		PL34B	6	
R5	PL31C	6	VREF1_6	PL34C	6	VREF1_6
R4	PL31D	6		PL34D	6	
T2	PL32A	6		PL35A	6	
U2	PL32B	6		PL35B	6	
T1	PL33A	6		PL38A	6	
U1	PL33B	6		PL38B	6	
V1	PL35A	6		PL42A	6	
W1	PL35B	6		PL42B	6	
V6	PL35D	6	DIFFR_6	PL42D	6	DIFFR_6
V2	PL36A	6		PL43A	6	
W2	PL36B	6		PL43B	6	
Y1	PL37A	6		PL44A	6	
AA1	PL37B	6		PL44B	6	
AB1	PL39A	6		PL48A	6	
AC1	PL39B	6		PL48B	6	
Y5	PL40A	6		PL49A	6	
Y6	PL40B	6		PL49B	6	
AD2	PL41A	6		PL51A	6	
AE2	PL41B	6		PL51B	6	
AB5	PL41D	6	VREF2_6	PL51D	6	VREF2_6
AC3	PL43A	6		PL52A	6	
AD3	PL43B	6		PL52B	6	
AF1	PL44A	6		PL55A	6	
AG1	PL44B	6		PL55B	6	
AB6	PL44C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL55C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AC5	PL44D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL55D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AF2	PL45A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL57A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AG2	PL45B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL57B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AC6	PL45C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL57C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AC7	PL45D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL57D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AE4	XRES	-		XRES	-	
AG4	VCC12	-		VCC12	-	
AD5	TEMP	6		TEMP	6	
AF5	VCC12	-		VCC12	-	
AH1	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AJ1	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA^{1, 2} (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AK14	PB25A	5		PB35A	5	
AK15	PB25B	5		PB35B	5	
AK16	PB27A	4		PB37A	4	
AK17	PB27B	4		PB37B	4	
AJ16	PB28A	4		PB38A	4	
AJ17	PB28B	4		PB38B	4	
AE16	PB28C	4		PB38C	4	
AH16	PB29A	4		PB39A	4	
AG16	PB29B	4		PB39B	4	
AK18	PB31A	4		PB41A	4	
AK19	PB31B	4		PB41B	4	
AH17	PB32A	4		PB42A	4	
AH18	PB32B	4		PB42B	4	
AG17	PB32D	4		PB42D	4	
AJ18	PB33A	4		PB43A	4	
AJ19	PB33B	4		PB43B	4	
AK20	PB35A	4	PCLKT4_2	PB46A	4	PCLKT4_2
AK21	PB35B	4	PCLKC4_2	PB46B	4	PCLKC4_2
AF18	PB36A	4	PCLKT4_1	PB47A	4	PCLKT4_1
AG18	PB36B	4	PCLKC4_1	PB47B	4	PCLKC4_1
AJ20	PB37A	4	PCLKT4_0	PB49A	4	PCLKT4_0
AJ21	PB37B	4	PCLKC4_0	PB49B	4	PCLKC4_0
AG19	PB37C	4	VREF2_4	PB49C	4	VREF2_4
AK22	PB39A	4	PCLKT4_5	PB51A	4	PCLKT4_5
AK23	PB39B	4	PCLKC4_5	PB51B	4	PCLKC4_5
AH19	PB39C	4		PB51C	4	
AK24	PB40A	4	PCLKT4_3	PB52A	4	PCLKT4_3
AK25	PB40B	4	PCLKC4_3	PB52B	4	PCLKC4_3
AE19	PB40C	4	PCLKT4_4	PB52C	4	PCLKT4_4
AE20	PB40D	4	PCLKC4_4	PB52D	4	PCLKC4_4
AE21	PB41A	4		PB53A	4	
AF21	PB41B	4		PB53B	4	
AG21	PB43A	4		PB55A	4	
AG22	PB43B	4		PB55B	4	
AH22	PB44A	4		PB56A	4	
AH23	PB44B	4		PB56B	4	
AH21	PB44C	4		PB56C	4	
AK28	PB45A	4		PB60A	4	
AK29	PB45B	4		PB60B	4	
AE22	PB45C	4		PB60C	4	
AJ28	PB47A	4		PB67A	4	
AH28	PB47B	4		PB67B	4	
AE24	PB47C	4	VREF1_4	PB67C	4	VREF1_4
AE25	PB47D	4		PB67D	4	
AJ29	PB48A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB68A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ31	PB9A	5		PB9A	5	
AH30	PB9B	5		PB9B	5	
AM30	PB11A	5		PB11A	5	
AM29	PB11B	5		PB11B	5	
AH29	PB11C	5		PB11C	5	
AH28	PB11D	5		PB11D	5	
AJ27	PB12A	5		PB13A	5	
AK27	PB12B	5		PB13B	5	
AE22	PB12C	5		PB13C	5	
AF23	PB12D	5		PB13D	5	
AL28	PB13A	5		PB15A	5	
AL27	PB13B	5		PB15B	5	
AC21	PB13C	5		PB15C	5	
AD21	PB13D	5		PB15D	5	
AM28	PB15A	5		PB17A	5	
AM27	PB15B	5		PB17B	5	
AG23	PB15C	5		PB17C	5	
AF22	PB15D	5		PB17D	5	
AG26	PB16A	5		PB19A	5	
AG25	PB16B	5		PB19B	5	
AL26	PB17A	5		PB22A	5	
AM26	PB17B	5		PB22B	5	
AJ24	PB19A	5		PB25A	5	
AK24	PB19B	5		PB25B	5	
AE21	PB19C	5		PB25C	5	
AE20	PB19D	5		PB25D	5	
AJ22	PB20A	5	PCLKT5_3	PB30A	5	PCLKT5_3
AK22	PB20B	5	PCLKC5_3	PB30B	5	PCLKC5_3
AG22	PB20C	5	PCLKT5_4	PB30C	5	PCLKT5_4
AH22	PB20D	5	PCLKC5_4	PB30D	5	PCLKC5_4
AL23	PB21A	5	PCLKT5_5	PB31A	5	PCLKT5_5
AL22	PB21B	5	PCLKC5_5	PB31B	5	PCLKC5_5
AH23	PB21C	5		PB31C	5	
AH24	PB21D	5		PB31D	5	
AJ21	PB23A	5	PCLKT5_0	PB33A	5	PCLKT5_0
AK21	PB23B	5	PCLKC5_0	PB33B	5	PCLKC5_0
AE19	PB23C	5		PB33C	5	
AF19	PB23D	5	VREF2_5	PB33D	5	VREF2_5
AM23	PB24A	5	PCLKT5_1	PB34A	5	PCLKT5_1
AM22	PB24B	5	PCLKC5_1	PB34B	5	PCLKC5_1
AH25	PB24C	5	PCLKT5_6	PB34C	5	PCLKT5_6
AH26	PB24D	5	PCLKC5_6	PB34D	5	PCLKC5_6
AL21	PB25A	5	PCLKT5_2	PB35A	5	PCLKT5_2
AL20	PB25B	5	PCLKC5_2	PB35B	5	PCLKC5_2
AG20	PB25C	5	PCLKT5_7	PB35C	5	PCLKT5_7
AG19	PB25D	5	PCLKC5_7	PB35D	5	PCLKC5_7
AJ19	PB28A	5		PB37A	5	
AK19	PB28B	5		PB37B	5	
AD18	PB28C	5		PB37C	5	
AE18	PB28D	5		PB37D	5	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH11	PB47C	4	PCLKT4_6	PB54C	4	PCLKT4_6
AH10	PB47D	4	PCLKC4_6	PB54D	4	PCLKC4_6
AK12	PB49A	4	PCLKT4_0	PB55A	4	PCLKT4_0
AJ12	PB49B	4	PCLKC4_0	PB55B	4	PCLKC4_0
AF14	PB49C	4	VREF2_4	PB55C	4	VREF2_4
AE14	PB49D	4		PB55D	4	
AL11	PB51A	4	PCLKT4_5	PB57A	4	PCLKT4_5
AL10	PB51B	4	PCLKC4_5	PB57B	4	PCLKC4_5
AH9	PB51C	4		PB57C	4	
AH8	PB51D	4		PB57D	4	
AK11	PB52A	4	PCLKT4_3	PB58A	4	PCLKT4_3
AJ11	PB52B	4	PCLKC4_3	PB58B	4	PCLKC4_3
AH7	PB52C	4	PCLKT4_4	PB58C	4	PCLKT4_4
AH6	PB52D	4	PCLKC4_4	PB58D	4	PCLKC4_4
AK8	PB53A	4		PB67A	4	
AJ8	PB53B	4		PB67B	4	
AF11	PB53C	4		PB67C	4	
AD12	PB55A	4		PB69A	4	
AE12	PB55B	4		PB69B	4	
AM6	PB56A	4		PB70A	4	
AM5	PB56B	4		PB70B	4	
AC12	PB56C	4		PB70C	4	
AL6	PB57A	4		PB73A	4	
AL5	PB57B	4		PB73B	4	
AG7	PB59A	4		PB74A	4	
AG8	PB59B	4		PB74B	4	
AK6	PB60A	4		PB75A	4	
AJ6	PB60B	4		PB75B	4	
AF10	PB60C	4		PB75C	4	
AE11	PB60D	4		PB75D	4	
AM4	PB61A	4		PB77A	4	
AM3	PB61B	4		PB77B	4	
AH5	PB63A	4		PB78A	4	
AH4	PB63B	4		PB78B	4	
AK5	PB64A	4		PB79A	4	
AJ5	PB64B	4		PB79B	4	
AF8	PB64C	4		PB79C	4	
AF7	PB64D	4		PB79D	4	
AL4	PB65A	4		PB81A	4	
AL3	PB65B	4		PB81B	4	
AG5	PB65C	4		PB81C	4	
AF6	PB65D	4		PB81D	4	
AK3	PB67A	4		PB82A	4	
AJ3	PB67B	4		PB82B	4	
AE10	PB67C	4	VREF1_4	PB82C	4	VREF1_4
AD10	PB67D	4		PB82D	4	
AL2	PB68A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D	PB83A	4	LRC_DLLT_IN_C/LRC_DLLT_FB_D
AK2	PB68B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB83B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AE9	PB68C	4		PB83C	4	
AE8	PB68D	4		PB83D	4	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P10	GND	-		GND	-	
P13	GND	-		GND	-	
P15	GND	-		GND	-	
P18	GND	-		GND	-	
P20	GND	-		GND	-	
P24	GND	-		GND	-	
R12	GND	-		GND	-	
R14	GND	-		GND	-	
R16	GND	-		GND	-	
R17	GND	-		GND	-	
R19	GND	-		GND	-	
R21	GND	-		GND	-	
R26	GND	-		GND	-	
R6	GND	-		GND	-	
T15	GND	-		GND	-	
T18	GND	-		GND	-	
T30	GND	-		GND	-	
T4	GND	-		GND	-	
U15	GND	-		GND	-	
U18	GND	-		GND	-	
U29	GND	-		GND	-	
U3	GND	-		GND	-	
V12	GND	-		GND	-	
V14	GND	-		GND	-	
V16	GND	-		GND	-	
V17	GND	-		GND	-	
V19	GND	-		GND	-	
V21	GND	-		GND	-	
V27	GND	-		GND	-	
V7	GND	-		GND	-	
W13	GND	-		GND	-	
W15	GND	-		GND	-	
W18	GND	-		GND	-	
W20	GND	-		GND	-	
W23	GND	-		GND	-	
W9	GND	-		GND	-	
Y12	GND	-		GND	-	
Y14	GND	-		GND	-	
Y19	GND	-		GND	-	
Y21	GND	-		GND	-	
Y30	GND	-		GND	-	
Y4	GND	-		GND	-	
N13	VCC	-		VCC	-	
N15	VCC	-		VCC	-	
N16	VCC	-		VCC	-	
N17	VCC	-		VCC	-	
N18	VCC	-		VCC	-	
N20	VCC	-		VCC	-	
P14	VCC	-		VCC	-	
P16	VCC	-		VCC	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AA7	VCCIO3	-		VCCIO3	-	
AB9	VCCIO3	-		VCCIO3	-	
AC4	VCCIO3	-		VCCIO3	-	
AD6	VCCIO3	-		VCCIO3	-	
AF3	VCCIO3	-		VCCIO3	-	
T3	VCCIO3	-		VCCIO3	-	
U4	VCCIO3	-		VCCIO3	-	
V6	VCCIO3	-		VCCIO3	-	
W10	VCCIO3	-		VCCIO3	-	
Y3	VCCIO3	-		VCCIO3	-	
AC11	VCCIO4	-		VCCIO4	-	
AD14	VCCIO4	-		VCCIO4	-	
AF15	VCCIO4	-		VCCIO4	-	
AF9	VCCIO4	-		VCCIO4	-	
AG12	VCCIO4	-		VCCIO4	-	
AJ13	VCCIO4	-		VCCIO4	-	
AJ7	VCCIO4	-		VCCIO4	-	
AK10	VCCIO4	-		VCCIO4	-	
AK16	VCCIO4	-		VCCIO4	-	
AK4	VCCIO4	-		VCCIO4	-	
AC19	VCCIO5	-		VCCIO5	-	
AD22	VCCIO5	-		VCCIO5	-	
AF21	VCCIO5	-		VCCIO5	-	
AG18	VCCIO5	-		VCCIO5	-	
AG24	VCCIO5	-		VCCIO5	-	
AJ17	VCCIO5	-		VCCIO5	-	
AJ23	VCCIO5	-		VCCIO5	-	
AJ30	VCCIO5	-		VCCIO5	-	
AK20	VCCIO5	-		VCCIO5	-	
AK26	VCCIO5	-		VCCIO5	-	
AA27	VCCIO6	-		VCCIO6	-	
AB23	VCCIO6	-		VCCIO6	-	
AC30	VCCIO6	-		VCCIO6	-	
AD26	VCCIO6	-		VCCIO6	-	
AF29	VCCIO6	-		VCCIO6	-	
T29	VCCIO6	-		VCCIO6	-	
U30	VCCIO6	-		VCCIO6	-	
V26	VCCIO6	-		VCCIO6	-	
W24	VCCIO6	-		VCCIO6	-	
Y29	VCCIO6	-		VCCIO6	-	
G30	VCCIO7	-		VCCIO7	-	
J27	VCCIO7	-		VCCIO7	-	
K29	VCCIO7	-		VCCIO7	-	
L24	VCCIO7	-		VCCIO7	-	
M26	VCCIO7	-		VCCIO7	-	
N30	VCCIO7	-		VCCIO7	-	
P23	VCCIO7	-		VCCIO7	-	
R27	VCCIO7	-		VCCIO7	-	
AA11	VCCAUX	-		VCCAUX	-	
AA12	VCCAUX	-		VCCAUX	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
D9	B_VDDIB2_R	-	
E12	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
F12	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
K11	VCC12	-	
A13	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D12	B_VDDOB2_R	-	
B13	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D13	B_VDDOB3_R	-	
B14	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
L11	VCC12	-	
A14	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
F13	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
E13	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
G13	VCC12	-	
E9	B_VDDIB3_R	-	
L13	VCC12	-	
J11	B_REFCLKN_R	-	
H11	B_REFCLKP_R	-	
M15	PT93D	1	HDC/SI
M16	PT93C	1	LDCN/SCS
F14	PT93B	1	D8/MPI_DATA8
G14	PT93A	1	CS1/MPI_CS1
L15	PT90D	1	D9/MPI_DATA9
L14	PT90C	1	D10/MPI_DATA10
D14	PT90B	1	CS0N/MPI_CS0N
E14	PT90A	1	RDN/MPI_STRB_N
L16	PT89D	1	WRN/MPI_WR_N
K16	PT89C	1	D7/MPI_DATA7
G15	PT89B	1	D6/MPI_DATA6
F15	PT89A	1	D5/MPI_DATA5
K14	PT87D	1	D4/MPI_DATA4
K13	PT87C	1	D3/MPI_DATA3
B15	PT87B	1	D2/MPI_DATA2
A15	PT87A	1	D1/MPI_DATA1
J14	PT86D	1	D16/PCLKC1_3/MPI_DATA16
H14	PT86C	1	D17/PCLKT1_3/MPI_DATA17
A16	PT86B	1	D0/MPI_DATA0
B16	PT86A	1	QOUT/CEON
J13	PT83D	1	VREF2_1
H13	PT83C	1	D18/MPI_DATA18
D15	PT83B	1	DOUT
E15	PT83A	1	MCA_DONE_IN
J16	PT81D	1	D19/PCLKC1_2/MPI_DATA19

LFSC/M115 Logic Signal Connections: 1152 fcBGA^{1, 2}

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
U22	VCCAUX	-	
V13	VCCAUX	-	
V22	VCCAUX	-	
V23	VCCAUX	-	
W13	VCCAUX	-	
W22	VCCAUX	-	
Y21	GND	-	
Y25	GND	-	
C18	VCCIO1	-	
D17	VCCIO1	-	
F16	VCCIO1	-	
G19	VCCIO1	-	
J20	VCCIO1	-	
K12	VCCIO1	-	
K15	VCCIO1	-	
L23	VCCIO1	-	
Y9	GND	-	
J9	VCCIO1	-	
E3	VCCIO2	-	
G6	VCCIO2	-	
H4	VCCIO2	-	
K7	VCCIO2	-	
L3	VCCIO2	-	
M11	VCCIO2	-	
N6	VCCIO2	-	
P4	VCCIO2	-	
R9	VCCIO2	-	
AA3	VCCIO3	-	
AB7	VCCIO3	-	
AC10	VCCIO3	-	
AD4	VCCIO3	-	
AE6	VCCIO3	-	
AG3	VCCIO3	-	
AK4	VCCIO3	-	
T7	VCCIO3	-	
U3	VCCIO3	-	
V4	VCCIO3	-	
W6	VCCIO3	-	
Y10	VCCIO3	-	
AD12	VCCIO4	-	
AF15	VCCIO4	-	
AF9	VCCIO4	-	
AH10	VCCIO4	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P38	PL26B	7		PL40B	7	
N35	PL26C	7		PL40C	7	
N36	PL26D	7		PL40D	7	
N39	PL29A	7		PL43A	7	
P39	PL29B	7		PL43B	7	
R34	PL29C	7	VREF1_7	PL43C	7	VREF1_7
T34	PL29D	7	DIFFR_7	PL43D	7	DIFFR_7
L41	PL30A	7		PL44A	7	
M41	PL30B	7		PL44B	7	
W29	PL30C	7		PL44C	7	
Y29	PL30D	7		PL44D	7	
L42	PL31A	7		PL45A	7	
M42	PL31B	7		PL45B	7	
U32	PL31C	7		PL45C	7	
V32	PL31D	7		PL45D	7	
R37	PL33A	7		PL47A	7	
T37	PL33B	7		PL47B	7	
M36	PL33C	7		PL47C	7	
M37	PL33D	7		PL47D	7	
P40	PL34A	7		PL48A	7	
N40	PL34B	7		PL48B	7	
R35	PL34C	7		PL48C	7	
T35	PL34D	7		PL48D	7	
N41	PL35A	7		PL49A	7	
P41	PL35B	7		PL49B	7	
V33	PL35C	7		PL49C	7	
U33	PL35D	7		PL49D	7	
R38	PL37A	7		PL51A	7	
T38	PL37B	7		PL51B	7	
R36	PL37C	7		PL51C	7	
T36	PL37D	7		PL51D	7	
N42	PL38A	7		PL52A	7	
P42	PL38B	7		PL52B	7	
Y31	PL38C	7		PL52C	7	
AA31	PL38D	7		PL52D	7	
U37	PL39A	7		PL53A	7	
V37	PL39B	7		PL53B	7	
U34	PL39C	7		PL53C	7	
V34	PL39D	7		PL53D	7	
U39	PL41A	7		PL55A	7	
T39	PL41B	7		PL55B	7	
V35	PL41C	7		PL55C	7	
W35	PL41D	7		PL55D	7	
R41	PL42A	7		PL56A	7	
T41	PL42B	7		PL56B	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AP41	PL91B	6		PL112B	6	
AK35	PL91C	6		PL112C	6	
AL35	PL91D	6		PL112D	6	
AN38	PL93A	6		PL115A	6	
AP38	PL93B	6		PL115B	6	
AL37	PL93C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F	PL115C	6	LLC_DLLT_IN_E/LLC_DLLT_FB_F
AM37	PL93D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F	PL115D	6	LLC_DLLC_IN_E/LLC_DLLC_FB_F
AR41	PL94A	6		PL116A	6	
AT41	PL94B	6		PL116B	6	
AN37	PL94C	6		PL116C	6	
AP37	PL94D	6		PL116D	6	
AR39	PL95A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E	PL117A	6	LLC_DLLT_IN_F/LLC_DLLT_FB_E
AR40	PL95B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E	PL117B	6	LLC_DLLC_IN_F/LLC_DLLC_FB_E
AN36	PL95C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A	PL117C	6	LLC_PLLT_IN_B/LLC_PLLT_FB_A
AP36	PL95D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A	PL117D	6	LLC_PLLC_IN_B/LLC_PLLC_FB_A
AT40	XRES	-		XRES	-	
AU41	TEMP	6		TEMP	6	
AU42	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B	PB3A	5	LLC_PLLT_IN_A/LLC_PLLT_FB_B
AV42	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B	PB3B	5	LLC_PLLC_IN_A/LLC_PLLC_FB_B
AL33	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D	PB3C	5	LLC_DLLT_IN_C/LLC_DLLT_FB_D
AL34	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D	PB3D	5	LLC_DLLC_IN_C/LLC_DLLC_FB_D
AU38	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C	PB4A	5	LLC_DLLT_IN_D/LLC_DLLT_FB_C
AV38	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C	PB4B	5	LLC_DLLC_IN_D/LLC_DLLC_FB_C
AM34	PB4C	5		PB4C	5	
AM33	PB4D	5		PB4D	5	
AV41	PB5A	5		PB5A	5	
AW41	PB5B	5		PB5B	5	
AK30	PB5C	5		PB5C	5	
AK29	PB5D	5	VREF1_5	PB5D	5	VREF1_5
AW42	PB7A	5		PB7A	5	
AY42	PB7B	5		PB7B	5	
AR37	PB7C	5		PB7C	5	
AR38	PB7D	5		PB7D	5	
AV40	PB8A	5		PB9A	5	
AV39	PB8B	5		PB9B	5	
AN35	PB8C	5		PB9C	5	
AN34	PB8D	5		PB9D	5	
AW40	PB9A	5		PB11A	5	
AY40	PB9B	5		PB11B	5	
AP34	PB9C	5		PB11C	5	
AP35	PB9D	5		PB11D	5	
AW39	PB11A	5		PB12A	5	
AW38	PB11B	5		PB12B	5	
AL32	PB11C	5		PB12C	5	
AL31	PB11D	5		PB12D	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCI/O Bank	Dual Function	Ball Function	VCCI/O Bank	Dual Function
AY41	PB12A	5		PB13A	5	
BA41	PB12B	5		PB13B	5	
AT39	PB12C	5		PB13C	5	
AT38	PB12D	5		PB13D	5	
AV37	PB13A	5		PB15A	5	
AV36	PB13B	5		PB15B	5	
AM31	PB13C	5		PB15C	5	
AM32	PB13D	5		PB15D	5	
BA40	PB15A	5		PB16A	5	
BB40	PB15B	5		PB16B	5	
AM29	PB15C	5		PB16C	5	
AL29	PB15D	5		PB16D	5	
AY39	PB16A	5		PB17A	5	
AY38	PB16B	5		PB17B	5	
AN33	PB16C	5		PB17C	5	
AN32	PB16D	5		PB17D	5	
BA39	PB17A	5		PB19A	5	
BA38	PB17B	5		PB19B	5	
AT37	PB17C	5		PB19C	5	
AT36	PB17D	5		PB19D	5	
AW36	PB19A	5		PB20A	5	
AW35	PB19B	5		PB20B	5	
AM28	PB19C	5		PB20C	5	
AL28	PB19D	5		PB20D	5	
BB38	PB20A	5		PB21A	5	
BB39	PB20B	5		PB21B	5	
AR34	PB20C	5		PB21C	5	
AR33	PB20D	5		PB21D	5	
AV35	PB21A	5		PB23A	5	
AV34	PB21B	5		PB23B	5	
AT33	PB21C	5		PB23C	5	
AT34	PB21D	5		PB23D	5	
BA37	PB23A	5		PB25A	5	
BA36	PB23B	5		PB25B	5	
AP33	PB23C	5		PB25C	5	
AP32	PB23D	5		PB25D	5	
AY36	PB24A	5		PB26A	5	
AY35	PB24B	5		PB26B	5	
AN31	PB24C	5		PB26C	5	
AN30	PB24D	5		PB26D	5	
BB37	PB25A	5		PB27A	5	
BB36	PB25B	5		PB27B	5	
AP31	PB25C	5		PB27C	5	
AP30	PB25D	5		PB27D	5	
AV33	PB27A	5		PB29A	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AV32	PB27B	5		PB29B	5	
AU36	PB27C	5		PB29C	5	
AU37	PB27D	5		PB29D	5	
BA35	PB28A	5		PB30A	5	
BA34	PB28B	5		PB30B	5	
AJ26	PB28C	5		PB30C	5	
AJ27	PB28D	5		PB30D	5	
AW33	PB29A	5		PB31A	5	
AW32	PB29B	5		PB31B	5	
AU35	PB29C	5		PB31C	5	
AU34	PB29D	5		PB31D	5	
BB35	PB31A	5		PB33A	5	
BB34	PB31B	5		PB33B	5	
AN29	PB31C	5		PB33C	5	
AP29	PB31D	5		PB33D	5	
AY33	PB32A	5		PB34A	5	
AY32	PB32B	5		PB34B	5	
AR31	PB32C	5		PB34C	5	
AR30	PB32D	5		PB34D	5	
AV31	PB33A	5		PB35A	5	
AV30	PB33B	5		PB35B	5	
AN28	PB33C	5		PB35C	5	
AP28	PB33D	5		PB35D	5	
BA33	PB35A	5		PB37A	5	
BA32	PB35B	5		PB37B	5	
AT30	PB35C	5		PB37C	5	
AT31	PB35D	5		PB37D	5	
BB33	PB36A	5		PB38A	5	
BB32	PB36B	5		PB38B	5	
AM26	PB36C	5		PB38C	5	
AL26	PB36D	5		PB38D	5	
AW30	PB37A	5		PB39A	5	
AW29	PB37B	5		PB39B	5	
AP27	PB37C	5		PB39C	5	
AN27	PB37D	5		PB39D	5	
BA31	PB39A	5		PB41A	5	
BA30	PB39B	5		PB41B	5	
AU32	PB39C	5		PB41C	5	
AU33	PB39D	5		PB41D	5	
BB31	PB40A	5		PB42A	5	
BB30	PB40B	5		PB42B	5	
AR28	PB40C	5		PB42C	5	
AR27	PB40D	5		PB42D	5	
AV29	PB41A	5		PB43A	5	
AV28	PB41B	5		PB43B	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA^{1, 2} (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCI/O Bank	Dual Function	Ball Function	VCCI/O Bank	Dual Function
AP1	PR90B	3		PR109B	3	
AN1	PR90A	3		PR109A	3	
AK10	PR89D	3	VREF2_3	PR107D	3	VREF2_3
AJ10	PR89C	3		PR107C	3	
AM5	PR89B	3		PR107B	3	
AL5	PR89A	3		PR107A	3	
AL7	PR86D	3		PR104D	3	
AK7	PR86C	3		PR104C	3	
AM1	PR86B	3		PR104B	3	
AL1	PR86A	3		PR104A	3	
AJ11	PR85D	3		PR103D	3	
AH11	PR85C	3		PR103C	3	
AK5	PR85B	3		PR103B	3	
AJ5	PR85A	3		PR103A	3	
AK9	PR84D	3		PR99D	3	
AJ9	PR84C	3		PR99C	3	
AK3	PR84B	3		PR99B	3	
AJ3	PR84A	3		PR99A	3	
AK6	PR82D	3		PR98D	3	
AJ6	PR82C	3		PR98C	3	
AK2	PR82B	3		PR98B	3	
AJ2	PR82A	3		PR98A	3	
AH10	PR81D	3		PR96D	3	
AG10	PR81C	3		PR96C	3	
AK1	PR81B	3		PR96B	3	
AJ1	PR81A	3		PR96A	3	
AH9	PR80D	3		PR94D	3	
AG9	PR80C	3		PR94C	3	
AH2	PR80B	3		PR94B	3	
AG2	PR80A	3		PR94A	3	
AH8	PR78D	3		PR92D	3	
AG8	PR78C	3		PR92C	3	
AG1	PR78B	3		PR92B	3	
AH1	PR78A	3		PR92A	3	
AG14	PR77D	3		PR91D	3	
AF14	PR77C	3		PR91C	3	
AG4	PR77B	3		PR91B	3	
AF4	PR77A	3		PR91A	3	
AH7	PR76D	3	DIFFR_3	PR90D	3	DIFFR_3
AG7	PR76C	3		PR90C	3	
AG3	PR76B	3		PR90B	3	
AF3	PR76A	3		PR90A	3	
AH6	PR74D	3		PR88D	3	
AG6	PR74C	3		PR88C	3	
AF1	PR74B	3		PR88B	3	