Lattice Semiconductor Corporation - LFSCM3GA80EP1-5FF1704C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

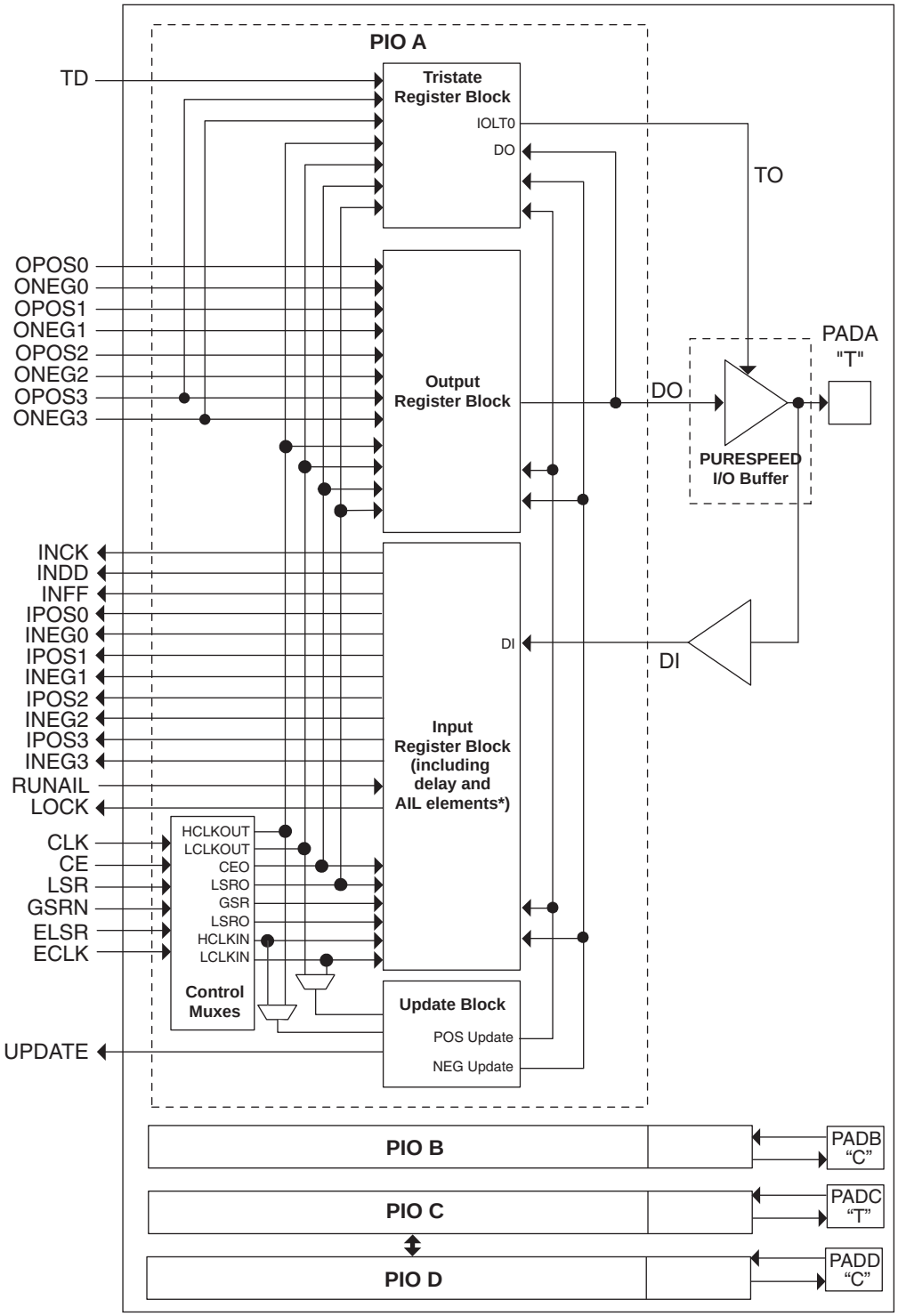
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	20000
Number of Logic Elements/Cells	80000
Total RAM Bits	5816320
Number of I/O	904
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1704-BBGA, FCBGA
Supplier Device Package	1704-OFCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga80ep1-5ff1704c

Figure 2-17. PIC Diagram



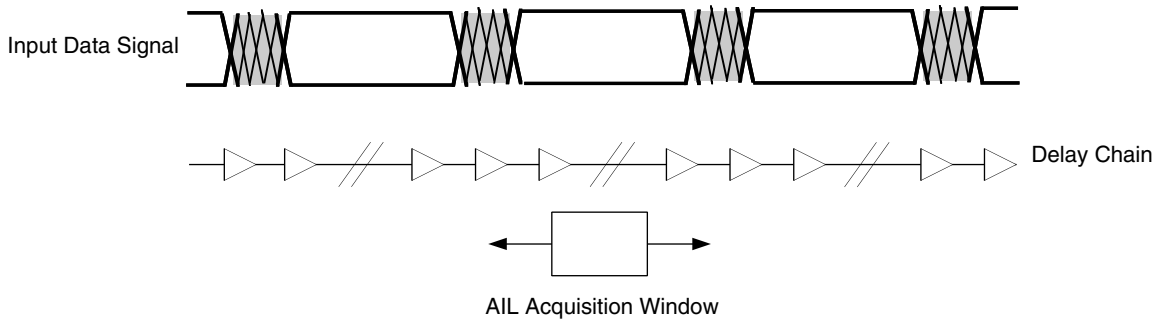
*AIL only on A or C pads located on the left, right and bottom of the device.

The A/B PIOs on the left and the right of the device can be paired to form a differentiated driver. The A/B and C/D PIOs on all sides of the device can be paired to form differential receivers. Either A or C PIOs on all sides except the one on top also provide a connection to an adaptive input logic capability that facilitates the implementation of

Adaptive Input Logic (AIL) Overview

The Adaptive Input Logic (AIL) provides the ability of the input logic to dynamically find a solution by monitoring multiple samples of the input data. The input data signal from the input buffer is run through a delay chain. Data, transitions, jitter, noise are all contained inside of the delay chain. The AIL will then search the delay chain for a clean sampling point for data. Once found the AIL will monitor and walk with the data dynamically. This novel approach of using a delay chain to create multiple copies of the data provides a lower power solution than oversampling data with a higher speed clock. Figure 2-19 provides a high level view of the AIL methodology.

Figure 2-19. LatticeSC AIL Delay of Input Data Waveform



The AIL slides the acquisition window through the delay chain searching for stable data based solely on data transitions. A specific training pattern is not required to perform this bit alignment, simply data transitions. The size of the acquisition window is user-selectable allowing the AIL to operate over the full range of the PURESPEED I/O range. Based on dynamic user control the AIL can either continuously adjust the window location based on data edge detection or it can be locked to a specific delay.

The AIL operates on single data and double data rate interfaces and is available on most FPGA input pins on the LatticeSC device and all buffer types. The AIL block is low power using only 0.003 mW/MHz typical (6 mW @ 2 Gbps) for PRBS 2^7 data. Multiple AIL inputs can be used to create a bus with a FPGA circuit to realign the bus to a common clock cycle. The FPGA circuit to realign the bus is required and is provided by Lattice as a reference design.

For more information on the LatticeSC AIL please refer to TN1158 LatticeSC PURESPEED I/O Adaptive Input Logic User's Guide.

Input DDR/Shift Block

The DDR/Shift block contains registers and associated logic that support DDR and shift register functions using the high-speed clock and the associated transfer to the low-speed clock domain. It functions as a gearbox allowing high-speed incoming data to be passed into the FPGA fabric. Each PIO supports DDR and x2 shift functions. If desired PIOs A and B or C and D can be combined to form x4 shift functions. The PIOs A and C on the left, right and bottom of the device also contain an optional Adaptive Input Logic (AIL) element. This logic automatically aligns incoming data with the clock allowing for easy design of high-speed interfaces. Figure 2-21 shows a simplified block diagram of the shift register block. The shift block in conjunction with the update and clock divider blocks automatically handles the hand off between the low-speed and high-speed clock domains.

PURESPEED I/O Single-Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 33	-0.3	0.8	2	3.465	0.4	2.4	24, 16, 8	-24, -16, -8
					0.2	VCCIO - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2	3.465	0.4	2.4	24, 16, 8	-24, -16, -8
					0.2	VCCIO - 0.2	0.1	-0.1
LVCMOS 25	-0.3	0.7	1.7	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVCMOS 18	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVCMOS 15	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.4	VCCIO - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	VCCIO - 0.2	0.1	-0.1
LVCMOS 12	-0.3	0.35VCCIO	0.65VCCIO	2.65	0.3	VCCIO - 0.3	12, 8, 4, 2	-12, -8, -4, -2
					0.2	VCCIO - 0.2	0.1	-0.1
PCIX15	-0.3	0.3VCCIO	0.5VCCIO	1.5	0.1VCCIO	0.9VCCIO	1.5	-0.5
PCI33	-0.3	0.3VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
PCIX33	-0.3	0.35VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
AGP-1X, AGP-2X	-0.3	0.3VCCIO	0.5VCCIO	3.465	0.1VCCIO	0.9VCCIO	1.5	-0.5
SSTL3_I	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.7	VCCIO - 1.1	8	-8
SSTS3_I OST[2]	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.9	VCCIO - 1.3	8	-8
SSTL3_II	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.5	VCCIO - 0.9	16	-16
SSTL3_II OST[2]	-0.3	VREF - 0.2	VREF + 0.2	3.465	0.9	VCCIO - 0.13	16	-16
SSTL2_I	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.54	VCCIO - 0.62	7.6	-7.6
SSTL2_I OST[2]	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.73	VCCIO - 0.81	7.6	-7.6
SSTL2_II	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.35	VCCIO - 0.43	15.2	-15.2
SSTL2_II OST[2]	-0.3	VREF - 0.18	VREF + 0.18	2.65	0.73	VCCIO - 0.81	15.2	-15.2
SSTL18_I	-0.3	VREF - 0.125	VREF + 0.125	2.65	0.28	VCCIO - 0.28	13.4	-13.4
SSTL18_II	-0.3	VREF - 0.125	VREF + 0.125	2.65	0.28	VCCIO - 0.28	13.4	-13.4
HSTL15_I	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	8	-8
HSTL15_II	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	16	-16
HSTL15_III[1]	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL15_IV[1]	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL18_I	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	9.6	-9.6
HSTL18_II	-0.3	VREF - 0.1	VREF + 0.1	2.65	0.4	VCCIO - 0.4	19.2	-19.2
HSTL18_III[1]	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
HSTL18_IV[1]	-0.3	VREF - 0.1	VREF + 0.1	2.65	N/A	N/A	N/A	N/A
GTL12[1], GTLPLUS15[1]	-0.3	VREF - 0.2	VREF + 0.2	N/A	N/A	N/A	N/A	N/A

1. Input only.
2. Input with on-chip series termination.

LatticeSC/M Family Timing Adders (Continued)

Over Recommended Operating Conditions at VCC = 1.2V +/- 5%

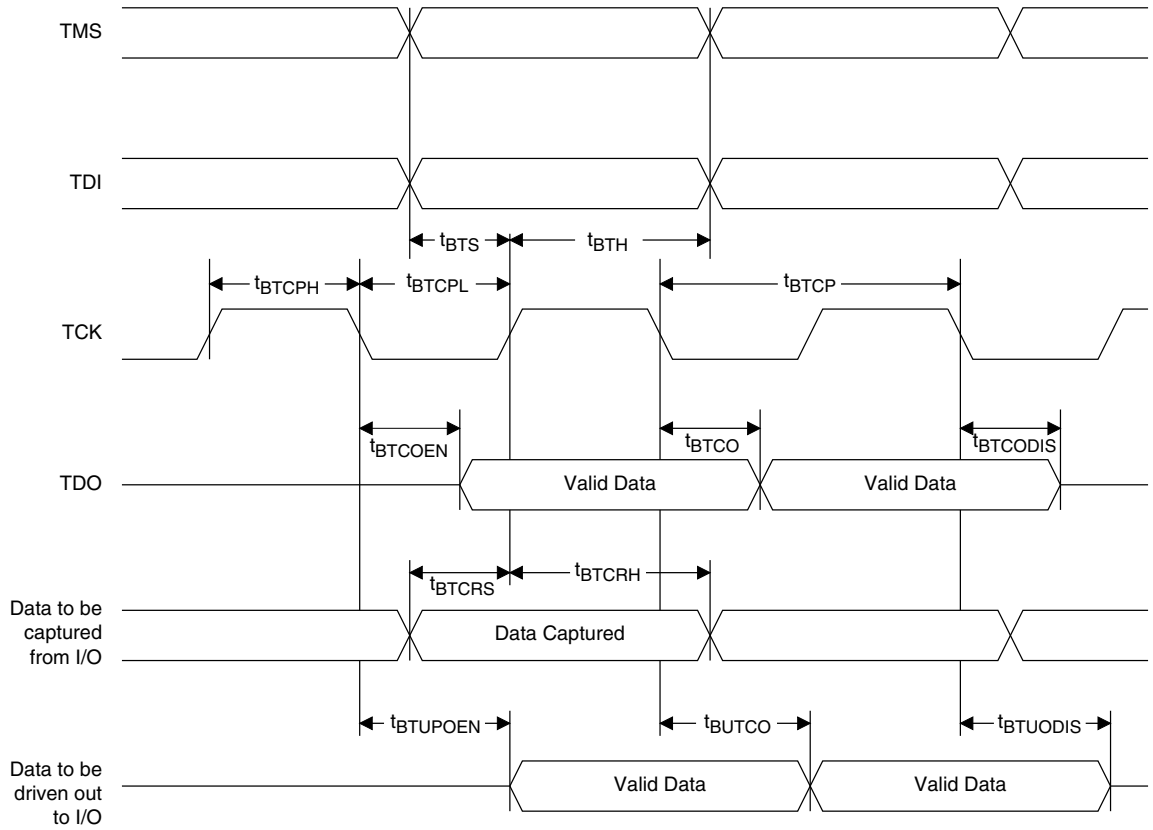
Buffer Type	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
LVCMOS18_12mA	LVCMOS 1.8 12mA drive	0.024	-0.106	0.019	-0.004	0.016	0.099	ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive	0.074	-0.134	0.08	-0.022	0.088	0.089	ns
LVCMOS18_OD	LVCMOS 1.8 open drain	0.002	-0.206	0	-0.196	-0.002	-0.221	ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive	-0.344	-0.164	-0.379	-0.186	-0.412	-0.209	ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive	-0.125	-0.137	-0.145	-0.157	-0.164	-0.176	ns
LVCMOS15_12mA	LVCMOS 1.5 12mA drive	-0.027	-0.166	-0.043	-0.07	-0.059	0.026	ns
LVCMOS15_16mA	LVCMOS 1.5 16mA drive	0.025	-0.195	0.013	-0.089	0.003	0.017	ns
LVCMOS15_OD	LVCMOS 1.5 open drain	-0.047	-0.267	-0.067	-0.267	-0.087	-0.299	ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive	-0.473	-0.293	-0.505	-0.317	-0.537	-0.34	ns
LVCMOS12_4mA	LVCMOS 1.2 4mA drive	-0.218	-0.239	-0.25	-0.271	-0.28	-0.303	ns
LVCMOS12_8mA	LVCMOS 1.2 8mA drive	-0.109	-0.269	-0.143	-0.181	-0.176	-0.093	ns
LVCMOS12_12mA	LVCMOS 1.2 12mA drive	-0.054	-0.3	-0.085	-0.203	-0.114	-0.106	ns
LVCMOS12_OD	LVCMOS 1.2 open drain	-0.126	-0.371	-0.166	-0.398	-0.204	-0.43	ns
PCI33	PCI	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX33	PCI-X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
PCIX15	PCI-X 1.5	0.208	0.227	0.233	0.312	0.259	0.398	ns
AGP1X33	AGP-1X 3.3	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns
AGP2X33	AGP-2X	-0.216	-0.791	-0.417	-1.263	-0.618	-1.735	ns

JTAG Port Timing Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
f_{MAX}		—	25	MHz
t_{BTCP}	TCK [BSCAN] Clock Pulse Width	40	—	ns
t_{BTCPH}	TCK [BSCAN] Clock Pulse Width High	20	—	ns
t_{BTCPL}	TCK [BSCAN] Clock Pulse Width Low	20	—	ns
t_{BTS}	TCK [BSCAN] Setup Time	8	—	ns
t_{BTH}	TCK [BSCAN] Hold Time	10	—	ns
t_{BTRF}	TCK [BSCAN] Rise/Fall Time	50	—	mV/ns
t_{BTCO}	TAP Controller Falling Edge of Clock to Valid Output	—	10	ns
$t_{BTCODIS}$	TAP Controller Falling Edge of Clock to Valid Disable	—	10	ns
t_{BTCOEN}	TAP Controller Falling Edge of Clock to Valid Enable	—	10	ns
t_{BTCRS}	BSCAN Test Capture Register Setup Time	8	—	ns
t_{BTCRH}	BSCAN Test Capture Register Hold Time	10	—	ns
t_{BUTCO}	BSCAN Test Update Register, Falling Edge of Clock to Valid Output	—	25	ns
$t_{BTUODIS}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Disable	—	25	ns
$t_{BTUPOEN}$	BSCAN Test Update Register, Falling Edge of Clock to Valid Enable	—	25	ns

Figure 3-14. JTAG Port Timing Waveforms



Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PIC row or the column of the device on which the PIC exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the PIC to which the pad is connected. Some of these user programmable pins are shared with special function pins. These pin when not used as special purpose pins can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
VREF1_x, VREF2_x	—	The reference supply pins for I/O bank x. Any I/O pin in a bank can be assigned as a reference supply pin, but software defaults use designated pin.
NC	—	No connect. NC pins should not be connected to any active signals, VCC or GND.
Non-SERDES Power Supplies		
VCCIOx	—	VCCIO - The power supply pins for I/O bank x. Dedicated pins.
VCC12[1]	—	1.2V supply for configuration logic, PLLs and SERDES Rx, Tx and PLL. All VCC12 pins must be connected. As VCC12 supplies power for analog circuitry, VCC12 should be quiet and isolated from noisy digital board supplies.
VTT_x	—	Termination voltage for bank x. When VTT termination is not required, or used to provide the common mode termination voltage (VCMT), these pins can be left unconnected on the device. VCMT function is not used in the bank. If the internal or external VCMT function for differential input termination is used, the VTT pins should be unconnected and allowed to float.
GND	—	GND - Ground. Dedicated pins. All grounds must be electrically connected at the board level.
VCC	—	VCC - The power supply pins for core logic. Dedicated pins (1.2V/1.0V).
VCCAUX	—	VCCAUX - Auxiliary power supply pin - powers all differential and referenced input buffers. Dedicated pins (2.5V).
VCCJ	—	VCCJ - The power supply pin for JTAG Test Access Port.
PROBE_VCC	—	VCC signal - Connected to internal VCC node. Can be used for feedback to control an external board power converter. Can be unconnected if not used.

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Pin Information Summary (Cont.)

Pin Type		1152 fcBGA			1704 fcBGA	
		LFSC/M40	LFSC/M80	LFSC/M115	LFSC/M80	LFSC/M115
Single Ended User I/O		604	660	660	904	942
Differential Pair User I/O		302	330	330	452	470
LVDS Output Pairs		78	102	102	114	132
Configuration	Dedicated	11	11	11	11	11
	Muxes/MPI sysBus	72	72	72	72	72
JTAG (excluding VCCJ)		4	4	4	4	4
Dedicated Pins		4	4	4	4	4
VCC		44	44	44	76	76
VCC12		52	52	52	88	88
VCCAUX		38	38	38	52	52
VCCIO	Bank 1	10	10	10	10	10
	Bank 2	9	9	9	12	12
	Bank 3	12	12	12	14	14
	Bank 4	12	12	12	14	14
	Bank 5	12	12	12	14	14
	Bank 6	12	12	12	14	14
	Bank 7	9	9	9	12	12
VTT	Bank 2	3	3	3	4	4
	Bank 3	3	3	3	4	4
	Bank 4	3	3	3	5	5
	Bank 5	3	3	3	5	5
	Bank 6	3	3	3	4	4
	Bank 7	3	3	3	4	4
GND		130	130	130	184	184
NC		62	6	6	52	14
Single Ended User / Differential I/O per Bank	Bank 1	80/40	80/40	80/40	80/40	80/40
	Bank 2	60/30	76/38	76/38	96/48	103/51
	Bank 3	96/48	108/54	108/54	132/66	144/72
	Bank 4	106/53	106/53	106/53	184/92	184/92
	Bank 5	106/53	106/53	106/53	184/92	184/92
	Bank 6	96/48	108/54	108/54	132/66	144/72
	Bank 7	60/30	76/38	76/38	96/48	103/51
LVDS Output Pairs Per Bank	Bank 2	15	21	21	24	27
	Bank 3	24	30	30	33	39
	Bank 6	24	30	30	33	39
	Bank 7	15	21	21	24	27
VCCJ		1	1	1	1	1
SERDES (signal + power supply)		108	108	108	212	212
Total		1152	1152	1152	1704	1704

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G1	NC	-		PL20B	7	
M4	NC	-		NC	-	
J3	NC	-		NC	-	
P5	NC	-		NC	-	
W5	NC	-		PL48C	6	
T6	NC	-		PL35C	6	
U3	NC	-		PL36A	6	
V3	NC	-		PL36B	6	
T5	NC	-		PL39A	6	
T4	NC	-		PL39B	6	
V5	NC	-		PL43C	6	
U6	NC	-		PL42C	6	
U4	NC	-		PL40A	6	
U5	NC	-		PL40B	6	
V4	NC	-		PL43D	6	
Y2	NC	-		PL47A	6	
AA2	NC	-		PL47B	6	
W3	NC	-		PL47D	6	
Y3	NC	-		PL47C	6	
AB3	NC	-		NC	-	
AC4	NC	-		PL53A	6	
AD4	NC	-		PL53B	6	
AE3	NC	-		PL56A	6	
AF3	NC	-		PL56B	6	
AF7	NC	-		PB7A	5	
AF6	NC	-		PB7B	5	
AH4	NC	-		PB8A	5	
AG5	NC	-		PB8B	5	
AF8	NC	-		PB9A	5	
AG8	NC	-		PB9B	5	
AG7	NC	-		NC	-	
AG10	NC	-		NC	-	
AF12	NC	-		NC	-	
AH7	NC	-		PB15A	5	
AE13	NC	-		PB15D	5	
AG13	NC	-		PB23C	5	
AH8	NC	-		PB15B	5	
AJ5	NC	-		PB17A	5	
AJ6	NC	-		PB17B	5	
AF15	NC	-		PB21D	5	
AJ7	NC	-		PB19A	5	
AJ8	NC	-		PB19B	5	
AE12	NC	-		PB15C	5	
AF16	NC	-		PB38D	4	
AF19	NC	-		PB49D	4	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
P22	VCCIO2	-		VCCIO2	-	
R22	VCCIO2	-		VCCIO2	-	
AA23	VCCIO3	-		VCCIO3	-	
AA24	VCCIO3	-		VCCIO3	-	
AB23	VCCIO3	-		VCCIO3	-	
AB24	VCCIO3	-		VCCIO3	-	
T22	VCCIO3	-		VCCIO3	-	
U22	VCCIO3	-		VCCIO3	-	
V22	VCCIO3	-		VCCIO3	-	
W22	VCCIO3	-		VCCIO3	-	
Y22	VCCIO3	-		VCCIO3	-	
Y23	VCCIO3	-		VCCIO3	-	
Y24	VCCIO3	-		VCCIO3	-	
AB16	VCCIO4	-		VCCIO4	-	
AB17	VCCIO4	-		VCCIO4	-	
AB18	VCCIO4	-		VCCIO4	-	
AB19	VCCIO4	-		VCCIO4	-	
AB20	VCCIO4	-		VCCIO4	-	
AC20	VCCIO4	-		VCCIO4	-	
AC21	VCCIO4	-		VCCIO4	-	
AC22	VCCIO4	-		VCCIO4	-	
AD20	VCCIO4	-		VCCIO4	-	
AD21	VCCIO4	-		VCCIO4	-	
AD22	VCCIO4	-		VCCIO4	-	
AB11	VCCIO5	-		VCCIO5	-	
AB12	VCCIO5	-		VCCIO5	-	
AB13	VCCIO5	-		VCCIO5	-	
AB14	VCCIO5	-		VCCIO5	-	
AB15	VCCIO5	-		VCCIO5	-	
AC10	VCCIO5	-		VCCIO5	-	
AC11	VCCIO5	-		VCCIO5	-	
AC9	VCCIO5	-		VCCIO5	-	
AD10	VCCIO5	-		VCCIO5	-	
AD11	VCCIO5	-		VCCIO5	-	
AD9	VCCIO5	-		VCCIO5	-	
AA7	VCCIO6	-		VCCIO6	-	
AA8	VCCIO6	-		VCCIO6	-	
AB7	VCCIO6	-		VCCIO6	-	
AB8	VCCIO6	-		VCCIO6	-	
T9	VCCIO6	-		VCCIO6	-	
U9	VCCIO6	-		VCCIO6	-	
V9	VCCIO6	-		VCCIO6	-	
W9	VCCIO6	-		VCCIO6	-	
Y7	VCCIO6	-		VCCIO6	-	
Y8	VCCIO6	-		VCCIO6	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
B1	GND	-		GND	-	
B32	GND	-		GND	-	
C11	GND	-		GND	-	
C12	GND	-		GND	-	
C16	GND	-		GND	-	
C21	GND	-		GND	-	
C22	GND	-		GND	-	
C24	GND	-		GND	-	
C25	GND	-		GND	-	
C26	GND	-		GND	-	
C27	GND	-		GND	-	
C29	GND	-		GND	-	
C3	GND	-		GND	-	
C30	GND	-		GND	-	
C4	GND	-		GND	-	
C6	GND	-		GND	-	
C7	GND	-		GND	-	
C8	GND	-		GND	-	
C9	GND	-		GND	-	
D17	GND	-		GND	-	
F18	GND	-		GND	-	
F3	GND	-		GND	-	
F30	GND	-		GND	-	
F9	GND	-		GND	-	
G15	GND	-		GND	-	
G24	GND	-		GND	-	
G29	GND	-		GND	-	
G3	GND	-		GND	-	
J14	GND	-		GND	-	
J22	GND	-		GND	-	
J26	GND	-		GND	-	
J6	GND	-		GND	-	
K11	GND	-		GND	-	
K19	GND	-		GND	-	
K30	GND	-		GND	-	
K4	GND	-		GND	-	
L23	GND	-		GND	-	
L9	GND	-		GND	-	
M13	GND	-		GND	-	
M15	GND	-		GND	-	
M18	GND	-		GND	-	
M20	GND	-		GND	-	
M27	GND	-		GND	-	
M7	GND	-		GND	-	
N12	GND	-		GND	-	
N14	GND	-		GND	-	
N19	GND	-		GND	-	
N21	GND	-		GND	-	
N29	GND	-		GND	-	
N3	GND	-		GND	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH11	PB57D	4		PB79D	4	
AN13	PB58A	4	PCLKT4_3	PB80A	4	PCLKT4_3
AN12	PB58B	4	PCLKC4_3	PB80B	4	PCLKC4_3
AD14	PB58C	4	PCLKT4_4	PB80C	4	PCLKT4_4
AD15	PB58D	4	PCLKC4_4	PB80D	4	PCLKC4_4
AP13	PB61A	4		PB73A	4	
AP12	PB61B	4		PB73B	4	
AK13	PB61C	4		PB73C	4	
AK12	PB61D	4		PB73D	4	
AP11	PB62A	4		PB83A	4	
AP10	PB62B	4		PB83B	4	
AN11	PB63A	4		PB99A	4	
AN10	PB63B	4		PB99B	4	
AF14	PB63C	4		PB99C	4	
AF13	PB63D	4		PB99D	4	
AM10	PB67A	4		PB101A	4	
AM9	PB67B	4		PB101B	4	
AE14	PB67C	4		PB101C	4	
AE13	PB67D	4		PB101D	4	
AP9	PB69A	4		PB104A	4	
AP8	PB69B	4		PB104B	4	
AK11	PB69C	4		PB104C	4	
AK10	PB69D	4		PB104D	4	
AL10	PB70A	4		PB107A	4	
AL9	PB70B	4		PB107B	4	
AF12	PB70C	4		PB107C	4	
AF11	PB70D	4		PB107D	4	
AN9	PB73A	4		PB109A	4	
AN8	PB73B	4		PB109B	4	
AG11	PB73C	4		PB109C	4	
AG10	PB73D	4		PB109D	4	
AP7	PB74A	4		PB111A	4	
AP6	PB74B	4		PB111B	4	
AG13	PB74C	4		PB111C	4	
AG12	PB74D	4		PB111D	4	
AN7	PB75A	4		PB113A	4	
AN6	PB75B	4		PB113B	4	
AK9	PB75C	4		PB113C	4	
AK8	PB75D	4		PB113D	4	
AP5	PB77A	4		PB115A	4	
AP4	PB77B	4		PB115B	4	
AD11	PB77C	4		PB115C	4	
AE11	PB77D	4		PB115D	4	
AM7	PB78A	4		PB117A	4	
AM6	PB78B	4		PB117B	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AV32	PB27B	5		PB29B	5	
AU36	PB27C	5		PB29C	5	
AU37	PB27D	5		PB29D	5	
BA35	PB28A	5		PB30A	5	
BA34	PB28B	5		PB30B	5	
AJ26	PB28C	5		PB30C	5	
AJ27	PB28D	5		PB30D	5	
AW33	PB29A	5		PB31A	5	
AW32	PB29B	5		PB31B	5	
AU35	PB29C	5		PB31C	5	
AU34	PB29D	5		PB31D	5	
BB35	PB31A	5		PB33A	5	
BB34	PB31B	5		PB33B	5	
AN29	PB31C	5		PB33C	5	
AP29	PB31D	5		PB33D	5	
AY33	PB32A	5		PB34A	5	
AY32	PB32B	5		PB34B	5	
AR31	PB32C	5		PB34C	5	
AR30	PB32D	5		PB34D	5	
AV31	PB33A	5		PB35A	5	
AV30	PB33B	5		PB35B	5	
AN28	PB33C	5		PB35C	5	
AP28	PB33D	5		PB35D	5	
BA33	PB35A	5		PB37A	5	
BA32	PB35B	5		PB37B	5	
AT30	PB35C	5		PB37C	5	
AT31	PB35D	5		PB37D	5	
BB33	PB36A	5		PB38A	5	
BB32	PB36B	5		PB38B	5	
AM26	PB36C	5		PB38C	5	
AL26	PB36D	5		PB38D	5	
AW30	PB37A	5		PB39A	5	
AW29	PB37B	5		PB39B	5	
AP27	PB37C	5		PB39C	5	
AN27	PB37D	5		PB39D	5	
BA31	PB39A	5		PB41A	5	
BA30	PB39B	5		PB41B	5	
AU32	PB39C	5		PB41C	5	
AU33	PB39D	5		PB41D	5	
BB31	PB40A	5		PB42A	5	
BB30	PB40B	5		PB42B	5	
AR28	PB40C	5		PB42C	5	
AR27	PB40D	5		PB42D	5	
AV29	PB41A	5		PB43A	5	
AV28	PB41B	5		PB43B	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AE1	PR74A	3		PR88A	3	
AF12	PR73D	3		PR87D	3	
AE12	PR73C	3		PR87C	3	
AF2	PR73B	3		PR87B	3	
AE2	PR73A	3		PR87A	3	
AF11	PR72D	3		PR86D	3	
AE11	PR72C	3		PR86C	3	
AF5	PR72B	3		PR86B	3	
AE5	PR72A	3		PR86A	3	
AF10	PR69D	3		PR83D	3	
AE10	PR69C	3		PR83C	3	
AD1	PR69B	3		PR83B	3	
AC1	PR69A	3		PR83A	3	
AF9	PR68D	3		PR82D	3	
AE9	PR68C	3		PR82C	3	
AD2	PR68B	3		PR82B	3	
AC2	PR68A	3		PR82A	3	
AF6	PR67D	3		PR81D	3	
AE6	PR67C	3		PR81C	3	
AD3	PR67B	3		PR81B	3	
AC3	PR67A	3		PR81A	3	
AE8	PR65D	3		PR79D	3	
AD8	PR65C	3		PR79C	3	
AD4	PR65B	3		PR79B	3	
AC4	PR65A	3		PR79A	3	
AE7	PR64D	3		PR78D	3	
AD7	PR64C	3		PR78C	3	
AD5	PR64B	3		PR78B	3	
AC5	PR64A	3		PR78A	3	
AD6	PR63D	3		PR77D	3	
AC6	PR63C	3		PR77C	3	
AB1	PR63B	3		PR77B	3	
AA1	PR63A	3		PR77A	3	
AD9	PR61D	3		PR75D	3	
AC9	PR61C	3		PR75C	3	
AB2	PR61B	3		PR75B	3	
AA2	PR61A	3		PR75A	3	
AD14	PR60D	3		PR74D	3	
AC14	PR60C	3		PR74C	3	
AB5	PR60B	3		PR74B	3	
AA5	PR60A	3		PR74A	3	
AD10	PR59D	3		PR73D	3	
AC10	PR59C	3		PR73C	3	
Y1	PR59B	3		PR73B	3	
W1	PR59A	3		PR73A	3	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
H18	PT77C	1	LDCN/SCS	PT93C	1	LDCN/SCS
F18	PT77B	1	D8/MPI_DATA8	PT93B	1	D8/MPI_DATA8
E18	PT77A	1	CS1/MPI_CS1	PT93A	1	CS1/MPI_CS1
H19	PT75D	1	D9/MPI_DATA9	PT90D	1	D9/MPI_DATA9
G19	PT75C	1	D10/MPI_DATA10	PT90C	1	D10/MPI_DATA10
D19	PT75B	1	CS0N/MPI_CS0N	PT90B	1	CS0N/MPI_CS0N
D18	PT75A	1	RDN/MPI_STRB_N	PT90A	1	RDN/MPI_STRB_N
J20	PT74D	1	WRN/MPI_WR_N	PT89D	1	WRN/MPI_WR_N
K20	PT74C	1	D7/MPI_DATA7	PT89C	1	D7/MPI_DATA7
E19	PT74B	1	D6/MPI_DATA6	PT89B	1	D6/MPI_DATA6
F19	PT74A	1	D5/MPI_DATA5	PT89A	1	D5/MPI_DATA5
K18	PT73D	1	D4/MPI_DATA4	PT87D	1	D4/MPI_DATA4
J18	PT73C	1	D3/MPI_DATA3	PT87C	1	D3/MPI_DATA3
A19	PT73B	1	D2/MPI_DATA2	PT87B	1	D2/MPI_DATA2
B19	PT73A	1	D1/MPI_DATA1	PT87A	1	D1/MPI_DATA1
H17	PT71D	1	D16/PCLKC1_3/MPI_DATA16	PT86D	1	D16/PCLKC1_3/MPI_DATA16
J17	PT71C	1	D17/PCLKT1_3/MPI_DATA17	PT86C	1	D17/PCLKT1_3/MPI_DATA17
B20	PT71B	1	D0/MPI_DATA0	PT86B	1	D0/MPI_DATA0
C20	PT71A	1	QOUT/CEON	PT86A	1	QOUT/CEON
M20	PT70D	1	VREF2_1	PT83D	1	VREF2_1
L20	PT70C	1	D18/MPI_DATA18	PT83C	1	D18/MPI_DATA18
F20	PT70B	1	DOUT	PT83B	1	DOUT
G20	PT70A	1	MCA_DONE_IN	PT83A	1	MCA_DONE_IN
K19	PT69D	1	D19/PCLKC1_2/MPI_DATA19	PT81D	1	D19/PCLKC1_2/MPI_DATA19
J19	PT69C	1	D20/PCLKT1_2/MPI_DATA20	PT81C	1	D20/PCLKT1_2/MPI_DATA20
D20	PT69B	1	MCA_CLK_P1_OUT	PT81B	1	MCA_CLK_P1_OUT
E20	PT69A	1	MCA_CLK_P1_IN	PT81A	1	MCA_CLK_P1_IN
H21	PT67D	1	D21/PCLKC1_1/MPI_DATA21	PT78D	1	D21/PCLKC1_1/MPI_DATA21
G21	PT67C	1	D22/PCLKT1_1/MPI_DATA22	PT78C	1	D22/PCLKT1_1/MPI_DATA22
B21	PT67B	1	MCA_CLK_P2_OUT	PT78B	1	MCA_CLK_P2_OUT
C21	PT67A	1	MCA_CLK_P2_IN	PT78A	1	MCA_CLK_P2_IN
M21	PT66D	1	MCA_DONE_OUT	PT75D	1	MCA_DONE_OUT
L21	PT66C	1	BUSYN/RCLK/SCK	PT75C	1	BUSYN/RCLK/SCK
A21	PT66B	1	DP0/MPI_PAR0	PT75B	1	DP0/MPI_PAR0
A20	PT66A	1	MPI_TA	PT75A	1	MPI_TA
J21	PT65D	1	D23/MPI_DATA23	PT73D	1	D23/MPI_DATA23
K21	PT65C	1	DP2/MPI_PAR2	PT73C	1	DP2/MPI_PAR2
E21	PT65B	1	PCLKC1_0	PT73B	1	PCLKC1_0
F21	PT65A	1	PCLKT1_0/MPI_CLK	PT73A	1	PCLKT1_0/MPI_CLK
G22	PT63D	1	DP3/PCLKC1_4/MPI_PAR3	PT71D	1	DP3/PCLKC1_4/MPI_PAR3
H22	PT63C	1	D24/PCLKT1_4/MPI_DATA24	PT71C	1	D24/PCLKT1_4/MPI_DATA24
A23	PT63B	1	MPI_RETRY	PT71B	1	MPI_RETRY
A22	PT63A	1	A0/MPI_ADDR14	PT71A	1	A0/MPI_ADDR14
L22	PT61D	1	A1/MPI_ADDR15	PT69D	1	A1/MPI_ADDR15
M22	PT61C	1	A2/MPI_ADDR16	PT69C	1	A2/MPI_ADDR16

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L8	VCCIO2	-		VCCIO2	-	
M3	VCCIO2	-		VCCIO2	-	
P7	VCCIO2	-		VCCIO2	-	
R4	VCCIO2	-		VCCIO2	-	
T12	VCCIO2	-		VCCIO2	-	
U8	VCCIO2	-		VCCIO2	-	
V3	VCCIO2	-		VCCIO2	-	
W11	VCCIO2	-		VCCIO2	-	
Y7	VCCIO2	-		VCCIO2	-	
AB3	VCCIO3	-		VCCIO3	-	
AC7	VCCIO3	-		VCCIO3	-	
AD11	VCCIO3	-		VCCIO3	-	
AE4	VCCIO3	-		VCCIO3	-	
AF8	VCCIO3	-		VCCIO3	-	
AG12	VCCIO3	-		VCCIO3	-	
AH3	VCCIO3	-		VCCIO3	-	
AJ7	VCCIO3	-		VCCIO3	-	
AK11	VCCIO3	-		VCCIO3	-	
AL4	VCCIO3	-		VCCIO3	-	
AM8	VCCIO3	-		VCCIO3	-	
AP3	VCCIO3	-		VCCIO3	-	
AR7	VCCIO3	-		VCCIO3	-	
AU4	VCCIO3	-		VCCIO3	-	
AL16	VCCIO4	-		VCCIO4	-	
AM13	VCCIO4	-		VCCIO4	-	
AM19	VCCIO4	-		VCCIO4	-	
AR11	VCCIO4	-		VCCIO4	-	
AR17	VCCIO4	-		VCCIO4	-	
AT14	VCCIO4	-		VCCIO4	-	
AT20	VCCIO4	-		VCCIO4	-	
AT8	VCCIO4	-		VCCIO4	-	
AW15	VCCIO4	-		VCCIO4	-	
AW21	VCCIO4	-		VCCIO4	-	
AW9	VCCIO4	-		VCCIO4	-	
AY12	VCCIO4	-		VCCIO4	-	
AY18	VCCIO4	-		VCCIO4	-	
AY6	VCCIO4	-		VCCIO4	-	
AL27	VCCIO5	-		VCCIO5	-	
AM24	VCCIO5	-		VCCIO5	-	
AM30	VCCIO5	-		VCCIO5	-	
AR26	VCCIO5	-		VCCIO5	-	
AR32	VCCIO5	-		VCCIO5	-	
AT23	VCCIO5	-		VCCIO5	-	
AT29	VCCIO5	-		VCCIO5	-	
AT35	VCCIO5	-		VCCIO5	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH22	VTT_5	5		VTT_5	5	
AJ22	VTT_5	5		VTT_5	5	
AJ23	VTT_5	5		VTT_5	5	
AJ24	VTT_5	5		VTT_5	5	
AJ25	VTT_5	5		VTT_5	5	
AB28	VTT_6	6		VTT_6	6	
AB29	VTT_6	6		VTT_6	6	
AE29	VTT_6	6		VTT_6	6	
AJ30	VTT_6	6		VTT_6	6	
AA28	VTT_7	7		VTT_7	7	
AA29	VTT_7	7		VTT_7	7	
R31	VTT_7	7		VTT_7	7	
V29	VTT_7	7		VTT_7	7	
Y24	GND	-		GND	-	
Y26	GND	-		GND	-	
Y8	GND	-		GND	-	
Y35	GND	-		GND	-	
AA16	VCC12	-		VCC12	-	
AA27	VCC12	-		VCC12	-	
AB16	VCC12	-		VCC12	-	
AB27	VCC12	-		VCC12	-	
AF16	VCC12	-		VCC12	-	
AF27	VCC12	-		VCC12	-	
AG17	VCC12	-		VCC12	-	
AG21	VCC12	-		VCC12	-	
G33	NC	-		NC	-	
G10	NC	-		NC	-	
M15	NC	-		NC	-	
L15	NC	-		NC	-	
K16	NC	-		NC	-	
J16	NC	-		NC	-	
M18	NC	-		NC	-	
L18	NC	-		NC	-	
M25	NC	-		NC	-	
L25	NC	-		NC	-	
J27	NC	-		NC	-	
K27	NC	-		NC	-	
L28	NC	-		NC	-	
M28	NC	-		NC	-	

1. Differential pair grouping within a PIC is A (True) and B (Complement) and C (True) and D (Complement).
2. The LatticeSC/M80 and LatticeSC/M115 in a 1704-pin package supports a 32-bit MPI interface.

Part Number Description

LF XXX XXX XX E PX – X XXXXXX X

LF = Lattice FPGA

Device Family
- LatticeSC FPGA
- LatticeSCM FPGA

SERDES Speed
- 3GA = 3.8G

Logic Capacity
- 15K LUTs
- 25K LUTs
- 40K LUTs
- 80K LUTs
- 115K LUTs

Supply Voltage
- E = 1.2V

Grade
- C = Commercial
- I = Industrial

Package[1]
- F256 = 256-ball fpBGA
- F900 = 900-ball fpBGA
- FF1020 = 1020-ball Organic fcBGA[2]
- FFA1020 = 1020-ball Organic fcBGA Revision 2
- FC1152 = 1152-ball Ceramic fcBGA[3]
- FF1152 = 1152-ball Organic fcBGA
- FC1704 = 1704-ball Ceramic fcBGA[3]
- FF1704 = 1704-ball Organic fcBGA

- FN256 = 256-ball Lead-Free fpBGA
- FN900 = 900-ball Lead-Free fpBGA
- FFN1020 = 1020-ball Lead-Free Organic fcBGA[2]
- FFAN1020 = 1020-ball Lead-Free Organic fcBGA Revision 2
- FCN1152 = 1152-ball Lead-Free Ceramic fcBGA[3]
- FFN1152 = 1152-ball Lead-Free Organic fcBGA
- FCN1704 = 1704-ball Lead-Free Ceramic fcBGA[3]
- FFN1704 = 1704-ball Lead-Free Organic fcBGA

Speed Grade
- -5 (Slowest)
- -6
- -7 (Fastest)[4]

Predefined Function (LatticeSCM Only)
- P1 = Initial MACO Option

1. fpBGA = 1.0 mm pitch BGA, fcBGA = 1.0 mm flip-chip BGA (organic and ceramic).
2. Converted to organic fcBGA per PCN #02A-10.
3. Converted to organic fcBGA per PCN #01A-10.
4. Not available in the LatticeSC115 and LatticeSCM115 devices.

Ordering Information

Depending on the speed and temperature grade, the device can either be dual marked or single marked. The commercial grade is one speed grade faster than the associated dual marked industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:

Lattice SC
LFSC3GA25E
6F900C-5I
XXXXXXXX

or

Lattice SC
LFSC3GA25E
7F900C
XXXXXXXX

Temperature Grade	Speed Grade	Single or Dual Mark?
Commercial	-7	Either OK
	-6	Dual Only
	-5	Single Only
Industrial	-6	Either OK
	-5	Dual Only

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Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FC1152I[1]	-6	Ceramic fcBGA	1152	IND	115.2
LFSC3GA115E-5FC1152I[1]	-5	Ceramic fcBGA	1152	IND	115.2
LFSC3GA115E-6FF1152I	-6	Organic fcBGA	1152	IND	115.2
LFSC3GA115E-5FF1152I	-5	Organic fcBGA	1152	IND	115.2
LFSC3GA115E-6FC1704I[1]	-6	Ceramic fcBGA	1704	IND	115.2
LFSC3GA115E-5FC1704I[1]	-5	Ceramic fcBGA	1704	IND	115.2
LFSC3GA115E-6FF1704I	-6	Organic fcBGA	1704	IND	115.2
LFSC3GA115E-5FF1704I	-5	Organic fcBGA	1704	IND	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FC1152I[1]	-6	Ceramic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-5FC1152I[1]	-5	Ceramic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-6FF1152I	-6	Organic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-5FF1152I	-5	Organic fcBGA	1152	IND	115.2
LFSCM3GA115EP1-6FC1704I[1]	-6	Ceramic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-5FC1704I[1]	-5	Ceramic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-6FF1704I	-6	Organic fcBGA	1704	IND	115.2
LFSCM3GA115EP1-5FF1704I	-5	Organic fcBGA	1704	IND	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA115EP1-6FCN1152C[1]	-6	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FCN1152C[1]	-5	Lead-Free Ceramic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FFN1152C	-6	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-5FFN1152C	-5	Lead-Free Organic fcBGA	1152	COM	115.2
LFSCM3GA115EP1-6FCN1704C[1]	-6	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FCN1704C[1]	-5	Lead-Free Ceramic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-6FFN1704C	-6	Lead-Free Organic fcBGA	1704	COM	115.2
LFSCM3GA115EP1-5FFN1704C	-5	Lead-Free Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Industrial

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA15E-6FN256I	-6	Lead-Free fpBGA	256	IND	15.2
LFSC3GA15E-5FN256I	-5	Lead-Free fpBGA	256	IND	15.2
LFSC3GA15E-6FN900I	-6	Lead-Free fpBGA	900	IND	15.2
LFSC3GA15E-5FN900I	-5	Lead-Free fpBGA	900	IND	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA15EP1-6FN256I	-6	Lead-Free fpBGA	256	IND	15.2
LFSCM3GA15EP1-5FN256I	-5	Lead-Free fpBGA	256	IND	15.2
LFSCM3GA15EP1-6FN900I	-6	Lead-Free fpBGA	900	IND	15.2
LFSCM3GA15EP1-5FN900I	-5	Lead-Free fpBGA	900	IND	15.2

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA25E-6FN900I	-6	Lead-Free fpBGA	900	IND	25.4
LFSC3GA25E-5FN900I	-5	Lead-Free fpBGA	900	IND	25.4
LFSC3GA25E-6FFN1020I[1]	-6	Lead-Free Organic fcBGA	1020	IND	25.4
LFSC3GA25E-5FFN1020I[1]	-5	Lead-Free Organic fcBGA	1020	IND	25.4
LFSC3GA25E-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4
LFSC3GA25E-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA25EP1-6FN900I	-6	Lead-Free fpBGA	900	IND	25.4
LFSCM3GA25EP1-5FN900I	-5	Lead-Free fpBGA	900	IND	25.4
LFSCM3GA25EP1-6FFN1020I[1]	-6	Lead-Free Organic fcBGA	1020	IND	25.4
LFSCM3GA25EP1-5FFN1020I[1]	-5	Lead-Free Organic fcBGA	1020	IND	25.4
LFSCM3GA25EP1-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4
LFSCM3GA25EP1-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	25.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA40E-6FFN1020I[1]	-6	Lead-Free Organic fcBGA	1020	IND	40.4
LFSC3GA40E-5FFN1020I[1]	-5	Lead-Free Organic fcBGA	1020	IND	40.4
LFSC3GA40E-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSC3GA40E-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSC3GA40E-6FCN1152I[2]	-6	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSC3GA40E-5FCN1152I[2]	-5	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSC3GA40E-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	40.4
LFSC3GA40E-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.