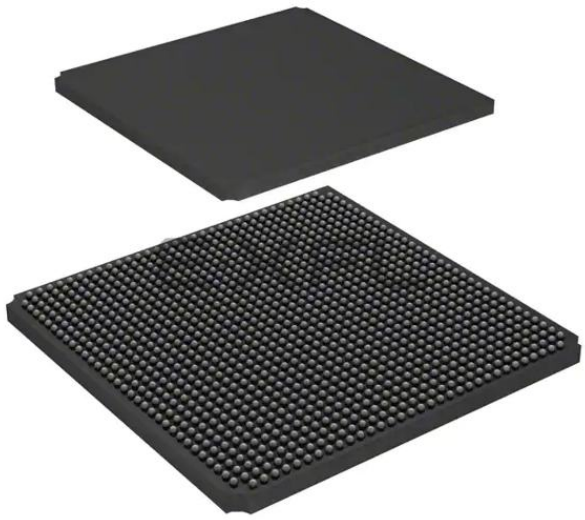
Lattice Semiconductor Corporation - LFSCM3GA80EP1-5FFN1152I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	20000
Number of Logic Elements/Cells	80000
Total RAM Bits	5816320
Number of I/O	660
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga80ep1-5ffn1152i

Modes of Operation

Each Slice is capable of four modes of operation: Logic, Ripple, RAM and ROM. Table 2-2 lists the modes and the capability of the Slice blocks.

Table 2-2. Slice Modes

	Logic	Ripple	RAM	ROM
PFU Slice	LUT 4x2 or LUT 5x1	2-bit Arithmetic Unit	SPR 16x2 DPR 16x2	ROM 16x2

Logic Mode

In this mode, the LUTs in each Slice are configured as combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any logic function with four inputs can be generated by programming this lookup table. Since there are two LUT4s per Slice, a LUT5 can be constructed within one Slice. Larger lookup tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other Slices in the PFU.

Ripple Mode

Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each Slice:

- Addition 2-bit
- Subtraction 2-bit
- Up counter 2-bit
- Down counter 2-bit
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B
  - A not-equal-to B
  - A less-than-or-equal-to B

Ripple Mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating Slices.

RAM Mode

In this mode, distributed RAM can be constructed using each LUT block as a 16x1-bit memory. Through the combination of LUTs and Slices, a variety of different memories can be constructed.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the Slice. Table 2-3 shows the number of Slices required to implement different distributed RAM primitives. Dual port memories involve the pairing of two Slices, one Slice functions as the read-write port. The other companion Slice supports the read-only port. For more information on RAM mode, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR16x2	DPR16x2
Number of Slices	1	2

Note: SPR = Single Port RAM, DPR = Dual Port RAM

ROM Mode

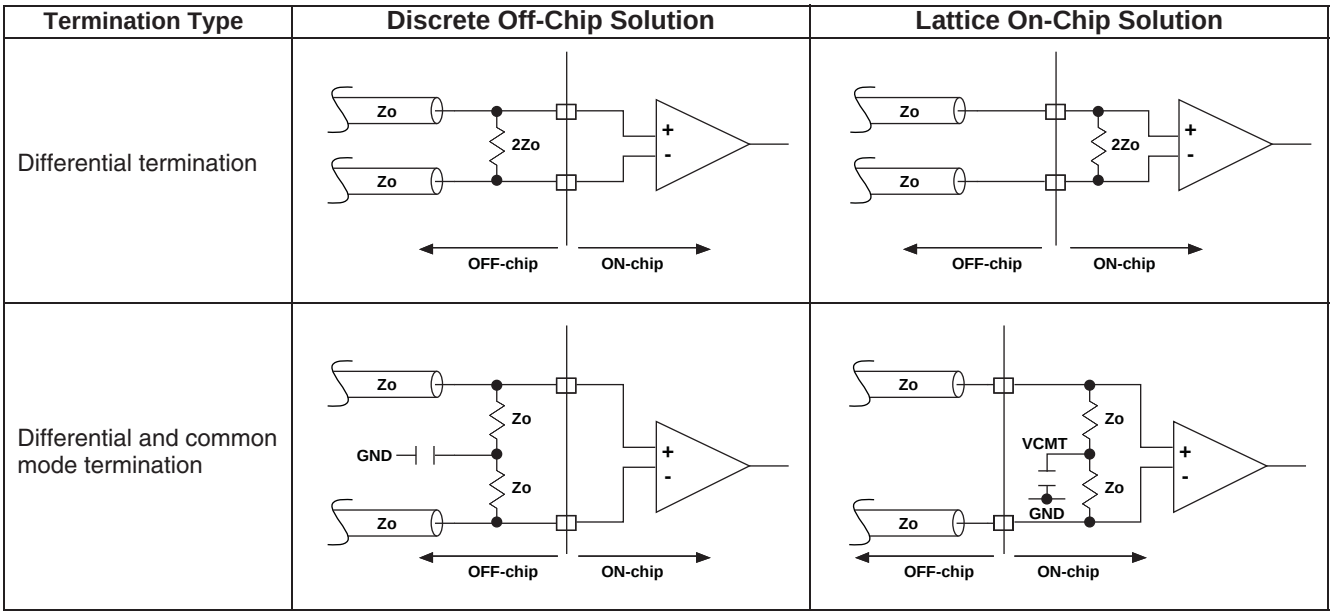
The ROM mode uses the same principal as the RAM modes, but without the Write port. Pre-loading is accomplished through the programming interface during configuration.

Differential Input Termination

The LatticeSC device allows two types of differential termination. The first is a single resistor across the differential inputs. The second is a center-tapped system where each input is terminated to the on-chip termination bus V_{CMT}. The V_{CMT} bus is DC-coupled through an internal capacitor to ground.

Figure 2-29 shows the differential termination schemes and Table 2-9 shows the nominal values of the termination resistors.

Figure 2-29. Differential Termination Scheme



Calibration

There are two calibration sources that are associated with the termination scheme used in the LatticeSC devices:

- DIFFR – This pin occurs in each bank that supports differential drivers and must be connected through a 1K+/-1% resistor to ground if differential outputs are used. Note that differential drivers are not supported in banks 1, 4 and 5.
- XRES – There is one of these pins per device. It is used for several functions including calibrating on-chip termination. This pin should always be connected through a 1K+/-1% resistor to ground.

The LatticeSC devices support two modes of calibration:

- Continuous – In this mode the SC devices continually calibrate the termination resistances. Calibration happens several times a second. Using this mode ensures that termination resistances remain calibrated as the silicon junction temperature changes.
- User Request – In this mode the calibration circuit operates continuously. However, the termination resistor values are only updated on the assertion of the calibration_update signal available to the core logic.

For more information on calibration, refer to the details of additional technical documentation at the end of this data sheet.

Hot Socketing

The LatticeSC devices have been carefully designed to ensure predictable behavior during power-up and power-down. To ensure proper power sequencing, care must be taken during power-up and power-down as described below. During power-up and power-down sequences, the I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits,

BLVDS

The LatticeSC devices support BLVDS standard. This standard is emulated using controlled impedance complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

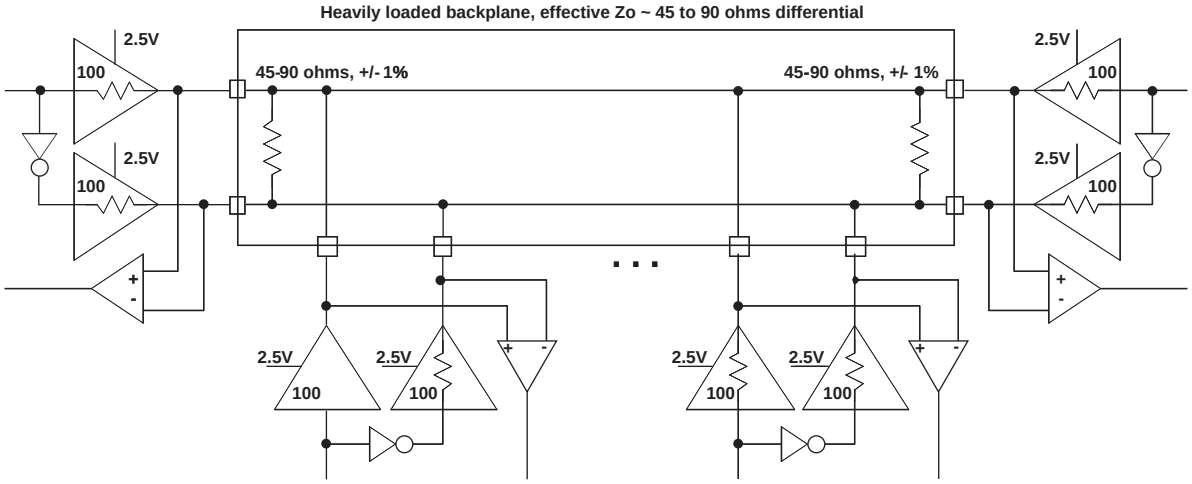


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Symbol	Description	Nominal		Units
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	100	100	ohm
R_{TLEFT}	Left end termination	45	90	ohm
R_{TRIGHT}	Right end termination	45	90	ohm
V_{OH}	Output high voltage	1.375	1.48	V
V_{OL}	Output low voltage	1.125	1.02	V
V_{OD}	Output differential voltage	0.25	0.46	V
V_{CM}	Output common mode voltage	1.25	1.25	V
I_{DC}	DC output current	11.2	10.2	mA

1. For input buffer, see LVDS table.

LatticeSC/M External Switching Characteristics[3]

Over Recommended Commercial Operating Conditions at VCC = 1.2V +/- 5%

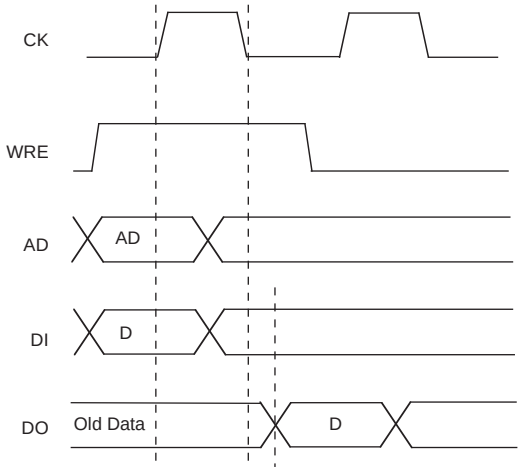
Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (using Primary Clock without PLL)[2]								
t_{CO}	Global Clock Input to Output - PIO Output Register	2.83	5.74	2.83	6.11	2.83	6.49	ns
t_{SU}	Global Clock Input Setup - PIO Input Register without fixed input delay	-0.66	—	-0.66	—	-0.66	—	ns
t_{H}	Global Clock Input Hold - PIO Input Register without fixed input delay	1.73	—	1.95	—	2.16	—	ns
t_{SU_IDLY}	Global Clock Input Setup - PIO Input Register with input delay	0.86	—	1.03	—	1.20	—	ns
t_{H_IDLY}	Global Clock Input Hold - PIO Input Register with input delay	-0.17	—	-0.17	—	-0.17	—	ns
f_{MAX_PFU}	Global Clock frequency of PFU register	—	700	—	700	—	700	MHz
f_{MAX_IO}	Global Clock frequency of I/O register	—	1000	—	1000	—	1000	MHz
t_{GC_SKEW}	Global Clock skew	—	89	—	103	—	116	ps
General I/O Pin Parameters (using Primary Clock with PLL)[1, 2]								
t_{CO}	Global Clock Input to Output - PIO Output Register	2.25	4.81	2.25	5.08	2.25	5.37	ns
t_{SU}	Global Clock Input Setup - PIO Input Register without fixed input delay	-0.07	—	-0.07	—	-0.07	—	ns
t_{H}	Global Clock Input Hold - PIO Input Register without fixed input delay	0.80	—	0.93	—	1.04	—	ns
General I/O Pin Parameters (using Edge Clock without PLL)[2]								
t_{CO}	Edge Clock Input to Output - PIO Output Register	2.38	4.77	2.38	5.04	2.38	5.33	ns
t_{SU}	Edge Clock Input Setup - PIO Input Register without fixed input delay	-0.08	—	-0.08	—	-0.08	—	ns
t_{H}	Edge Clock Input Hold - PIO Input Register	0.49	—	0.58	—	0.66	—	ns
t_{SU_IDLY}	Edge Clock Input Setup - PIO Input Register with input delay	0.81	—	0.97	—	1.12	—	ns
t_{H_IDLY}	Edge Clock Input Hold - PIO Input Register with input delay	-0.34	—	-0.34	—	-0.34	—	ns
t_{EC_SKEW}	Edge Clock skew	—	28	—	32	—	36	ps
General I/O Pin Parameters (using Latch FF without PLL)[2]								
t_{SU}	Latch FF, Input Setup - PIO Input Register without fixed input delay	-0.14	—	-0.14	—	-0.14	—	ns
t_{H}	Latch FF, Input Hold - PIO Input Register without fixed input delay	0.58	—	0.68	—	0.77	—	ns
t_{SU_IDLY}	Latch FF, Input Setup - PIO Input Register with input delay	0.70	—	0.68	—	0.77	—	ns
t_{H_IDLY}	Latch FF, Input Hold - PIO Input Register with input delay	-0.30	—	-0.30	—	-0.30	—	ns

1. No PLL delay tuning (clock injection removal mode, system clock feedback).
2. Using LVCMOS25 12mA I/O. Timing adders for other supported I/O technologies are specified in the LatticeSC Family Timing Adders table.
3. Complete Timing Parameters for a user design are incorporated when running ispLEVER. This is a sampling of the key timing parameters. Timing specs are for non-AIL applications.

Timing Diagrams

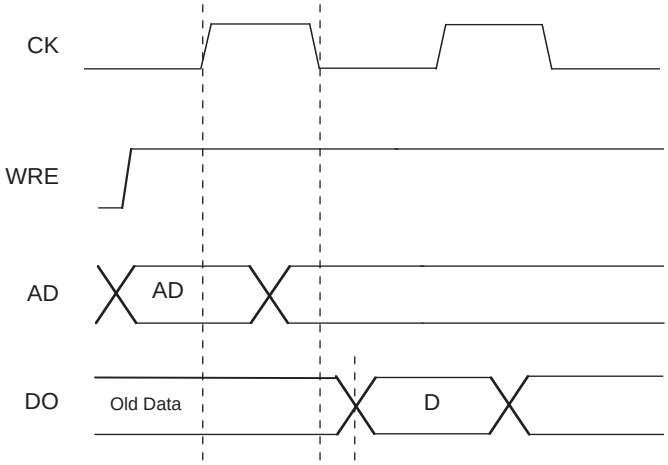
PFU Timing Diagrams

Figure 3-4. Slice Single/Dual Port Write Cycle Timing



Notes:
- Rising Edge for latching WREN, WAD and DATAIN.
- WREN must continue past falling edge clock.
- Data output occurs on negative edge.

Figure 3-5. Slice Single/Dual Port Read Cycle Timing



LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
E19	NC	-		NC	-	
G21	NC	-		NC	-	
G20	NC	-		NC	-	
G19	NC	-		NC	-	
F9	NC	-		NC	-	
A11	NC	-		NC	-	
G7	NC	-		NC	-	
AH9	NC	-		NC	-	
H8	VCC12	-		VCC12	-	
T8	VCC12	-		VCC12	-	
AB9	VCC12	-		VCC12	-	
AC8	VCC12	-		VCC12	-	
AB22	VCC12	-		VCC12	-	
AC23	VCC12	-		VCC12	-	
R23	VCC12	-		VCC12	-	
H23	VCC12	-		VCC12	-	
H15	VCC12	-		VCC12	-	
L24	VTT_2	2		VTT_2	2	
T23	VTT_2	2		VTT_2	2	
AC24	VTT_3	3		VTT_3	3	
T25	VTT_3	3		VTT_3	3	
W25	VTT_3	3		VTT_3	3	
AD24	VTT_4	4		VTT_4	4	
AE17	VTT_4	4		VTT_4	4	
AE18	VTT_4	4		VTT_4	4	
AC15	VTT_5	5		VTT_5	5	
AD16	VTT_5	5		VTT_5	5	
AE9	VTT_5	5		VTT_5	5	
AA6	VTT_6	6		VTT_6	6	
T7	VTT_6	6		VTT_6	6	
W6	VTT_6	6		VTT_6	6	
L7	VTT_7	7		VTT_7	7	
P7	VTT_7	7		VTT_7	7	
AA10	VCC	-		VCC	-	
AA11	VCC	-		VCC	-	
AA12	VCC	-		VCC	-	
AA13	VCC	-		VCC	-	
AA14	VCC	-		VCC	-	
AA17	VCC	-		VCC	-	
AA18	VCC	-		VCC	-	
AA19	VCC	-		VCC	-	
AA20	VCC	-		VCC	-	
AA21	VCC	-		VCC	-	
AA22	VCC	-		VCC	-	
AA9	VCC	-		VCC	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB10	VCC	-		VCC	-	
AB21	VCC	-		VCC	-	
J10	VCC	-		VCC	-	
J21	VCC	-		VCC	-	
K10	VCC	-		VCC	-	
K11	VCC	-		VCC	-	
K12	VCC	-		VCC	-	
K13	VCC	-		VCC	-	
K14	VCC	-		VCC	-	
K17	VCC	-		VCC	-	
K18	VCC	-		VCC	-	
K19	VCC	-		VCC	-	
K20	VCC	-		VCC	-	
K21	VCC	-		VCC	-	
K22	VCC	-		VCC	-	
K9	VCC	-		VCC	-	
L10	VCC	-		VCC	-	
L21	VCC	-		VCC	-	
M10	VCC	-		VCC	-	
M21	VCC	-		VCC	-	
N10	VCC	-		VCC	-	
N21	VCC	-		VCC	-	
P10	VCC	-		VCC	-	
P21	VCC	-		VCC	-	
U10	VCC	-		VCC	-	
U21	VCC	-		VCC	-	
V10	VCC	-		VCC	-	
V21	VCC	-		VCC	-	
W10	VCC	-		VCC	-	
W21	VCC	-		VCC	-	
Y10	VCC	-		VCC	-	
Y21	VCC	-		VCC	-	
H11	VCCAUX	-		VCCAUX	-	
H12	VCCAUX	-		VCCAUX	-	
H19	VCCAUX	-		VCCAUX	-	
H20	VCCAUX	-		VCCAUX	-	
M23	VCCAUX	-		VCCAUX	-	
M24	VCCAUX	-		VCCAUX	-	
N23	VCCAUX	-		VCCAUX	-	
N24	VCCAUX	-		VCCAUX	-	
U23	VCCAUX	-		VCCAUX	-	
U24	VCCAUX	-		VCCAUX	-	
V23	VCCAUX	-		VCCAUX	-	
V24	VCCAUX	-		VCCAUX	-	
W23	VCCAUX	-		VCCAUX	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
W24	VCCAUX	-		VCCAUX	-	
AC17	VCCAUX	-		VCCAUX	-	
AC18	VCCAUX	-		VCCAUX	-	
AC19	VCCAUX	-		VCCAUX	-	
AD17	VCCAUX	-		VCCAUX	-	
AD18	VCCAUX	-		VCCAUX	-	
AD19	VCCAUX	-		VCCAUX	-	
AC12	VCCAUX	-		VCCAUX	-	
AC13	VCCAUX	-		VCCAUX	-	
AC14	VCCAUX	-		VCCAUX	-	
AD12	VCCAUX	-		VCCAUX	-	
AD13	VCCAUX	-		VCCAUX	-	
AD14	VCCAUX	-		VCCAUX	-	
U7	VCCAUX	-		VCCAUX	-	
U8	VCCAUX	-		VCCAUX	-	
V7	VCCAUX	-		VCCAUX	-	
V8	VCCAUX	-		VCCAUX	-	
W7	VCCAUX	-		VCCAUX	-	
W8	VCCAUX	-		VCCAUX	-	
M7	VCCAUX	-		VCCAUX	-	
M8	VCCAUX	-		VCCAUX	-	
N7	VCCAUX	-		VCCAUX	-	
N8	VCCAUX	-		VCCAUX	-	
H10	VCCIO1	-		VCCIO1	-	
H21	VCCIO1	-		VCCIO1	-	
H22	VCCIO1	-		VCCIO1	-	
H9	VCCIO1	-		VCCIO1	-	
J11	VCCIO1	-		VCCIO1	-	
J12	VCCIO1	-		VCCIO1	-	
J13	VCCIO1	-		VCCIO1	-	
J14	VCCIO1	-		VCCIO1	-	
J15	VCCIO1	-		VCCIO1	-	
J16	VCCIO1	-		VCCIO1	-	
J17	VCCIO1	-		VCCIO1	-	
J18	VCCIO1	-		VCCIO1	-	
J19	VCCIO1	-		VCCIO1	-	
J20	VCCIO1	-		VCCIO1	-	
J23	VCCIO2	-		VCCIO2	-	
J24	VCCIO2	-		VCCIO2	-	
K23	VCCIO2	-		VCCIO2	-	
K24	VCCIO2	-		VCCIO2	-	
L22	VCCIO2	-		VCCIO2	-	
L23	VCCIO2	-		VCCIO2	-	
M22	VCCIO2	-		VCCIO2	-	
N22	VCCIO2	-		VCCIO2	-	

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AJ27	GND	-		GND	-	
AF23	GND	-		GND	-	
AF22	GND	-		GND	-	
AE27	GND	-		GND	-	
AA27	GND	-		GND	-	
AB29	GND	-		GND	-	
Y26	GND	-		GND	-	
AC30	GND	-		GND	-	
Y29	GND	-		GND	-	
F30	GND	-		GND	-	
E27	GND	-		GND	-	
F27	GND	-		GND	-	
P25	GND	-		GND	-	
H29	GND	-		GND	-	
K29	GND	-		GND	-	
R24	GND	-		GND	-	
M28	GND	-		GND	-	
J27	GND	-		GND	-	
N26	GND	-		GND	-	
E20	GND	-		GND	-	
E21	GND	-		GND	-	
F21	GND	-		GND	-	
F23	GND	-		GND	-	
G23	GND	-		GND	-	
D21	GND	-		GND	-	
D20	GND	-		GND	-	
E18	GND	-		GND	-	
C20	GND	-		GND	-	
C11	GND	-		GND	-	
A12	GND	-		GND	-	
E11	GND	-		GND	-	
F8	GND	-		GND	-	
G8	GND	-		GND	-	
D11	GND	-		GND	-	
D10	GND	-		GND	-	
H7	GND	-		GND	-	
F10	GND	-		GND	-	
E10	GND	-		GND	-	
AC16	NC	-		NC	-	
J22	VCC	-		VCC	-	
J9	VCC	-		VCC	-	
B2	NC	-		NC	-	
C2	RESPN_ULC	-		RESPN_ULC	-	
C29	RESPN_URC	-		RESPN_URC	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2]

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
C28	A_REFCLKP_L	-		A_REFCLKP_L	-	
D28	A_REFCLKN_L	-		A_REFCLKN_L	-	
B28	VCC12	-		VCC12	-	
F28	RESP_ULC	-		RESP_ULC	-	
J21	RESETN	1		RESETN	1	
J20	TSALLN	1		TSALLN	1	
K20	DONE	1		DONE	1	
K21	INITN	1		INITN	1	
K23	M0	1		M0	1	
J23	M1	1		M1	1	
J24	M2	1		M2	1	
K24	M3	1		M3	1	
K25	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
J25	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
K26	PL16C	7		PL16C	7	
K27	PL16D	7		PL16D	7	
D32	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
D31	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
M23	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
N23	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
E32	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
E31	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
J28	PL18C	7		PL18C	7	
K28	PL18D	7	VREF2_7	PL18D	7	VREF2_7
F32	PL20A	7		PL21A	7	
F31	PL20B	7		PL21B	7	
L25	PL20C	7		PL21C	7	
L26	PL20D	7		PL21D	7	
G31	PL21A	7		PL22A	7	
G32	PL21B	7		PL22B	7	
J29	PL22A	7		PL25A	7	
H29	PL22B	7		PL25B	7	
M25	PL22C	7		PL25C	7	
N25	PL22D	7		PL25D	7	
H31	PL25A	7		PL23A	7	
H32	PL25B	7		PL23B	7	
M24	PL25C	7	VREF1_7	PL23C	7	VREF1_7
N24	PL25D	7	DIFFR_7	PL23D	7	DIFFR_7
L32	PL26A	7	PCLKT7_1	PL35A	7	PCLKT7_1
M32	PL26B	7	PCLKC7_1	PL35B	7	PCLKC7_1
R25	PL26C	7	PCLKT7_3	PL35C	7	PCLKT7_3
R24	PL26D	7	PCLKC7_3	PL35D	7	PCLKC7_3
N31	PL27A	7	PCLKT7_0	PL36A	7	PCLKT7_0
N32	PL27B	7	PCLKC7_0	PL36B	7	PCLKC7_0
P27	PL27C	7	PCLKT7_2	PL36C	7	PCLKT7_2
P28	PL27D	7	PCLKC7_2	PL36D	7	PCLKC7_2
P30	PL29A	6	PCLKT6_0	PL38A	6	PCLKT6_0
P29	PL29B	6	PCLKC6_0	PL38B	6	PCLKC6_0
T23	PL29C	6	PCLKT6_1	PL38C	6	PCLKT6_1
T24	PL29D	6	PCLKC6_1	PL38D	6	PCLKC6_1

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L1	PR31A	2		PR43A	2	
T10	PR30D	2		PR42D	2	
U10	PR30C	2		PR42C	2	
N2	PR30B	2		PR42B	2	
M2	PR30A	2		PR42A	2	
R11	PR29D	2		PR37D	2	
P11	PR29C	2		PR37C	2	
N4	PR29B	2		PR37B	2	
M4	PR29A	2		PR37A	2	
N5	PR27D	2		PR35D	2	
M5	PR27C	2		PR35C	2	
L2	PR27B	2		PR35B	2	
K2	PR27A	2		PR35A	2	
P8	PR26D	2		PR33D	2	
N8	PR26C	2		PR33C	2	
J2	PR26B	2		PR33B	2	
H2	PR26A	2		PR33A	2	
M6	PR25D	2		PR31D	2	
L6	PR25C	2		PR31C	2	
K3	PR25B	2		PR31B	2	
J3	PR25A	2		PR31A	2	
M8	PR23D	2	DIFFR_2	PR29D	2	DIFFR_2
L8	PR23C	2	VREF1_2	PR29C	2	VREF1_2
K4	PR23B	2		PR29B	2	
J4	PR23A	2		PR29A	2	
M7	PR22D	2		PR21D	2	
L7	PR22C	2		PR21C	2	
J5	PR22B	2		PR21B	2	
H5	PR22A	2		PR21A	2	
N9	PR21D	2		PR20D	2	
P9	PR21C	2		PR20C	2	
G3	PR21B	2		PR20B	2	
F3	PR21A	2		PR20A	2	
J6	PR18D	2	VREF2_2	PR18D	2	VREF2_2
H6	PR18C	2		PR18C	2	
E2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
D2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
G4	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
F4	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
J7	PR16D	2		PR16D	2	
H7	PR16C	2		PR16C	2	
G5	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
F5	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
H21	PT38D	1	D28/PCLKC1_6/MPI_DATA28	PT57D	1	D28/PCLKC1_6/MPI_DATA28
J21	PT38C	1	D29/PCLKT1_6/MPI_DATA29	PT57C	1	D29/PCLKT1_6/MPI_DATA29
A19	PT38B	1	A9/MPI_ADDR23	PT57B	1	A9/MPI_ADDR23
B19	PT38A	1	A10/MPI_ADDR24	PT57A	1	A10/MPI_ADDR24
H22	PT37D	1	D30/PCLKC1_7/MPI_DATA30	PT56D	1	D30/PCLKC1_7/MPI_DATA30
J22	PT37C	1	D31/PCLKT1_7/MPI_DATA31	PT56C	1	D31/PCLKT1_7/MPI_DATA31
F20	PT37B	1	A11/MPI_ADDR25	PT56B	1	A11/MPI_ADDR25
G20	PT37A	1	A12/MPI_ADDR26	PT56A	1	A12/MPI_ADDR26
K21	PT35D	1	D11/MPI_DATA11	PT55D	1	D11/MPI_DATA11
K22	PT35C	1	D12/MPI_DATA12	PT55C	1	D12/MPI_DATA12
A20	PT35B	1	A13/MPI_ADDR27	PT55B	1	A13/MPI_ADDR27
B20	PT35A	1	A14/MPI_ADDR28	PT55A	1	A14/MPI_ADDR28
L21	PT33D	1	A16/MPI_ADDR30	PT53D	1	A16/MPI_ADDR30
L20	PT33C	1	D13/MPI_DATA13	PT53C	1	D13/MPI_DATA13
D20	PT33B	1	A15/MPI_ADDR29	PT53B	1	A15/MPI_ADDR29
E20	PT33A	1	A17/MPI_ADDR31	PT53A	1	A17/MPI_ADDR31
L19	PT30D	1	A19/MPI_TSIZ1	PT52D	1	A19/MPI_TSIZ1
K19	PT30C	1	A20/MPI_BDIP	PT52C	1	A20/MPI_BDIP
D21	PT30B	1	A18/MPI_TSIZ0	PT52B	1	A18/MPI_TSIZ0
E21	PT30A	1	MPI_TEA	PT52A	1	MPI_TEA
M20	PT28D	1	D14/MPI_DATA14	PT51D	1	D14/MPI_DATA14
M19	PT28C	1	DP1/MPI_PAR1	PT51C	1	DP1/MPI_PAR1
F21	PT27B	1	A21/MPI_BURST	PT51B	1	A21/MPI_BURST
G21	PT27A	1	D15/MPI_DATA15	PT51A	1	D15/MPI_DATA15
H24	B_REFCLKP_L	-		B_REFCLKP_L	-	
J24	B_REFCLKN_L	-		B_REFCLKN_L	-	
L22	VCC12	-		VCC12	-	
E26	B_VDDIB3_L	-		B_VDDIB3_L	-	
G22	VCC12	-		VCC12	-	
E22	B_HDINP3_L	-	PCS 361 CH 3 IN P	B_HDINP3_L	-	PCS 361 CH 3 IN P
F22	B_HDINN3_L	-	PCS 361 CH 3 IN N	B_HDINN3_L	-	PCS 361 CH 3 IN N
A21	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P	B_HDOUTP3_L	-	PCS 361 CH 3 OUT P
L24	VCC12	-		VCC12	-	
B21	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N	B_HDOUTN3_L	-	PCS 361 CH 3 OUT N
D22	B_VDDOB3_L	-		B_VDDOB3_L	-	
B22	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N	B_HDOUTN2_L	-	PCS 361 CH 2 OUT N
D23	B_VDDOB2_L	-		B_VDDOB2_L	-	
A22	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P	B_HDOUTP2_L	-	PCS 361 CH 2 OUT P
K24	VCC12	-		VCC12	-	
F23	B_HDINN2_L	-	PCS 361 CH 2 IN N	B_HDINN2_L	-	PCS 361 CH 2 IN N
E23	B_HDINP2_L	-	PCS 361 CH 2 IN P	B_HDINP2_L	-	PCS 361 CH 2 IN P
D26	B_VDDIB2_L	-		B_VDDIB2_L	-	
G23	VCC12	-		VCC12	-	
D27	B_VDDIB1_L	-		B_VDDIB1_L	-	
G24	VCC12	-		VCC12	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

Ball Number	LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function
AN15	PB89A	4	PCLKT4_2
AN14	PB89B	4	PCLKC4_2
AE16	PB89C	4	PCLKT4_7
AD16	PB89D	4	PCLKC4_7
AK15	PB90A	4	PCLKT4_1
AK14	PB90B	4	PCLKC4_1
AG15	PB90C	4	PCLKT4_6
AG14	PB90D	4	PCLKC4_6
AM13	PB91A	4	PCLKT4_0
AM12	PB91B	4	PCLKC4_0
AJ12	PB91C	4	VREF2_4
AJ11	PB91D	4	
AL13	PB93A	4	PCLKT4_5
AL12	PB93B	4	PCLKC4_5
AH12	PB93C	4	
AH11	PB93D	4	
AN13	PB94A	4	PCLKT4_3
AN12	PB94B	4	PCLKC4_3
AD14	PB94C	4	PCLKT4_4
AD15	PB94D	4	PCLKC4_4
AP13	PB87A	4	
AP12	PB87B	4	
AK13	PB87C	4	
AK12	PB87D	4	
AP11	PB97A	4	
AP10	PB97B	4	
AN11	PB113A	4	
AN10	PB113B	4	
AF14	PB113C	4	
AF13	PB113D	4	
AM10	PB115A	4	
AM9	PB115B	4	
AE14	PB115C	4	
AE13	PB115D	4	
AP9	PB118A	4	
AP8	PB118B	4	
AK11	PB118C	4	
AK10	PB118D	4	
AL10	PB121A	4	
AL9	PB121B	4	
AF12	PB121C	4	
AF11	PB121D	4	
AN9	PB123A	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2]

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
G34	A_REFCLKP_L	-		A_REFCLKP_L	-	
H34	A_REFCLKN_L	-		A_REFCLKN_L	-	
N30	VCC12	-		VCC12	-	
H33	RESP_ULC	-		RESP_ULC	-	
P25	RESETN	1		RESETN	1	
P26	TSALLN	1		TSALLN	1	
P31	DONE	1		DONE	1	
P23	INITN	1		INITN	1	
P30	M0	1		M0	1	
P22	M1	1		M1	1	
P24	M2	1		M2	1	
R22	M3	1		M3	1	
J37	PL16A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
J38	PL16B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
P32	PL16C	7		PL15C	7	
R32	PL16D	7		PL15D	7	
G40	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
H40	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N33	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P33	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
G41	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
H41	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
T29	PL18C	7		PL18C	7	
U29	PL18D	7	VREF2_7	PL18D	7	VREF2_7
G42	PL20A	7		PL19A	7	
H42	PL20B	7		PL19B	7	
M34	PL20C	7		PL19C	7	
M35	PL20D	7		PL19D	7	
K37	PL21A	7		PL26A	7	
L37	PL21B	7		PL26B	7	
N34	PL21C	7		PL26C	7	
P34	PL21D	7		PL26D	7	
K38	PL22A	7		PL30A	7	
L38	PL22B	7		PL30B	7	
T33	PL22C	7		PL30C	7	
R33	PL22D	7		PL30D	7	
J41	PL24A	7		PL34A	7	
K41	PL24B	7		PL34B	7	
U31	PL24C	7		PL34C	7	
V31	PL24D	7		PL34D	7	
K42	PL25A	7		PL38A	7	
J42	PL25B	7		PL38B	7	
J36	PL25C	7		PL38C	7	
K36	PL25D	7		PL38D	7	
N38	PL26A	7		PL40A	7	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
BB12	PB88B	4		PB102B	4	
AM17	PB88C	4		PB102C	4	
AL17	PB88D	4		PB102D	4	
AW14	PB89A	4		PB103A	4	
AW13	PB89B	4		PB103B	4	
AP16	PB89C	4		PB103C	4	
AN16	PB89D	4		PB103D	4	
BA13	PB91A	4		PB105A	4	
BA12	PB91B	4		PB105B	4	
AU13	PB91C	4		PB105C	4	
AU12	PB91D	4		PB105D	4	
BB11	PB92A	4		PB106A	4	
BB10	PB92B	4		PB106B	4	
AP15	PB92C	4		PB106C	4	
AN15	PB92D	4		PB106D	4	
AV13	PB93A	4		PB107A	4	
AV12	PB93B	4		PB107B	4	
AT13	PB93C	4		PB107C	4	
AT12	PB93D	4		PB107D	4	
BA11	PB95A	4		PB109A	4	
BA10	PB95B	4		PB109B	4	
AR13	PB95C	4		PB109C	4	
AR12	PB95D	4		PB109D	4	
AY11	PB96A	4		PB110A	4	
AY10	PB96B	4		PB110B	4	
AP14	PB96C	4		PB110C	4	
AN14	PB96D	4		PB110D	4	
BB9	PB97A	4		PB111A	4	
BB8	PB97B	4		PB111B	4	
AU11	PB97C	4		PB111C	4	
AU10	PB97D	4		PB111D	4	
AW11	PB99A	4		PB113A	4	
AW10	PB99B	4		PB113B	4	
AJ16	PB99C	4		PB113C	4	
AJ17	PB99D	4		PB113D	4	
BA9	PB100A	4		PB114A	4	
BA8	PB100B	4		PB114B	4	
AM15	PB100C	4		PB114C	4	
AL15	PB100D	4		PB114D	4	
AV11	PB101A	4		PB115A	4	
AV10	PB101B	4		PB115B	4	
AP13	PB101C	4		PB115C	4	
AP12	PB101D	4		PB115D	4	
BB7	PB103A	4		PB117A	4	
BB6	PB103B	4		PB117B	4	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
J1	PR25B	2		PR38B	2	
K1	PR25A	2		PR38A	2	
V12	PR24D	2		PR34D	2	
U12	PR24C	2		PR34C	2	
K2	PR24B	2		PR34B	2	
J2	PR24A	2		PR34A	2	
R10	PR22D	2		PR30D	2	
T10	PR22C	2		PR30C	2	
L5	PR22B	2		PR30B	2	
K5	PR22A	2		PR30A	2	
P9	PR21D	2		PR26D	2	
N9	PR21C	2		PR26C	2	
L6	PR21B	2		PR26B	2	
K6	PR21A	2		PR26A	2	
M8	PR20D	2		PR19D	2	
M9	PR20C	2		PR19C	2	
H1	PR20B	2		PR19B	2	
G1	PR20A	2		PR19A	2	
U14	PR18D	2	VREF2_2	PR18D	2	VREF2_2
T14	PR18C	2		PR18C	2	
H2	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
G2	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
P10	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
N10	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
H3	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
G3	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
R11	PR16D	2		PR15D	2	
P11	PR16C	2		PR15C	2	
J5	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
J6	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
P18	VCCJ	-		VCCJ	-	
P19	TDO	-	TDO	TDO	-	TDO
R21	TMS	-		TMS	-	
P20	TCK	-		TCK	-	
P12	TDI	-		TDI	-	
P17	PROGRAMN	1		PROGRAMN	1	
P21	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
P13	CCLK	1		CCLK	1	
H10	RESP_URC	-		RESP_URC	-	
N13	VCC12	-		VCC12	-	
H9	A_REFCLKN_R	-		A_REFCLKN_R	-	
G9	A_REFCLKP_R	-		A_REFCLKP_R	-	
F2	VCC12	-		VCC12	-	
H4	A_VDDIB0_R	-		A_VDDIB0_R	-	
C1	A_HDINP0_R	-	PCS 3E0 CH 0 IN P	A_HDINP0_R	-	PCS 3E0 CH 0 IN P

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AC24	GND	-		GND	-	
AC26	GND	-		GND	-	
AC35	GND	-		GND	-	
AC8	GND	-		GND	-	
AD12	GND	-		GND	-	
AD16	GND	-		GND	-	
AD18	GND	-		GND	-	
AD20	GND	-		GND	-	
AD23	GND	-		GND	-	
AD25	GND	-		GND	-	
AD27	GND	-		GND	-	
AD31	GND	-		GND	-	
AE17	GND	-		GND	-	
AE19	GND	-		GND	-	
AE24	GND	-		GND	-	
AE26	GND	-		GND	-	
AE3	GND	-		GND	-	
AE39	GND	-		GND	-	
AF18	GND	-		GND	-	
AF20	GND	-		GND	-	
AF23	GND	-		GND	-	
AF25	GND	-		GND	-	
AF36	GND	-		GND	-	
AF7	GND	-		GND	-	
AG11	GND	-		GND	-	
AG16	GND	-		GND	-	
AG19	GND	-		GND	-	
AG24	GND	-		GND	-	
AG27	GND	-		GND	-	
AG32	GND	-		GND	-	
AH15	GND	-		GND	-	
AH28	GND	-		GND	-	
AH4	GND	-		GND	-	
AH40	GND	-		GND	-	
AJ35	GND	-		GND	-	
AJ8	GND	-		GND	-	
AK12	GND	-		GND	-	
AK31	GND	-		GND	-	
AL13	GND	-		GND	-	
AL19	GND	-		GND	-	
AL24	GND	-		GND	-	
AL3	GND	-		GND	-	
AL30	GND	-		GND	-	
AL39	GND	-		GND	-	
AM16	GND	-		GND	-	

Commercial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-7FC1152C[1]	-7	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-6FC1152C[1]	-6	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-5FC1152C[1]	-5	Ceramic fcBGA	1152	COM	80.1
LFSC3GA80E-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSC3GA80E-7FC1704C[1]	-7	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-6FC1704C[1]	-6	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-5FC1704C[1]	-5	Ceramic fcBGA	1704	COM	80.1
LFSC3GA80E-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSC3GA80E-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-7FC1152C[1]	-7	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FC1152C[1]	-6	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FC1152C[1]	-5	Ceramic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FF1152C	-7	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-6FF1152C	-6	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-5FF1152C	-5	Organic fcBGA	1152	COM	80.1
LFSCM3GA80EP1-7FC1704C[1]	-7	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FC1704C[1]	-6	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FC1704C[1]	-5	Ceramic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-7FF1704C	-7	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-6FF1704C	-6	Organic fcBGA	1704	COM	80.1
LFSCM3GA80EP1-5FF1704C	-5	Organic fcBGA	1704	COM	80.1

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA115E-6FC1152C[1]	-6	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-5FC1152C[1]	-5	Ceramic fcBGA	1152	COM	115.2
LFSC3GA115E-6FF1152C	-6	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-5FF1152C	-5	Organic fcBGA	1152	COM	115.2
LFSC3GA115E-6FC1704C[1]	-6	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-5FC1704C[1]	-5	Ceramic fcBGA	1704	COM	115.2
LFSC3GA115E-6FF1704C	-6	Organic fcBGA	1704	COM	115.2
LFSC3GA115E-5FF1704C	-5	Organic fcBGA	1704	COM	115.2

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-6FFN1020I[1]	-6	Lead-Free Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-5FFN1020I[1]	-5	Lead-Free Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-6FFAN1020I	-6	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-5FFAN1020I	-5	Lead-Free Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-6FCN1152I[2]	-6	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FCN1152I[2]	-5	Lead-Free Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-6FCN1152I[1]	-6	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-5FCN1152I[1]	-5	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	80.1
LFSC3GA80E-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	80.1
LFSC3GA80E-6FCN1704I[1]	-6	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-5FCN1704I[1]	-5	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	80.1
LFSC3GA80E-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-6FCN1152I[1]	-6	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FCN1152I[1]	-5	Lead-Free Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FFN1152I	-6	Lead-Free Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FFN1152I	-5	Lead-Free Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FCN1704I[1]	-6	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FCN1704I[1]	-5	Lead-Free Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-6FFN1704I	-6	Lead-Free Organic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FFN1704I	-5	Lead-Free Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Date	Version	Section	Change Summary
September 2007	01.7	Pinout Information	Added Thermal Management text section.
		Supplemental Information	Updated title list.
November 2007	01.8	Ordering Information	Removed -7 speed grade information for 115K LUT devices in the Ordering Information tables.
January 2008	01.9	Introduction	Corrections/Additions to memory controller list (Tables 1-2).
		Architecture	AIL Overview – Modified power used by AIL block.
			PURESPEED I/O Buffer Banks – Modified VTT termination info. Added info about complimentary drivers for all banks.
			Supported Source Synchronous Interfaces – Modified data for DDRII in Table 2-11.
		DC and Switching Characteristics	Recommended Operating Conditions – Changed footnote 3.
			Initialization and Standby Supply Current – Inserted a paragraph with info regarding the table. Also updated the table.
			Typical Building Block Function Performance – Added VCC=1.2V=1.2V+/-5% above Pin to Pin Performance table.
			LatticeSC External Switching Characteristics – Added VCC=1.2V=1.2V+/-5% above table. Reworded footnote 3.
			LatticeSC Family Timing Adders – Added VCC=1.2V=1.2V+/-5% above table.
			LatticeSC Internal Timing Parameters – Added VCC=1.2V=1.2V+/-5% above table. Reworded footnote 1.
			GSR Timing – Added a new table for Internal System Bus Timing after GSR Timing.
			LatticeSC sysCONFIG Port Timing – Corrected sysCONFIG SPI Port information.
		Pinout Information	Signal Descriptions – Modified info for VTT_x, PROBE_VCC, and PROBE_GND. Modified info for [LOC]_DLL[T,C]_IN[C,D,E,F].
		Supplemental Information	Updated list of technical notes, added reference to LatticeSC/M flexiPCS Data Sheet.
March 2008	02.0	DC and Switching Characteristics	Updated Internal Timing Parameters table.
			Updated Read Mode timing diagram.
			Updated Read Mode with Input Registers Only timing diagram.
June 2008	02.1	—	Data sheet status changed from preliminary to final.
		Architecture	Removed Read-Before-Write sysMEM EBR mode.
		DC and Switching Characteristics	Updated LatticeSC/M External Switching Characteristics table.
			Updated LatticeSC/M Internal Timing Parameters table.
			Removed Read-Before-Write sysMEM EBR mode.
December 2008	02.2	Architecture	Output/Tristate DDR/Shift Register Block Diagram - corrected connection to POS.
		DC and Switching Characteristics	DC and Switching Characteristics table - updated data for $t_{SUI\_PIO.}$
			Added $T_{R,}$ T_F parameter to PURESPEED I/O Differential Electrical Characteristics (LVDS) table.
		Multiple	Removed references to HyperTransport throughout the data sheet.
January 2010	02.3	Introduction	Updated per PCN #01A-10 (ceramic fcBGA conversion to organic fcBGA for the 1152-ball and 1704-ball fcBGA packages) and PCN #02A-10 (1020-ball organic fcBGA conversion to 1020-ball organic fcBGA revision 2 package).
		Ordering Information	