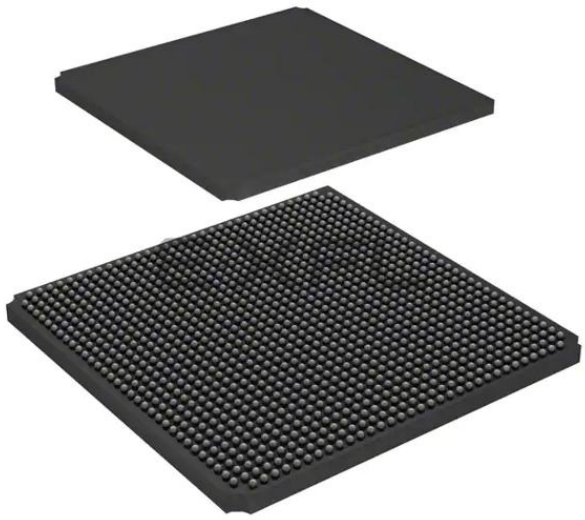
Lattice Semiconductor Corporation - LFSCM3GA80EP1-6FFN1152C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

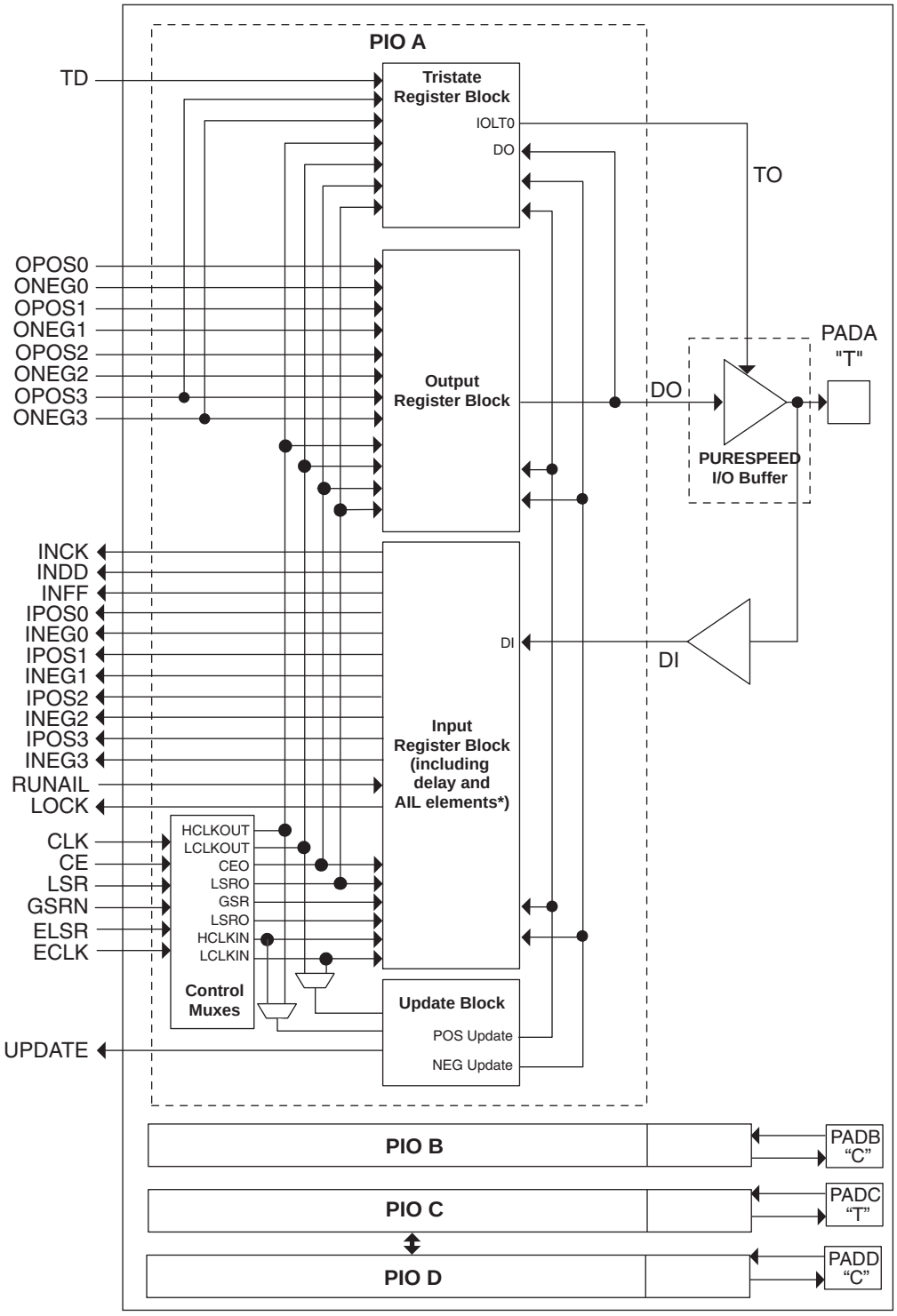
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	20000
Number of Logic Elements/Cells	80000
Total RAM Bits	5816320
Number of I/O	660
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA
Supplier Device Package	1152-FPBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga80ep1-6ffn1152c

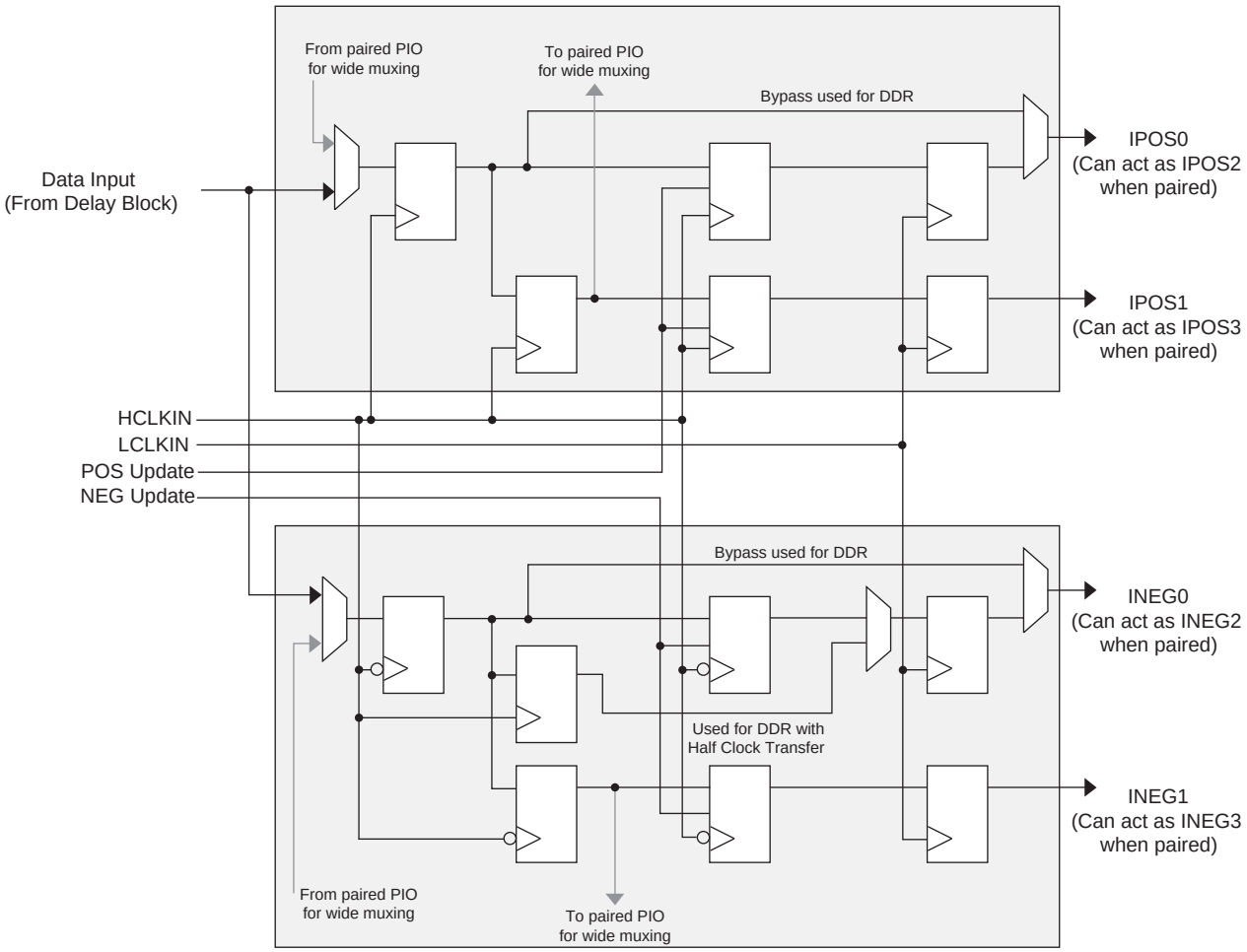
Figure 2-17. PIC Diagram



*AIL only on A or C pads located on the left, right and bottom of the device.

The A/B PIOs on the left and the right of the device can be paired to form a differentiated driver. The A/B and C/D PIOs on all sides of the device can be paired to form differential receivers. Either A or C PIOs on all sides except the one on top also provide a connection to an adaptive input logic capability that facilitates the implementation of

Figure 2-21. Input DDR/Shift Register Block



Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the PURESPEED I/O buffers. The block contains a register for SDR operation and a group of registers for DDR and shift register operation. The output signal (DO) can be derived directly from one of the inputs (bypass mode), the SDR register or the DDR/shift register block. Figure 2-22 shows the diagram of the Output Register Block.

Output SDR Register/Latch Block

The SDR register operates on the positive edge of the high-speed clock. It has clock enable that is driven by the clock enable output signal generated by the control MUX. In addition it has a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR (LSR has precedence over CE) and Global Set Reset GSR enable or disable. The register LSR input is driven from LSRO, which is generated from the PIO control MUX. The GSR inputs is driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

Output DDR/Shift Block

The DDR/Shift block contains registers and associated logic that support DDR and shift register functions using the high-speed clock and the associated transfer from the low-speed clock domain. It functions as a gearbox allowing low-speed parallel data from the FPGA fabric be output as a higher speed serial stream. Each PIO supports DDR and x2 shift functions. If desired PIOs A and B or C and D can be combined to form x4 shift functions. Figure 2-22 shows a simplified block diagram of the shift register block.

Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the PURESPEED I/O buffers. The block contains a register for SDR operation and a group of three registers for DDR and shift register operation. The output signal tri-state control signal (TO) can be derived directly from one of the inputs (bypass mode), the SDR shift register, the DDR registers or the data associated with the buffer (for open drain emulation). Figure 2-24 shows the diagram of the Tristate Register Block.

Tristate SDR Register/Latch Block

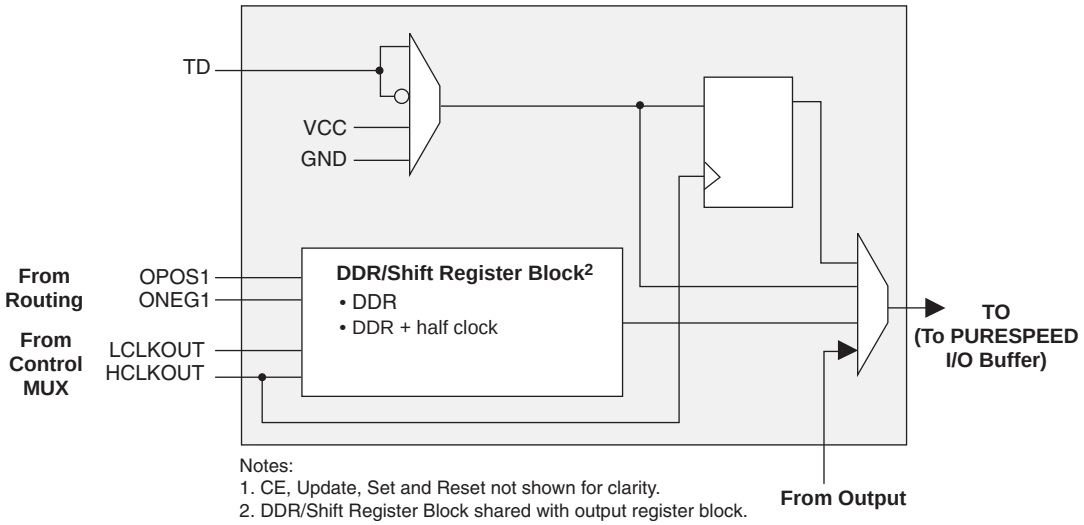
The SDR register operates on the positive edge of the high-speed clock. In it has a variety of programmable options for set/reset including, set or reset, asynchronous or synchronous Local Set Reset LSR and Global Set Reset GSR enable or disable. The register LSR input is driven from LSRO, which is generated from the PIO control MUX. The GSR input is driven from the GSR output of the PIO control MUX, which allows the global set-reset to be disabled on a PIO basis.

Tristate DDR/Shift Register Block

The DDR/Shift block is shared with the output block allowing DDR support using the high-speed clock and the associated transfer from the low-speed clock domain. It functions as a gearbox allowing low–speed parallel data from the FPGA fabric to provide a high-speed tri-state control stream.

There is a special mode for DDR-II memory interfaces where the termination is controlled by the output tristate signal. During WRITE cycle when the FPGA is driving the lines, the parallel terminations are turned off. During READ cycle when the FPGA is receiving data, the parallel terminations are turned on.

Figure 2-24. Tristate Register Block[1]



I/O Architecture Rules

Table 2-6 shows the PIO usage for x1, x2, x4 gearing. The checkmarks in the columns show the specific PIOs that are used for each gearing mode. When using x2 or x4 gearing, any PIO which is not used for gearing can still be used as an output.

VDDAX25 needs to be connected independent of the use of the SERDES. This supply is used to control the SERDES CML I/O regardless of the SERDES being used in the design.

Supported Source Synchronous Interfaces

The LatticeSC devices contain a variety of hardware, such as delay elements, DDR registers and PLLs, to simplify the implementation of Source Synchronous interfaces. Table 2-11 lists Source Synchronous and DDR/QDR standards supported in the LatticeSC. For additional detail refer to technical information at the end of the data sheet.

Table 2-11. Source Synchronous Standards Table[1]

Source Synchronous Standard	Clocking	Speeds (MHz)	Data Rate (Mbps)
RapidIO	DDR	500	1000
SPI4.2 (POS-PHY4)/NPSI	DDR	500	1000
SFI4/XSBI	DDR SDR	334 667	667
XGMII	DDR	156.25	312
CSIX	SDR	250	250
QDRII/QDRII+ memory interface	DDR	300	600
DDR memory interface	DDR	240	480
DDRII memory interface	DDR	333	667
RLDRAM memory interface	DDR	400	800

1. Memory width is dependent on the system design and limited by the number of I/Os in the device.

flexiPCS™ (Physical Coding Sublayer Block)

flexiPCS Functionality

The LatticeSC family combines a high-performance FPGA fabric, high-performance I/Os and large embedded RAM in a single industry leading architecture. LatticeSC devices also feature up to 32 channels of embedded SERDES with associated Physical Coding Sublayer (PCS) logic. The flexiPCS logic can be configured to support numerous industry standard high-speed data transfer protocols.

Each channel of flexiPCS logic contains dedicated transmit and receive SERDES for high-speed, full-duplex serial data transfers at data rates up to 3.8 Gbps. The PCS logic in each channel can be configured to support an array of popular data protocols including SONET (STS-12/STS-12c, STS-48/STS-48c, and TFI-5 support of 10 Gbps or above), Gigabit Ethernet (compliant to the IEEE 1000BASE-X specification), 1.02 or 2.04 Gbps Fibre Channel, PCI-Express, and Serial RapidIO. In addition, the protocol based logic can be fully or partially bypassed in a number of configurations to allow users flexibility in designing their own high-speed data interface.

Protocols requiring data rates above 3.8 Gbps can be accommodated by dedicating either one pair or all four channels in one flexiPCS quad block to one data link. One quad can support full-duplex serial data transfers at data rates up to 15.2 Gbps. A single flexiPCS quad can be configured to support 10Gb Ethernet (with a fully compliant XAUI interface), 10Gb Fibre Channel, and x4 PCI-Express and 4x RapidIO.

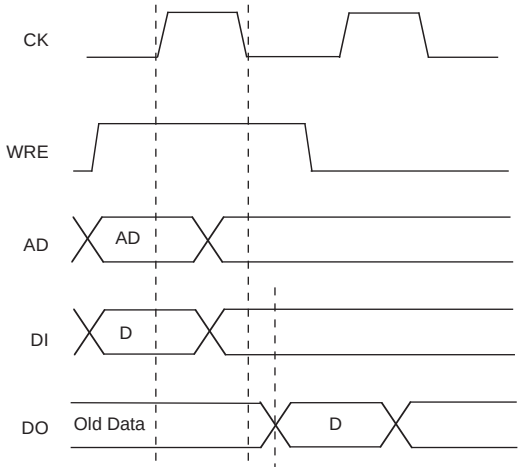
The flexiPCS also provides bypass modes that allow a direct 8-bit or 10-bit interface from the SERDES to the FPGA logic which can also be geared to run at 1/2 speed for a 16-bit or 20-bit interface to the FPGA logic. Each SERDES pin can be DC coupled independently and can allow for both high-speed and low-speed operation down to DC rates on the same SERDES pin, as required by some Serial Digital Video applications.

The ispLEVER design tools from Lattice support all modes of the flexiPCS. Most modes are dedicated to applications associated with a specific industry standard data protocol. Other more general purpose modes allow a user to define their own operation. With ispLEVER, the user can define the mode for each quad in a design. Nine modes are currently supported by the ispLEVER design flow:

Timing Diagrams

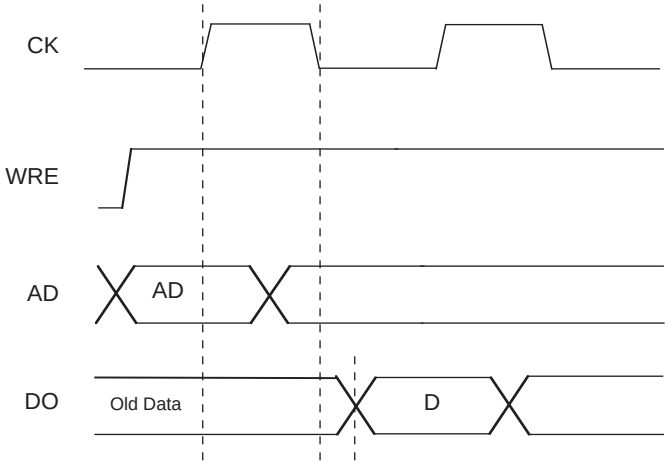
PFU Timing Diagrams

Figure 3-4. Slice Single/Dual Port Write Cycle Timing



Notes:
- Rising Edge for latching WREN, WAD and DATAIN.
- WREN must continue past falling edge clock.
- Data output occurs on negative edge.

Figure 3-5. Slice Single/Dual Port Read Cycle Timing



LatticeSC/M sysCONFIG Port Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
General Configuration Timing				
t_{SMODE}	M[3:0] Setup Time to INITN High	0	—	ns
t_{HMODE}	M[3:0] Hold Time from INITN High	600	—	ns
t_{RW}	RESETN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
t_{PGW}	PROGRAMN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
$f_{ESB\_CLK\_FRQ}$	System Bus ESB_CLK Frequency (No Wait States)	—	133	MHz
sysCONFIG Master Parallel Configuration Mode				
t_{SMB}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMB}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMB}	RCLK Low Time (Non-compressed Bitstreams)	0.5	0.5	CCLK periods
	RCLK Low Time (Compressed Bitstreams)	0.5	7.5	CCLK periods
t_{CHMB}	RCLK High Time	0.5	0.5	CCLK periods
sysCONFIG SPI Port				
t_{CFGX}	INITN High to CSCK Low	—	80	ns
t_{CSSPI}	INITN High to CSSPIN Low	0	2	µs
t_{SCK}	CSCK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CSCK Low to Output Valid	—	15	ns
t_{CSPID}	CSSPIN Low to CSCK high Setup Time	—	15	ns
f_{MAXSPI}	Max CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN=0)	—	50	MHz
t_{SUSPI}	SOSPI/D0 Data Setup Time Before CSCK	7	—	ns
t_{HSPI}	SOSPI/D0 Data Hold Time After CSCK	2	—	ns
	Master Clock Frequency	Selected value - 30%	Selected value + 30%	MHz
	Duty Cycle	40	60	%
sysCONFIG Master Serial Configuration Mode				
t_{SMS}	DIN Setup Time	4.4	—	ns
t_{HMS}	DIN Hold Time	0	—	ns
f_{CMS}	CCLK Frequency (No Divider)	90	190	MHz
f_{C_DIV}	CCLK Frequency (Div 128)	0.70	1.48	MHz
t_{D}	CCLK to DOUT Delay	—	7.5	ns
sysCONFIG Master Parallel Configuration Mode				
t_{AVMP}	RCLK to Address Valid	—	10	ns
t_{SMP}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMP}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMP}	RCLK Low Time (Non-compressed Bitstream)	7.5	7.5	CCLK periods
	RCLK Low Time (Compressed Bitstream)	0.5	63.5	
t_{CHMP}	RCLK High Time	0.5	0.5	CCLK periods
t_{DMP}	CCLK to DOUT	—	7.5	ns

Signal Descriptions (Cont.)

Signal Name	I/O	Description
MPI_STRBN	I	Driven active low indicates the start of a transaction on the PowerPC bus. MPI will strobe the address bus at next rising edge of clock.
MPI_ADDR[31:14]	I	Address bus driven by a PowerPC bus master. Only 18-bit width is needed. It has to be the least significant bit of the PowerPC 32-bit address A[31:14].
MPI_DAT[n:0]	I/O	Selectable data bus width from 8, and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction.
MPI_PAR[m:0]	I/O	Selectable parity bus width from 1, 2, and 3-bit. MPI_DP[0] for MPI_D[7:0], MPI_DP[1] for MPI_D[15:8] and MPI_DP[2] for MPI_D[23:16].
MPI_TA	O	Transfer acknowledge. Driven active low indicates that MPI received the data on the write cycle or returned data on the read cycle.
MPI_TEA	O	Transfer Error Acknowledge. Driven active low indicates that MPI detects a bus error on the internal system bus for current transaction.
MPI_RETRY	O	Active low MPI Retry requests the MPC860 to relinquish the bus and retry the cycle.
Multi-chip Alignment (User I/O if not used.)		
MCA_DONE_OUT	O	Multi-chip alignment done output (to second MCA chip)
MCA_DONE_IN	I	Multi-chip alignment done input (from second MCA chip)
MCA_CLK_P[1:2]_OUT	O	Multi-chip alignment clock [1:2] output (sourced by MCA master chip)
MCA_CLK_P[1:2]_IN	I	Multi-chip alignment clock [1:2] input (from MCA master chip
TEMP	—	Temperature sensing diode pin. Dedicated pin. Accuracy is typically +/- 10°C.
Miscellaneous Dedicated Pins		
XRES	—	External reference resistor between this pin and ground. The reference resistor is used to calibrate the programmable terminating resistors used in the I/Os. Dedicated pin. Value: 1K ± 1% ohm.
DIFFRx	—	Only used if a differential driver is used in a bank. This DIFFRx must be connected to ground via an external 1K ±1% ohm resistor for all banks that have a differential driver.
SERDES Block (Dedicated Pins)		
[A:D]_HDINPx_[L/R]	I	High-speed input (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDINNx_[L/R]	I	High-speed input (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTPx_[L/R]	O	High-speed output (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTNx_[L/R]	O	High-speed output (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_REFCLKP_[L/R]	I	Ref clock input (positive), aux channel on left [L] or right [R] side of device.
[A:D]_REFCLKN_[L/R]	I	Ref clock input (negative), aux channel on left [L] or right [R] side of device.

Pin Information Summary

Pin Type		256 fpBGA	900 fpBGA		1020 fcBGA	
		LFSC/M15	LFSC/M15	LFSC/M25	LFSC/M25	LFSC/M40
Single Ended User I/O		139	300	378	476	562
Differential Pair User I/O		60	141	182	235	277
LVDS Output Pairs		22	44	60	60	78
Configuration	Dedicated	9	11	11	11	11
	Muxes/MPI sysBus	0	55	55	55	72
JTAG (excluding VCCJ)		4	4	4	4	4
Dedicated Pins		2	4	4	4	4
VCC		10	46	46	40	40
VCC12		10	35	35	36	36
VCCAUX		10	36	36	32	32
VCCIO	Bank 1	3	18	18	10	10
	Bank 2	2	14	14	8	8
	Bank 3	2	15	15	10	10
	Bank 4	3	15	15	10	10
	Bank 5	3	15	15	10	10
	Bank 6	2	15	15	10	10
	Bank 7	2	16	16	8	8
VTT	Bank 2	0	2	2	2	2
	Bank 3	0	3	3	3	3
	Bank 4	0	3	3	3	3
	Bank 5	0	3	3	3	3
	Bank 6	0	3	3	3	3
	Bank 7	0	2	2	2	2
GND		26	177	177	134	134
NC		0	102	24	92	6
Single Ended User / Differential I/O per Bank	Bank 1	21/8	63/30	63/30	68/32	68/32
	Bank 2	15/7	26/13	30/15	34/17	54/27
	Bank 3	19/8	43/20	62/29	84/42	94/47
	Bank 4	25/11	50/22	66/32	84/41	99/48
	Bank 5	25/11	49/23	65/32	88/44	99/49
	Bank 6	19/8	43/20	62/29	84/42	94/47
	Bank 7	15/7	26/13	30/15	34/17	54/27
LVDS Output Pairs Per Bank	Bank 2	5	7	9	9	15
	Bank 3	6	15	21	21	24
	Bank 6	6	15	21	21	24
	Bank 7	5	7	9	9	15
VCCJ		1	1	1	1	1
SERDES (signal + power supply)		28	60	60	108	108
Total		256	900	900	1020	1152

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH29	PB48B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D	PB68B	4	LRC_DLLC_IN_C/LRC_DLLC_FB_D
AE26	PB48C	4		PB68C	4	
AD25	PB48D	4		PB68D	4	
AJ30	PB49A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B	PB69A	4	LRC_PLLT_IN_A/LRC_PLLT_FB_B
AH30	PB49B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B	PB69B	4	LRC_PLLC_IN_A/LRC_PLLC_FB_B
AG28	PB49C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C	PB69C	4	LRC_DLLT_IN_D/LRC_DLLT_FB_C
AG29	PB49D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C	PB69D	4	LRC_DLLC_IN_D/LRC_DLLC_FB_C
AF26	VCC12	-		VCC12	-	
AD27	PROBE_VCC	-		PROBE_VCC	-	
AG27	VCC12	-		VCC12	-	
AE28	PROBE_GND	-		PROBE_GND	-	
AC25	PR45D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A	PR57D	3	LRC_PLLC_IN_B/LRC_PLLC_FB_A
AD26	PR45C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A	PR57C	3	LRC_PLLT_IN_B/LRC_PLLT_FB_A
AF28	PR45B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E	PR57B	3	LRC_DLLC_IN_F/LRC_DLLC_FB_E
AF29	PR45A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E	PR57A	3	LRC_DLLT_IN_F/LRC_DLLT_FB_E
AC26	PR44D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F	PR55D	3	LRC_DLLC_IN_E/LRC_DLLC_FB_F
AB26	PR44C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F	PR55C	3	LRC_DLLT_IN_E/LRC_DLLT_FB_F
AG30	PR44B	3		PR55B	3	
AF30	PR44A	3		PR55A	3	
AC28	PR43B	3		PR52B	3	
AB28	PR43A	3		PR52A	3	
AB27	PR41D	3	VREF2_3	PR51D	3	VREF2_3
AE30	PR41B	3		PR51B	3	
AD30	PR41A	3		PR51A	3	
AB25	PR40B	3		PR49B	3	
AA25	PR40A	3		PR49A	3	
AA30	PR39B	3		PR48B	3	
Y30	PR39A	3		PR48A	3	
W29	PR37B	3		PR44B	3	
V29	PR37A	3		PR44A	3	
U30	PR36B	3		PR43B	3	
T30	PR36A	3		PR43A	3	
V25	PR35D	3	DIFFR_3	PR42D	3	DIFFR_3
W28	PR35B	3		PR42B	3	
V28	PR35A	3		PR42A	3	
R30	PR33B	3		PR38B	3	
P30	PR33A	3		PR38A	3	
N30	PR32B	3		PR35B	3	
M29	PR32A	3		PR35A	3	
U26	PR31D	3		PR34D	3	
T26	PR31C	3	VREF1_3	PR34C	3	VREF1_3
U28	PR31B	3		PR34B	3	
T28	PR31A	3		PR34A	3	
M30	PR28D	3	PCLKC3_2	PR31D	3	PCLKC3_2
L29	PR28C	3	PCLKT3_2	PR31C	3	PCLKT3_2

LFSC/M15, LFSC/M25 Logic Signal Connections: 900 fpBGA[1, 2] (Cont.)

Ball Number	LFSC/M15			LFSC/M25		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
R29	PR28B	3		PR31B	3	
P29	PR28A	3		PR31A	3	
P27	PR27C	3	PCLKT3_3	PR30C	3	PCLKT3_3
N29	PR27B	3		PR30B	3	
N28	PR27A	3		PR30A	3	
R25	PR26D	3	PCLKC3_1	PR29D	3	PCLKC3_1
R26	PR26C	3	PCLKT3_1	PR29C	3	PCLKT3_1
R28	PR26B	3	PCLKC3_0	PR29B	3	PCLKC3_0
P28	PR26A	3	PCLKT3_0	PR29A	3	PCLKT3_0
N27	PR24D	2	PCLKC2_2	PR27D	2	PCLKC2_2
P26	PR24C	2	PCLKT2_2	PR27C	2	PCLKT2_2
L30	PR24B	2	PCLKC2_0	PR27B	2	PCLKC2_0
K30	PR24A	2	PCLKT2_0	PR27A	2	PCLKT2_0
J30	PR23B	2	PCLKC2_1	PR26B	2	PCLKC2_1
H30	PR23A	2	PCLKT2_1	PR26A	2	PCLKT2_1
M26	PR22D	2	DIFFR_2	PR25D	2	DIFFR_2
M25	PR22C	2	VREF1_2	PR25C	2	VREF1_2
G29	PR22B	2		PR25B	2	
F29	PR22A	2		PR25A	2	
H28	PR19D	2		PR22D	2	
J28	PR19C	2		PR22C	2	
E30	PR19B	2		PR22B	2	
E29	PR19A	2		PR22A	2	
L26	PR18D	2	VREF2_2	PR18D	2	VREF2_2
L25	PR18C	2		PR18C	2	
F28	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C	PR18B	2	URC_DLLC_IN_D/URC_DLLC_FB_C
G28	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C	PR18A	2	URC_DLLT_IN_D/URC_DLLT_FB_C
K26	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A	PR17D	2	URC_PLLC_IN_B/URC_PLLC_FB_A
K25	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A	PR17C	2	URC_PLLT_IN_B/URC_PLLT_FB_A
D30	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D	PR17B	2	URC_DLLC_IN_C/URC_DLLC_FB_D
D29	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
G26	PR15D	2		PR16D	2	
H26	PR15C	2		PR16C	2	
E28	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B	PR16B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
D28	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B	PR16A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
J25	VCCJ	-		VCCJ	-	
H25	TDO	-	TDO	TDO	-	TDO
J26	TMS	-		TMS	-	
G25	TCK	-		TCK	-	
G24	TDI	-		TDI	-	
F26	PROGRAMN	1		PROGRAMN	1	
H24	MPIIRQN	1	CFGIRQN/MPI_IRQ_N	MPIIRQN	1	CFGIRQN/MPI_IRQ_N
F25	CCLK	1		CCLK	1	
D27	VCC12	-		VCC12	-	
E26	VCC12	-		VCC12	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
B30	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N	A_HDOUTN0_L	-	PCS 360 CH 0 OUT N
D30	A_VDDOB0_L	-		A_VDDOB0_L	-	
A30	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P	A_HDOUTP0_L	-	PCS 360 CH 0 OUT P
C31	A_HDINN0_L	-	PCS 360 CH 0 IN N	A_HDINN0_L	-	PCS 360 CH 0 IN N
C32	A_HDINP0_L	-	PCS 360 CH 0 IN P	A_HDINP0_L	-	PCS 360 CH 0 IN P
B31	A_VDDIB0_L	-		A_VDDIB0_L	-	
AL25	NC	-		PB26A	5	
AL24	NC	-		PB26B	5	
AG27	NC	-		PB26C	5	
AH27	NC	-		PB26D	5	
AM25	NC	-		PB27A	5	
AM24	NC	-		PB27B	5	
AL9	NC	-		PB62A	4	
AL8	NC	-		PB62B	4	
AK9	NC	-		PB63A	4	
AJ9	NC	-		PB63B	4	
AG10	NC	-		PB63C	4	
AG11	NC	-		PB63D	4	
J30	NC	-		PL26A	7	
H30	NC	-		PL26B	7	
M28	NC	-		PL26C	7	
N28	NC	-		PL26D	7	
J32	NC	-		PL27A	7	
J31	NC	-		PL27B	7	
N26	NC	-		PL27C	7	
N27	NC	-		PL27D	7	
K31	NC	-		PL29A	7	
K32	NC	-		PL29B	7	
P25	NC	-		PL29C	7	
P26	NC	-		PL29D	7	
L27	NC	-		PL22C	7	
L28	NC	-		PL22D	7	
M29	NC	-		PL30A	7	
L29	NC	-		PL30B	7	
M30	NC	-		PL31A	7	
L30	NC	-		PL31B	7	
L31	NC	-		PL34A	7	
M31	NC	-		PL34B	7	
AA29	NC	-		PL56A	6	
AA30	NC	-		PL56B	6	
AB31	NC	-		PL57A	6	
AA31	NC	-		PL57B	6	
AG30	NC	-		PL57C	6	
AG29	NC	-		PL57D	6	
AB29	NC	-		PL58A	6	
AB30	NC	-		PL58B	6	
Y25	NC	-		PL58C	6	
AA25	NC	-		PL58D	6	
AA8	NC	-		PR58D	3	
Y8	NC	-		PR58C	3	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
L33	PL27B	7		PL35B	7	
M30	PL27C	7		PL35C	7	
N30	PL27D	7		PL35D	7	
M31	PL29A	7		PL37A	7	
N31	PL29B	7		PL37B	7	
P24	PL29C	7		PL37C	7	
R24	PL29D	7		PL37D	7	
M33	PL30A	7		PL42A	7	
N33	PL30B	7		PL42B	7	
U25	PL30C	7		PL42C	7	
T25	PL30D	7		PL42D	7	
L34	PL31A	7		PL43A	7	
M34	PL31B	7		PL43B	7	
P29	PL31C	7		PL43C	7	
R29	PL31D	7		PL43D	7	
N34	PL34A	7		PL46A	7	
P34	PL34B	7		PL46B	7	
R27	PL34C	7		PL46C	7	
T27	PL34D	7		PL46D	7	
R32	PL35A	7	PCLKT7_1	PL47A	7	PCLKT7_1
R31	PL35B	7	PCLKC7_1	PL47B	7	PCLKC7_1
U24	PL35C	7	PCLKT7_3	PL47C	7	PCLKT7_3
T24	PL35D	7	PCLKC7_3	PL47D	7	PCLKC7_3
P33	PL36A	7	PCLKT7_0	PL48A	7	PCLKT7_0
R33	PL36B	7	PCLKC7_0	PL48B	7	PCLKC7_0
T26	PL36C	7	PCLKT7_2	PL48C	7	PCLKT7_2
U26	PL36D	7	PCLKC7_2	PL48D	7	PCLKC7_2
T32	PL38A	6	PCLKT6_0	PL50A	6	PCLKT6_0
T31	PL38B	6	PCLKC6_0	PL50B	6	PCLKC6_0
U29	PL38C	6	PCLKT6_1	PL50C	6	PCLKT6_1
V29	PL38D	6	PCLKC6_1	PL50D	6	PCLKC6_1
T30	PL39A	6		PL51A	6	
U30	PL39B	6		PL51B	6	
U27	PL39C	6	PCLKT6_3	PL51C	6	PCLKT6_3
V27	PL39D	6	PCLKC6_3	PL51D	6	PCLKC6_3
R34	PL40A	6		PL52A	6	
T34	PL40B	6		PL52B	6	
U28	PL40C	6	PCLKT6_2	PL52C	6	PCLKT6_2
V28	PL40D	6	PCLKC6_2	PL52D	6	PCLKC6_2
V30	PL43A	6		PL55A	6	
W30	PL43B	6		PL55B	6	
W27	PL43C	6	VREF1_6	PL55C	6	VREF1_6
Y27	PL43D	6		PL55D	6	
T33	PL44A	6		PL56A	6	
U33	PL44B	6		PL56B	6	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AH11	PB57D	4		PB79D	4	
AN13	PB58A	4	PCLKT4_3	PB80A	4	PCLKT4_3
AN12	PB58B	4	PCLKC4_3	PB80B	4	PCLKC4_3
AD14	PB58C	4	PCLKT4_4	PB80C	4	PCLKT4_4
AD15	PB58D	4	PCLKC4_4	PB80D	4	PCLKC4_4
AP13	PB61A	4		PB73A	4	
AP12	PB61B	4		PB73B	4	
AK13	PB61C	4		PB73C	4	
AK12	PB61D	4		PB73D	4	
AP11	PB62A	4		PB83A	4	
AP10	PB62B	4		PB83B	4	
AN11	PB63A	4		PB99A	4	
AN10	PB63B	4		PB99B	4	
AF14	PB63C	4		PB99C	4	
AF13	PB63D	4		PB99D	4	
AM10	PB67A	4		PB101A	4	
AM9	PB67B	4		PB101B	4	
AE14	PB67C	4		PB101C	4	
AE13	PB67D	4		PB101D	4	
AP9	PB69A	4		PB104A	4	
AP8	PB69B	4		PB104B	4	
AK11	PB69C	4		PB104C	4	
AK10	PB69D	4		PB104D	4	
AL10	PB70A	4		PB107A	4	
AL9	PB70B	4		PB107B	4	
AF12	PB70C	4		PB107C	4	
AF11	PB70D	4		PB107D	4	
AN9	PB73A	4		PB109A	4	
AN8	PB73B	4		PB109B	4	
AG11	PB73C	4		PB109C	4	
AG10	PB73D	4		PB109D	4	
AP7	PB74A	4		PB111A	4	
AP6	PB74B	4		PB111B	4	
AG13	PB74C	4		PB111C	4	
AG12	PB74D	4		PB111D	4	
AN7	PB75A	4		PB113A	4	
AN6	PB75B	4		PB113B	4	
AK9	PB75C	4		PB113C	4	
AK8	PB75D	4		PB113D	4	
AP5	PB77A	4		PB115A	4	
AP4	PB77B	4		PB115B	4	
AD11	PB77C	4		PB115C	4	
AE11	PB77D	4		PB115D	4	
AM7	PB78A	4		PB117A	4	
AM6	PB78B	4		PB117B	4	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M40			LFSC/M80		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB15	VCC12	-		VCC12	-	
AB20	VCC12	-		VCC12	-	
N15	VCC12	-		VCC12	-	
N20	VCC12	-		VCC12	-	
R13	VCC12	-		VCC12	-	
R22	VCC12	-		VCC12	-	
Y13	VCC12	-		VCC12	-	
Y22	VCC12	-		VCC12	-	
AA12	VCCAUX	-		VCCAUX	-	
AA23	VCCAUX	-		VCCAUX	-	
AB12	VCCAUX	-		VCCAUX	-	
AB16	VCCAUX	-		VCCAUX	-	
AB17	VCCAUX	-		VCCAUX	-	
AB18	VCCAUX	-		VCCAUX	-	
AB19	VCCAUX	-		VCCAUX	-	
AB23	VCCAUX	-		VCCAUX	-	
AC12	VCCAUX	-		VCCAUX	-	
AC13	VCCAUX	-		VCCAUX	-	
Y19	GND	-		GND	-	
AC14	VCCAUX	-		VCCAUX	-	
AC17	VCCAUX	-		VCCAUX	-	
AC21	VCCAUX	-		VCCAUX	-	
AC22	VCCAUX	-		VCCAUX	-	
AC23	VCCAUX	-		VCCAUX	-	
M13	VCCAUX	-		VCCAUX	-	
M14	VCCAUX	-		VCCAUX	-	
M18	VCCAUX	-		VCCAUX	-	
M21	VCCAUX	-		VCCAUX	-	
M22	VCCAUX	-		VCCAUX	-	
N12	VCCAUX	-		VCCAUX	-	
N16	VCCAUX	-		VCCAUX	-	
N17	VCCAUX	-		VCCAUX	-	
N18	VCCAUX	-		VCCAUX	-	
N19	VCCAUX	-		VCCAUX	-	
N23	VCCAUX	-		VCCAUX	-	
P12	VCCAUX	-		VCCAUX	-	
P23	VCCAUX	-		VCCAUX	-	
T13	VCCAUX	-		VCCAUX	-	
T22	VCCAUX	-		VCCAUX	-	
U12	VCCAUX	-		VCCAUX	-	
U13	VCCAUX	-		VCCAUX	-	
U22	VCCAUX	-		VCCAUX	-	
V13	VCCAUX	-		VCCAUX	-	
V22	VCCAUX	-		VCCAUX	-	
V23	VCCAUX	-		VCCAUX	-	

Figure 3-12. Waveforms First Read after Full Flag

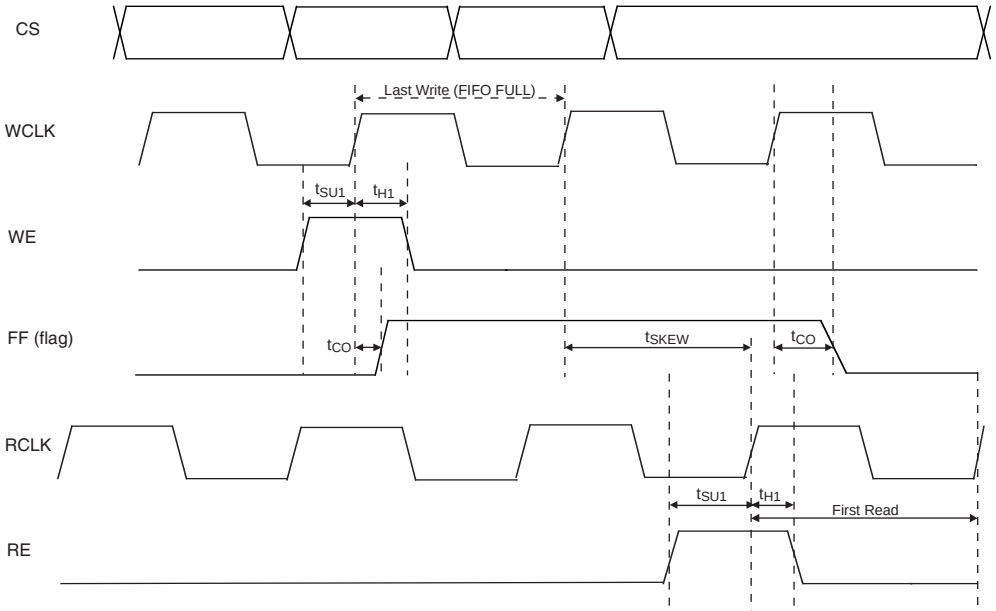


Figure 3-13. Waveform First Write after Empty Flag