Lattice Semiconductor Corporation - LFSCM3GA80EP1-6FFN1704C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	20000
Number of Logic Elements/Cells	80000
Total RAM Bits	5816320
Number of I/O	904
Number of Gates	-
Voltage - Supply	0.95V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1704-BBGA, FCBGA
Supplier Device Package	1704-OFCBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfscm3ga80ep1-6ffn1704c

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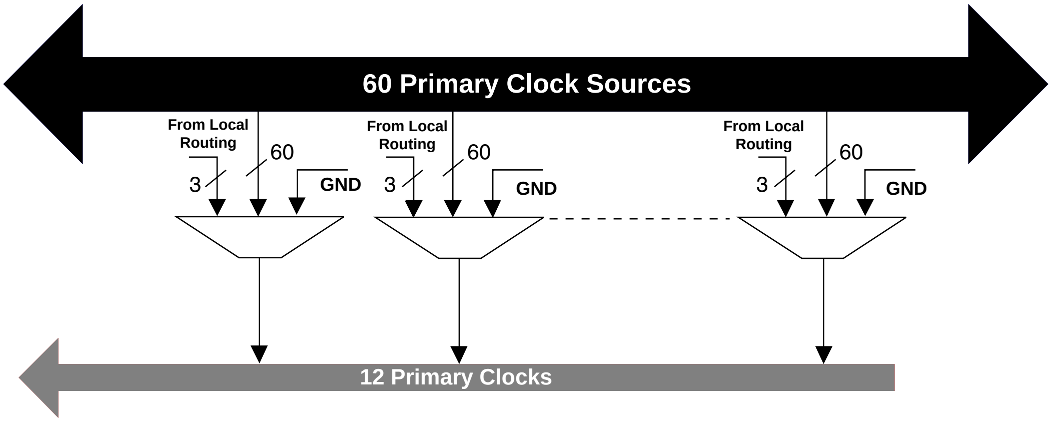
Figure 2-6. Per Quadrant Clock Selection



Note: GND is available to switch off the network.

Secondary Clocks

In addition to the primary clock network and edge clocks the LatticeSC devices also contain a secondary clock network. Built of X6 style routing elements this secondary clock network is ideal for routing slower speed clock and control signals throughout the device preserving high-speed clock networks for the most timing critical signals.

Edge Clocks

LatticeSC devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are eight edge clocks per bank for the top and bottom of the device. The left and right sides have eight edge clocks per side for both banks located on that side. Figure 2-7 shows the arrangement of edge clocks.

Edge clock resources can be driven from a variety of sources. Edge clock resources can be driven from:

- Edge clock PIOs in the same bank
- Primary clock PIOs in the same bank
- Routing
- Adjacent PLLs and DLLs
- ELSR output from the clock divider

Table 2-5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
FIFO	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output. A clock is required even in asynchronous read mode.

The EBR memory supports two forms of write behavior for dual port operation:

1. **Normal** — data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output.
2. **Write Through** — a copy of the input data appears at the output of the same port.

FIFO Configuration

The FIFO has a write port with Data-in, WCE, WE and WCLK signals. There is a separate read port with Data-out, RCE, RE and RCLK signals. The FIFO internally generates Almost Full, Full, Almost Empty, and Empty Flags. The Full and Almost Full flags are registered with WCLK. The Empty and Almost Empty flags are registered with RCLK.

- 8-bit SERDES Only
- 10-bit SERDES Only
- SONET (STS-12/STS-48)
- Gigabit Ethernet
- Fibre Channel
- XAUI
- Serial RapidIO
- PCI-Express
- Generic 8b10b

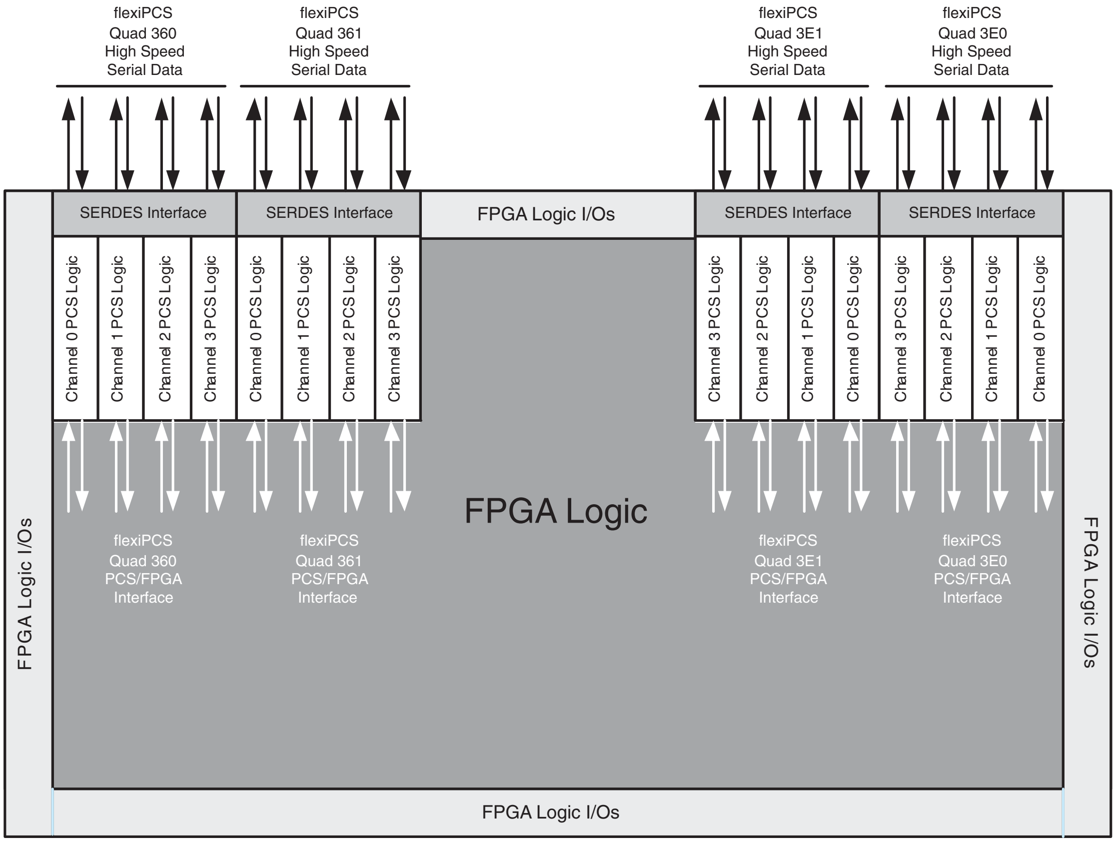
flexiPCS Quad

The flexiPCS logic is arranged in quads containing logic for four independent full-duplex data channels. Each device in the LatticeSC family has up to eight quads of flexiPCS logic. The LatticeSC Family Selection Guide table on the first page of this data sheet contains the number of flexiPCS channels present on the chip. Note that in some packages (particularly lower pin count packages), not all channels from all quads on a given device may be bonded to package pins.

Each quad supports up to four channels of full-duplex data and can be programmed into any one of several protocol based modes. Each quad requires its own reference clock which can be sourced externally or from the FPGA logic. The user can utilize between one and four channels in a quad, depending on the application.

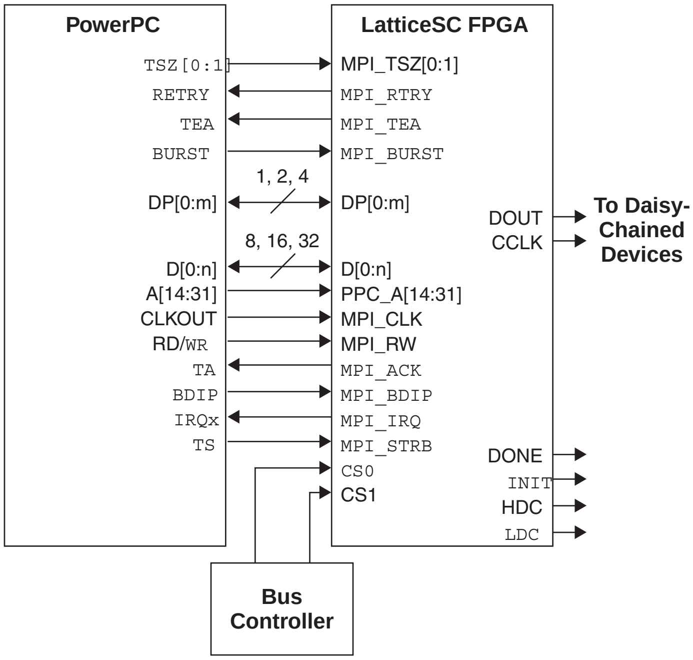
Figure 2-30 shows an example of four flexiPCS quads in a LatticeSC device. Quads are labeled according to the address of their software controlled registers.

Figure 2-30. LatticeSC flexiPCS



Since each quad has its own reference clock, different quads can support different standards on the same chip. This feature makes the LatticeSC family of devices ideal for bridging between different standards.

Figure 2-32. PowerPCI and MPI Schematic



Configuration and Testing

The following section describes the configuration and testing features of the LatticeSC family of devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeSC devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS33, 25 and 18 standards. For additional detail refer to technical information at the end of the data sheet.

Device Configuration

All LatticeSC devices contain three possible ports that can be used for device configuration. The serial port, which supports bit-wide configuration, and the sysCONFIG port that supports both byte-wide and serial configuration. The MPI port supports 8-bit, 16-bit or 32-bit configuration.

The serial port supports both the IEEE Std. 1149.1 Boundary Scan specification and the IEEE Std. 1532 In-System Configuration specification. The sysCONFIG port is a 20-pin interface with six of the I/Os used as dedicated pins and the rest being dual-use pins. When sysCONFIG mode is not used, these dual-use pins are available for general purpose I/O. All I/Os for the sysCONFIG and MPI ports are in I/O bank #1.

On power-up, the FPGA SRAM is ready to be configured with the sysCONFIG port active. The IEEE 1149.1 serial mode can be activated any time after power-up by sending the appropriate command through the TAP port. Once a configuration port is selected, that port is locked and another configuration port cannot be activated until the next re-initialization sequence. For additional detail refer to technical information at the end of the data sheet.

PURESPEED I/O Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 33	3.135	3.3	3.465	—	—	—
LVCMOS 25	2.375	2.5	2.625	—	—	—
LVCMOS 18	1.71	1.8	1.89	—	—	—
LVCMOS 15	1.425	1.5	1.575	—	—	—
LVCMOS 12	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
PCI33	3.135	3.3	3.465	—	—	—
PCIX33	3.135	3.3	3.465	—	—	—
PCIX15	1.425	1.5	1.575	$0.49V_{CCIO}$	$0.5V_{CCIO}$	$0.51V_{CCIO}$
AGP1X33	3.135	3.3	3.465	—	—	—
AGP2X33	3.135	3.3	3.465	$0.39V_{CCIO}$	$0.4V_{CCIO}$	$0.41V_{CCIO}$
SSTL18_I, II[3]	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I, II[3]	2.375	2.5	2.625	1.15	1.25	1.35
SSTL33_I, II[3]	3.135	3.3	3.465	1.3	1.5	1.7
HSTL15_I, II[3]	1.425	1.5	1.575	0.68	0.75	0.9
HSTL15_III[1, 3] and IV[1, 3]	1.425	1.5	1.575	0.68	0.9	0.9
HSTL 18_I[3], II[3]	1.71	1.8	1.89	0.816	0.9	1.08
HSTL 18_ III[1, 3], IV[1, 3]	1.71	1.8	1.89	0.816	1.08	1.08
GTL12[1, 3], GTLPLUS15[1, 3]	—	—	—	0.882	1.0	1.122
LVDS	—	—	—	—	—	—
Mini-LVDS	—	—	—	—	—	—
RSDS	—	—	—	—	—	—
LVPECL33 (outputs)[2]	3.135	3.3	3.465	—	—	—
LVPECL33 (inputs)[2, 4]	—	≤ 2.5	—	—	—	—
BLVDS25[2, 3]	2.375	2.5	2.625	—	—	—
MLVDS25[2, 3]	2.375	2.5	2.625	—	—	—
SSTL18D_I[3], II[3]	1.71	1.8	1.89	—	—	—
SSTL25D_I[3], II[3]	2.375	2.5	2.625	—	—	—
SSTL33D_I[3], II[3]	3.135	3.3	3.465	—	—	—
HSTL15D_I[3], II[3]	1.425	1.5	1.575	—	—	—
HSTL18D_I[3], II[3]	1.71	1.8	1.89	—	—	—

1. Input only.
2. Inputs on chip. Outputs are implemented with the addition of external resisters.
3. Input for this standard does not depend on the value of V_{CCIO}.
4. Inputs for this standard cannot be in 3.3V VCCIO banks (≤ 2.5V only).

PURESPEED I/O Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input voltage		0	—	2.4	V
V_{THD}	Differential input threshold ($Q-\overline{Q}$)		+/-100	—	—	mV
V_{CM}	Input common mode voltage		0.05	1.2	2.35	V
I_{IN}	Input current	Power on or power off	—	—	+/-10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9V	1.03	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50	mV
V_{OS}	Output voltage offset	(V_{OP} - V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50	mV
I_{SAB}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	12	mA
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	500	ps	T_R, T_F

Notes:
1. Data is for 3.5mA differential current drive. Other differential driver current options are available.
2. If the low power mode of the input buffer is used, the minimum V_{CM} is 600 mV.

Mini-LVDS

Over Recommended Operating Conditions

Parameter Symbol	Description	Min.	Typ.	Max.	Units
Z_O	Single-ended PCB trace impedance	30	50	75	ohms
R_T	Differential termination resistance	60	100	150	ohms
V_{OD}	Output voltage, differential, $\lvert V_{OP} - V_{OM} \rvert$	300	—	600	mV
V_{OS}	Output voltage, common mode, $\lvert V_{OP} + V_{OM} \rvert /2$	1	1.2	1.4	V
ΔV_{OD}	Change in V_{OD}, between H and L	—	—	50	mV
ΔV_{ID}	Change in V_{OS}, between H and L	—	—	50	mV
V_{THD}	Input voltage, differential, $\lvert V_{INP} - V_{INM} \rvert$	200	—	600	mV
V_{CM}	Input voltage, common mode, $\lvert V_{INP} + V_{INM} \rvert /2$	0.3+(V_{THD}/2)	—	2.1-(V_{THD}/2)	
T_R, T_F	Output rise and fall times, 20% to 80%	—	—	500	ps
T_{ODUTY}	Output clock duty cycle	45	—	55	%
T_{IDUTY}	Input clock duty cycle	40	—	60	%

Note: Data is for 6mA differential current drive. Other differential driver current options are available.

LatticeSC/M sysCONFIG Port Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
General Configuration Timing				
t_{SMODE}	M[3:0] Setup Time to INITN High	0	—	ns
t_{HMODE}	M[3:0] Hold Time from INITN High	600	—	ns
t_{RW}	RESETN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
t_{PGW}	PROGRAMN Pulse Width Low to Start Reconfiguration (1.2 V)	50 (or 100 at 0.95V)	—	ns
$f_{ESB\_CLK\_FRQ}$	System Bus ESB_CLK Frequency (No Wait States)	—	133	MHz
sysCONFIG Master Parallel Configuration Mode				
t_{SMB}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMB}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMB}	RCLK Low Time (Non-compressed Bitstreams)	0.5	0.5	CCLK periods
	RCLK Low Time (Compressed Bitstreams)	0.5	7.5	CCLK periods
t_{CHMB}	RCLK High Time	0.5	0.5	CCLK periods
sysCONFIG SPI Port				
t_{CFGX}	INITN High to CSCK Low	—	80	ns
t_{CSSPI}	INITN High to CSSPIN Low	0	2	µs
t_{SCK}	CSCK Low before CSSPIN Low	0	—	ns
t_{SOCDO}	CSCK Low to Output Valid	—	15	ns
t_{CSPID}	CSSPIN Low to CSCK high Setup Time	—	15	ns
f_{MAXSPI}	Max CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN=0)	—	50	MHz
t_{SUSPI}	SOSPI/D0 Data Setup Time Before CSCK	7	—	ns
t_{HSPI}	SOSPI/D0 Data Hold Time After CSCK	2	—	ns
	Master Clock Frequency	Selected value - 30%	Selected value + 30%	MHz
	Duty Cycle	40	60	%
sysCONFIG Master Serial Configuration Mode				
t_{SMS}	DIN Setup Time	4.4	—	ns
t_{HMS}	DIN Hold Time	0	—	ns
f_{CMS}	CCLK Frequency (No Divider)	90	190	MHz
f_{C_DIV}	CCLK Frequency (Div 128)	0.70	1.48	MHz
t_D	CCLK to DOUT Delay	—	7.5	ns
sysCONFIG Master Parallel Configuration Mode				
t_{AVMP}	RCLK to Address Valid	—	10	ns
t_{SMP}	D[7:0] Setup Time to RCLK High	6	—	ns
t_{HMP}	D[7:0] Hold Time to RCLK High	0	—	ns
t_{CLMP}	RCLK Low Time (Non-compressed Bitstream)	7.5	7.5	CCLK periods
	RCLK Low Time (Compressed Bitstream)	0.5	63.5	
t_{CHMP}	RCLK High Time	0.5	0.5	CCLK periods
t_{DMP}	CCLK to DOUT	—	7.5	ns

Switching Test Conditions

Figure 3-15 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-4.

Figure 3-15. Output Test Load, LVTTL and LVCMOS Standards

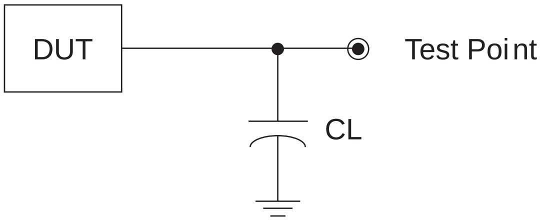


Table 3-4. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	**C_L**	**Timing Ref.**	**V_T**
LVTTL and other LVCMOS settings (L -> H, H -> L)	30pF	LVCMOS 3.3 = 1.5V	—
		LVCMOS 2.5 = $V_{CCIO}/2$	—
		LVCMOS 1.8 = $V_{CCIO}/2$	—
		LVCMOS 1.5 = $V_{CCIO}/2$	—
		LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	30pF	$V_{CCIO}/2$	V_{OL}
LVCMOS 2.5 I/O (Z -> L)		$V_{CCIO}/2$	V_{OH}
LVCMOS 2.5 I/O (H -> Z)		V_{OH} - 0.15	V_{OL}
LVCMOS 2.5 I/O (L -> Z)		V_{OL} + 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
MPI_STRBN	I	Driven active low indicates the start of a transaction on the PowerPC bus. MPI will strobe the address bus at next rising edge of clock.
MPI_ADDR[31:14]	I	Address bus driven by a PowerPC bus master. Only 18-bit width is needed. It has to be the least significant bit of the PowerPC 32-bit address A[31:14].
MPI_DAT[n:0]	I/O	Selectable data bus width from 8, and 16-bit. Driven by a bus master in a write transaction. Driven by MPI in a read transaction.
MPI_PAR[m:0]	I/O	Selectable parity bus width from 1, 2, and 3-bit. MPI_DP[0] for MPI_D[7:0], MPI_DP[1] for MPI_D[15:8] and MPI_DP[2] for MPI_D[23:16].
MPI_TA	O	Transfer acknowledge. Driven active low indicates that MPI received the data on the write cycle or returned data on the read cycle.
MPI_TEA	O	Transfer Error Acknowledge. Driven active low indicates that MPI detects a bus error on the internal system bus for current transaction.
MPI_RETRY	O	Active low MPI Retry requests the MPC860 to relinquish the bus and retry the cycle.
Multi-chip Alignment (User I/O if not used.)		
MCA_DONE_OUT	O	Multi-chip alignment done output (to second MCA chip)
MCA_DONE_IN	I	Multi-chip alignment done input (from second MCA chip)
MCA_CLK_P[1:2]_OUT	O	Multi-chip alignment clock [1:2] output (sourced by MCA master chip)
MCA_CLK_P[1:2]_IN	I	Multi-chip alignment clock [1:2] input (from MCA master chip
TEMP	—	Temperature sensing diode pin. Dedicated pin. Accuracy is typically +/- 10°C.
Miscellaneous Dedicated Pins		
XRES	—	External reference resistor between this pin and ground. The reference resistor is used to calibrate the programmable terminating resistors used in the I/Os. Dedicated pin. Value: 1K ± 1% ohm.
DIFFRx	—	Only used if a differential driver is used in a bank. This DIFFRx must be connected to ground via an external 1K ±1% ohm resistor for all banks that have a differential driver.
SERDES Block (Dedicated Pins)		
[A:D]_HDINPx_[L/R]	I	High-speed input (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDINNx_[L/R]	I	High-speed input (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTPx_[L/R]	O	High-speed output (positive) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_HDOUTNx_[L/R]	O	High-speed output (negative) channel x on left [L] or right [R] side of device. PCS quad is defined in the dual function name column of the Logic Signal Connection table.
[A:D]_REFCLKP_[L/R]	I	Ref clock input (positive), aux channel on left [L] or right [R] side of device.
[A:D]_REFCLKN_[L/R]	I	Ref clock input (negative), aux channel on left [L] or right [R] side of device.

LFSC/M15 Logic Signal Connections: 256 fpBGA[1,2] (Cont.)

	LFSC/M15		
Ball Number	Ball Function	VCCIO Bank	Dual Function
F14	PR17A	2	URC_DLLT_IN_C/URC_DLLT_FB_D
E15	PR15B	2	URC_PLLC_IN_A/URC_PLLC_FB_B
E14	PR15A	2	URC_PLLT_IN_A/URC_PLLT_FB_B
D9	VCCJ	-	
C16	TDO	-	TDO
B15	TMS	-	
B16	TCK	-	
E13	TDI	-	
C14	PROGRAMN	1	
C15	CCLK	1	
A15	PT43D	1	HDC/SI
A14	PT43C	1	LDCN/SCS
B14	PT41A	1	CS1
E12	PT39B	1	CS0N
D13	PT39A	1	RDN
D12	PT37D	1	WRN
E10	PT37C	1	D7
C11	PT37B	1	D6
D10	PT37A	1	D5
A13	PT36D	1	D4
B12	PT36C	1	D3
A12	PT35B	1	D2
C12	PT35A	1	D1
A11	PT33B	1	D0
B11	PT33A	1	QOUT/CEON
E9	PT32D	1	VREF2_1
E8	PT32B	1	DOUT
D8	PT28C	1	BUSYN/RCLK/SCK
A10	PT27B	1	PCLKC1_0
C10	PT27A	1	PCLKT1_0
E7	PT21C	1	VREF1_1
C9	A_VDDIB3_L	-	
A9	A_HDINP3_L	-	PCS 360 CH 3 IN P
B9	A_HDINN3_L	-	PCS 360 CH 3 IN N
A8	A_HDOUTP3_L	-	PCS 360 CH 3 OUT P
B8	A_HDOUTN3_L	-	PCS 360 CH 3 OUT N
C8	A_VDDOB3_L	-	
B7	A_HDOUTN2_L	-	PCS 360 CH 2 OUT N
C7	A_VDDOB2_L	-	
A7	A_HDOUTP2_L	-	PCS 360 CH 2 OUT P
B6	A_HDINN2_L	-	PCS 360 CH 2 IN N
A6	A_HDINP2_L	-	PCS 360 CH 2 IN P
C6	A_VDDIB2_L	-	

LFSC/M25, LFSC/M40 Logic Signal Connections: 1020 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M25			LFSC/M40		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AB3	NC	-		PR58B	3	
AB4	NC	-		PR58A	3	
AG4	NC	-		PR57D	3	
AG3	NC	-		PR57C	3	
AA2	NC	-		PR57B	3	
AB2	NC	-		PR57A	3	
AA3	NC	-		PR56B	3	
AA4	NC	-		PR56A	3	
L5	NC	-		PR22D	2	
L6	NC	-		PR22C	2	
M2	NC	-		PR34B	2	
L2	NC	-		PR34A	2	
L3	NC	-		PR31B	2	
M3	NC	-		PR31A	2	
L4	NC	-		PR30B	2	
M4	NC	-		PR30A	2	
P7	NC	-		PR29D	2	
P8	NC	-		PR29C	2	
K1	NC	-		PR29B	2	
K2	NC	-		PR29A	2	
N6	NC	-		PR27D	2	
N7	NC	-		PR27C	2	
J2	NC	-		PR27B	2	
J1	NC	-		PR27A	2	
N5	NC	-		PR26D	2	
M5	NC	-		PR26C	2	
H3	NC	-		PR26B	2	
J3	NC	-		PR26A	2	
A5	VDDAX25_R	-		VDDAX25_R	-	
A28	VDDAX25_L	-		VDDAX25_L	-	
AJ25	NC	-		PB21A	5	
AK25	NC	-		PB21B	5	
AF20	NC	-		PB27C	5	
AG6	NC	-		PB62C	4	
AM7	NC	-		PB66A	4	
AL7	NC	-		PB66B	4	
AD13	NC	-		PB66C	4	
AC13	NC	-		PB66D	4	
AC20	NC	-		PB22C	5	
AD20	NC	-		PB22D	5	
AM9	NC	-		PB61A	4	
AM8	NC	-		PB61B	4	
AF13	NC	-		PB61C	4	
AE13	NC	-		PB61D	4	
E30	VCC12	-		VCC12	-	
E29	VCC12	-		VCC12	-	
E27	VCC12	-		VCC12	-	
E26	VCC12	-		VCC12	-	
E25	VCC12	-		VCC12	-	
E24	VCC12	-		VCC12	-	

LFSC/M40, LFSC/M80 Logic Signal Connections: 1152 fcBGA[1, 2] (Cont.)

	LFSC/M40			LFSC/M80		
Ball Number	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AD8	PR65C	3		PR89C	3	
AJ3	PR65B	3		PR89B	3	
AH3	PR65A	3		PR89A	3	
AD7	PR62D	3		PR86D	3	
AC7	PR62C	3		PR86C	3	
AJ2	PR62B	3		PR86B	3	
AH2	PR62A	3		PR86A	3	
AF6	PR61D	3		PR85D	3	
AF5	PR61C	3		PR85C	3	
AF4	PR61B	3		PR85B	3	
AE4	PR61A	3		PR85A	3	
AD6	PR60D	3		PR84D	3	
AC6	PR60C	3		PR84C	3	
AG2	PR60B	3		PR84B	3	
AF2	PR60A	3		PR84A	3	
AC8	PR58D	3		PR82D	3	
AB8	PR58C	3		PR82C	3	
AK1	PR58B	3		PR82B	3	
AJ1	PR58A	3		PR82A	3	
AB10	PR57D	3		PR81D	3	
AA10	PR57C	3		PR81C	3	
AF3	PR57B	3		PR81B	3	
AE3	PR57A	3		PR81A	3	
AE5	PR56D	3		PR80D	3	
AD5	PR56C	3		PR80C	3	
AE2	PR56B	3		PR80B	3	
AD2	PR56A	3		PR80A	3	
AC5	PR53D	3		PR78D	3	
AB5	PR53C	3		PR78C	3	
AF1	PR53B	3		PR78B	3	
AE1	PR53A	3		PR78A	3	
AA11	PR52D	3		PR77D	3	
Y11	PR52C	3		PR77C	3	
AC4	PR52B	3		PR77B	3	
AB4	PR52A	3		PR77A	3	
AA8	PR51D	3	DIFFR_3	PR76D	3	DIFFR_3
AA9	PR51C	3		PR76C	3	
AC3	PR51B	3		PR76B	3	
AB3	PR51A	3		PR76A	3	
AA7	PR49D	3		PR65D	3	
Y7	PR49C	3		PR65C	3	
AA2	PR49B	3		PR65B	3	
Y2	PR49A	3		PR65A	3	
AA6	PR48D	3		PR63D	3	
Y6	PR48C	3		PR63C	3	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

	LFSC/M115		
Ball Number	Ball Function	VCCIO Bank	Dual Function
G27	A_REFCLKP_L	-	
H27	A_REFCLKN_L	-	
H25	VCC12	-	
H26	RESP_ULC	-	
B33	RESETN	1	
C34	TSALLN	1	
D34	DONE	1	
C33	INITN	1	
J27	M0	1	
K27	M1	1	
M26	M2	1	
L26	M3	1	
F30	PL15A	7	ULC_PLLT_IN_A/ULC_PLLT_FB_B
G30	PL15B	7	ULC_PLLC_IN_A/ULC_PLLC_FB_B
H28	PL15C	7	
J28	PL15D	7	
F31	PL17A	7	ULC_DLLT_IN_C/ULC_DLLT_FB_D
G31	PL17B	7	ULC_DLLC_IN_C/ULC_DLLC_FB_D
N25	PL17C	7	ULC_PLLT_IN_B/ULC_PLLT_FB_A
P25	PL17D	7	ULC_PLLC_IN_B/ULC_PLLC_FB_A
D33	PL18A	7	ULC_DLLT_IN_D/ULC_DLLT_FB_C
E33	PL18B	7	ULC_DLLC_IN_D/ULC_DLLC_FB_C
H29	PL18C	7	
J29	PL18D	7	VREF2_7
F32	PL19A	7	
G32	PL19B	7	
P26	PL19C	7	
N26	PL19D	7	
H30	PL26A	7	
J30	PL26B	7	
L28	PL26C	7	
M28	PL26D	7	
J31	PL43A	7	
K31	PL43B	7	
L27	PL43C	7	VREF1_7
M27	PL43D	7	DIFFR_7
J32	PL45A	7	
K32	PL45B	7	
L29	PL45C	7	
M29	PL45D	7	
H33	PL47A	7	
J33	PL47B	7	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

	LFSC/M115		
Ball Number	Ball Function	VCCIO Bank	Dual Function
F6	A_VDDOB0_R	-	
B4	A_HDOUTN0_R	-	PCS 3E0 CH 0 OUT N
F7	A_VDDOB1_R	-	
B5	A_HDOUTN1_R	-	PCS 3E0 CH 1 OUT N
E6	VCC12	-	
A5	A_HDOUTP1_R	-	PCS 3E0 CH 1 OUT P
B6	A_HDINN1_R	-	PCS 3E0 CH 1 IN N
A6	A_HDINP1_R	-	PCS 3E0 CH 1 IN P
C6	VCC12	-	
D4	A_VDDIB1_R	-	
C7	VCC12	-	
D5	A_VDDIB2_R	-	
A7	A_HDINP2_R	-	PCS 3E0 CH 2 IN P
B7	A_HDINN2_R	-	PCS 3E0 CH 2 IN N
E7	VCC12	-	
A8	A_HDOUTP2_R	-	PCS 3E0 CH 2 OUT P
F8	A_VDDOB2_R	-	
B8	A_HDOUTN2_R	-	PCS 3E0 CH 2 OUT N
F9	A_VDDOB3_R	-	
B9	A_HDOUTN3_R	-	PCS 3E0 CH 3 OUT N
E8	VCC12	-	
A9	A_HDOUTP3_R	-	PCS 3E0 CH 3 OUT P
B10	A_HDINN3_R	-	PCS 3E0 CH 3 IN N
A10	A_HDINP3_R	-	PCS 3E0 CH 3 IN P
C10	VCC12	-	
D6	A_VDDIB3_R	-	
G10	VCC12	-	
D7	B_VDDIB0_R	-	
E10	B_HDINP0_R	-	PCS 3E1 CH 0 IN P
F10	B_HDINN0_R	-	PCS 3E1 CH 0 IN N
K10	VCC12	-	
A11	B_HDOUTP0_R	-	PCS 3E1 CH 0 OUT P
D10	B_VDDOB0_R	-	
B11	B_HDOUTN0_R	-	PCS 3E1 CH 0 OUT N
D11	B_VDDOB1_R	-	
B12	B_HDOUTN1_R	-	PCS 3E1 CH 1 OUT N
L10	VCC12	-	
A12	B_HDOUTP1_R	-	PCS 3E1 CH 1 OUT P
F11	B_HDINN1_R	-	PCS 3E1 CH 1 IN N
E11	B_HDINP1_R	-	PCS 3E1 CH 1 IN P
G11	VCC12	-	
D8	B_VDDIB1_R	-	
G12	VCC12	-	

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

	LFSC/M115		
Ball Number	Ball Function	VCCIO Bank	Dual Function
D9	B_VDDIB2_R	-	
E12	B_HDINP2_R	-	PCS 3E1 CH 2 IN P
F12	B_HDINN2_R	-	PCS 3E1 CH 2 IN N
K11	VCC12	-	
A13	B_HDOUTP2_R	-	PCS 3E1 CH 2 OUT P
D12	B_VDDOB2_R	-	
B13	B_HDOUTN2_R	-	PCS 3E1 CH 2 OUT N
D13	B_VDDOB3_R	-	
B14	B_HDOUTN3_R	-	PCS 3E1 CH 3 OUT N
L11	VCC12	-	
A14	B_HDOUTP3_R	-	PCS 3E1 CH 3 OUT P
F13	B_HDINN3_R	-	PCS 3E1 CH 3 IN N
E13	B_HDINP3_R	-	PCS 3E1 CH 3 IN P
G13	VCC12	-	
E9	B_VDDIB3_R	-	
L13	VCC12	-	
J11	B_REFCLKN_R	-	
H11	B_REFCLKP_R	-	
M15	PT93D	1	HDC/SI
M16	PT93C	1	LDCN/SCS
F14	PT93B	1	D8/MPI_DATA8
G14	PT93A	1	CS1/MPI_CS1
L15	PT90D	1	D9/MPI_DATA9
L14	PT90C	1	D10/MPI_DATA10
D14	PT90B	1	CS0N/MPI_CS0N
E14	PT90A	1	RDN/MPI_STRB_N
L16	PT89D	1	WRN/MPI_WR_N
K16	PT89C	1	D7/MPI_DATA7
G15	PT89B	1	D6/MPI_DATA6
F15	PT89A	1	D5/MPI_DATA5
K14	PT87D	1	D4/MPI_DATA4
K13	PT87C	1	D3/MPI_DATA3
B15	PT87B	1	D2/MPI_DATA2
A15	PT87A	1	D1/MPI_DATA1
J14	PT86D	1	D16/PCLKC1_3/MPI_DATA16
H14	PT86C	1	D17/PCLKT1_3/MPI_DATA17
A16	PT86B	1	D0/MPI_DATA0
B16	PT86A	1	QOUT/CEON
J13	PT83D	1	VREF2_1
H13	PT83C	1	D18/MPI_DATA18
D15	PT83B	1	DOUT
E15	PT83A	1	MCA_DONE_IN
J16	PT81D	1	D19/PCLKC1_2/MPI_DATA19

LFSC/M115 Logic Signal Connections: 1152 fcBGA[1, 2]

	LFSC/M115		
Ball Number	Ball Function	VCCIO Bank	Dual Function
Y18	VCC	-	
Y20	VCC	-	
AB15	VCC12	-	
AB20	VCC12	-	
N15	VCC12	-	
N20	VCC12	-	
R13	VCC12	-	
R22	VCC12	-	
Y13	VCC12	-	
Y22	VCC12	-	
AA12	VCCAUX	-	
AA23	VCCAUX	-	
AB12	VCCAUX	-	
AB16	VCCAUX	-	
AB17	VCCAUX	-	
AB18	VCCAUX	-	
AB19	VCCAUX	-	
AB23	VCCAUX	-	
AC12	VCCAUX	-	
AC13	VCCAUX	-	
Y19	GND	-	
AC14	VCCAUX	-	
AC17	VCCAUX	-	
AC21	VCCAUX	-	
AC22	VCCAUX	-	
AC23	VCCAUX	-	
M13	VCCAUX	-	
M14	VCCAUX	-	
M18	VCCAUX	-	
M21	VCCAUX	-	
M22	VCCAUX	-	
N12	VCCAUX	-	
N16	VCCAUX	-	
N17	VCCAUX	-	
N18	VCCAUX	-	
N19	VCCAUX	-	
N23	VCCAUX	-	
P12	VCCAUX	-	
P23	VCCAUX	-	
T13	VCCAUX	-	
T22	VCCAUX	-	
U12	VCCAUX	-	
U13	VCCAUX	-	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

	LFSC/M80			LFSC/M115		
Ball Number	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AV32	PB27B	5		PB29B	5	
AU36	PB27C	5		PB29C	5	
AU37	PB27D	5		PB29D	5	
BA35	PB28A	5		PB30A	5	
BA34	PB28B	5		PB30B	5	
AJ26	PB28C	5		PB30C	5	
AJ27	PB28D	5		PB30D	5	
AW33	PB29A	5		PB31A	5	
AW32	PB29B	5		PB31B	5	
AU35	PB29C	5		PB31C	5	
AU34	PB29D	5		PB31D	5	
BB35	PB31A	5		PB33A	5	
BB34	PB31B	5		PB33B	5	
AN29	PB31C	5		PB33C	5	
AP29	PB31D	5		PB33D	5	
AY33	PB32A	5		PB34A	5	
AY32	PB32B	5		PB34B	5	
AR31	PB32C	5		PB34C	5	
AR30	PB32D	5		PB34D	5	
AV31	PB33A	5		PB35A	5	
AV30	PB33B	5		PB35B	5	
AN28	PB33C	5		PB35C	5	
AP28	PB33D	5		PB35D	5	
BA33	PB35A	5		PB37A	5	
BA32	PB35B	5		PB37B	5	
AT30	PB35C	5		PB37C	5	
AT31	PB35D	5		PB37D	5	
BB33	PB36A	5		PB38A	5	
BB32	PB36B	5		PB38B	5	
AM26	PB36C	5		PB38C	5	
AL26	PB36D	5		PB38D	5	
AW30	PB37A	5		PB39A	5	
AW29	PB37B	5		PB39B	5	
AP27	PB37C	5		PB39C	5	
AN27	PB37D	5		PB39D	5	
BA31	PB39A	5		PB41A	5	
BA30	PB39B	5		PB41B	5	
AU32	PB39C	5		PB41C	5	
AU33	PB39D	5		PB41D	5	
BB31	PB40A	5		PB42A	5	
BB30	PB40B	5		PB42B	5	
AR28	PB40C	5		PB42C	5	
AR27	PB40D	5		PB42D	5	
AV29	PB41A	5		PB43A	5	
AV28	PB41B	5		PB43B	5	

LFSC/M80, LFSC/M115 Logic Signal Connections: 1704 fcBGA[1, 2] (Cont.)

Ball Number	LFSC/M80			LFSC/M115		
	Ball Function	VCCIO Bank	Dual Function	Ball Function	VCCIO Bank	Dual Function
AP1	PR90B	3		PR109B	3	
AN1	PR90A	3		PR109A	3	
AK10	PR89D	3	VREF2_3	PR107D	3	VREF2_3
AJ10	PR89C	3		PR107C	3	
AM5	PR89B	3		PR107B	3	
AL5	PR89A	3		PR107A	3	
AL7	PR86D	3		PR104D	3	
AK7	PR86C	3		PR104C	3	
AM1	PR86B	3		PR104B	3	
AL1	PR86A	3		PR104A	3	
AJ11	PR85D	3		PR103D	3	
AH11	PR85C	3		PR103C	3	
AK5	PR85B	3		PR103B	3	
AJ5	PR85A	3		PR103A	3	
AK9	PR84D	3		PR99D	3	
AJ9	PR84C	3		PR99C	3	
AK3	PR84B	3		PR99B	3	
AJ3	PR84A	3		PR99A	3	
AK6	PR82D	3		PR98D	3	
AJ6	PR82C	3		PR98C	3	
AK2	PR82B	3		PR98B	3	
AJ2	PR82A	3		PR98A	3	
AH10	PR81D	3		PR96D	3	
AG10	PR81C	3		PR96C	3	
AK1	PR81B	3		PR96B	3	
AJ1	PR81A	3		PR96A	3	
AH9	PR80D	3		PR94D	3	
AG9	PR80C	3		PR94C	3	
AH2	PR80B	3		PR94B	3	
AG2	PR80A	3		PR94A	3	
AH8	PR78D	3		PR92D	3	
AG8	PR78C	3		PR92C	3	
AG1	PR78B	3		PR92B	3	
AH1	PR78A	3		PR92A	3	
AG14	PR77D	3		PR91D	3	
AF14	PR77C	3		PR91C	3	
AG4	PR77B	3		PR91B	3	
AF4	PR77A	3		PR91A	3	
AH7	PR76D	3	DIFFR_3	PR90D	3	DIFFR_3
AG7	PR76C	3		PR90C	3	
AG3	PR76B	3		PR90B	3	
AF3	PR76A	3		PR90A	3	
AH6	PR74D	3		PR88D	3	
AG6	PR74C	3		PR88C	3	
AF1	PR74B	3		PR88B	3	

Industrial, Cont.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA40EP1-6FF1020I[1]	-6	Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-5FF1020I[1]	-5	Organic fcBGA	1020	IND	40.4
LFSCM3GA40EP1-6FFA1020I	-6	Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-5FFA1020I	-5	Organic fcBGA Revision 2	1020	IND	40.4
LFSCM3GA40EP1-6FC1152I[2]	-6	Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FC1152I[2]	-5	Ceramic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-6FF1152I	-6	Organic fcBGA	1152	IND	40.4
LFSCM3GA40EP1-5FF1152I	-5	Organic fcBGA	1152	IND	40.4

1. Converted to organic flip-chip BGA package revision 2 per PCN #02A-10.
2. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSC3GA80E-6FC1152I[1]	-6	Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-5FC1152I[1]	-5	Ceramic fcBGA	1152	IND	80.1
LFSC3GA80E-6FF1152I	-6	Organic fcBGA	1152	IND	80.1
LFSC3GA80E-5FF1152I	-5	Organic fcBGA	1152	IND	80.1
LFSC3GA80E-6FC1704I[1]	-6	Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-5FC1704I[1]	-5	Ceramic fcBGA	1704	IND	80.1
LFSC3GA80E-6FF1704I	-6	Organic fcBGA	1704	IND	80.1
LFSC3GA80E-5FF1704I	-5	Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Part Number	Grade	Package	Balls	Temp.	LUTs (K)
LFSCM3GA80EP1-6FC1152I[1]	-6	Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FC1152I[1]	-5	Ceramic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FF1152I	-6	Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-5FF1152I	-5	Organic fcBGA	1152	IND	80.1
LFSCM3GA80EP1-6FC1704I[1]	-6	Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FC1704I[1]	-5	Ceramic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-6FF1704I	-6	Organic fcBGA	1704	IND	80.1
LFSCM3GA80EP1-5FF1704I	-5	Organic fcBGA	1704	IND	80.1

1. Converted to organic flip-chip BGA package per PCN #01A-10.

Date	Version	Section	Change Summary
August 2006 (cont.)	01.3 (cont.)	DC and Switching Characteristics (cont.)	Updated LatticeSC Family Timing Adders with ispLEVER 6.0 SP1 results
			Updated PLL Timing Parameters based on PDE testing results
			Removed RDDATA parameter from sysCONFIG readback timing table
		Multiple	Changed TDO/RDDATA to TDO
		Pinout Information	Removed all MPI signals from SC15 256 pin package Dual Function Column
			Added note to SC15, SC25 900 pin package that the package supports a 16 bit MPI
			Added note that pin D3 in an SC15 and SC25 900 pin package should not be used for single-ended outputs
			Added note that pin D28 in an SC15 and SC25 900 pin package should not be used for single-ended outputs
			Added note to SC25 1020 pin package that the package supports a 16 bit MPI
			Added note to SC80 1152 pin package that the package supports a 32 bit MPI
			Added note to SC80 1704 pin package that the package supports a 32 bit MPI
		Ordering Information	Changed “fcBGA” for the 1020 packages to “ffBGA”
November 2006	01.4	Introduction	LatticeSC Family Selection Guide table – I/O count for SC80 device, 1704 fcBGA package changed to 904/32. I/O count for SC115 device, 1704 fcBGA package changed to 942/32.
		DC and Switching Characteristics	DC Electrical Characteristics table – Updated the initialization and standby supply current values.
			DC Electrical Characteristics table – Updated the sysCONFIG Master Parallel mode RCLK low and RCLK high time specifications.
			DC Electrical Characteristics table – Updated VCCIO values for LVPECL33 I/Os.
		Pin Information	Pin Information Summary table - Changed number of single ended user I/Os from 906 to 904 for 1704 fcBGA.
			Removed the single-ended only output restriction on pins D3 and D28 in an SC15 and SC25 900 pin package.
		Ordering Information	Ordering Information tables - Changed number of I/Os from 906 to 904 for 1704 fcBGA.
			Added ordering part numbers for LatticeSC/SCM 40K and 115K LUT devices.
			Added lead-free ordering part numbers.
		Multiple	Changed number of available SC80 I/O from 906 to 904.
			Changed number of available SC115 I/O from 944 to 942.
January 2007	01.4a	Architecture	Added EBR Asynchronous Reset section.
February 2007	01.4b	Architecture	Updated EBR Asynchronous Reset section.
March 2007	01.5	Architecture	Added EBR asynchronous reset clarification
			Clarified that differential drivers are not supported in banks 1, 4 and 5
		DC and Switching Characteristics	Added clarification for the description of the junction temperature specification in the Absolute Maximum Ratings section.
			Updated Initialization and Standby Current table.
			Updated LatticeSC External Switching Characteristics with ispLEVER 6.1 SP1 results.