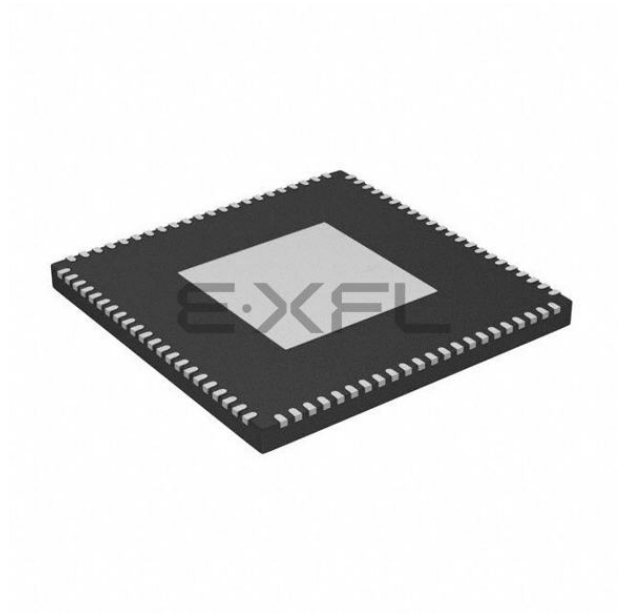

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI, EBI/EMI, I²C, SPI, SPORT, UART/USART
Clock Rate	200MHz
Non-Volatile Memory	ROM (4Mbit)
On-Chip RAM	3Mbit
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	88-VFQFN Exposed Pad, CSP
Supplier Device Package	88-LFCSP-VQ (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ad21478wycpz1a02

buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

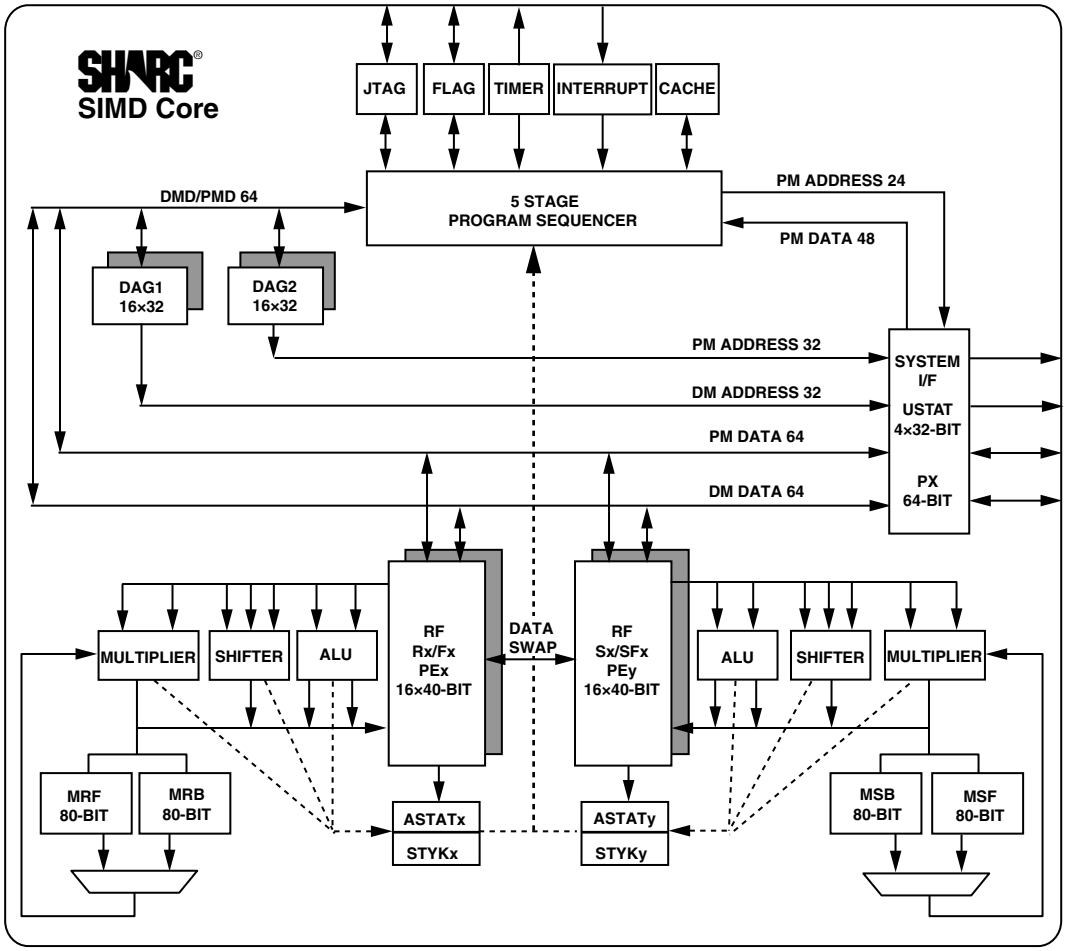

Figure 2. SHARC Core Block Diagram

Instruction Cache

The processor includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full speed execution of core looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators with Zero-Overhead Hardware Circular Buffer Support

The processor's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the processors contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the processors can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

Variable Instruction Set Architecture (VISA)

In addition to supporting the standard 48-bit instructions from previous SHARC processors, the processors support new instructions of 16 and 32 bits. This feature, called Variable Instruction Set Architecture (VISA), drops redundant/unused

bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external SDRAM memory. This support is not extended to the asynchronous memory interface (AMI). Source modules need to be built using the VISA option, in order to allow code generation tools to create these more efficient opcodes.

On-Chip Memory

The processors contain varying amounts of internal RAM and internal ROM which is shown in Table 3 through Table 5. Each block can be configured for different combinations of code and data storage. Each memory block supports single-cycle, independent accesses by the core processor and I/O processor.

The processor's SRAM can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5M bits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

The memory maps in Table 3 through Table 5 display the internal memory address space of the processors. The 48-bit space section describes what this address range looks like to an instruction that retrieves 48-bit memory. The 32-bit section describes what this address range looks like to an instruction that retrieves 32-bit memory.

Table 3. ADSP-21477 Internal Memory Space (2M bits)

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 FFFF
Block 0 SRAM 0x0004 9000–0x0004 BFFF	Block 0 SRAM 0x0008 C000–0x0008 FFFF	Block 0 SRAM 0x0009 2000–0x0009 7FFF	Block 0 SRAM 0x0012 4000–0x0012 FFFF
Reserved 0x0004 C000–0x0004 FFFF	Reserved 0x0009 000–0x0009 5554	Reserved 0x0009 8000–0x0009 FFFF	Reserved 0x0013 0000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000AFFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 BFFF	Block 1 SRAM 0x000A C000–0x000A FFFF	Block 1 SRAM 0x000B 2000–0x000B 7FFF	Block 1 SRAM 0x0016 4000–0x0016 FFFF
Reserved 0x0005 C000–0x0005 FFFF	Reserved 0x000B 0000–0x000B 5554	Reserved 0x000B 8000–0x000B FFFF	Reserved 0x0017 0000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 0FFF	Block 2 SRAM 0x000C 0000–0x000C 1554	Block 2 SRAM 0x000C 0000–0x000C 1FFF	Block 2 SRAM 0x0018 0000–0x0018 3FFF
Reserved 0x0006 1000– 0x0006 FFFF	Reserved 0x000C 1555–0x000D 5554	Reserved 0x000C 2000–0x000D FFFF	Reserved 0x0018 4000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 0FFF	Block 3 SRAM 0x000E 0000–0x000E 1554	Block 3 SRAM 0x000E 0000–0x000E 1FFF	Block 3 SRAM 0x001C 0000–0x001C 3FFF
Reserved 0x0007 1000–0x0007 FFFF	Reserved 0x000E 1555–0x000F 5554	Reserved 0x000E 2000–0x000F FFFF	Reserved 0x001C 4000–0x001F FFFF

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface ports (SPI), one universal asynchronous receiver-transmitter (UART), 12 flags, a 2-wire interface (TWI), three PWM modules (PWM3–1), and two general-purpose timers.

Serial Peripheral (Compatible) Interface (SPI)

The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible port to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multi-master environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The SPI-compatible port uses open drain drivers to support a multi-master configuration and to avoid data contention.

UART Port

The processors provide a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Support for bit rates ranging from (f_{PCLK}/1,048,576) to (f_{PCLK}/16) bits per second.
- Support for data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs generating 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

PWM signals can be mapped to the external port address lines or to the DPI pins.

Timers

The processors have a total of three timers: a core timer that can generate periodic software interrupts and two general-purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watch dog mode

The core timer can be configured to use FLAG3 as a timer expired signal, and the general-purpose timers have one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables the general-purpose timer.

2-Wire Interface Port (TWI)

The TWI is a bidirectional 2-wire serial bus used to move 8-bit data while maintaining compliance with the I^2C bus protocol. The TWI master incorporates the following features:

- 7-bit addressing
- Simultaneous master and slave operation on multiple device systems with support for multi-master data arbitration
- Digital filtering and timed event processing
- 100 kbps and 400 kbps data rates
- Low interrupt rate

seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

PIN FUNCTION DESCRIPTIONS

Table 11. Pin Descriptions

Name	Type	State During/ After Reset	Description
$ADDR_{23-0}$	I/O/T (ipu)	High-Z/driven low (boot)	**External Address.** The processor outputs addresses for external memory and peripherals on these pins. The ADDR pins can be multiplexed to support the external memory interface address, FLAGS15–8 (I/O) and PWM (O). After reset, all ADDR pins are in EMIF mode, and FLAG(0–3) pins are in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the $ADDR_{23-4}$ pins for parallel input data.
$DATA_{15-0}$	I/O/T (ipu)	High-Z	**External Data.** The data pins can be multiplexed to support the external memory interface data (I/O) and $FLAGS_{7-0}$ (I/O).
AMI_ACK	I (ipu)		**Memory Acknowledge.** External devices can deassert AMI_ACK (low) to add wait states to an external memory access. AMI_ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{MS}_{0-1}$	O/T (ipu)	High-Z	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{1-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, when the condition evaluates as true. The $\overline{MS1}$ pin can be used in EPORT/FLASH boot mode. For more information on processor booting, see the *ADSP-214xx SHARC Processor Hardware Reference*.
$\overline{AMI\_RD}$	O/T (ipu)	High-Z	**AMI Port Read Enable.** $\overline{AMI\_RD}$ is asserted whenever the processor reads a word from external memory.
$\overline{AMI\_WR}$	O/T (ipu)	High-Z	**AMI Port Write Enable.** $\overline{AMI\_WR}$ is asserted when the processor writes a word to external memory.
FLAG0/$\overline{IRQ0}$	I/O (ipu)	FLAG[0] INPUT	**FLAG0/Interrupt Request0.**
FLAG1/$\overline{IRQ1}$	I/O (ipu)	FLAG[1] INPUT	**FLAG1/Interrupt Request1.**
FLAG2/$\overline{IRQ2}$/$\overline{MS2}$	I/O (ipu)	FLAG[2] INPUT	**FLAG2/Interrupt Request2/Memory Select2.** This pin is multiplexed with $\overline{MS2}$ in the 196-ball BGA package only.
FLAG3/TMREXP/$\overline{MS3}$	I/O (ipu)	FLAG[3] INPUT	**FLAG3/Timer Expired/Memory Select3.** This pin is multiplexed with $\overline{MS3}$ in the 196-ball BGA package only.

The following symbols appear in the Type column of Table 11: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be 26 kΩ to 63 kΩ. The range of an ipd resistor can be 31 kΩ to 85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.

Not all pins are available in the 88-lead LFCSP_VQ and 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 62 on Page 70.

SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter[1]	Description	200 MHz			266 MHz			300 MHz			Unit
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{DD_INT}	Internal (Core) Supply Voltage	1.14	1.2	1.26	1.14	1.2	1.26	1.25	1.3	1.35	V
V_{DD_EXT}	External (I/O) Supply Voltage	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
V_{DD_THD}	Thermal Diode Supply Voltage	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
V_{DD_RTC}	Real-Time Clock Power Supply Voltage	2.0	3.0	3.6	2.0	3.0	3.6	2.0	3.0	3.6	V
V_{IH}[2]	High Level Input Voltage @ V_{DD_EXT} = Max	2.0			2.0			2.0			V
V_{IL}[3]	Low Level Input Voltage @ V_{DD_EXT} = Min			0.8			0.8			0.8	V
V_{IH_CLKIN}[3]	High Level Input Voltage @ V_{DD_EXT} = Max	2.2		V_{DD_EXT}	2.2		V_{DD_EXT}	2.2		V_{DD_EXT}	V
V_{IL_CLKIN}	Low Level Input Voltage @ V_{DD_EXT} = Max	–0.3		+0.8	–0.3		+0.8	–0.3		+0.8	V
T_J	Junction Temperature 88-Lead LFCSP_VQ @ $T_{AMBIENT}$ 0°C to +70°C	0		105	N/A		N/A	N/A		N/A	°C
T_J	Junction Temperature 88-Lead LFCSP_VQ @ $T_{AMBIENT}$ –40°C to +85°C	–40		+115	N/A		N/A	N/A		N/A	°C
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C	0		105	0		105	N/A		N/A	°C
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	N/A		N/A	–40		+125	N/A		N/A	°C
T_J[4]	Junction Temperature 196-Ball CSP_BGA @ $T_{AMBIENT}$ 0°C to +70°C	N/A		N/A	0		105	0		100	°C
T_J	Junction Temperature 196-Ball CSP_BGA @ $T_{AMBIENT}$ –40°C to +85°C	N/A		N/A	–40		+125	N/A		N/A	°C
AUTOMOTIVE USE ONLY											
T_J	Junction Temperature 88-Lead LFCSP_VQ @ $T_{AMBIENT}$ –40°C to +105°C (Automotive Grade)	–40		+125[5]	N/A		N/A	N/A		N/A	°C
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +105°C (Automotive Grade)	–40		+125[5]	–40		+125	N/A		N/A	°C
T_J[4]	Junction Temperature 196-Ball CSP_BGA @ $T_{AMBIENT}$ –40°C to +105°C (Automotive Grade)	–40		+125[5]	N/A		N/A	N/A		N/A	°C

[1] Specifications subject to change without notice.

[2] Applies to input and bidirectional pins: ADDR23–0, DATA15–0, FLAG3–0, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{\text{RUNRSTIN}}$, $\overline{\text{RESET}}$, TCK, TMS, TDI, $\overline{\text{TRST}}$, SDA10, AMI_ACK, MLBCLK, MLBDAT, MLBSIG.

[3] Applies to input pin CLKIN, WDT_CLKIN.

[4] Real Time Clock (RTC) is supported only for products in the BGA package with a temperature range of 0°C to +70°C. For the status of unused RTC pins please see Table 11.

[5] Automotive application use profile only. Not supported for nonautomotive use. Contact Analog Devices for more information.

Total Power Dissipation

The information in this section should be augmented with *Estimating Power for ADSP-214xx SHARC Processors (EE-348)*. Total power dissipation has two components:

1. Internal power consumption is additionally comprised of two components:
   - Static current due to leakage. Table 14 shows the static current consumption ($I_{DD\_INT\_STATIC}$) as a function of junction temperature (T_J) and core voltage (V_{DD_INT}).
   - Dynamic current ($I_{DD\_INT\_DYNAMIC}$), due to transistor switching characteristics and activity level of the processor. The activity level is reflected by the Activity Scaling Factor (ASF), which represents the activity level of the application code running on the processor core and having various levels of peripheral and external port activity (Table 13). Dynamic current consumption is calculated by selecting the ASF that corresponds most closely with the user application and then multiplying that with the dynamic current consumption (Table 15).
2. External power consumption is due to the switching activity of the external pins.

Table 13. Activity Scaling Factors (ASF)[1]

Activity	Scaling Factor (ASF)
Idle	0.31
Low	0.53
Medium Low	0.62
Medium High	0.78
Peak-Typical (50:50)[2]	0.85
Peak-Typical (60:40)[2]	0.93
Peak-Typical (70:30)[2]	1.00
High Typical	1.18
High	1.28
Peak	1.34

[1] See *Estimating Power for ADSP-214xx SHARC Processors (EE-348)* for more information on the explanation of the power vectors specific to the ASF table.
[2] Ratio of continuous instruction loop (core) to SDRAM control code reads and writes.

Table 14. Static Current—$I_{DD\_INT\_STATIC}$ (mA)[1]

	Voltage (V_{DD_INT})						
T_J (°C)	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V
–45	< 0.1	< 0.1	0.4	0.8	1.3	2.1	3.3
–35	< 0.1	< 0.1	0.4	0.7	1.1	1.7	2.9
–25	< 0.1	0.2	0.4	0.8	1.2	1.7	2.9
–15	< 0.1	0.4	0.6	1.0	1.4	1.9	3.2
–5	0.2	0.6	0.9	1.3	1.8	2.3	3.7
+5	0.5	0.9	1.3	1.8	2.3	3.0	4.4
+15	0.8	1.4	1.8	2.3	3.0	3.7	5.1
+25	1.3	1.9	2.5	3.1	3.9	4.7	6.2
+35	2.0	2.8	3.4	4.2	5.1	6.0	8.0
+45	3.0	3.9	4.7	5.7	6.7	7.8	10.1
+55	4.3	5.4	6.3	7.6	8.8	10.3	12.9
+65	6.0	7.3	8.6	10.1	11.7	13.5	16.4
+75	8.3	9.9	11.5	13.3	15.3	17.4	21.2
+85	11.2	13.2	15.3	17.5	19.9	22.6	27.1
+95	15.2	17.6	20.1	22.9	26.1	29.4	34.6
+100	17.4	20.2	22.9	25.9	29.4	33.0	39.2
+105	20.0	23.0	26.1	29.5	33.4	N/A	N/A
+115	26.3	30.0	33.9	38.2	42.9	N/A	N/A
+125	34.4	38.9	43.6	48.8	54.8	N/A	N/A

[1] Valid temperature and voltage ranges are model-specific. See Operating Conditions.

Running Reset

The following timing specification applies to $\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$ pin when it is configured as $\overline{\text{RUNRSTIN}}$.

Table 22. Running Reset

Parameter		Min	Max	Unit
Timing Requirements				
$t_{WRUNRST}$	Running $\overline{\text{RESET}}$ Pulse Width Low	$4 \times t_{CK}$		ns
$t_{SRUNRST}$	Running $\overline{\text{RESET}}$ Setup Before CLKIN High	8		ns

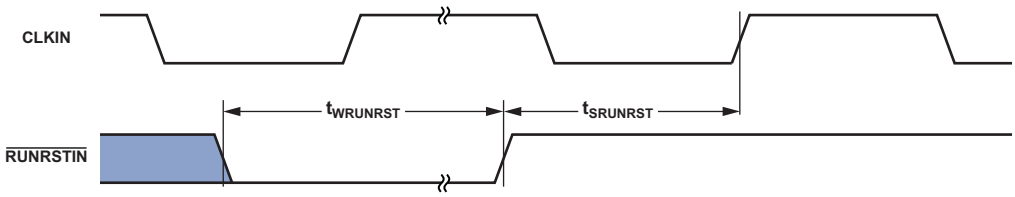

Figure 10. Running Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts, as well as the DAI_P20–1 and DPI_P14–1 pins when they are configured as interrupts.

Table 23. Interrupts

Parameter		Min	Max	Unit
Timing Requirement				
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{PCLK} + 2$		ns

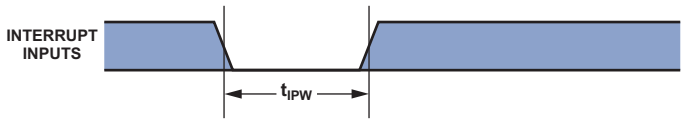

Figure 11. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

Table 24. Core Timer

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Switching Characteristic						
t_{WCTIM}	TMREXP Pulse Width	$4 \times t_{PCLK} - 1.55$		$4 \times t_{PCLK} - 1.2$		ns

Figure 12. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to timer0 and timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 25. Timer PWM_OUT Timing

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Switching Characteristic						
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 1.65$	$2 \times (2^{31} - 1) \times t_{PCLK}$	$2 \times t_{PCLK} - 1.2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

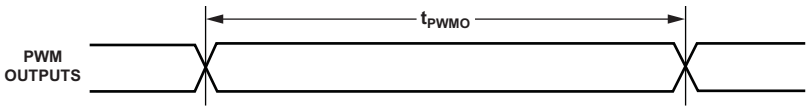

Figure 13. Timer PWM_OUT Timing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 – DAI_P20).

Table 29. Precision Clock Generator (Direct Pin Routing)

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{PCGIP}	Input Clock Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		3		ns
Switching Characteristics						
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2.5	$2 \times t_{PCLK}$	2.5	12.5	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2.5 + (2.5 \times t_{PCGIP})$	$2 \times t_{PCLK} + (2.5 \times t_{PCGIP})$	$2.5 + (2.5 \times t_{PCGIP})$	$12.5 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$2 \times t_{PCLK} + ((2.5 + D - PH) \times t_{PCGIP})$	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$12.5 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}[1]	Output Clock Period	$2 \times t_{PCGIP} - 1$		$2 \times t_{PCGIP} - 1$		ns

D = FSxDIV, PH = FSxPHASE. For more information, see the ADSP-214xx SHARC Processor Hardware Reference, "Precision Clock Generators" chapter.

[1] Normal mode of operation.

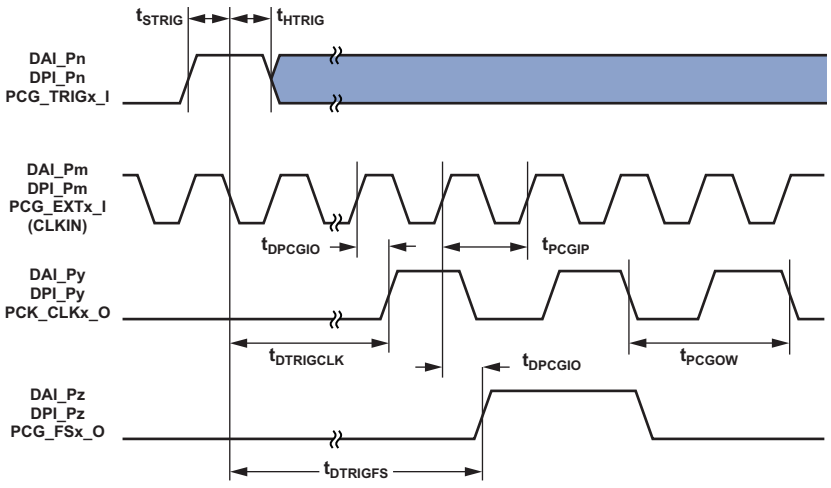

Figure 17. Precision Clock Generator (Direct Pin Routing)

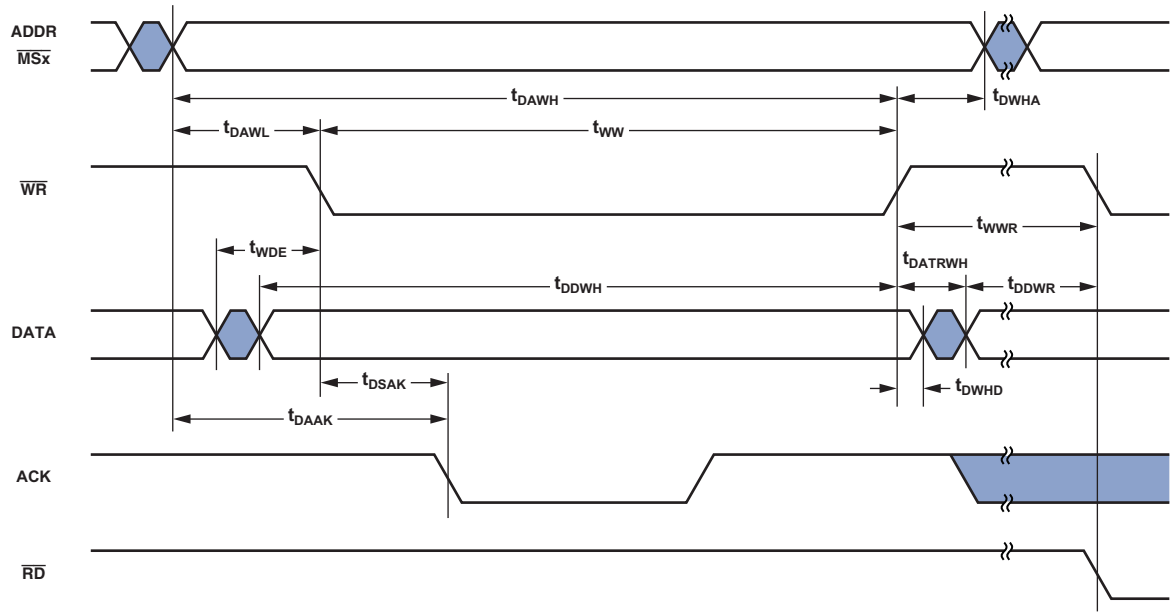

Figure 21. AMI Write

Serial Ports

In slave transmitter mode and master receiver mode, the maximum serial port frequency is $f_{PCLK}/8$. In master transmitter mode and slave receiver mode, the maximum serial port clock frequency is $f_{PCLK}/4$.

To determine whether communication is possible between two devices at clock speed, n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Serial port signals (SCLK, FS, Data Channel A, Data Channel B) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 34. Serial Ports—External Clock

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{SFSE}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	4		2.5		ns
t_{HFSE}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	4		2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	4		2.5		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	4		2.5		ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 1.5$		$(t_{PCLK} \times 4) \div 2 - 1.5$		ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns
Switching Characteristics						
t_{DFSE}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)		15		15	ns
t_{HOFSE}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)	2		2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		15		15	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 35. Serial Ports—Internal Clock

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	13		10.5		ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5		2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	13		10.5		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		2.5		ns
Switching Characteristics						
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		5		5	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1.0		–1.0		ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		10.7		10.7	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1.0		–1.0		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		4		4	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0		–1.0		ns
t_{SCKLIW}	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

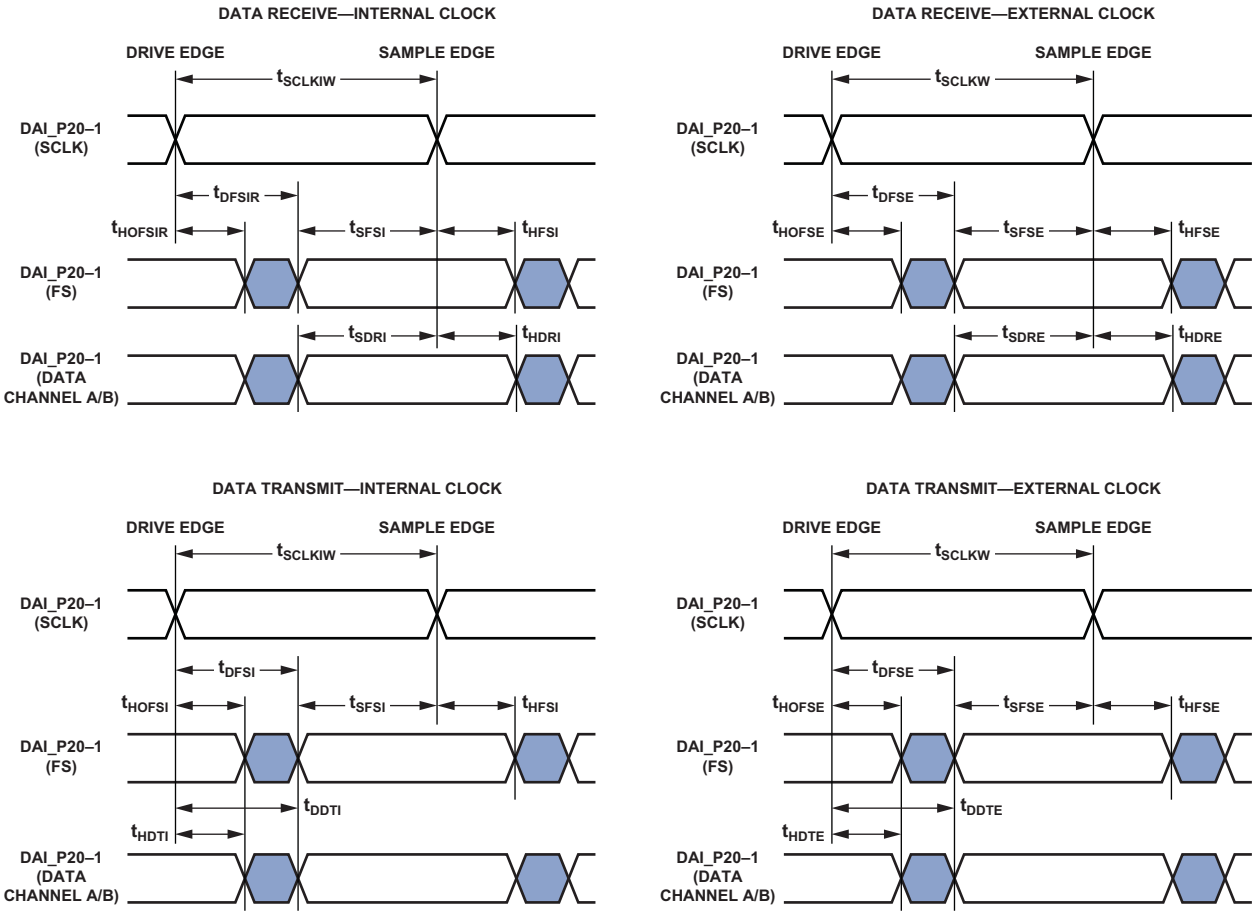

Figure 22. Serial Ports

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 39. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 39. Input Data Port (IDP)

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4.5		3.8		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		2.5		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	4		2.5		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

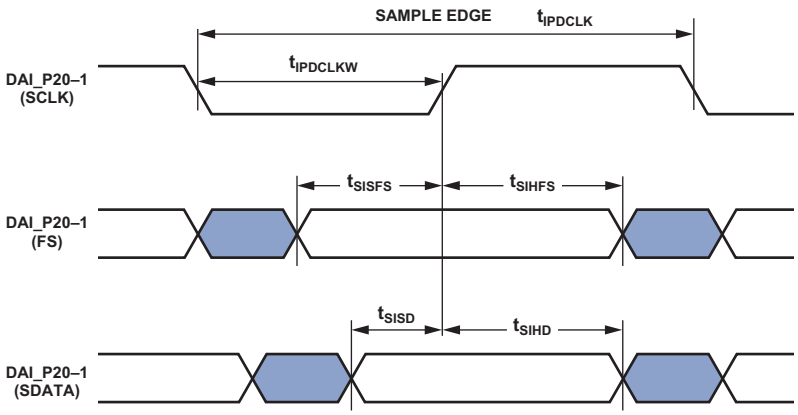

Figure 26. IDP Master Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left-justified, I²S, or right-justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 31 shows the right-justified mode. Frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed the minimum in 24-bit output mode or the maximum in 16-bit output mode from a frame sync transition, so that when there are 64 serial clock periods per frame sync period, the LSB of the data is right-justified to the next frame sync transition.

Figure 32 shows the default I²S-justified mode. The frame sync is low for the left channel and high for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition but with a delay.

Table 44. S/PDIF Transmitter Right-Justified Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{RJD}	FS to MSB Delay in Right-Justified Mode		
	16-Bit Word Mode	16	SCLK
	18-Bit Word Mode	14	SCLK
	20-Bit Word Mode	12	SCLK
	24-Bit Word Mode	8	SCLK

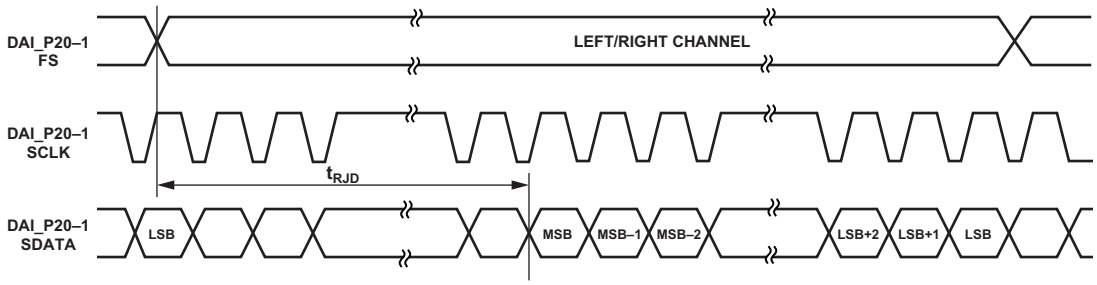

Figure 31. Right-Justified Mode

Table 45. S/PDIF Transmitter I²S Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{I2SD}	FS to MSB Delay in I²S Mode	1	SCLK

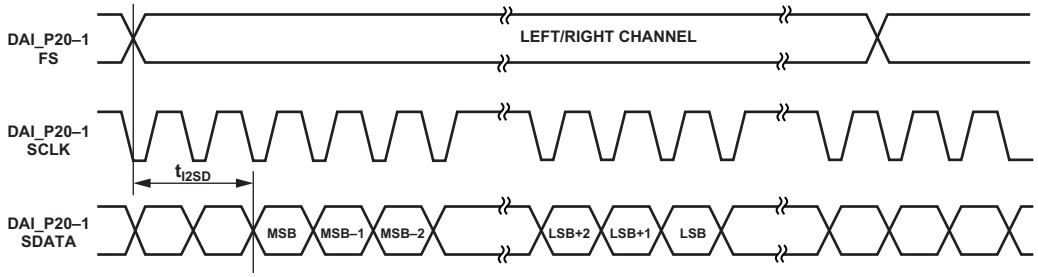

Figure 32. I²S-Justified Mode

Figure 33 shows the left-justified mode. The frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition with no delay.

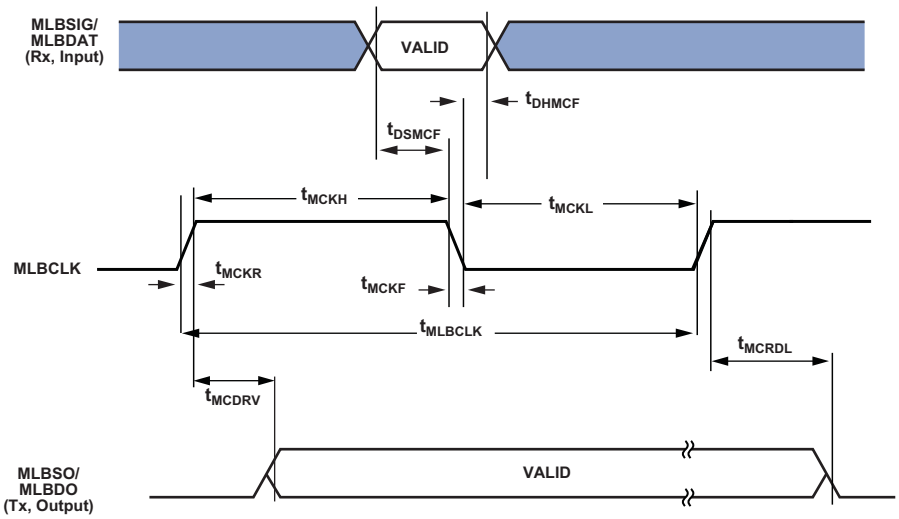

Figure 39. MLB Timing (5-Pin Interface)

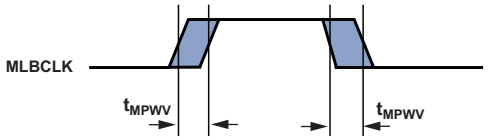

Figure 40. MLB 3-Pin and 5-Pin MLBCLK Pulse Width Variation Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the *ADSP-214xx SHARC Hardware Reference Manual*.

2-Wire Interface (TWI)—Receive and Transmit Timing

For information on the TWI receive and transmit operations, see the *ADSP-214xx SHARC Hardware Reference Manual*.

JTAG Test Access Port and Emulation

Table 55. JTAG Test Access Port and Emulation

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{TCK}	TCK Period	20		20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		$4 \times t_{CK}$		ns
Switching Characteristics						
t_{DTDO}	TDO Delay from TCK Low		11.5		10.5	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = DATA15–0, CLK_CFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, DAI_Px, DPI_Px, FLAG3–0, MLBCLK, MLBDAT, MLBSIG, SR_SCLK, $\overline{\text{SR_CLR}}$, SR_SDI, and SR_LAT.

[2] System Outputs = DAI_Px, DPI_Px, ADDR23–0, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, FLAG3–0, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, SDCKE, SDA10, SDDQM, SDCLK, MLBDAT, MLBSIG, MLBDO, MLBSO, SR_SDO, SR_LDO, and $\overline{\text{EMU}}$.

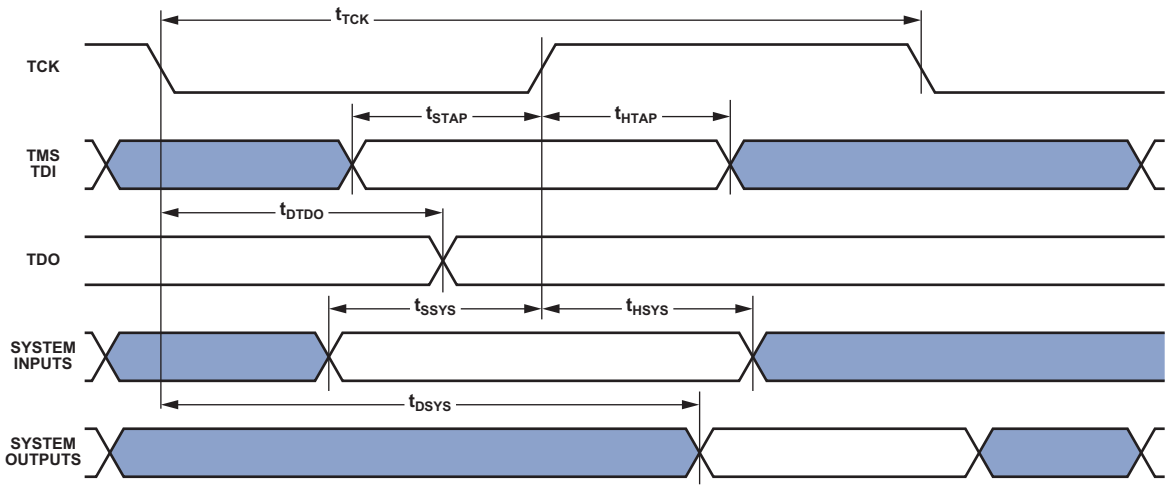

Figure 46. IEEE 1149.1 JTAG Test Access Port

Figure 53 shows the top view of the 88-lead LFCSP_VQ pin configuration. Figure 54 shows the bottom view.

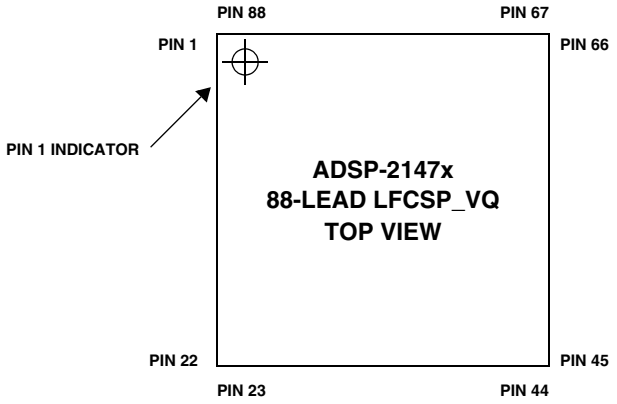

Figure 53. 88-Lead LFCSP_VQ Lead Configuration (Top View)

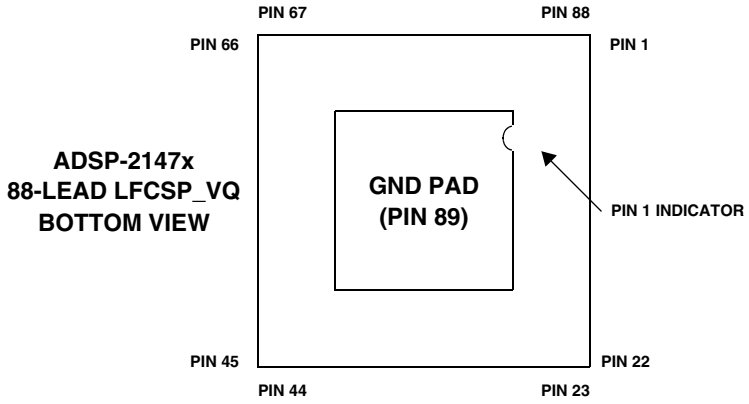

Figure 54. 88-Lead LFCSP_VQ Lead Configuration (Bottom View)

100-LQFP_EP LEAD ASSIGNMENT

Table 62 lists the 100-Lead LQFP_EP lead names.

Table 62. 100-Lead LQFP_EP Lead Assignments (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
V_{DD_INT}	1	V_{DD_EXT}	26	DAI_P10	51	V_{DD_INT}	76
CLK_CFG1	2	DPI_P08	27	V_{DD_INT}	52	FLAG0	77
BOOT_CFG0	3	DPI_P07	28	V_{DD_EXT}	53	V_{DD_INT}	78
V_{DD_EXT}	4	V_{DD_INT}	29	DAI_P20	54	V_{DD_INT}	79
V_{DD_INT}	5	DPI_P09	30	V_{DD_INT}	55	FLAG1	80
BOOT_CFG1	6	DPI_P10	31	DAI_P08	56	FLAG2	81
GND	7	DPI_P11	32	DAI_P04	57	FLAG3	82
NC	8	DPI_P12	33	DAI_P14	58	MLBCLK	83
NC	9	DPI_P13	34	DAI_P18	59	MLBDAT	84
CLK_CFG0	10	DAI_P03	35	DAI_P17	60	MLBDO	85
V_{DD_INT}	11	DPI_P14	36	DAI_P16	61	V_{DD_EXT}	86
CLKIN	12	V_{DD_INT}	37	DAI_P15	62	MLBSIG	87
XTAL	13	V_{DD_INT}	38	DAI_P12	63	V_{DD_INT}	88
V_{DD_EXT}	14	V_{DD_INT}	39	V_{DD_INT}	64	MLBSO	89
V_{DD_INT}	15	DAI_P13	40	DAI_P11	65	$\overline{TRST}$	90
V_{DD_INT}	16	DAI_P07	41	V_{DD_INT}	66	$\overline{EMU}$	91
$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	17	DAI_P19	42	V_{DD_INT}	67	TDO	92
V_{DD_INT}	18	DAI_P01	43	GND	68	V_{DD_EXT}	93
DPI_P01	19	DAI_P02	44	THD_M	69	V_{DD_INT}	94
DPI_P02	20	V_{DD_INT}	45	THD_P	70	TDI	95
DPI_P03	21	V_{DD_EXT}	46	V_{DD_THD}	71	TCK	96
V_{DD_INT}	22	V_{DD_INT}	47	V_{DD_INT}	72	V_{DD_INT}	97
DPI_P05	23	DAI_P06	48	V_{DD_INT}	73	$\overline{RESET}$	98
DPI_P04	24	DAI_P05	49	V_{DD_INT}	74	TMS	99
DPI_P06	25	DAI_P09	50	V_{DD_INT}	75	V_{DD_INT}	100
						GND	101*

* Lead no. 101 is the GND supply (see Figure 55 and Figure 56) for the processor; this pad must be **robustly** connected to GND.
MLB pins (pins 83, 84, 85, 87, and 89) are available for automotive models only. For non-automotive models, these pins should be connected to ground (GND).