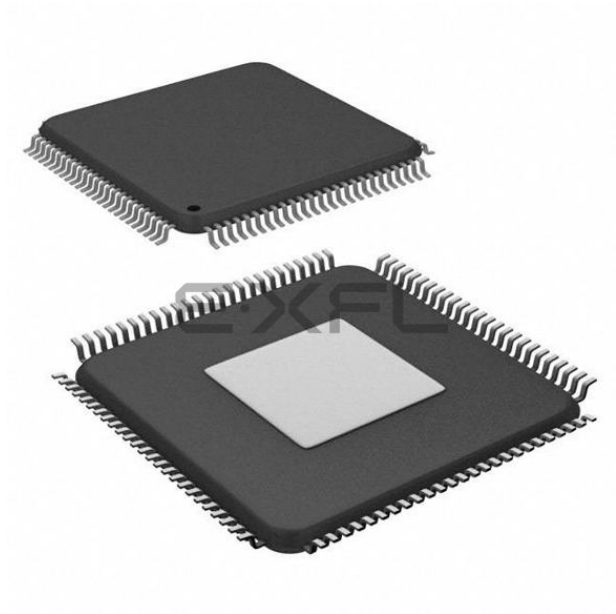

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI, EBI/EMI, I²C, SPI, SPORT, UART/USART
Clock Rate	266MHz
Non-Volatile Memory	ROM (4Mbit)
On-Chip RAM	3Mbit
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	100-LQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ad21478wyswz2a02

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REVISION HISTORY

4/2017—Rev. C to Rev. D

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PRODUCT APPLICATION RESTRICTION

Not for use in in-vivo applications for body fluid constituent monitoring, including monitoring one or more of the components that form, or may be a part of, or contaminate human blood or other body fluids, such as, but not limited to, carboxyhemoglobin, methemoglobin total hemoglobin, oxygen saturation, oxygen content, fractional arterial oxygen saturation, bilirubin, glucose, drugs, lipids, water, protein, and pH.

The block diagram of the ADSP-2147x on Page 1 also shows the peripheral clock domain (also known as the I/O processor), which contains the following features:

- IOD0 (peripheral DMA) and IOD1 (external port DMA) buses for 32-bit data transfers
- Peripheral and external port buses for core connection
- External port with an asynchronous memory interface (AMI) and SDRAM controller
- 4 units for pulse width modulation (PWM) control
- 1 memory-to-memory (MTM) unit for internal-to-internal memory transfers
- Digital applications interface that includes four precision clock generators (PCG), an input data port (IDP/PDAP) for serial and parallel interconnect, an S/PDIF receiver/transmitter, four asynchronous sample rate converters, eight serial ports, a shift register, and a flexible signal routing unit (DAI SRU).
- Digital peripheral interface that includes two timers, a 2-wire interface, one UART, two serial peripheral interfaces (SPI), two precision clock generators (PCG), three pulse width modulation (PWM) units, and a flexible signal routing unit (DPI SRU).

As shown in the SHARC core block diagram on Page 5, the processors use two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. With its SIMD computational hardware, the processors can perform 1.8 GFLOPS running at 300 MHz.

FAMILY CORE ARCHITECTURE

The processors are code compatible at the assembly level with the ADSP-2146x, ADSP-2137x, ADSP-2136x, ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-2147x share architectural features with the ADSP-2126x, ADSP-2136x, ADSP-2137x, ADSP-2146x, and ADSP-2116x SIMD SHARC processors, as shown in Figure 2 and detailed in the following sections.

SIMD Computational Engine

The processors contain two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. SIMD mode allows the processor to execute the same instruction in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

SIMD mode also affects the way data is transferred between memory and the processing elements because twice the data bandwidth is required to sustain computational operation in the processing elements. Therefore, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each memory or register file access.

SIMD mode is supported from external SDRAM but is not supported in the AMI.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Timer

The processor contains a core timer that can generate periodic software interrupts. The core timer can be configured to use FLAG3 as a timer expired signal.

Data Register File

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the processor's enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Context Switch

Many of the processor's registers have secondary registers that can be activated during interrupt servicing for a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result registers all have secondary registers. The primary registers are active at reset, while the secondary registers are activated by control bits in a mode control register.

Universal Registers

Universal registers can be used for general-purpose tasks. The USTAT (4) registers allow easy bit manipulations (Set, Clear, Toggle, Test, XOR) for all peripheral control and status registers.

The data bus exchange register (PX) permits data to be passed between the 64-bit PM data bus and the 64-bit DM data bus, or between the 40-bit register file and the PM/DM data bus. These registers contain hardware to handle the data width difference.

Single-Cycle Fetch of Instruction and Four Operands

The processors feature an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 2). With its separate program and data memory

Table 4. ADSP-21478 Internal Memory Space (3M bits)[1]

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 3FFF
Block 0 SRAM 0x0004 9000–0x0004 CFFF	Block 0 SRAM 0x0008 C000–0x0009 1554	Block 0 SRAM 0x0009 2000–0x0009 9FFF	Block 0 SRAM 0x0012 4000–0x0013 3FFF
Reserved 0x0004 D000–0x0004 FFFF	Reserved 0x0009 1555–0x0009 FFFF	Reserved 0x0009 A000–0x0009 FFFF	Reserved 0x0013 4000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 CFFF	Block 1 SRAM 0x000A C000–0x000B 1554	Block 1 SRAM 0x000B 2000–0x000B 9FFF	Block 1 SRAM 0x0016 4000–0x0017 3FFF
Reserved 0x0005 D000–0x0005 FFFF	Reserved 0x000B 1555–0x000B FFFF	Reserved 0x000B A000–0x000B FFFF	Reserved 0x0017 4000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 1FFF	Block 2 SRAM 0x000C 0000–0x000C 2AA9	Block 2 SRAM 0x000C 0000–0x000C 3FFF	Block 2 SRAM 0x0018 0000–0x0018 7FFF
Reserved 0x0006 2000– 0x0006 FFFF	Reserved 0x000C 2AAA–0x000D FFFF	Reserved 0x000C 4000–0x000D FFFF	Reserved 0x0018 8000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 1FFF	Block 3 SRAM 0x000E 0000–0x000E 2AA9	Block 3 SRAM 0x000E 0000–0x000E 3FFF	Block 3 SRAM 0x001C 0000–0x001C 7FFF
Reserved 0x0007 2000–0x0007 FFFF	Reserved 0x000E 2AAA–0x000F FFFF	Reserved 0x000E 4000–0x000F FFFF	Reserved 0x001C 8000–0x001F FFFF

[1] Some processors include a customer-definable ROM block. ROM addresses on these models are not reserved as shown in this table. Please contact your Analog Devices sales representative for additional details.

External Memory

The external memory interface supports access to the external memory through core and DMA accesses. The external memory address space is divided into four banks. Any bank can be programmed as either asynchronous or synchronous memory. The external ports are comprised of the following modules.

- An AMI which communicates with SRAM, FLASH, and other devices that meet the standard asynchronous SRAM access protocol. The AMI supports 6M words of external memory in Bank 0 and 8M words of external memory in Bank 1, Bank 2, and Bank 3.
- An SDRAM controller that supports a glueless interface with any of the standard SDRAMs. The SDC supports 62M words of external memory in Bank 0, and 64M words of external memory in Bank 1, Bank 2, and Bank 3.
- Arbitration logic to coordinate core and DMA transfers between internal and external memory over the external port.

External Port

The external port provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The external port, available on the 196-ball CSP_BGA, may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers. The first is an SDRAM controller for connection of industry-standard synchronous DRAM devices while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types. Non-SDRAM external memory address space is shown in Table 6.

Table 6. External Memory for Non-SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	6M	0x0020 0000–0x007F FFFF
Bank 1	8M	0x0400 0000–0x047F FFFF
Bank 2	8M	0x0800 0000–0x087F FFFF
Bank 3	8M	0x0C00 0000–0x0C7F FFFF

SIMD Access to External Memory

The SDRAM controller supports SIMD access on the 64-bit external port data bus (EPD) which allows access to the complementary registers on the PEy unit in the normal word space (NW). This improves performance since there is no need to explicitly load the complementary registers (as in SISD mode).

VISA and ISA Access to External Memory

The SDRAM controller supports VISA code operation which reduces the memory load since the VISA instructions are compressed. Moreover, bus fetching is reduced because, in the best case, one 48-bit fetch contains three valid instructions. Code execution from the traditional ISA operation is also supported. Note that code execution is only supported from Bank 0 regardless of VISA/ISA. Table 7 shows the address ranges for instruction fetch in each mode.

Table 7. External Bank 0 Instruction Fetch

Access Type	Size in Words	Address Range
ISA (NW)	4M	0x0020 0000–0x005F FFFF
VISA (SW)	10M	0x0060 0000–0x00FF FFFF

SDRAM Controller

The SDRAM controller, available on the ADSP-2147x in the 196-ball CSP_BGA package, provides an interface of up to four separate banks of industry-standard SDRAM devices or DIMMs, at speeds up to f_{SDCLK}. Fully compliant with the SDRAM standard, each bank has its own memory select line ($\overline{MS0}$–$\overline{MS3}$), and can be configured to contain between 4 Mbytes and 256 Mbytes of memory. SDRAM external memory address space is shown in Table 8.

Table 8. External Memory for SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000–0x03FF FFFF
Bank 1	64M	0x0400 0000–0x07FF FFFF
Bank 2	64M	0x0800 0000–0x0BFF FFFF
Bank 3	64M	0x0C00 0000–0x0FFF FFFF

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. The SDRAM and the AMI interface do not support 32-bit wide devices.

The SDRAM controller address, data, clock, and control pins can drive loads up to distributed 30 pF. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

Note that the external memory bank addresses shown are for normal-word (32-bit) accesses. If 48-bit instructions as well as 32-bit data are both placed in the same external memory bank, care must be taken while mapping them to avoid overlap.

Asynchronous Memory Controller

The asynchronous memory controller, available on the ADSP-2147x in the 196-ball CSP_BGA package, provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 6M word window and Banks 1, 2, and 3

Shift Register

The shift register can be used as a serial to parallel data converter. The shift register module consists of an 18-stage serial shift register, 18-bit latch, and three-state output buffers. The shift register and latch have separate clocks. Data is shifted into the serial shift register on the positive-going transitions of the shift register serial clock (SR_SCLK) input. The data in each flip-flop is transferred to the respective latch on a positive-going transition of the shift register latch clock (SR_LAT) input.

The shift register's signals can be configured as follows.

- The SR_SCLK can come from any of the SPORT0–7 SCLK outputs, PCGA/B clock, any of the DAI pins (1–8), and one dedicated pin (SR_SCLK).
- The SR_LAT can come from any of SPORT0–7 frame sync outputs, PCGA/B frame sync, any of the DAI pins (1–8), and one dedicated pin (SR_LAT).
- The SR_SDI input can from any of SPORT0–7 serial data outputs, any of the DAI pins (1–8), and one dedicated pin (SR_SDI).

Note that the SR_SCLK, SR_LAT, and SR_SDI inputs must come from same source except in the case of where SR_SCLK comes from PCGA/B or SR_SCLK and SR_LAT come from PCGA/B.

If SR_SCLK comes from PCGA/B, then SPORT0–7 generates the SR_LAT and SR_SDI signals. If SR_SCLK and SR_LAT come from PCGA/B, then SPORT0–7 generates the SR_SDI signal.

I/O PROCESSOR FEATURES

The I/O processor provides up to 65 channels of DMA as well as an extensive set of peripherals.

DMA Controller

The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the processor's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP) or the UART.

Up to 65 channels of DMA are available on the processors as shown in Table 9.

Programs can be downloaded using DMA transfers. Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

Table 9. DMA Channels

Peripheral	DMA Channels
SPORTs	16
PDAP	8
SPI	2
UART	2
External Port	2
Accelerators	2
Memory-to-Memory	2
MediaLB[1]	31

[1] Automotive models only.

Delay Line DMA

The processor provides delay line DMA functionality. This allows processor reads and writes to external delay line buffers (and therefore to external memory) with limited core interaction.

Scatter/Gather DMA

The processor provides scatter/gather DMA functionality. This allows processor DMA reads/writes to/from noncontiguous memory blocks.

FFT Accelerator

The FFT accelerator implements radix-2 complex/real input, complex output FFTs with no core intervention. The FFT accelerator runs at the peripheral clock frequency.

FIR Accelerator

The FIR (finite impulse response) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency.

IIR Accelerator

The IIR (infinite impulse response) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency.

Watchdog Timer (WDT)

The processors include a 32-bit watchdog timer that can be used to implement a software watchdog function. A software watchdog can improve system reliability by forcing the processor to a known state through generation of a system reset if the timer expires before being reloaded by software. Software initializes the count value of the timer, and then enables the timer.

The WDT is used to supervise the stability of the system software. When used in this way, software reloads the WDT in a regular manner so that the downward counting timer never expires. An expiring timer then indicates that system software might be out of control.

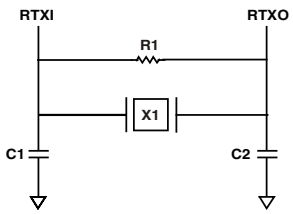
The WDT resets both the core and the internal peripherals. Software must be able to determine if the watch dog was the source of the hardware reset by interrogating a status bit in the watch dog timer control register.

The watch dog timer also has an internal RC oscillator that can be used as the clock source. The internal RC oscillator can be used as an optional alternative to using an external clock applied to the WDT_CLIN pin.

Real-Time Clock

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the SHARC processor. Connect RTC pins RTXI and RTXO with external components as shown in Figure 3.

The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time. An RTCLKOUT signal that operates at 1 Hz is also provided for calibration.



NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

Figure 3. External Components for RTC

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and a 32,768-day counter. When the alarm interrupt is enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: The first alarm is for a time of day. The second alarm is for a day and time of that day.

The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch interrupt is enabled and the counter underflows, an interrupt is generated.

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory boots at system power-up from an 8-bit EPROM via the external port, an SPI master, or an SPI slave. Booting is determined by the boot configuration (BOOT_CFG2–0) pins in Table 10.

Table 10. Boot Mode Selection

BOOT_CFG2–0[1]	Booting Mode
000	SPI Slave Boot
001	SPI Master Boot (from Flash and Other Slaves)
010	AMI User Boot (for 8-bit Flash Boot)
011	No Boot (Processor Executes from Internal ROM After Reset)
100	Reserved
1xx	Reserved

[1] The BOOT_CFG2 pin is not available on the 100-lead or 88-lead packages.

A running reset feature is used to reset the processor core and peripherals without resetting the PLL and SDRAM controller, or performing a boot. The functionality of the $\overline{\text{RESETOUT}}$ /$\overline{\text{RUNRSTIN}}$ pin has now been extended to also act as the input for initiating a running reset. For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*.

Power Supplies

The processors have separate power supply connections for the internal (V_{DD_INT}) and external (V_{DD_EXT}) power supplies. The internal and analog supplies must meet the V_{DD_INT} specifications. The external supply must meet the V_{DD_EXT} specification. All external supply pins must be connected to the same power supply.

To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DD_INT} and GND.

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the processors to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate emulator hardware user's guide.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2147x architecture and functionality. For detailed information on the family core architecture and instruction set, refer to the *SHARC Processor Programming Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Reference Designs page provides a link to Circuits from the Lab™ (www.analog.com/signal chains) which contains:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	200 MHz Min	200 MHz Max	266 MHz Min	266 MHz Max	300 MHz Min	300 MHz Max	Unit
V_{OH}[2]	High Level Output Voltage	@ V_{DD_EXT} = Min, I_{OH} = –1.0 mA[3]	2.4		2.4		2.4		V
V_{OL}[2]	Low Level Output Voltage	@ V_{DD_EXT} = Min, I_{OL} = 1.0 mA[3]		0.4		0.4		0.4	V
I_{IH}[4, 5]	High Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max		10		10		10	µA
I_{IL}[4]	Low Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = 0 V		–10		–10		–10	µA
I_{ILPU}[5]	Low Level Input Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V		200		200		200	µA
I_{OZH}[6, 7]	Three-State Leakage Current	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max		10		10		10	µA
I_{OZL}[6]	Three-State Leakage Current	@ V_{DD_EXT} = Max, V_{IN} = 0 V		–10		–10		–10	µA
I_{OZLPU}[7]	Three-State Leakage Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V		200		200		200	µA
I_{OZHPD}[8]	Three-State Leakage Current Pull-down	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max		200		200		200	µA
I_{DD_RTC}	V_{DD_RTC} Current	@ V_{DD_RTC} = 3.0, T_J = 25°C		0.76		0.76		0.76	µA
I_{DD_INT}[9]	Supply Current (Internal)	f_{CCLK} > 0 MHz		Table 14 + Table 15 × ASF		Table 14 + Table 15 × ASF		Table 14 + Table 15 × ASF	mA
C_{IN}[10, 11]	Input Capacitance	T_{CASE} = 25°C		5		5		5	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: ADDR23-0, DATA15-0, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, FLAG3–0, DAI_Px, DPI_Px, $\overline{\text{EMU}}$, TDO, $\overline{\text{RESETOUT}}$,MLBSIG, MLBDAT, MLBDO, MLBSO, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, SDCKE, SDA10, SDDQM, MS0-1.
[3] See Output Drive Currents for typical drive current capabilities.
[4] Applies to input pins: BOOT_CFGx, CLK_CFGx, TCK, $\overline{\text{RESET}}$, CLKIN.
[5] Applies to input pins with internal pull-ups: $\overline{\text{TRST}}$, TMS, TDI.
[6] Applies to three-statable pins: TDO, MLBDAT, MLBSIG, MLBDO, and MLBSO.
[7] Applies to three-statable pins with pull-ups: DAI_Px, DPI_Px, $\overline{\text{EMU}}$.
[8] Applies to three-statable pin with pull-down: SDCLK.
[9] See Engineer-to-Engineer Note “Estimating Power Dissipation for ADSP-214xx SHARC Processors” for further information.
[10] Applies to all signal pins.
[11] Guaranteed, but not tested.

Timer WDTH_CAP Timing

The following timing specification applies to timer0 and timer1, and in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the timing specification provided below is valid at the DPI_P14–1 pins.

Table 26. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

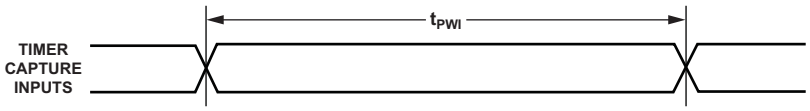


Figure 14. Timer Width Capture Timing

Watchdog Timer Timing

Table 27. Watchdog Timer Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{WDTCLKPER}$		100	1000	ns
Switching Characteristics				
t_{RST}	WDT Clock Rising Edge to Watchdog Timer $\overline{\text{RESET}}$ Falling Edge	3	7.6	ns
t_{RSTPW}	Reset Pulse Width	$64 \times t_{WDTCLKPER}$[1]		ns

[1] When the internal oscillator is used, the $1/t_{WDTCLKPER}$ varies from 1.5 MHz to 2.5 MHz and the WDT_CLKIN pin should be pulled low.

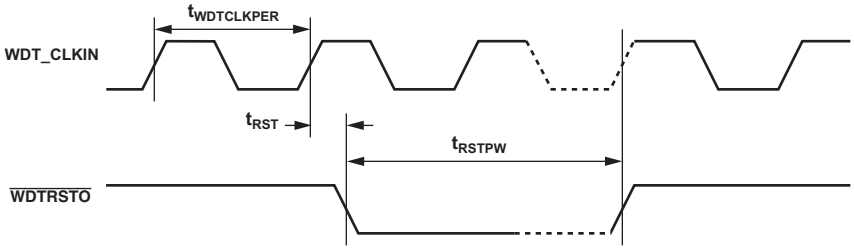


Figure 15. Watchdog Timer Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 28. DAI/DPI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid	1.5	10	ns

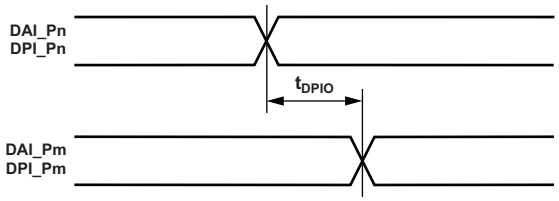


Figure 16. DAI Pin to Pin Direct Routing

AMI Read

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 32. AMI Read

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}[1, 2, 3]	Address Selects Delay to Data Valid		W + t_{SDCLK} – 6.32	ns
t_{DRLD}[1, 3]	$\overline{\text{AMI\_RD}}$ Low to Data Valid		W – 3	ns
t_{SDS}[4, 5]	Data Setup to $\overline{\text{AMI\_RD}}$ High	2.6		ns
t_{HDRH}	Data Hold from $\overline{\text{AMI\_RD}}$ High	0.4		ns
t_{DAAK}[2, 6]	AMI_ACK Delay from Address Selects		t_{SDCLK} – 10 + W	ns
t_{DSAK}[4]	AMI_ACK Delay from $\overline{\text{AMI\_RD}}$ Low		W – 7.0	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{\text{AMI\_RD}}$ High	RHC + 0.38		ns
t_{DARL}[2]	Address Selects to $\overline{\text{AMI\_RD}}$ Low	t_{SDCLK} – 5		ns
t_{RW}	$\overline{\text{AMI\_RD}}$ Pulse Width	W – 1.4		ns
t_{RWR}	$\overline{\text{AMI\_RD}}$ High to $\overline{\text{AMI\_RD}}$ Low	HI + t_{SDCLK} – 1.2		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
RHC = (number of Read Hold Cycles specified in AMICTLx register) × t_{SDCLK}
Where PREDIS = 0
HI = RHC (if IC = 0): Read to Read from same bank
HI = RHC+ t_{SDCLK} (if IC > 0): Read to Read from same bank
HI = RHC + IC: Read to Read from different bank
HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank
Where PREDIS = 1
HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank
HI = RHC + (3 × t_{SDCLK}): Read to Read from same bank
HI = RHC + Max (IC, (3 × t_{SDCLK})): Read to Read from different bank
IC = (number of idle cycles specified in AMICTLx register) × t_{SDCLK}
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}.

[1] Data delay/setup: System must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{\text{AMI_MS}}$x, is referenced.
[3] The maximum limit of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.
[4] Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.
[5] Data hold: User must meet t_{HDRH} in asynchronous access mode. See Test Conditions for the calculation of hold times given capacitive and dc loads.
[6] AMI_ACK delay/setup: User must meet t_{daak}, or t_{dsak}, for deassertion of AMI_ACK (low).

Table 35. Serial Ports—Internal Clock

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	13		10.5		ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5		2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	13		10.5		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		2.5		ns
Switching Characteristics						
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		5		5	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1.0		–1.0		ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		10.7		10.7	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1.0		–1.0		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		4		4	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0		–1.0		ns
t_{SCKLIW}	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

The SPORTx_TDV_O output signal (routing unit) becomes active in SPORT multichannel/packed mode. During transmit slots (enabled with active channel selection registers), the SPORTx_TDV_O is asserted for communication with external devices.

Table 38. Serial Ports—TDV (Transmit Data Valid)

Parameter		88-Lead LFCSP Package		All Other Packages		Unit
		Min	Max	Min	Max	
Switching Characteristics[1]						
t_{DRDVEN}	TDV Assertion Delay from Drive Edge of External Clock	3		3		ns
t_{DFDVEN}	TDV Deassertion Delay from Drive Edge of External Clock		$2 \times t_{PCLK}$		13.25	ns
t_{DRDVIN}	TDV Assertion Delay from Drive Edge of Internal Clock	–0.1		–0.1		ns
t_{DFDVIN}	TDV Deassertion Delay from Drive Edge of Internal Clock		3.5		3.5	ns

[1] Referenced to drive edge.

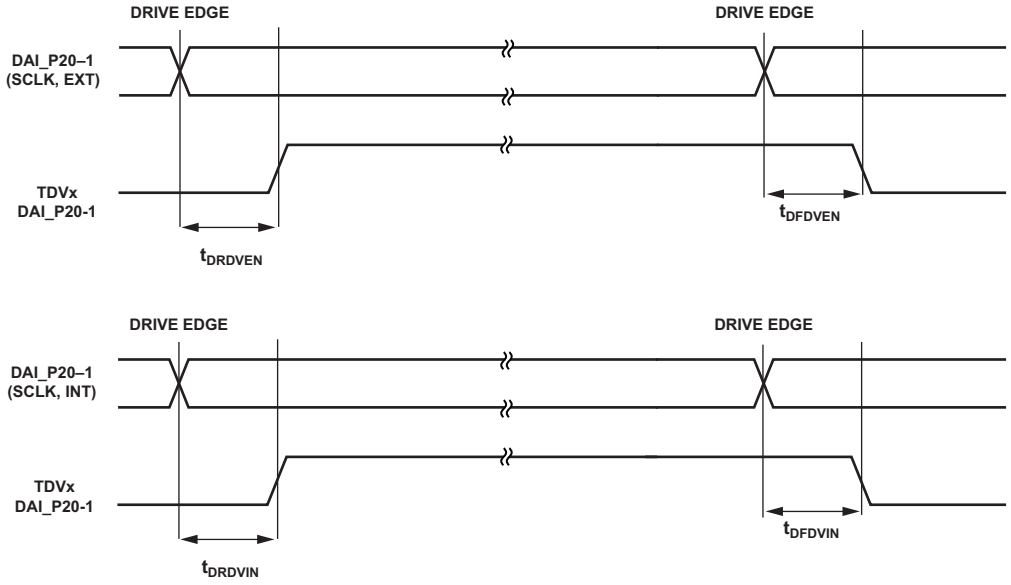


Figure 25. Serial Ports—TDV Internal and External Clock

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 39. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 39. Input Data Port (IDP)

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4.5		3.8		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		2.5		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	4		2.5		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

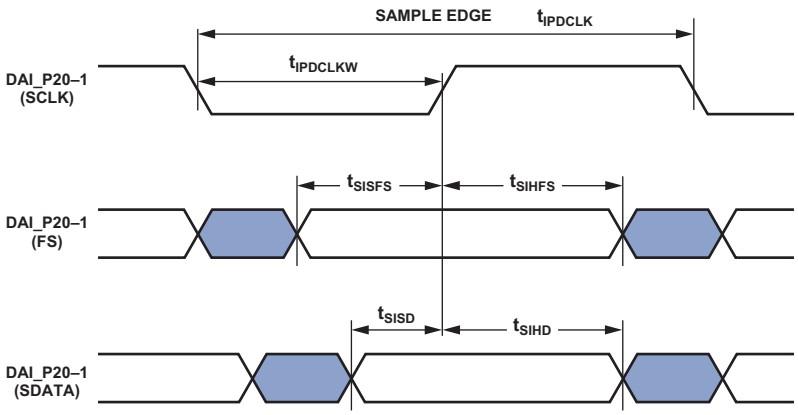


Figure 26. IDP Master Timing

Sample Rate Converter—Serial Input Port

The ASRC input signals are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 41 are valid at the DAI_P20–1 pins.

Table 41. ASRC, Serial Input Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
t_{SRCSD}[1]	Data Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHD}[1]	Data Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{SRCCLK}	Clock Period	$t_{PCLK} \times 4$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

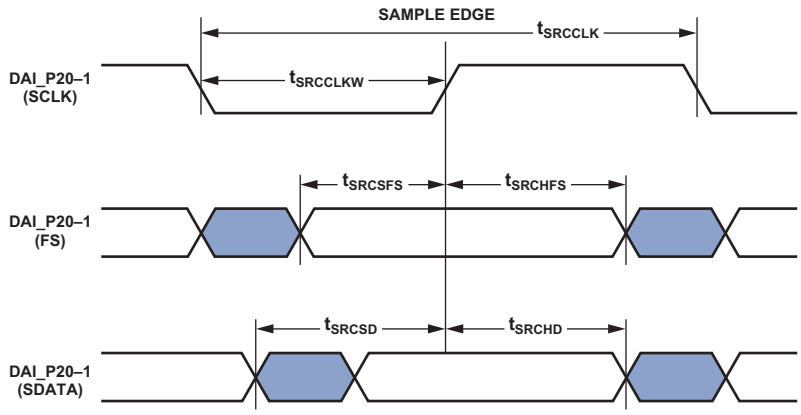


Figure 28. ASRC Serial Input Port Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the *ADSP-214xx SHARC Hardware Reference Manual*.

2-Wire Interface (TWI)—Receive and Transmit Timing

For information on the TWI receive and transmit operations, see the *ADSP-214xx SHARC Hardware Reference Manual*.

JTAG Test Access Port and Emulation

Table 55. JTAG Test Access Port and Emulation

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{TCK}	TCK Period	20		20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		$4 \times t_{CK}$		ns
Switching Characteristics						
t_{DTDO}	TDO Delay from TCK Low		11.5		10.5	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = DATA15–0, CLK_CFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, DAI_Px, DPI_Px, FLAG3–0, MLBCLK, MLBDAT, MLBSIG, SR_SCLK, $\overline{\text{SR_CLR}}$, SR_SDI, and SR_LAT.

[2] System Outputs = DAI_Px, DPI_Px, ADDR23–0, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, FLAG3–0, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, SDCKE, SDA10, SDDQM, SDCLK, MLBDAT, MLBSIG, MLBDO, MLBSO, SR_SDO, SR_LDO, and $\overline{\text{EMU}}$.

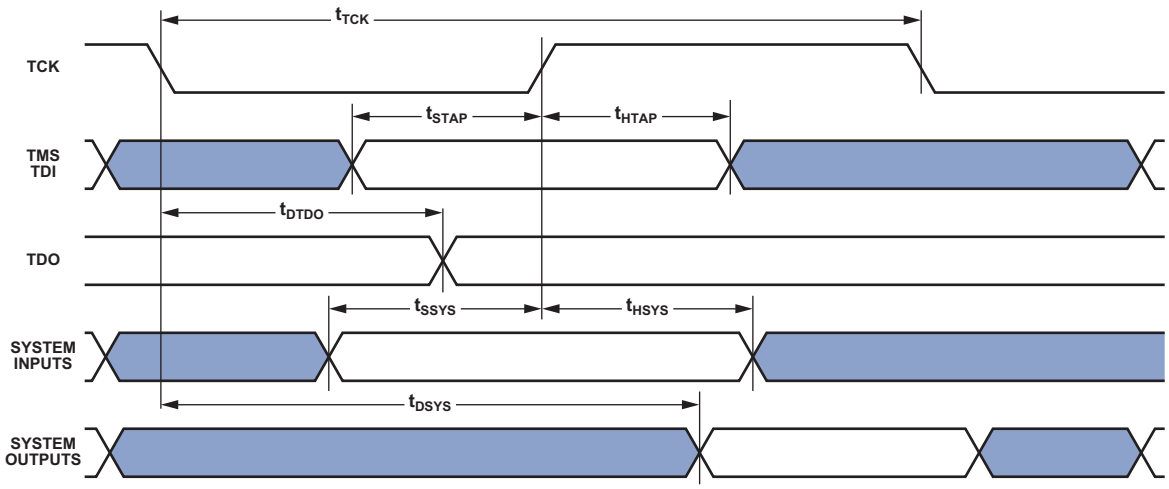


Figure 46. IEEE 1149.1 JTAG Test Access Port

Thermal Diode

The processors incorporate thermal diode/s to monitor the die temperature. The thermal diode is a grounded collector, PNP bipolar junction transistor (BJT). The THD_P pin is connected to the emitter, and the THD_M pin is connected to the base of the transistor. These pins can be used by an external temperature sensor (such as ADM1021A or LM86 or others) to read the die temperature of the chip.

The technique used by the external temperature sensor is to measure the change in VBE when the thermal diode is operated at two different currents. This is shown in the following equation:

$$\Delta V_{BE} = n \times \frac{kT}{q} \times ln(N)$$

where:

n = multiplication factor close to 1, depending on process variations

k = Boltzmann constant

T = temperature (°C)

q = charge of the electron

N = ratio of the two currents

The two currents are usually in the range of 10 µA to 300 µA for the common temperature sensor chips available.

Table 60 contains the thermal diode specifications using the transistor model.

Table 60. Thermal Diode Parameters—Transistor Model[1]

Symbol	Parameter	Min	Typ	Max	Unit
I_{FW}[2]	Forward Bias Current	10		300	µA
I_E	Emitter Current	10		300	µA
n_Q[3, 4]	Transistor Ideality	1.012	1.015	1.017	
R_T[3, 5]	Series Resistance	0.12	0.2	0.28	Ω

[1] Analog Devices does not recommend operation of the thermal diode under reverse bias.
[2] Analog Devices does not recommend operation of the thermal diode under reverse bias.
[3] Specified by design characterization.
[4] The ideality factor, nQ, represents the deviation from ideal diode behavior as exemplified by the diode equation: $I_C = I_S \times (e^{qVBE/nqkT} - 1)$ where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the diode, k = Boltzmann constant, and T = absolute temperature (Kelvin).
[5] The series resistance (R_T) can be used for more accurate readings as needed.

100-LQFP_EP LEAD ASSIGNMENT

Table 62 lists the 100-Lead LQFP_EP lead names.

Table 62. 100-Lead LQFP_EP Lead Assignments (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
V_{DD_INT}	1	V_{DD_EXT}	26	DAI_P10	51	V_{DD_INT}	76
CLK_CFG1	2	DPI_P08	27	V_{DD_INT}	52	FLAG0	77
BOOT_CFG0	3	DPI_P07	28	V_{DD_EXT}	53	V_{DD_INT}	78
V_{DD_EXT}	4	V_{DD_INT}	29	DAI_P20	54	V_{DD_INT}	79
V_{DD_INT}	5	DPI_P09	30	V_{DD_INT}	55	FLAG1	80
BOOT_CFG1	6	DPI_P10	31	DAI_P08	56	FLAG2	81
GND	7	DPI_P11	32	DAI_P04	57	FLAG3	82
NC	8	DPI_P12	33	DAI_P14	58	MLBCLK	83
NC	9	DPI_P13	34	DAI_P18	59	MLBDAT	84
CLK_CFG0	10	DAI_P03	35	DAI_P17	60	MLBDO	85
V_{DD_INT}	11	DPI_P14	36	DAI_P16	61	V_{DD_EXT}	86
CLKIN	12	V_{DD_INT}	37	DAI_P15	62	MLBSIG	87
XTAL	13	V_{DD_INT}	38	DAI_P12	63	V_{DD_INT}	88
V_{DD_EXT}	14	V_{DD_INT}	39	V_{DD_INT}	64	MLBSO	89
V_{DD_INT}	15	DAI_P13	40	DAI_P11	65	$\overline{TRST}$	90
V_{DD_INT}	16	DAI_P07	41	V_{DD_INT}	66	$\overline{EMU}$	91
$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	17	DAI_P19	42	V_{DD_INT}	67	TDO	92
V_{DD_INT}	18	DAI_P01	43	GND	68	V_{DD_EXT}	93
DPI_P01	19	DAI_P02	44	THD_M	69	V_{DD_INT}	94
DPI_P02	20	V_{DD_INT}	45	THD_P	70	TDI	95
DPI_P03	21	V_{DD_EXT}	46	V_{DD_THD}	71	TCK	96
V_{DD_INT}	22	V_{DD_INT}	47	V_{DD_INT}	72	V_{DD_INT}	97
DPI_P05	23	DAI_P06	48	V_{DD_INT}	73	$\overline{RESET}$	98
DPI_P04	24	DAI_P05	49	V_{DD_INT}	74	TMS	99
DPI_P06	25	DAI_P09	50	V_{DD_INT}	75	V_{DD_INT}	100
						GND	101*

* Lead no. 101 is the GND supply (see Figure 55 and Figure 56) for the processor; this pad must be **robustly** connected to GND.
MLB pins (pins 83, 84, 85, 87, and 89) are available for automotive models only. For non-automotive models, these pins should be connected to ground (GND).

196-BGA BALL ASSIGNMENT

Table 63. 196-Ball CSP_BGA Ball Assignment (Numerical by Ball No.)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	GND	D1	ADDR6	G1	XTAL	K1	DPI_P02	N1	DPI_P14
A2	SDCKE	D2	ADDR4	G2	SDA10	K2	DPI_P04	N2	SR_LDO1
A3	SDDQM	D3	ADDR1	G3	ADDR11	K3	DPI_P05	N3	SR_LDO4
A4	$\overline{\text{SDRAS}}$	D4	CLK_CFG0	G4	GND	K4	DPI_P09	N4	SR_LDO8
A5	$\overline{\text{SDWE}}$	D5	V_{DD_EXT}	G5	V_{DD_INT}	K5	V_{DD_INT}	N5	SR_LDO10
A6	DATA12	D6	V_{DD_EXT}	G6	GND	K6	GND	N6	DAI_P01
A7	DATA13	D7	V_{DD_EXT}	G7	GND	K7	GND	N7	SR_LDO9
A8	DATA10	D8	V_{DD_EXT}	G8	GND	K8	GND	N8	DAI_P02
A9	DATA9	D9	V_{DD_EXT}	G9	GND	K9	GND	N9	SR_LDO13
A10	DATA7	D10	V_{DD_EXT}	G10	V_{DD_INT}	K10	V_{DD_INT}	N10	SR_SCLK
A11	DATA3	D11	V_{DD_EXT}	G11	V_{DD_EXT}	K11	GND	N11	DAI_P09
A12	DATA1	D12	ADDR14	G12	ADDR21	K12	DAI_P16	N12	SR_SDI
A13	DATA2	D13	ADDR20	G13	ADDR19	K13	DAI_P18	N13	SR_LDO17
A14	GND	D14	WDT_CLKO	G14	RTXO	K14	DAI_P15	N14	DAI_P14
B1	ADDR0	E1	ADDR8	H1	ADDR13	L1	DAI_P03	P1	GND
B2	CLK_CFG1	E2	ADDR7	H2	ADDR12	L2	DPI_P10	P2	SR_LDO3
B3	BOOT_CFG0	E3	ADDR5	H3	ADDR10	L3	DPI_P08	P3	SR_LDO2
B4	TMS	E4	V_{DD_EXT}	H4	ADDR17	L4	DPI_P06	P4	SR_LDO6
B5	$\overline{\text{RESET}}$	E5	V_{DD_INT}	H5	V_{DD_INT}	L5	V_{DD_INT}	P5	$\overline{\text{WDTRSTO}}$
B6	DATA14	E6	V_{DD_INT}	H6	GND	L6	V_{DD_INT}	P6	DAI_P19
B7	DATA11	E7	V_{DD_INT}	H7	GND	L7	V_{DD_INT}	P7	DAI_P13
B8	DATA4	E8	V_{DD_INT}	H8	GND	L8	V_{DD_INT}	P8	SR_LDO11
B9	DATA8	E9	V_{DD_INT}	H9	GND	L9	V_{DD_INT}	P9	SR_LDO15
B10	DATA6	E10	V_{DD_INT}	H10	V_{DD_INT}	L10	V_{DD_INT}	P10	$\overline{\text{SR\_CLR}}$
B11	DATA5	E11	V_{DD_EXT}	H11	V_{DD_EXT}	L11	DAI_P10	P11	SR_LAT
B12	$\overline{\text{TRST}}$	E12	$\overline{\text{AMI\_RD}}$	H12	BOOT_CFG2	L12	DAI_P20	P12	SR_LDO14
B13	FLAG1	E13	ADDR22	H13	ADDR23	L13	DAI_P17	P13	SR_LDO12
B14	DATA0	E14	FLAG2	H14	RTXI	L14	DAI_P04	P14	GND
C1	ADDR2	F1	CLKIN	J1	DPI_P01	M1	DPI_P13		
C2	ADDR3	F2	ADDR9	J2	DPI_P03	M2	DPI_P12		
C3	RTCLKOUT	F3	BOOT_CFG1	J3	ADDR18	M3	SR_LDO0		
C4	$\overline{\text{MS0}}$	F4	NC	J4	$\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$	M4	DPI_P07		
C5	$\overline{\text{SDCAS}}$	F5	NC	J5	V_{DD_INT}	M5	DPI_P11		
C6	DATA15	F6	GND	J6	GND	M6	SR_LDO5		
C7	TCK	F7	GND	J7	GND	M7	SR_LDO7		
C8	TDI	F8	GND	J8	GND	M8	DAI_P07		
C9	SDCLK	F9	GND	J9	GND	M9	SR_LDO16		
C10	$\overline{\text{EMU}}$	F10	V_{DD_INT}	J10	V_{SS_RTC}	M10	SR_SDO		
C11	TDO	F11	V_{DD_EXT}	J11	V_{DD_RTC}	M11	DAI_P06		
C12	FLAG3	F12	ADDR15	J12	DAI_P11	M12	DAI_P05		
C13	ADDR16	F13	FLAG0	J13	AMI_ACK	M13	DAI_P08		
C14	WDT_CLKIN	F14	$\overline{\text{AMI\_WR}}$	J14	$\overline{\text{MS1}}$	M14	DAI_P12		

ORDERING GUIDE

Model[1]	Temperature Range[2]	On-Chip SRAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21477KCPZ-1A	0°C to +70°C	2M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21477KSWZ-1A	0°C to +70°C	2M Bits	200 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21477BCPZ-1A	–40°C to +85°C	2M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21478KCPZ-1A	0°C to +70°C	3M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21478BCPZ-1A	–40°C to +85°C	3M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21478BBCZ-2A	–40°C to +85°C	3M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478BSWZ-2A	–40°C to +85°C	3M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21478KBCZ-1A	0°C to +70°C	3M Bits	200 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478KBCZ-2A	0°C to +70°C	3M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478KBCZ-3A	0°C to +70°C	3M Bits	300 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478KSWZ-1A	0°C to +70°C	3M Bits	200 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21478KSWZ-2A	0°C to +70°C	3M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21479KCPZ-1A	0°C to +70°C	5M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21479BCPZ-1A	–40°C to +85°C	5M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21479BBCZ-2A	–40°C to +85°C	5M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479BSWZ-2A	–40°C to +85°C	5M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21479KBCZ-1A	0°C to +70°C	5M Bits	200 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479KBCZ-2A	0°C to +70°C	5M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479KBCZ-3A	0°C to +70°C	5M Bits	300 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479KSWZ-1A	0°C to +70°C	5M Bits	200 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21479KSWZ-2A	0°C to +70°C	5M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2

[1] Z =RoHS compliant part.
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions for junction temperature (T_J) specification, which is the only temperature specification.