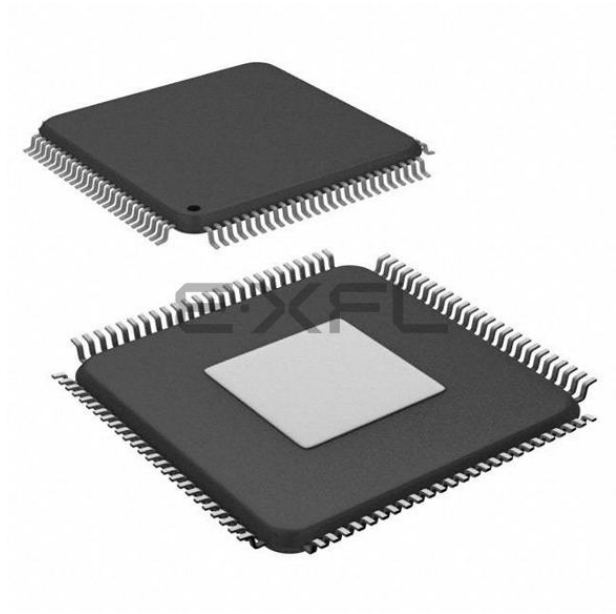

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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Active |
| Type | Floating Point |
| Interface | DAI, DPI, EBI/EMI, I²C, SPI, SPORT, UART/USART |
| Clock Rate | 266MHz |
| Non-Volatile Memory | ROM (4Mbit) |
| On-Chip RAM | 3Mbit |
| Voltage - I/O | 3.30V |
| Voltage - Core | 1.20V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP Exposed Pad |
| Supplier Device Package | 100-LQFP-EP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/ad21478wyswz2b02 |

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## REVISION HISTORY

**4/2017—Rev. C to Rev. D**

Change to RTXI Description in Table 11 of Pin Function Descriptions ..... 16
Changes to Operating Conditions ..... 21
Change to Figure 5 of Core Clock Requirements ..... 25
Changes to AMI Read ..... 37
Change to $t_{WDE}$ Switching Characteristic in AMI Write ..... 39
Change to Table 64 of Automotive Products ..... 75

## PRODUCT APPLICATION RESTRICTION

**Not for use in in-vivo applications for body fluid constituent monitoring, including monitoring one or more of the components that form, or may be a part of, or contaminate human blood or other body fluids, such as, but not limited to, carboxyhemoglobin, methemoglobin total hemoglobin, oxygen saturation, oxygen content, fractional arterial oxygen saturation, bilirubin, glucose, drugs, lipids, water, protein, and pH.**

### *Shift Register*

The shift register can be used as a serial to parallel data converter. The shift register module consists of an 18-stage serial shift register, 18-bit latch, and three-state output buffers. The shift register and latch have separate clocks. Data is shifted into the serial shift register on the positive-going transitions of the shift register serial clock (SR_SCLK) input. The data in each flip-flop is transferred to the respective latch on a positive-going transition of the shift register latch clock (SR_LAT) input.

The shift register's signals can be configured as follows.

- The SR_SCLK can come from any of the SPORT0–7 SCLK outputs, PCGA/B clock, any of the DAI pins (1–8), and one dedicated pin (SR_SCLK).
- The SR_LAT can come from any of SPORT0–7 frame sync outputs, PCGA/B frame sync, any of the DAI pins (1–8), and one dedicated pin (SR_LAT).
- The SR_SDI input can from any of SPORT0–7 serial data outputs, any of the DAI pins (1–8), and one dedicated pin (SR_SDI).

Note that the SR_SCLK, SR_LAT, and SR_SDI inputs must come from same source except in the case of where SR_SCLK comes from PCGA/B or SR_SCLK and SR_LAT come from PCGA/B.

If SR_SCLK comes from PCGA/B, then SPORT0–7 generates the SR_LAT and SR_SDI signals. If SR_SCLK and SR_LAT come from PCGA/B, then SPORT0–7 generates the SR_SDI signal.

## I/O PROCESSOR FEATURES

The I/O processor provides up to 65 channels of DMA as well as an extensive set of peripherals.

### *DMA Controller*

The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the processor's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP) or the UART.

Up to 65 channels of DMA are available on the processors as shown in Table 9.

Programs can be downloaded using DMA transfers. Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

**Table 9. DMA Channels**

| Peripheral | DMA Channels |
|---|---|
| SPORTs | 16 |
| PDAP | 8 |
| SPI | 2 |
| UART | 2 |
| External Port | 2 |
| Accelerators | 2 |
| Memory-to-Memory | 2 |
| MediaLB[1] | 31 |

[1] Automotive models only.

#### Delay Line DMA

The processor provides delay line DMA functionality. This allows processor reads and writes to external delay line buffers (and therefore to external memory) with limited core interaction.

#### Scatter/Gather DMA

The processor provides scatter/gather DMA functionality. This allows processor DMA reads/writes to/from noncontiguous memory blocks.

### *FFT Accelerator*

The FFT accelerator implements radix-2 complex/real input, complex output FFTs with no core intervention. The FFT accelerator runs at the peripheral clock frequency.

### *FIR Accelerator*

The FIR (finite impulse response) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency.

### *IIR Accelerator*

The IIR (infinite impulse response) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency.

### *Watchdog Timer (WDT)*

The processors include a 32-bit watchdog timer that can be used to implement a software watchdog function. A software watchdog can improve system reliability by forcing the processor to a known state through generation of a system reset if the timer expires before being reloaded by software. Software initializes the count value of the timer, and then enables the timer.

The WDT is used to supervise the stability of the system software. When used in this way, software reloads the WDT in a regular manner so that the downward counting timer never expires. An expiring timer then indicates that system software might be out of control.

The WDT resets both the core and the internal peripherals. Software must be able to determine if the watch dog was the source of the hardware reset by interrogating a status bit in the watch dog timer control register.

## ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2147x architecture and functionality. For detailed information on the family core architecture and instruction set, refer to the *SHARC Processor Programming Reference*.

## RELATED SIGNAL CHAINS

A *signal chain* is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Reference Designs page provides a link to Circuits from the Lab™ (www.analog.com/signal chains) which contains:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

**Table 11. Pin Descriptions (Continued)**

| Name | Type | State During/ After Reset | Description |
|---|---|---|---|
| TDI | I (ipu) | | **Test Data Input (JTAG).** Provides serial data for the boundary scan logic. |
| TDO | O/T | High-Z | **Test Data Output (JTAG).** Serial scan output of the boundary scan path. |
| TMS | I (ipu) | | **Test Mode Select (JTAG).** Used to control the test state machine. |
| TCK | I | | **Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the device. |
| $\overline{\text{TRST}}$ | I (ipu) | | **Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor. |
| $\overline{\text{EMU}}$ | O (O/D, ipu) | High-Z | **Emulation Status.** Must be connected to the Analog Devices DSP Tools product line of JTAG emulators target board connector only. |
| $\text{CLK\_CFG}_{1-0}$ | I | | **Core to CLKIN Ratio Control.** These pins set the startup clock frequency. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset. The allowed values are:<br>00 = 8:1<br>01 = 32:1<br>10 = 16:1<br>11 = reserved |
| CLKIN | I | | **Local Clock In.** Used in conjunction with XTAL. CLKIN is the clock input. It configures the processors to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processors to use the external clock source such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency. |
| XTAL | O | | **Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal. |
| $\overline{\text{RESET}}$ | I | | **Processor Reset.** Resets the processor to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up. |
| $\overline{\text{RESETOUT}}/\overline{\text{RUNRSTIN}}$ | I/O (ipu) | | **Reset Out/Running Reset In.** The default setting on this pin is reset out. This pin also has a second function as RUNRSTIN which is enabled by setting bit 0 of the RUNRSTCTL register. For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*. |
| $\text{BOOT\_CFG}_{2-0}$ | I | | **Boot Configuration Select.** These pins select the boot mode for the processor. The BOOT_CFG pins must be valid before $\overline{\text{RESET}}$ (hardware and software) is de-asserted.<br>The BOOT_CFG2 pin is only available on the 196-lead package. |

The following symbols appear in the Type column of Table 11: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be 26 kΩ to 63 kΩ. The range of an ipd resistor can be 31 kΩ to 85 kΩ. The three-state voltage of ipu pads will not reach to full the $V_{DD\_EXT}$ level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.

Not all pins are available in the 88-lead LFCSP_VQ and 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 62 on Page 70.

### *Timer WDTH_CAP Timing*

The following timing specification applies to timer0 and timer1, and in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the timing specification provided below is valid at the DPI_P14–1 pins.

**Table 26. Timer Width Capture Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirement* | | | | |
| $t_{PWI}$ | Timer Pulse Width | $2 \times t_{PCLK}$ | $2 \times (2^{31} - 1) \times t_{PCLK}$ | ns |

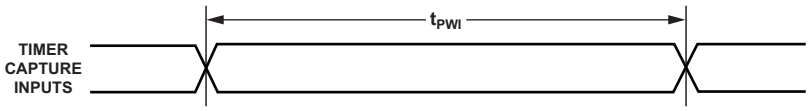


*Figure 14. Timer Width Capture Timing*

### *Watchdog Timer Timing*

**Table 27. Watchdog Timer Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirement* | | | | |
| $t_{WDTCLKPER}$ | | 100 | 1000 | ns |
| *Switching Characteristics* | | | | |
| $t_{RST}$ | WDT Clock Rising Edge to Watchdog Timer $\overline{\text{RESET}}$ Falling Edge | 3 | 7.6 | ns |
| $t_{RSTPW}$ | Reset Pulse Width | $64 \times t_{WDTCLKPER}$[1] | | ns |

[1] When the internal oscillator is used, the $1/t_{WDTCLKPER}$ varies from 1.5 MHz to 2.5 MHz and the WDT_CLKIN pin should be pulled low.

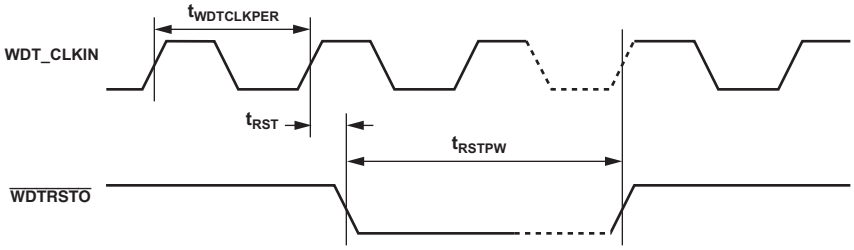


*Figure 15. Watchdog Timer Timing*

### *SDRAM Interface Timing*

**Table 31. SDRAM Interface Timing**

| Parameter | | 133 MHz Min | 133 MHz Max | 150 MHz Min | 150 MHz Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{SSDAT}$ | DATA Setup Before SDCLK | 0.7 | | 0.7 | | ns |
| $t_{HSDAT}$ | DATA Hold After SDCLK | 1.66 | | 1.5 | | ns |
| *Switching Characteristics* | | | | | | |
| $t_{SDCLK}$[1] | SDCLK Period | 7.5 | | 6.66 | | ns |
| $t_{SDCLKH}$ | SDCLK Width High | 2.5 | | 2.2 | | ns |
| $t_{SDCLKL}$ | SDCLK Width Low | 2.5 | | 2.2 | | ns |
| $t_{DCAD}$[2] | Command, ADDR, Data Delay After SDCLK | | 5 | | 4.75 | ns |
| $t_{HCAD}$[2] | Command, ADDR, Data Hold After SDCLK | 1 | | 1 | | ns |
| $t_{DSDAT}$ | Data Disable After SDCLK | | 6.2 | | 5.3 | ns |
| $t_{ENSDAT}$ | Data Enable After SDCLK | 0.3 | | 0.3 | | ns |

[1] Systems should use the SDRAM model with a speed grade higher than the desired SDRAM controller speed. For example, to run the SDRAM controller at 133 MHz the SDRAM model with a speed grade of 143 MHz or above should be used. See Engineer-to-Engineer Note "Interfacing SDRAM memory to SHARC processors (EE-286)" for more information on hardware design guidelines for the SDRAM interface.
[2] Command pins include: $\overline{SDCAS}$, $\overline{SDRAS}$, $\overline{SDWE}$, $\overline{MSx}$, SDA10, SDQM, SDCKE.

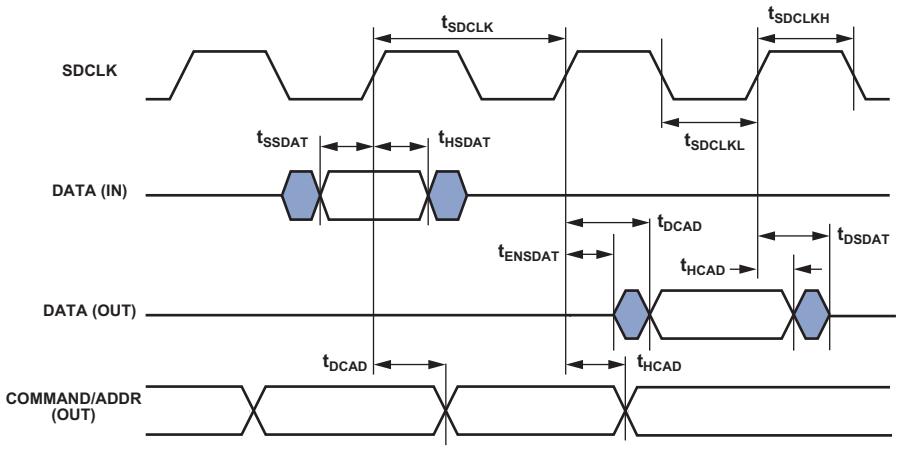


*Figure 19. SDRAM Interface Timing*

### *AMI Read*

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

**Table 32. AMI Read**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{DAD}$[1, 2, 3] | Address Selects Delay to Data Valid | | W + $t_{SDCLK}$ – 6.32 | ns |
| $t_{DRLD}$[1, 3] | $\overline{\text{AMI\_RD}}$ Low to Data Valid | | W – 3 | ns |
| $t_{SDS}$[4, 5] | Data Setup to $\overline{\text{AMI\_RD}}$ High | 2.6 | | ns |
| $t_{HDRH}$ | Data Hold from $\overline{\text{AMI\_RD}}$ High | 0.4 | | ns |
| $t_{DAAK}$[2, 6] | AMI_ACK Delay from Address Selects | | $t_{SDCLK}$ – 10 + W | ns |
| $t_{DSAK}$[4] | AMI_ACK Delay from $\overline{\text{AMI\_RD}}$ Low | | W – 7.0 | ns |
| *Switching Characteristics* | | | | |
| $t_{DRHA}$ | Address Selects Hold After $\overline{\text{AMI\_RD}}$ High | RHC + 0.38 | | ns |
| $t_{DARL}$[2] | Address Selects to $\overline{\text{AMI\_RD}}$ Low | $t_{SDCLK}$ – 5 | | ns |
| $t_{RW}$ | $\overline{\text{AMI\_RD}}$ Pulse Width | W – 1.4 | | ns |
| $t_{RWR}$ | $\overline{\text{AMI\_RD}}$ High to $\overline{\text{AMI\_RD}}$ Low | HI + $t_{SDCLK}$ – 1.2 | | ns |

W = (number of wait states specified in AMICTLx register) × $t_{SDCLK}$.
RHC = (number of Read Hold Cycles specified in AMICTLx register) × $t_{SDCLK}$
Where PREDIS = 0
HI = RHC (if IC = 0): Read to Read from same bank
HI = RHC+ $t_{SDCLK}$ (if IC > 0): Read to Read from same bank
HI = RHC + IC: Read to Read from different bank
HI = RHC + Max (IC, (4 × $t_{SDCLK}$)): Read to Write from same or different bank
Where PREDIS = 1
HI = RHC + Max (IC, (4 × $t_{SDCLK}$)): Read to Write from same or different bank
HI = RHC + (3 × $t_{SDCLK}$): Read to Read from same bank
HI = RHC + Max (IC, (3 × $t_{SDCLK}$)): Read to Read from different bank
IC = (number of idle cycles specified in AMICTLx register) × $t_{SDCLK}$
H = (number of hold cycles specified in AMICTLx register) × $t_{SDCLK}$.

[1] Data delay/setup: System must meet $t_{DAD}$, $t_{DRLD}$, or $t_{SDS}$.
[2] The falling edge of $\overline{\text{AMI_MS}}$x, is referenced.
[3] The maximum limit of timing requirement values for $t_{DAD}$ and $t_{DRLD}$ parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.
[4] Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.
[5] Data hold: User must meet $t_{HDRH}$ in asynchronous access mode. See Test Conditions for the calculation of hold times given capacitive and dc loads.
[6] AMI_ACK delay/setup: User must meet $t_{daak}$, or $t_{dsak}$, for deassertion of AMI_ACK (low).

**Table 35. Serial Ports—Internal Clock**

| Parameter | | 88-Lead LFCSP Package Min | 88-Lead LFCSP Package Max | All Other Packages Min | All Other Packages Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{SFSI}$[1] | Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode) | 13 | | 10.5 | | ns |
| $t_{HFSI}$[1] | Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode) | 2.5 | | 2.5 | | ns |
| $t_{SDRI}$[1] | Receive Data Setup Before SCLK | 13 | | 10.5 | | ns |
| $t_{HDRI}$[1] | Receive Data Hold After SCLK | 2.5 | | 2.5 | | ns |
| *Switching Characteristics* | | | | | | |
| $t_{DFSI}$[2] | Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode) | | 5 | | 5 | ns |
| $t_{HOFSI}$[2] | Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode) | –1.0 | | –1.0 | | ns |
| $t_{DFSIR}$[2] | Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode) | | 10.7 | | 10.7 | ns |
| $t_{HOFSIR}$[2] | Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode) | –1.0 | | –1.0 | | ns |
| $t_{DDTI}$[2] | Transmit Data Delay After SCLK | | 4 | | 4 | ns |
| $t_{HDTI}$[2] | Transmit Data Hold After SCLK | –1.0 | | –1.0 | | ns |
| $t_{SCKLIW}$ | Transmit or Receive SCLK Width | $2 \times t_{PCLK} - 1.5$ | $2 \times t_{PCLK} + 1.5$ | $2 \times t_{PCLK} - 1.5$ | $2 \times t_{PCLK} + 1.5$ | ns |

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

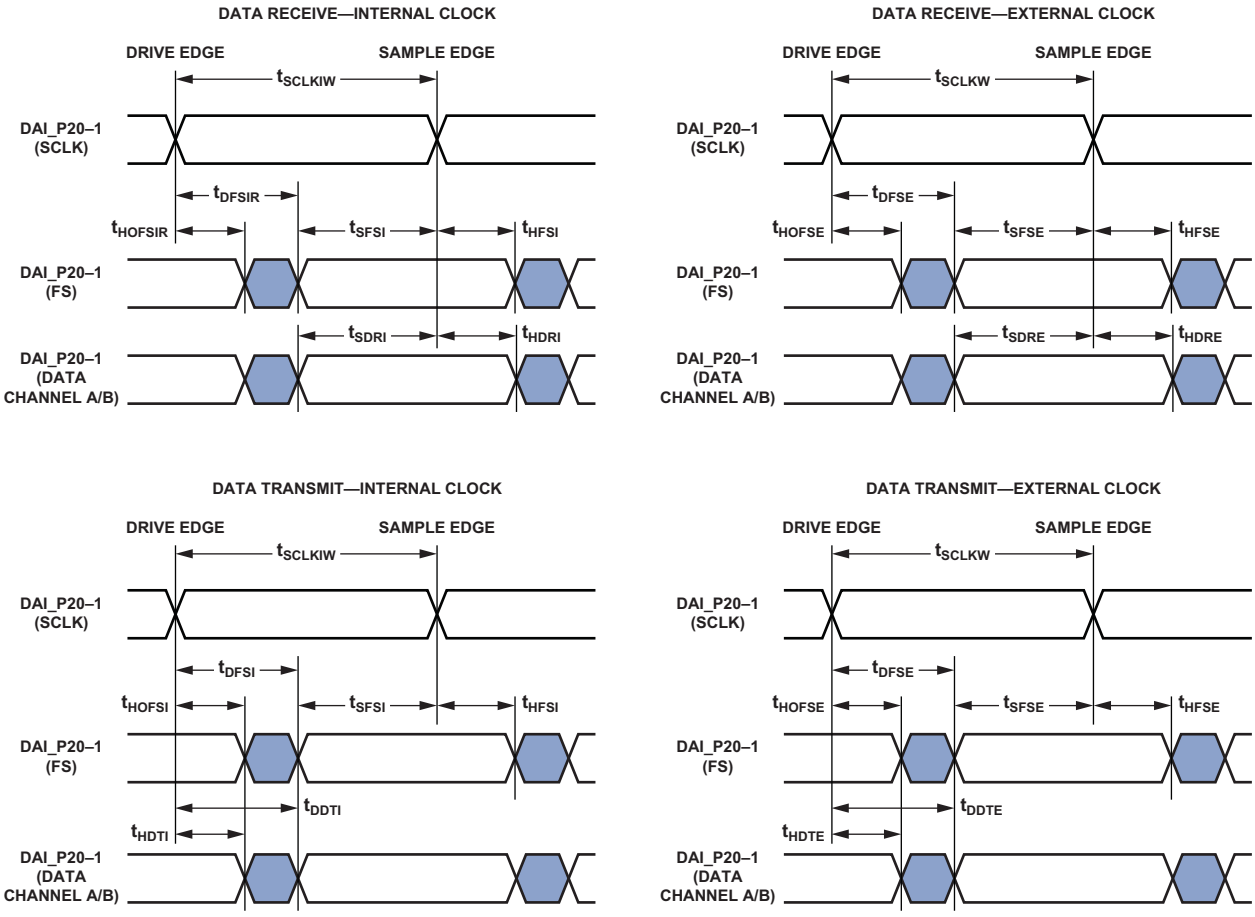


*Figure 22. Serial Ports*

### *Parallel Data Acquisition Port (PDAP)*

The timing requirements for the PDAP are provided in Table 40. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the *ADSP-214xx SHARC Processor Hardware Reference*. Note that the 20 bits of external PDAP data can be provided through the ADDR23–0 pins or over the DAI pins.

**Table 40. Parallel Data Acquisition Port (PDAP)**

| Parameter | | 88-Lead LFCSP Package Min | 88-Lead LFCSP Package Max | All Other Packages Min | All Other Packages Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{SPHOLD}$[1] | PDAP_HOLD Setup Before PDAP_CLK Sample Edge | 4 | | 2.5 | | ns |
| $t_{HPHOLD}$[1] | PDAP_HOLD Hold After PDAP_CLK Sample Edge | 4 | | 2.5 | | ns |
| $t_{PDSD}$[1] | PDAP_DAT Setup Before SCLK PDAP_CLK Sample Edge | 5 | | 3.85 | | ns |
| $t_{PDHD}$[1] | PDAP_DAT Hold After SCLK PDAP_CLK Sample Edge | 4 | | 2.5 | | ns |
| $t_{PDCLKW}$ | Clock Width | $(t_{PCLK} \times 4) \div 2 - 3$ | | $(t_{PCLK} \times 4) \div 2 - 3$ | | ns |
| $t_{PDCLK}$ | Clock Period | $t_{PCLK} \times 4$ | | $t_{PCLK} \times 4$ | | ns |
| *Switching Characteristics* | | | | | | |
| $t_{PDHLDD}$ | Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word | $2 \times t_{PCLK} + 3$ | | $2 \times t_{PCLK} + 3$ | | ns |
| $t_{PDSTRB}$ | PDAP Strobe Pulse Width | $2 \times t_{PCLK} - 1.5$ | | $2 \times t_{PCLK} - 1.5$ | | ns |

[1] Source pins of DATA and control are ADDR23–0 or DAI pins. Source pins for SCLK and FS are: 1) DAI pins, 2) CLKIN through PCG, or 3) DAI pins through PCG.

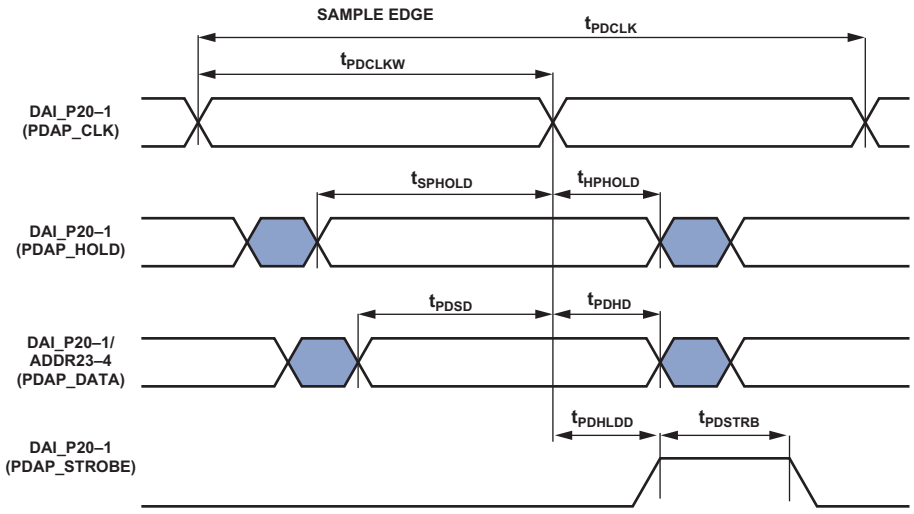


*Figure 27. PDAP Timing*

### *Sample Rate Converter—Serial Input Port*

The ASRC input signals are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 41 are valid at the DAI_P20–1 pins.

**Table 41. ASRC, Serial Input Port**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SRCSFS}$[1] | Frame Sync Setup Before Serial Clock Rising Edge | 4 | | ns |
| $t_{SRCHFS}$[1] | Frame Sync Hold After Serial Clock Rising Edge | 5.5 | | ns |
| $t_{SRCSD}$[1] | Data Setup Before Serial Clock Rising Edge | 4 | | ns |
| $t_{SRCHD}$[1] | Data Hold After Serial Clock Rising Edge | 5.5 | | ns |
| $t_{SRCCLKW}$ | Clock Width | $(t_{PCLK} \times 4) \div 2 - 1$ | | ns |
| $t_{SRCCLK}$ | Clock Period | $t_{PCLK} \times 4$ | | ns |

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

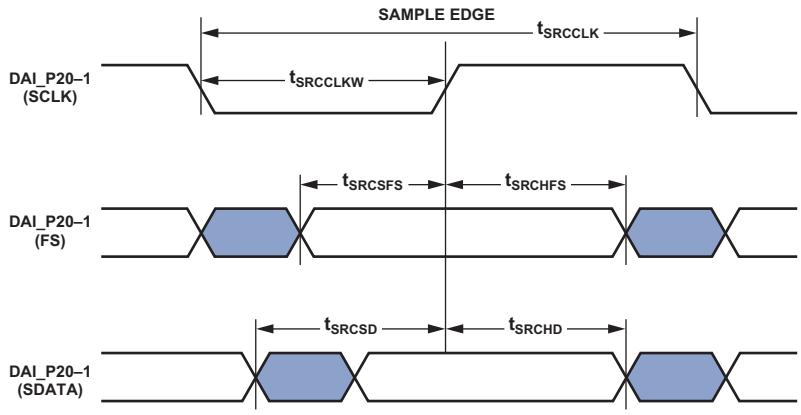


*Figure 28. ASRC Serial Input Port Timing*

### S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 47. Input signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

**Table 47. S/PDIF Transmitter Input Data Timing**

| Parameter | | 88-Lead LFCSP Package Min | 88-Lead LFCSP Package Max | All Other Packages Min | All Other Packages Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{SISFS}$[1] | Frame Sync Setup Before Serial Clock Rising Edge | 4.5 | | 3 | | ns |
| $t_{SIHFS}$[1] | Frame Sync Hold After Serial Clock Rising Edge | 3 | | 3 | | ns |
| $t_{SISD}$[1] | Data Setup Before Serial Clock Rising Edge | 4.5 | | 3 | | ns |
| $t_{SIHD}$[1] | Data Hold After Serial Clock Rising Edge | 3 | | 3 | | ns |
| $t_{SITXCLKW}$ | Transmit Clock Width | 9 | | 9 | | ns |
| $t_{SITXCLK}$ | Transmit Clock Period | 20 | | 20 | | ns |
| $t_{SISCLKW}$ | Clock Width | 36 | | 36 | | ns |
| $t_{SISCLK}$ | Clock Period | 80 | | 80 | | ns |

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

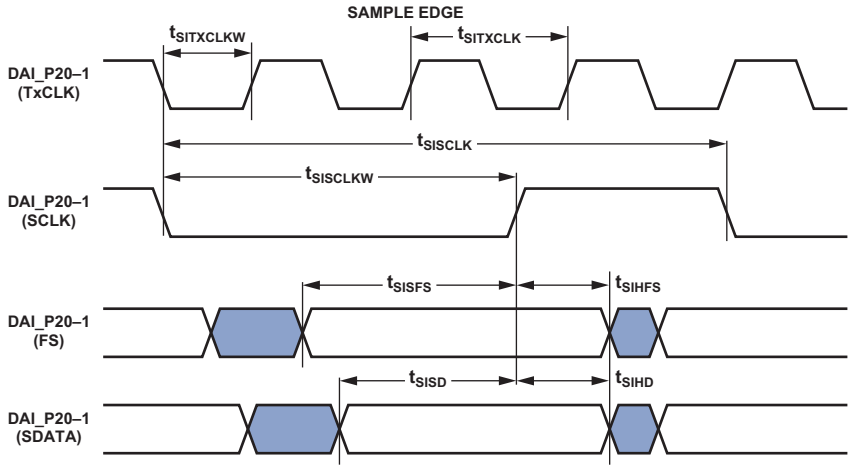


*Figure 34. S/PDIF Transmitter Input Timing*

### Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

**Table 48. Oversampling Clock (TxCLK) Switching Characteristics**

| Parameter | Max | Unit |
|---|---|---|
| Frequency for TxCLK = 384 × Frame Sync | Oversampling Ratio × Frame Sync ≤ $1/t_{SITXCLK}$ | MHz |
| Frequency for TxCLK = 256 × Frame Sync | 49.2 | MHz |
| Frame Rate (FS) | 192.0 | kHz |

### *SPI Interface—Slave*

**Table 51. SPI Interface Protocol—Slave Switching and Timing Specifications**

| Parameter | | 88-Lead LFCSP Package Min | 88-Lead LFCSP Package Max | All Other Packages Min | All Other Packages Max | Unit |
|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | |
| $t_{SPICLKS}$ | Serial Clock Cycle | $4 \times t_{PCLK} - 2$ | | $4 \times t_{PCLK} - 2$ | | ns |
| $t_{SPICHS}$ | Serial Clock High Period | $2 \times t_{PCLK} - 2$ | | $2 \times t_{PCLK} - 2$ | | ns |
| $t_{SPICLS}$ | Serial Clock Low Period | $2 \times t_{PCLK} - 2$ | | $2 \times t_{PCLK} - 2$ | | ns |
| $t_{SDSCO}$ | $\overline{SPIDS}$ Assertion to First SPICLK Edge, CPHASE = 0 or CPHASE = 1 | $2 \times t_{PCLK}$ | | $2 \times t_{PCLK}$ | | ns |
| $t_{HDS}$ | Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0 | $2 \times t_{PCLK}$ | | $2 \times t_{PCLK}$ | | ns |
| $t_{SSPIDS}$ | Data Input Valid to SPICLK Edge (Data Input Setup Time) | 2 | | 2 | | ns |
| $t_{HSPIDS}$ | SPICLK Last Sampling Edge to Data Input Not Valid | 2 | | 2 | | ns |
| $t_{SDPPW}$ | $\overline{SPIDS}$ Deassertion Pulse Width (CPHASE = 0) | $2 \times t_{PCLK}$ | | $2 \times t_{PCLK}$ | | ns |
| *Switching Characteristics* | | | | | | |
| $t_{DSOE}$ | $\overline{SPIDS}$ Assertion to Data Out Active | 0 | 13 | 0 | 10.25 | ns |
| $t_{DSOE}$[1] | $\overline{SPIDS}$ Assertion to Data Out Active (SPI2) | 0 | 13 | 0 | 10.25 | ns |
| $t_{DSDHI}$ | $\overline{SPIDS}$ Deassertion to Data High Impedance | 0 | $2 \times t_{PCLK}$ | 0 | 13.25 | ns |
| $t_{DSDHI}$[1] | $\overline{SPIDS}$ Deassertion to Data High Impedance (SPI2) | 0 | $2 \times t_{PCLK}$ | 0 | 13.25 | ns |
| $t_{DDSPIDS}$ | SPICLK Edge to Data Out Valid (Data Out Delay Time) | | 13 | | 11.5 | ns |
| $t_{HDSPIDS}$ | SPICLK Edge to Data Out Not Valid (Data Out Hold Time) | $2 \times t_{PCLK}$ | | $2 \times t_{PCLK}$ | | ns |
| $t_{DSOV}$ | $\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0) | | $5 \times t_{PCLK}$ | | $5 \times t_{PCLK}$ | ns |

[1] The timing for these parameters applies when the SPI is routed through the signal routing unit. For more information, see the processor hardware reference, "Serial Peripheral Interface Port (SPI)" chapter.

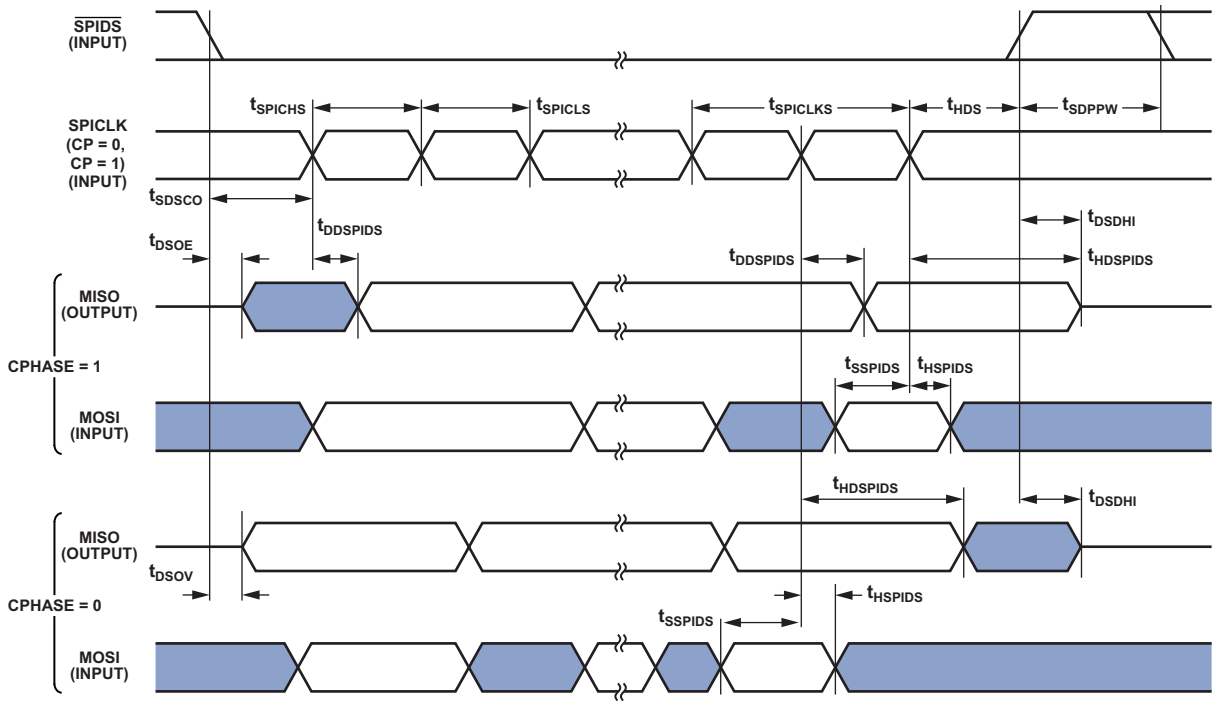


*Figure 37. SPI Slave Timing*

### *Shift Register*

**Table 54. Shift Register**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SSDI}$ | SR_SDI Setup Before SR_SCLK Rising Edge | 7 | | ns |
| $t_{HSDI}$ | SR_SDI Hold After SR_SCLK Rising Edge | 2 | | ns |
| $t_{SSDIDAI}$[1] | DAI_P08–01 (SR_SDI) Setup Before DAI_P08–01 (SR_SCLK) Rising Edge | 7 | | ns |
| $t_{HSDIDAI}$[1] | DAI_P08–01 (SR_SDI) Hold After DAI_P08–01 (SR_SCLK) Rising Edge | 2 | | ns |
| $t_{SSCK2LCK}$[2] | SR_SCLK to SR_LAT Setup | 2 | | ns |
| $t_{SSCK2LCKDAI}$[1, 2] | DAI_P08–01 (SR_SCLK) to DAI_P08–01 (SR_LAT) Setup | 2 | | ns |
| $t_{CLRREM2SCK}$ | Removal Time $\overline{SR\_CLR}$ to SR_SCLK | $3 \times t_{PCLK} - 5$ | | ns |
| $t_{CLRREM2LCK}$ | Removal Time $\overline{SR\_CLR}$ to SR_LAT | $2 \times t_{PCLK} - 5$ | | ns |
| $t_{CLRW}$ | $\overline{SR\_CLR}$ Pulse Width | $4 \times t_{PCLK} - 5$ | | ns |
| $t_{SCKW}$ | SR_SCLK Clock Pulse Width | $2 \times t_{PCLK} - 2$ | | ns |
| $t_{LCKW}$ | SR_LAT Clock Pulse Width | $2 \times t_{PCLK} - 5$ | | ns |
| $f_{MAX}$ | Maximum Clock Frequency SR_SCLK or SR_LAT | | $f_{PCLK} \div 4$ | MHz |
| *Switching Characteristics* | | | | ns |
| $t_{DSDO1}$[3] | SR_SDO Hold After SR_SCLK Rising Edge | 3 | | ns |
| $t_{DSDO2}$[3] | SR_SDO Max. Delay After SR_SCLK Rising Edge | | 13 | ns |
| $t_{DSDODAI1}$[1, 3] | SR_SDO Hold After DAI_P08–01 (SR_SCLK) Rising Edge | 3 | | ns |
| $t_{DSDODAI2}$[1, 3] | SR_SDO Max. Delay After DAI_P08–01 (SR_SCLK) Rising Edge | | 13 | ns |
| $t_{DSDOSP1}$[3, 4] | SR_SDO Hold After DAI_P20–01 (SR_SCLK) Rising Edge | –2 | | ns |
| $t_{DSDOSP2}$[3, 4] | SR_SDO Max. Delay After DAI_P20–01 (SR_SCLK) Rising Edge | | 5 | ns |
| $t_{DSDOPCG1}$[3, 5, 6] | SR_SDO Hold After DAI_P20–01 (SR_SCLK) Rising Edge | –2 | | ns |
| $t_{DSDOPCG2}$[3, 5, 6] | SR_SDO Max. Delay After DAI_P20–01 (SR_SCLK) Rising Edge | | 5 | ns |
| $t_{DSDOCLR1}$[3] | $\overline{SR\_CLR}$ to SR_SDO Min. Delay | 4 | | ns |
| $t_{DSDOCLR2}$[3] | $\overline{SR\_CLR}$ to SR_SDO Max. Delay | | 13 | ns |
| $t_{DLDO1}$[3] | SR_LDO Hold After SR_LAT Rising Edge | 3 | | ns |
| $t_{DLDO2}$[3] | SR_LDO Max. Delay After SR_LAT Rising Edge | | 13 | ns |
| $t_{DLDODAI1}$[3] | SR_LDO Hold After DAI_P08–01 (SR_LAT) Rising Edge | 3 | | ns |
| $t_{DLDODAI2}$[3] | SR_LDO Max. Delay After DAI_P08–01 (SR_LAT) Rising Edge | | 13 | ns |
| $t_{DLDOSP1}$[3, 4] | SR_LDO Hold After DAI_P20–01 (SR_LAT) Rising Edge | –2 | | ns |
| $t_{DLDOSP2}$[3, 4] | SR_LDO Max. Delay After DAI_P20–01 (SR_LAT) Rising Edge | | 5 | ns |
| $t_{DLDOPCG1}$[3, 5, 6] | SR_LDO Hold After DAI_P20–01 (SR_LAT) Rising Edge | –2 | | ns |
| $t_{DLDOPCG2}$[3, 5, 6] | SR_LDO Max. Delay After DAI_P20–01 (SR_LAT) Rising Edge | | 5 | ns |
| $t_{DLDOCLR1}$[3] | $\overline{SR\_CLR}$ to SR_LDO Min. Delay | 4 | | ns |
| $t_{DLDOCLR2}$[3] | $\overline{SR\_CLR}$ to SR_LDO Max. Delay | | 14 | ns |

[1] Any of the DAI_P08–01 pins can be routed to the shift register clock, latch clock and serial data input via the SRU.
[2] Both clocks can be connected to the same clock source. If both clocks are connected to same clock source, then data in the 18-stage shift register is always one cycle ahead of latch register data.
[3] For setup/hold timing requirements of off-chip shift register interfacing devices.
[4] SPORTx serial clock out, frame sync out, and serial data outputs are routed to shift register block internally and are also routed onto DAI_P20–01.
[5] PCG serial clock output is routed to SPORT and shift register block internally and are also routed onto DAI_P20–01. The SPORTs generate SR_LAT and SDI internally.
[6] PCG Serial clock and frame sync outputs are routed to SPORT and shift register block internally and are also routed onto DAI_P20–01. The SPORTs generate SDI internally.

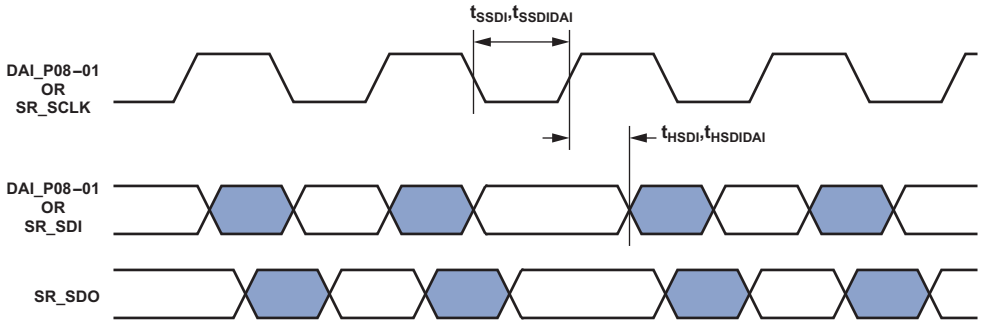


*Figure 41. SR_SDI Setup, Hold*

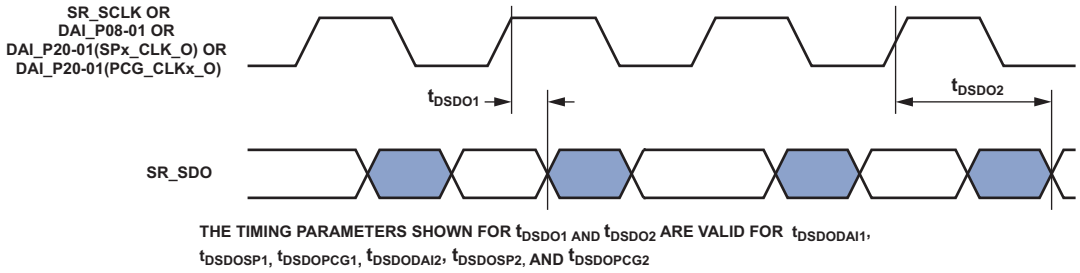


*Figure 42. SR_ SDO Delay*

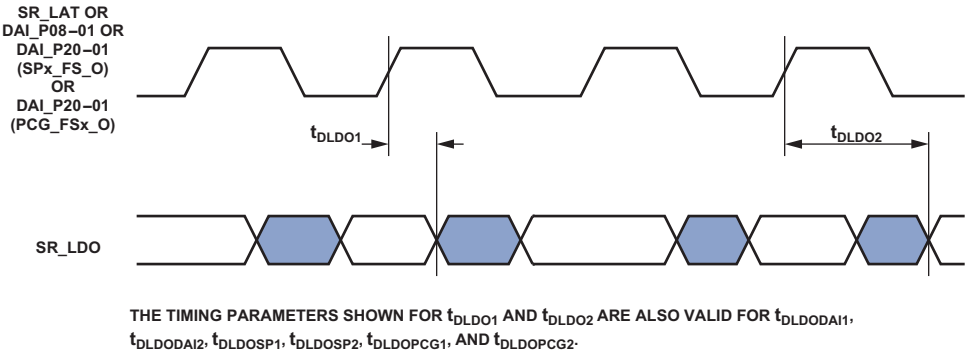


*Figure 43. SR_LDO Delay*

# 88-LFCSP_VQ LEAD ASSIGNMENT

Table 61 lists the 88-Lead LFCSP_VQ package lead names.

**Table 61. 88-Lead LFCSP_VQ Lead Assignments (Numerical by Lead Number)**

| Lead Name | Lead No. | Lead Name | Lead No. | Lead Name | Lead No. | Lead Name | Lead No. |
|---|---|---|---|---|---|---|---|
| CLK_CFG1 | 1 | $V_{DD\_EXT}$ | 23 | DAI_P10 | 45 | $V_{DD\_INT}$ | 67 |
| BOOT_CFG0 | 2 | DPI_P08 | 24 | $V_{DD\_INT}$ | 46 | FLAG0 | 68 |
| $V_{DD\_EXT}$ | 3 | DPI_P07 | 25 | $V_{DD\_EXT}$ | 47 | $V_{DD\_INT}$ | 69 |
| $V_{DD\_INT}$ | 4 | DPI_P09 | 26 | DAI_P20 | 48 | FLAG1 | 70 |
| BOOT_CFG1 | 5 | DPI_P10 | 27 | $V_{DD\_INT}$ | 49 | FLAG2 | 71 |
| GND | 6 | DPI_P11 | 28 | DAI_P08 | 50 | FLAG3 | 72 |
| CLK_CFG0 | 7 | DPI_P12 | 29 | DAI_P04 | 51 | GND | 73 |
| $V_{DD\_INT}$ | 8 | DPI_P13 | 30 | DAI_P14 | 52 | GND | 74 |
| CLKIN | 9 | DAI_P03 | 31 | DAI_P18 | 53 | $V_{DD\_EXT}$ | 75 |
| XTAL | 10 | DPI_P14 | 32 | DAI_P17 | 54 | GND | 76 |
| $V_{DD\_EXT}$ | 11 | $V_{DD\_INT}$ | 33 | DAI_P16 | 55 | $V_{DD\_INT}$ | 77 |
| $V_{DD\_INT}$ | 12 | DAI_P13 | 34 | DAI_P15 | 56 | $\overline{TRST}$ | 78 |
| $V_{DD\_INT}$ | 13 | DAI_P07 | 35 | DAI_P12 | 57 | $\overline{EMU}$ | 79 |
| $\overline{RESETOUT}$/$\overline{RUNRSTIN}$ | 14 | DAI_P19 | 36 | DAI_P11 | 58 | TDO | 80 |
| $V_{DD\_INT}$ | 15 | DAI_P01 | 37 | $V_{DD\_INT}$ | 59 | $V_{DD\_EXT}$ | 81 |
| DPI_P01 | 16 | DAI_P02 | 38 | GND | 60 | $V_{DD\_INT}$ | 82 |
| DPI_P02 | 17 | $V_{DD\_INT}$ | 39 | THD_M | 61 | TDI | 83 |
| DPI_P03 | 18 | $V_{DD\_EXT}$ | 40 | THD_P | 62 | TCK | 84 |
| $V_{DD\_INT}$ | 19 | $V_{DD\_INT}$ | 41 | $V_{DD\_THD}$ | 63 | $V_{DD\_INT}$ | 85 |
| DPI_P05 | 20 | DAI_P06 | 42 | $V_{DD\_INT}$ | 64 | $\overline{RESET}$ | 86 |
| DPI_P04 | 21 | DAI_P05 | 43 | $V_{DD\_INT}$ | 65 | TMS | 87 |
| DPI_P06 | 22 | DAI_P09 | 44 | $V_{DD\_INT}$ | 66 | $V_{DD\_INT}$ | 88 |
| | | | | | | GND | 89* |

* Lead no. 89 is the GND supply (see Figure 53 and Figure 54) for the processor; this pad must be **robustly** connected to GND in order for the processor to function.

Figure 55 shows the top view configuration of the 100-lead LQFP_EP package. Figure 56 shows the bottom view configuration of the 100-lead LQFP_EP package.

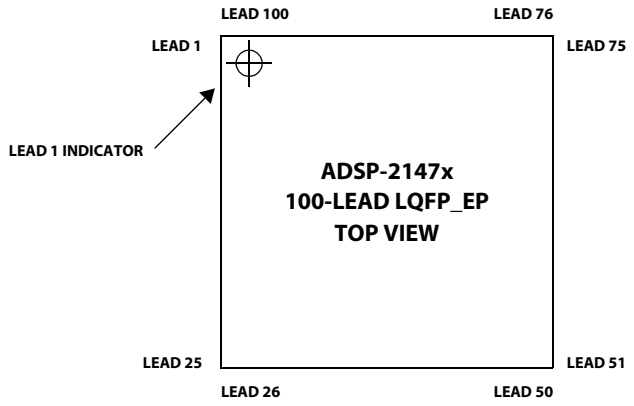


*Figure 55. 100-Lead LQFP_EP Lead Configuration (Top View)*

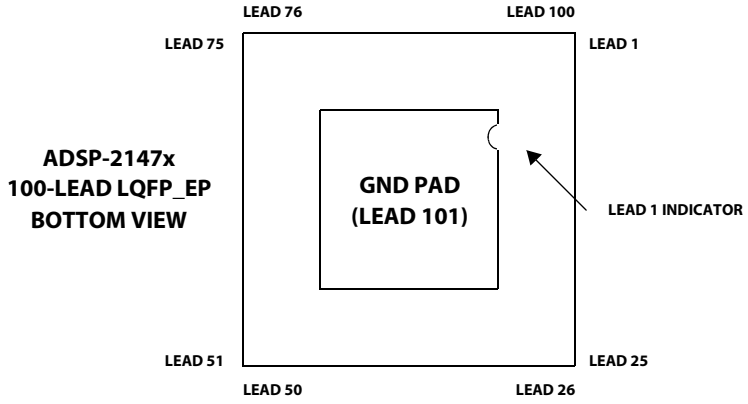


*Figure 56. 100-Lead LQFP_EP Lead Configuration (Bottom View)*

# 196-BGA BALL ASSIGNMENT

**Table 63. 196-Ball CSP_BGA Ball Assignment (Numerical by Ball No.)**

| Ball No. | Signal | Ball No. | Signal | Ball No. | Signal | Ball No. | Signal | Ball No. | Signal |
|---|---|---|---|---|---|---|---|---|---|
| A1 | GND | D1 | ADDR6 | G1 | XTAL | K1 | DPI_P02 | N1 | DPI_P14 |
| A2 | SDCKE | D2 | ADDR4 | G2 | SDA10 | K2 | DPI_P04 | N2 | SR_LDO1 |
| A3 | SDDQM | D3 | ADDR1 | G3 | ADDR11 | K3 | DPI_P05 | N3 | SR_LDO4 |
| A4 | $\overline{\text{SDRAS}}$ | D4 | CLK_CFG0 | G4 | GND | K4 | DPI_P09 | N4 | SR_LDO8 |
| A5 | $\overline{\text{SDWE}}$ | D5 | $V_{DD\_EXT}$ | G5 | $V_{DD\_INT}$ | K5 | $V_{DD\_INT}$ | N5 | SR_LDO10 |
| A6 | DATA12 | D6 | $V_{DD\_EXT}$ | G6 | GND | K6 | GND | N6 | DAI_P01 |
| A7 | DATA13 | D7 | $V_{DD\_EXT}$ | G7 | GND | K7 | GND | N7 | SR_LDO9 |
| A8 | DATA10 | D8 | $V_{DD\_EXT}$ | G8 | GND | K8 | GND | N8 | DAI_P02 |
| A9 | DATA9 | D9 | $V_{DD\_EXT}$ | G9 | GND | K9 | GND | N9 | SR_LDO13 |
| A10 | DATA7 | D10 | $V_{DD\_EXT}$ | G10 | $V_{DD\_INT}$ | K10 | $V_{DD\_INT}$ | N10 | SR_SCLK |
| A11 | DATA3 | D11 | $V_{DD\_EXT}$ | G11 | $V_{DD\_EXT}$ | K11 | GND | N11 | DAI_P09 |
| A12 | DATA1 | D12 | ADDR14 | G12 | ADDR21 | K12 | DAI_P16 | N12 | SR_SDI |
| A13 | DATA2 | D13 | ADDR20 | G13 | ADDR19 | K13 | DAI_P18 | N13 | SR_LDO17 |
| A14 | GND | D14 | WDT_CLKO | G14 | RTXO | K14 | DAI_P15 | N14 | DAI_P14 |
| B1 | ADDR0 | E1 | ADDR8 | H1 | ADDR13 | L1 | DAI_P03 | P1 | GND |
| B2 | CLK_CFG1 | E2 | ADDR7 | H2 | ADDR12 | L2 | DPI_P10 | P2 | SR_LDO3 |
| B3 | BOOT_CFG0 | E3 | ADDR5 | H3 | ADDR10 | L3 | DPI_P08 | P3 | SR_LDO2 |
| B4 | TMS | E4 | $V_{DD\_EXT}$ | H4 | ADDR17 | L4 | DPI_P06 | P4 | SR_LDO6 |
| B5 | $\overline{\text{RESET}}$ | E5 | $V_{DD\_INT}$ | H5 | $V_{DD\_INT}$ | L5 | $V_{DD\_INT}$ | P5 | $\overline{\text{WDTRSTO}}$ |
| B6 | DATA14 | E6 | $V_{DD\_INT}$ | H6 | GND | L6 | $V_{DD\_INT}$ | P6 | DAI_P19 |
| B7 | DATA11 | E7 | $V_{DD\_INT}$ | H7 | GND | L7 | $V_{DD\_INT}$ | P7 | DAI_P13 |
| B8 | DATA4 | E8 | $V_{DD\_INT}$ | H8 | GND | L8 | $V_{DD\_INT}$ | P8 | SR_LDO11 |
| B9 | DATA8 | E9 | $V_{DD\_INT}$ | H9 | GND | L9 | $V_{DD\_INT}$ | P9 | SR_LDO15 |
| B10 | DATA6 | E10 | $V_{DD\_INT}$ | H10 | $V_{DD\_INT}$ | L10 | $V_{DD\_INT}$ | P10 | $\overline{\text{SR\_CLR}}$ |
| B11 | DATA5 | E11 | $V_{DD\_EXT}$ | H11 | $V_{DD\_EXT}$ | L11 | DAI_P10 | P11 | SR_LAT |
| B12 | $\overline{\text{TRST}}$ | E12 | $\overline{\text{AMI\_RD}}$ | H12 | BOOT_CFG2 | L12 | DAI_P20 | P12 | SR_LDO14 |
| B13 | FLAG1 | E13 | ADDR22 | H13 | ADDR23 | L13 | DAI_P17 | P13 | SR_LDO12 |
| B14 | DATA0 | E14 | FLAG2 | H14 | RTXI | L14 | DAI_P04 | P14 | GND |
| C1 | ADDR2 | F1 | CLKIN | J1 | DPI_P01 | M1 | DPI_P13 | | |
| C2 | ADDR3 | F2 | ADDR9 | J2 | DPI_P03 | M2 | DPI_P12 | | |
| C3 | RTCLKOUT | F3 | BOOT_CFG1 | J3 | ADDR18 | M3 | SR_LDO0 | | |
| C4 | $\overline{\text{MS0}}$ | F4 | NC | J4 | $\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$ | M4 | DPI_P07 | | |
| C5 | $\overline{\text{SDCAS}}$ | F5 | NC | J5 | $V_{DD\_INT}$ | M5 | DPI_P11 | | |
| C6 | DATA15 | F6 | GND | J6 | GND | M6 | SR_LDO5 | | |
| C7 | TCK | F7 | GND | J7 | GND | M7 | SR_LDO7 | | |
| C8 | TDI | F8 | GND | J8 | GND | M8 | DAI_P07 | | |
| C9 | SDCLK | F9 | GND | J9 | GND | M9 | SR_LDO16 | | |
| C10 | $\overline{\text{EMU}}$ | F10 | $V_{DD\_INT}$ | J10 | $V_{SS\_RTC}$ | M10 | SR_SDO | | |
| C11 | TDO | F11 | $V_{DD\_EXT}$ | J11 | $V_{DD\_RTC}$ | M11 | DAI_P06 | | |
| C12 | FLAG3 | F12 | ADDR15 | J12 | DAI_P11 | M12 | DAI_P05 | | |
| C13 | ADDR16 | F13 | FLAG0 | J13 | AMI_ACK | M13 | DAI_P08 | | |
| C14 | WDT_CLKIN | F14 | $\overline{\text{AMI\_WR}}$ | J14 | $\overline{\text{MS1}}$ | M14 | DAI_P12 | | |

# OUTLINE DIMENSIONS

The processors are available in 88-lead LFCSP_VQ, 100-lead LQFP_EP and 196-ball CSP_BGA RoHS compliant packages. For package assignment by model, see Ordering Guide.

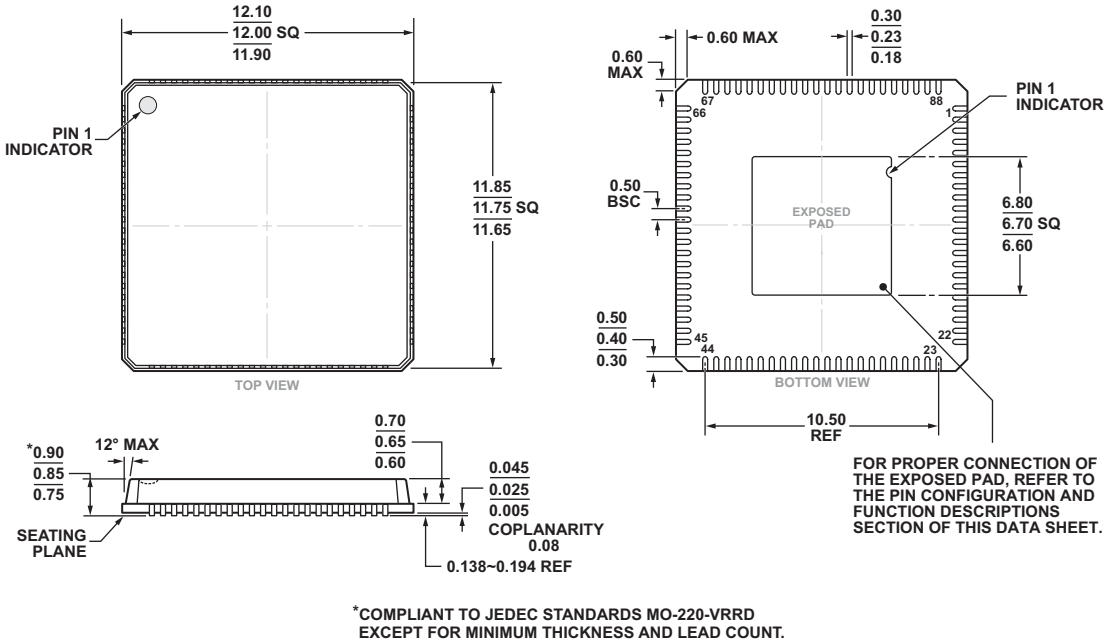


*Figure 57. 88-Lead Lead Frame Chip Scale Package [LFCSP_VQ[1]]*
*(CP-88-5)*
*Dimensions Shown in Millimeters*

[1] For information relating to the exposed pad on the CP-88-5 package, see the table endnote on Page 68.

## ORDERING GUIDE

| Model[1] | Temperature Range[2] | On-Chip SRAM | Processor Instruction Rate (Max) | Package Description | Package Option |
|---|---|---|---|---|---|
| ADSP-21477KCPZ-1A | 0°C to +70°C | 2M Bits | 200 MHz | 88-Lead LFCSP_VQ | CP-88-5 |
| ADSP-21477KSWZ-1A | 0°C to +70°C | 2M Bits | 200 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21477BCPZ-1A | –40°C to +85°C | 2M Bits | 200 MHz | 88-Lead LFCSP_VQ | CP-88-5 |
| ADSP-21478KCPZ-1A | 0°C to +70°C | 3M Bits | 200 MHz | 88-Lead LFCSP_VQ | CP-88-5 |
| ADSP-21478BCPZ-1A | –40°C to +85°C | 3M Bits | 200 MHz | 88-Lead LFCSP_VQ | CP-88-5 |
| ADSP-21478BBCZ-2A | –40°C to +85°C | 3M Bits | 266 MHz | 196-Ball CSP_BGA | BC-196-8 |
| ADSP-21478BSWZ-2A | –40°C to +85°C | 3M Bits | 266 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21478KBCZ-1A | 0°C to +70°C | 3M Bits | 200 MHz | 196-Ball CSP_BGA | BC-196-8 |
| ADSP-21478KBCZ-2A | 0°C to +70°C | 3M Bits | 266 MHz | 196-Ball CSP_BGA | BC-196-8 |
| ADSP-21478KBCZ-3A | 0°C to +70°C | 3M Bits | 300 MHz | 196-Ball CSP_BGA | BC-196-8 |
| ADSP-21478KSWZ-1A | 0°C to +70°C | 3M Bits | 200 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21478KSWZ-2A | 0°C to +70°C | 3M Bits | 266 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21479KCPZ-1A | 0°C to +70°C | 5M Bits | 200 MHz | 88-Lead LFCSP_VQ | CP-88-5 |
| ADSP-21479BCPZ-1A | –40°C to +85°C | 5M Bits | 200 MHz | 88-Lead LFCSP_VQ | CP-88-5 |
| ADSP-21479BBCZ-2A | –40°C to +85°C | 5M Bits | 266 MHz | 196-Ball CSP_BGA | BC-196-8 |
| ADSP-21479BSWZ-2A | –40°C to +85°C | 5M Bits | 266 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21479KBCZ-1A | 0°C to +70°C | 5M Bits | 200 MHz | 196-Ball CSP_BGA | BC-196-8 |
| ADSP-21479KBCZ-2A | 0°C to +70°C | 5M Bits | 266 MHz | 196-Ball CSP_BGA | BC-196-8 |
| ADSP-21479KBCZ-3A | 0°C to +70°C | 5M Bits | 300 MHz | 196-Ball CSP_BGA | BC-196-8 |
| ADSP-21479KSWZ-1A | 0°C to +70°C | 5M Bits | 200 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21479KSWZ-2A | 0°C to +70°C | 5M Bits | 266 MHz | 100-Lead LQFP_EP | SW-100-2 |

[1] Z =RoHS compliant part.
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions for junction temperature ($T_J$) specification, which is the only temperature specification.