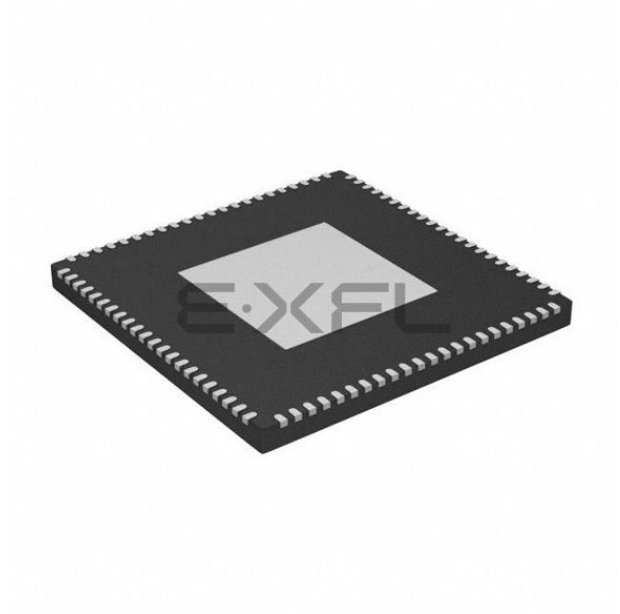

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI, EBI/EMI, I²C, SPI, SPORT, UART/USART
Clock Rate	200MHz
Non-Volatile Memory	ROM (4Mbit)
On-Chip RAM	5Mbit
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	88-VFQFN Exposed Pad, CSP
Supplier Device Package	88-LFCSP-VQ (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ad21479wycpz1b02

buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

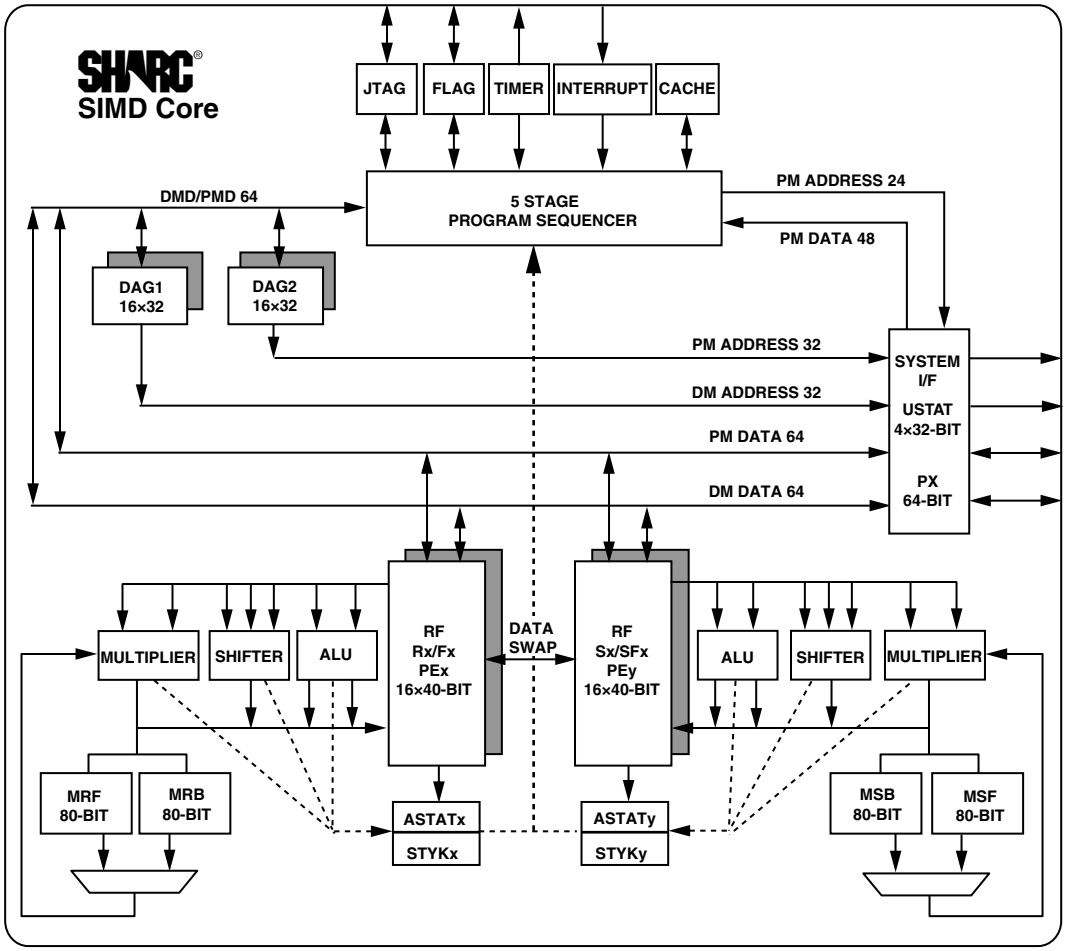

Figure 2. SHARC Core Block Diagram

Instruction Cache

The processor includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full speed execution of core looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators with Zero-Overhead Hardware Circular Buffer Support

The processor's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the processors contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the processors can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

Variable Instruction Set Architecture (VISA)

In addition to supporting the standard 48-bit instructions from previous SHARC processors, the processors support new instructions of 16 and 32 bits. This feature, called Variable Instruction Set Architecture (VISA), drops redundant/unused

occupy a 8M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic.

External Port Throughput

The throughput for the external port, based on 133 MHz clock and 16-bit data bus, is 88 Mbytes/sec for the AMI and 266 Mbytes/sec for SDRAM.

MediaLB

The automotive models of the processors have an MLB interface which allows the processor to function as a media local bus device. It includes support for both 3-pin and 5-pin MLB protocols. It supports speeds up to 1024 FS (49.25M bits/sec, FS = 48.1 kHz) and up to 31 logical channels, with up to 124 bytes of data per media local bus frame. For a list of automotive products, see Automotive Products.

Digital Applications Interface (DAI)

The digital applications interface (DAI) provides the ability to connect various peripherals to any of the DAI pins (DAI_P20–1).

Programs make these connections using the signal routing unit (SRU), shown in Figure 1.

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with non configurable signal paths.

The associated peripherals include eight serial ports, four precision clock generators (PCG), a S/PDIF transceiver, four ASRCs, and an input data port (IDP). The IDP provides an additional input path to the SHARC core, configurable as either eight channels of serial data, or a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

Serial Ports (SPORTs)

The processors feature eight synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports can support up to 16 transmit or 16 receive DMA channels of audio data when all eight SPORTs are enabled, or four full duplex TDM streams of 128 channels per frame.

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a bi phase encoded signal. The serial data input to the receiver/transmitter can be formatted as left justified, I^2S or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources, such as the SPORTs, external pins, the precision clock generators (PCGs), and are controlled by the SRU control registers.

Asynchronous Sample Rate Converter (SRC)

The sample rate converter contains four blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter. The SRC block provides up to 128 dB SNR and is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Input Data Port

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I^2S, left-justified sample pair, or right-justified mode.

The IDP also provides a parallel data acquisition port (PDAP) which can be used for receiving parallel data. The PDAP port has a clock input and a hold input. The data for the PDAP can be received from DAI pins or from the external port pins. The PDAP supports a maximum of 20-bit data and four different packing modes to receive the incoming data.

Precision Clock Generators

The precision clock generators (PCG) consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A B, C, and D are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

The outputs of PCG A and B can be routed through the DAI pins and the outputs of PCG C and D can be driven on to the DAI as well as the DPI pins.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2147x architecture and functionality. For detailed information on the family core architecture and instruction set, refer to the *SHARC Processor Programming Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Reference Designs page provides a link to Circuits from the Lab™ (www.analog.com/signal chains) which contains:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

Table 11. Pin Descriptions

Name	Type	State During/ After Reset	Description
$ADDR_{23-0}$	I/O/T (ipu)	High-Z/driven low (boot)	**External Address.** The processor outputs addresses for external memory and peripherals on these pins. The ADDR pins can be multiplexed to support the external memory interface address, FLAGS15–8 (I/O) and PWM (O). After reset, all ADDR pins are in EMIF mode, and FLAG(0–3) pins are in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the $ADDR_{23-4}$ pins for parallel input data.
$DATA_{15-0}$	I/O/T (ipu)	High-Z	**External Data.** The data pins can be multiplexed to support the external memory interface data (I/O) and $FLAGS_{7-0}$ (I/O).
AMI_ACK	I (ipu)		**Memory Acknowledge.** External devices can deassert AMI_ACK (low) to add wait states to an external memory access. AMI_ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{MS}_{0-1}$	O/T (ipu)	High-Z	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{1-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, when the condition evaluates as true. The $\overline{MS1}$ pin can be used in EPORT/FLASH boot mode. For more information on processor booting, see the *ADSP-214xx SHARC Processor Hardware Reference*.
$\overline{AMI\_RD}$	O/T (ipu)	High-Z	**AMI Port Read Enable.** $\overline{AMI\_RD}$ is asserted whenever the processor reads a word from external memory.
$\overline{AMI\_WR}$	O/T (ipu)	High-Z	**AMI Port Write Enable.** $\overline{AMI\_WR}$ is asserted when the processor writes a word to external memory.
FLAG0/$\overline{IRQ0}$	I/O (ipu)	FLAG[0] INPUT	**FLAG0/Interrupt Request0.**
FLAG1/$\overline{IRQ1}$	I/O (ipu)	FLAG[1] INPUT	**FLAG1/Interrupt Request1.**
FLAG2/$\overline{IRQ2}$/$\overline{MS2}$	I/O (ipu)	FLAG[2] INPUT	**FLAG2/Interrupt Request2/Memory Select2.** This pin is multiplexed with $\overline{MS2}$ in the 196-ball BGA package only.
FLAG3/TMREXP/$\overline{MS3}$	I/O (ipu)	FLAG[3] INPUT	**FLAG3/Timer Expired/Memory Select3.** This pin is multiplexed with $\overline{MS3}$ in the 196-ball BGA package only.

The following symbols appear in the Type column of Table 11: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be 26 kΩ to 63 kΩ. The range of an ipd resistor can be 31 kΩ to 85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.

Not all pins are available in the 88-lead LFCSP_VQ and 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 62 on Page 70.

Table 11. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
THD_P	I		**Thermal Diode Anode.** When not used, this pin can be left floating.
THD_M	O		**Thermal Diode Cathode.** When not used, this pin can be left floating.
MLBCLK	I		**Media Local Bus Clock.** This clock is generated by the MLB controller that is synchronized to the MOST network and provides the timing for the entire MLB interface at 49.152 MHz at FS = 48 kHz. When the MLB controller is not used, this pin should be grounded.
MLBDAT	I/O/T in 3 pin mode. I in 5 pin mode.	High-Z	**Media Local Bus Data.** The MLBDAT line is driven by the transmitting MLB device and is received by all other MLB devices including the MLB controller. The MLBDAT line carries the actual data. In 5-pin MLB mode, this pin is an input only. When the MLB controller is not used, this pin should be grounded.
MLBSIG	I/O/T in 3 pin mode. I in 5 pin mode	High-Z	**Media Local Bus Signal.** This is a multiplexed signal which carries the Channel/Address generated by the MLB Controller, as well as the Command and RxStatus bytes from MLB devices. In 5-pin mode, this pin is input only. When the MLB controller is not used, this pin should be grounded.
MLBDO	O/T	High-Z	**Media Local Bus Data Output (in 5 Pin Mode).** This pin is used only in 5-pin MLB mode and serves as the output data pin. When the MLB controller is not used, this pin should be grounded.
MLBSO	O/T	High-Z	**Media Local Bus Signal Output (in 5 Pin Mode).** This pin is used only in 5-pin MLB mode and serves as the output signal pin. When the MLB controller is not used, this pin should be grounded.
SR_SCLK	I (ipu)		**Shift Register Serial Clock.** (Active high, rising edge sensitive)
$\overline{\text{SR\_CLR}}$	I (ipu)		**Shift Register Reset.** (Active low)
SR_SDI	I (ipu)		**Shift Register Serial Data Input.**
SR_SDO	O (ipu)	Driven Low	**Shift Register Serial Data Output.**
SR_LAT	I (ipu)		**Shift Register Latch Clock Input.** (Active high, rising edge sensitive)
SR_LDO_{17-0}	O/T (ipu)	High-Z	**Shift Register Parallel Data Output.**
RTXI	I		**RTC Crystal Input.** If RTC is not used, then this pin can be NC (no connect) or grounded and the RTC_PDN and RTC_BUSDIS bits of the RTC_INIT register must be set to 1.
RTXO	O		**RTC Crystal Output.** If RTC is not used, then this pin needs to be NC (No Connect).
RTCLKOUT	O (ipd)		**RTC Clock Output.** For calibration purposes. The clock runs at 1 Hz. If RTC is not used, then this pin needs to be NC (No Connect).

The following symbols appear in the Type column of Table 11: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be 26 kΩ to 63 kΩ. The range of an ipd resistor can be 31 kΩ to 85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.

Not all pins are available in the 88-lead LFCSP_VQ and 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 62 on Page 70.

Table 11. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
TDI	I (ipu)		**Test Data Input (JTAG).** Provides serial data for the boundary scan logic.
TDO	O/T	High-Z	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
TMS	I (ipu)		**Test Mode Select (JTAG).** Used to control the test state machine.
TCK	I		**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the device.
$\overline{\text{TRST}}$	I (ipu)		**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor.
$\overline{\text{EMU}}$	O (O/D, ipu)	High-Z	**Emulation Status.** Must be connected to the Analog Devices DSP Tools product line of JTAG emulators target board connector only.
CLK_CFG_{1-0}	I		**Core to CLKIN Ratio Control.** These pins set the startup clock frequency. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset. The allowed values are: 00 = 8:1 01 = 32:1 10 = 16:1 11 = reserved
CLKIN	I		**Local Clock In.** Used in conjunction with XTAL. CLKIN is the clock input. It configures the processors to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processors to use the external clock source such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency.
XTAL	O		**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal.
$\overline{\text{RESET}}$	I		**Processor Reset.** Resets the processor to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
$\overline{\text{RESETOUT}}/\overline{\text{RUNRSTIN}}$	I/O (ipu)		**Reset Out/Running Reset In.** The default setting on this pin is reset out. This pin also has a second function as RUNRSTIN which is enabled by setting bit 0 of the RUNRSTCTL register. For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*.
BOOT_CFG_{2-0}	I		**Boot Configuration Select.** These pins select the boot mode for the processor. The BOOT_CFG pins must be valid before $\overline{\text{RESET}}$ (hardware and software) is de-asserted. The BOOT_CFG2 pin is only available on the 196-lead package.

The following symbols appear in the Type column of Table 11: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be 26 kΩ to 63 kΩ. The range of an ipd resistor can be 31 kΩ to 85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.

Not all pins are available in the 88-lead LFCSP_VQ and 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 62 on Page 70.

Clock Input

Table 20. Clock Input

Parameter		200 MHz Min	200 MHz Max	266 MHz Min	266 MHz Max	300 MHz Min	300 MHz Max	Unit
Timing Requirements								
t_{CK}	CLKIN Period	40	100	30[1]	100	26.66[1]	100	ns
t_{CKL}	CLKIN Width Low	20	45	15	45	13.33	45	ns
t_{CKH}	CLKIN Width High	20	45	15	45	13.33	45	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3	ns
t_{CCLK}[2]	CCLK Period	5	10	3.75	10	3.33	10	ns
f_{VCO}[3]	VCO Frequency	200	600	200	600	200	600	MHz
t_{CKJ}[4, 5]	CLKIN Jitter Tolerance	–250	+250	–250	+250	–250	+250	ps

[1] Applies only for CLKCFG1–0 = 00 and default values for PLL control bits in PMCTL.
[2] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{cclk}.
[3] See Figure 5 for VCO diagram.
[4] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[5] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

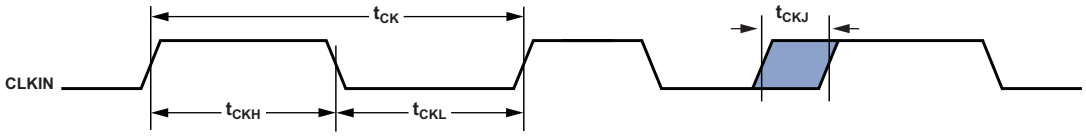

Figure 7. Clock Input

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

Table 24. Core Timer

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Switching Characteristic						
t_{WCTIM}	TMREXP Pulse Width	$4 \times t_{PCLK} - 1.55$		$4 \times t_{PCLK} - 1.2$		ns

Figure 12. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to timer0 and timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 25. Timer PWM_OUT Timing

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Switching Characteristic						
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 1.65$	$2 \times (2^{31} - 1) \times t_{PCLK}$	$2 \times t_{PCLK} - 1.2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

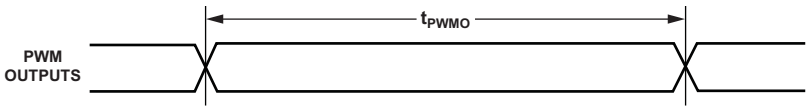

Figure 13. Timer PWM_OUT Timing

SDRAM Interface Timing

Table 31. SDRAM Interface Timing

Parameter		133 MHz Min	133 MHz Max	150 MHz Min	150 MHz Max	Unit
Timing Requirements						
t_{SSDAT}	DATA Setup Before SDCLK	0.7		0.7		ns
t_{HSDAT}	DATA Hold After SDCLK	1.66		1.5		ns
Switching Characteristics						
t_{SDCLK}[1]	SDCLK Period	7.5		6.66		ns
t_{SDCLKH}	SDCLK Width High	2.5		2.2		ns
t_{SDCLKL}	SDCLK Width Low	2.5		2.2		ns
t_{DCAD}[2]	Command, ADDR, Data Delay After SDCLK		5		4.75	ns
t_{HCAD}[2]	Command, ADDR, Data Hold After SDCLK	1		1		ns
t_{DSDAT}	Data Disable After SDCLK		6.2		5.3	ns
t_{ENSDAT}	Data Enable After SDCLK	0.3		0.3		ns

[1] Systems should use the SDRAM model with a speed grade higher than the desired SDRAM controller speed. For example, to run the SDRAM controller at 133 MHz the SDRAM model with a speed grade of 143 MHz or above should be used. See Engineer-to-Engineer Note "Interfacing SDRAM memory to SHARC processors (EE-286)" for more information on hardware design guidelines for the SDRAM interface.
[2] Command pins include: $\overline{SDCAS}$, $\overline{SDRAS}$, $\overline{SDWE}$, $\overline{MSx}$, SDA10, SDQM, SDCKE.

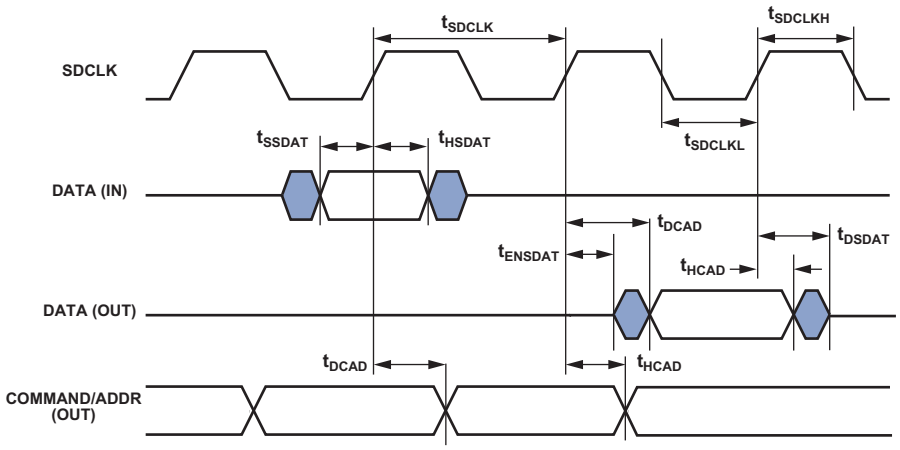

Figure 19. SDRAM Interface Timing

Table 35. Serial Ports—Internal Clock

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	13		10.5		ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5		2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	13		10.5		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		2.5		ns
Switching Characteristics						
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		5		5	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1.0		–1.0		ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		10.7		10.7	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1.0		–1.0		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		4		4	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0		–1.0		ns
t_{SCKLIW}	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left-justified, I²S, or right-justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 31 shows the right-justified mode. Frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed the minimum in 24-bit output mode or the maximum in 16-bit output mode from a frame sync transition, so that when there are 64 serial clock periods per frame sync period, the LSB of the data is right-justified to the next frame sync transition.

Figure 32 shows the default I²S-justified mode. The frame sync is low for the left channel and high for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition but with a delay.

Table 44. S/PDIF Transmitter Right-Justified Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{RJD}	FS to MSB Delay in Right-Justified Mode		
	16-Bit Word Mode	16	SCLK
	18-Bit Word Mode	14	SCLK
	20-Bit Word Mode	12	SCLK
	24-Bit Word Mode	8	SCLK

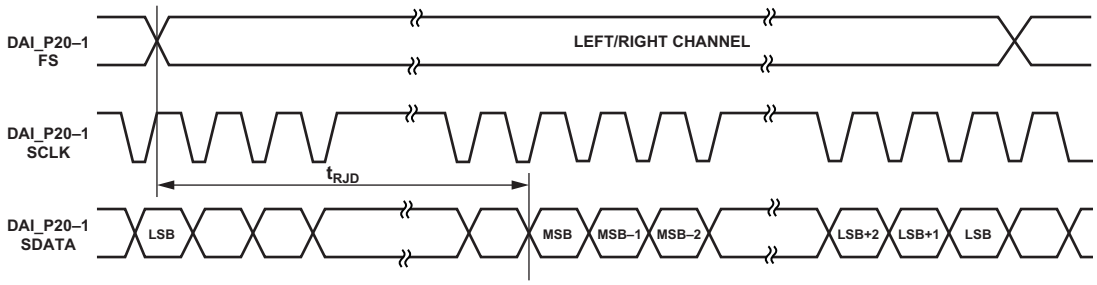

Figure 31. Right-Justified Mode

Table 45. S/PDIF Transmitter I²S Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{I2SD}	FS to MSB Delay in I²S Mode	1	SCLK

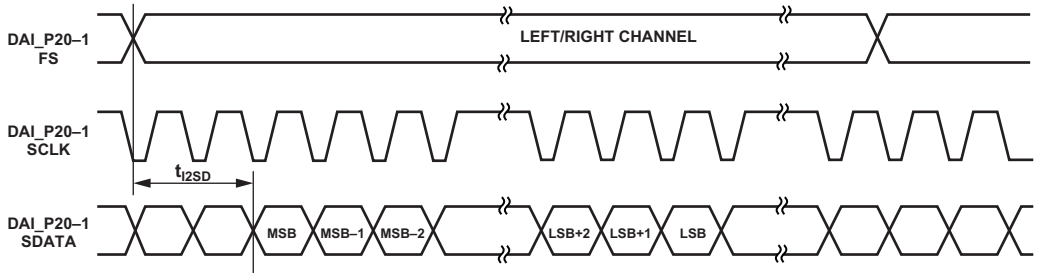

Figure 32. I²S-Justified Mode

Figure 33 shows the left-justified mode. The frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition with no delay.

Media Local Bus

All the numbers given are applicable for all speed modes (1024 FS, 512 FS, and 256 FS for 3-pin; 512 FS and 256 FS for 5-pin) unless otherwise specified. Please refer to MediaLB specification document rev 3.0 for more details.

Table 52. MLB Interface, 3-Pin Specifications

Parameter		Min	Typ	Max	Unit
3-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	1024 FS		20.3		ns
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	1024 FS	6.1			ns
	512 FS	14			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	1024 FS	9.3			ns
	512 FS	14			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})				
	1024 FS			1	ns
	512 FS/256 FS			3	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})				
	1024 FS			1	ns
	512 FS/256 FS			3	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation				
	1024 FS			0.7	ns p-p
	512 FS/256			2.0	ns p-p
t_{DSMCF}	DAT/SIG Input Setup Time	1			ns
t_{DHMCF}	DAT/SIG Input Hold Time	1.2			ns
t_{MCFDZ}	DAT/SIG Output Time to Three-State	0		15	ns
t_{MCDRV}	DAT/SIG Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MDZH}[2]	Bus Hold Time				
	1024 FS	2			ns
	512 FS/256	4			ns
C_{MLB}	DAT/SIG Pin Load				
	1024 FS			40	pf
	512 FS/256			60	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (p-p).
[2] The board must be designed to ensure that the high impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

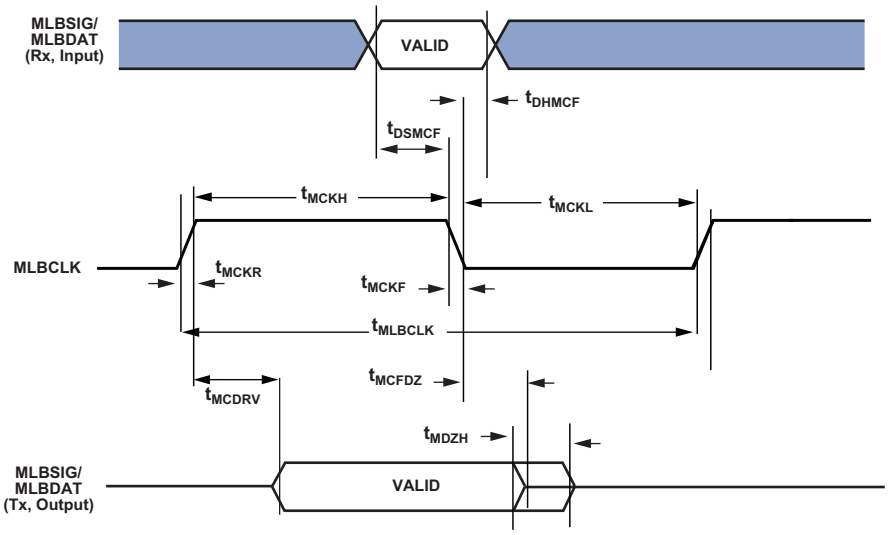

Figure 38. MLB Timing (3-Pin Interface)

Table 53. MLB Interface, 5-Pin Specifications

Parameter		Min	Typ	Max	Unit
5-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})			6	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})			6	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation			2	ns p-p
t_{DSMCF}[2]	DAT/SIG Input Setup Time	3			ns
t_{DHMCF}	DAT/SIG Input Hold Time	5			ns
t_{MCDRV}	DS/DO Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MCRDL}[3]	DO/SO Low From MLBCLK High				
	512 FS			10	ns
	256 FS			20	ns
C_{mlb}	DS/DO Pin Load			40	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (p-p).
[2] Gate delays due to OR'ing logic on the pins must be accounted for.
[3] When a node is not driving valid data onto the bus, the MLBSO and MLBDO output lines shall remain low. If the output lines can float at anytime, including while in reset, external pull-down resistors are required to keep the outputs from corrupting the MediaLB signal lines when not being driven.

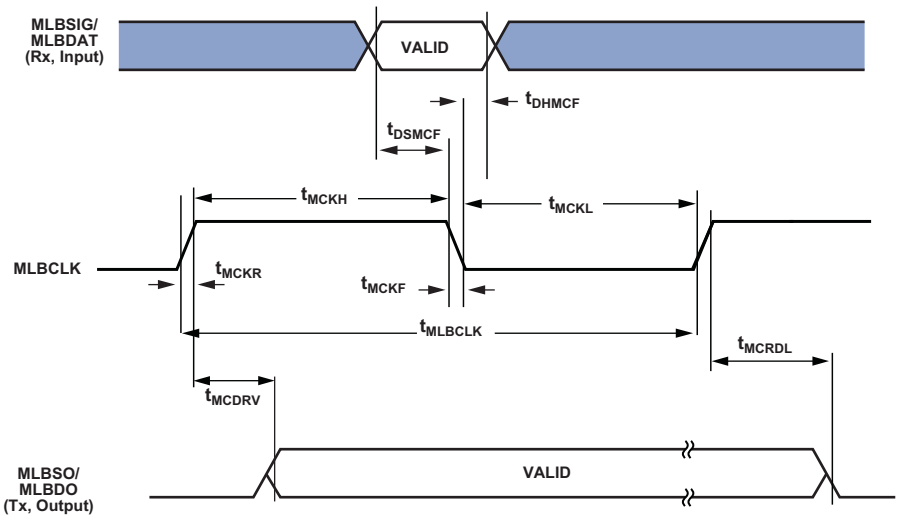

Figure 39. MLB Timing (5-Pin Interface)

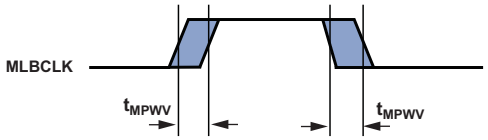

Figure 40. MLB 3-Pin and 5-Pin MLBCLK Pulse Width Variation Timing

Shift Register

Table 54. Shift Register

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDI}	SR_SDI Setup Before SR_SCLK Rising Edge	7		ns
t_{HSDI}	SR_SDI Hold After SR_SCLK Rising Edge	2		ns
$t_{SSDIDAI}$[1]	DAI_P08–01 (SR_SDI) Setup Before DAI_P08–01 (SR_SCLK) Rising Edge	7		ns
$t_{HSDIDAI}$[1]	DAI_P08–01 (SR_SDI) Hold After DAI_P08–01 (SR_SCLK) Rising Edge	2		ns
$t_{SSCK2LCK}$[2]	SR_SCLK to SR_LAT Setup	2		ns
$t_{SSCK2LCKDAI}$[1, 2]	DAI_P08–01 (SR_SCLK) to DAI_P08–01 (SR_LAT) Setup	2		ns
$t_{CLRREM2SCK}$	Removal Time $\overline{SR\_CLR}$ to SR_SCLK	$3 \times t_{PCLK} - 5$		ns
$t_{CLRREM2LCK}$	Removal Time $\overline{SR\_CLR}$ to SR_LAT	$2 \times t_{PCLK} - 5$		ns
t_{CLRW}	$\overline{SR\_CLR}$ Pulse Width	$4 \times t_{PCLK} - 5$		ns
t_{SCKW}	SR_SCLK Clock Pulse Width	$2 \times t_{PCLK} - 2$		ns
t_{LCKW}	SR_LAT Clock Pulse Width	$2 \times t_{PCLK} - 5$		ns
f_{MAX}	Maximum Clock Frequency SR_SCLK or SR_LAT		$f_{PCLK} \div 4$	MHz
Switching Characteristics				ns
t_{DSDO1}[3]	SR_SDO Hold After SR_SCLK Rising Edge	3		ns
t_{DSDO2}[3]	SR_SDO Max. Delay After SR_SCLK Rising Edge		13	ns
$t_{DSDODAI1}$[1, 3]	SR_SDO Hold After DAI_P08–01 (SR_SCLK) Rising Edge	3		ns
$t_{DSDODAI2}$[1, 3]	SR_SDO Max. Delay After DAI_P08–01 (SR_SCLK) Rising Edge		13	ns
$t_{DSDOSP1}$[3, 4]	SR_SDO Hold After DAI_P20–01 (SR_SCLK) Rising Edge	–2		ns
$t_{DSDOSP2}$[3, 4]	SR_SDO Max. Delay After DAI_P20–01 (SR_SCLK) Rising Edge		5	ns
$t_{DSDOPCG1}$[3, 5, 6]	SR_SDO Hold After DAI_P20–01 (SR_SCLK) Rising Edge	–2		ns
$t_{DSDOPCG2}$[3, 5, 6]	SR_SDO Max. Delay After DAI_P20–01 (SR_SCLK) Rising Edge		5	ns
$t_{DSDOCLR1}$[3]	$\overline{SR\_CLR}$ to SR_SDO Min. Delay	4		ns
$t_{DSDOCLR2}$[3]	$\overline{SR\_CLR}$ to SR_SDO Max. Delay		13	ns
t_{DLDO1}[3]	SR_LDO Hold After SR_LAT Rising Edge	3		ns
t_{DLDO2}[3]	SR_LDO Max. Delay After SR_LAT Rising Edge		13	ns
$t_{DLDODAI1}$[3]	SR_LDO Hold After DAI_P08–01 (SR_LAT) Rising Edge	3		ns
$t_{DLDODAI2}$[3]	SR_LDO Max. Delay After DAI_P08–01 (SR_LAT) Rising Edge		13	ns
$t_{DLDOSP1}$[3, 4]	SR_LDO Hold After DAI_P20–01 (SR_LAT) Rising Edge	–2		ns
$t_{DLDOSP2}$[3, 4]	SR_LDO Max. Delay After DAI_P20–01 (SR_LAT) Rising Edge		5	ns
$t_{DLDOPCG1}$[3, 5, 6]	SR_LDO Hold After DAI_P20–01 (SR_LAT) Rising Edge	–2		ns
$t_{DLDOPCG2}$[3, 5, 6]	SR_LDO Max. Delay After DAI_P20–01 (SR_LAT) Rising Edge		5	ns
$t_{DLDOCLR1}$[3]	$\overline{SR\_CLR}$ to SR_LDO Min. Delay	4		ns
$t_{DLDOCLR2}$[3]	$\overline{SR\_CLR}$ to SR_LDO Max. Delay		14	ns

[1] Any of the DAI_P08–01 pins can be routed to the shift register clock, latch clock and serial data input via the SRU.
[2] Both clocks can be connected to the same clock source. If both clocks are connected to same clock source, then data in the 18-stage shift register is always one cycle ahead of latch register data.
[3] For setup/hold timing requirements of off-chip shift register interfacing devices.
[4] SPORTx serial clock out, frame sync out, and serial data outputs are routed to shift register block internally and are also routed onto DAI_P20–01.
[5] PCG serial clock output is routed to SPORT and shift register block internally and are also routed onto DAI_P20–01. The SPORTs generate SR_LAT and SDI internally.
[6] PCG Serial clock and frame sync outputs are routed to SPORT and shift register block internally and are also routed onto DAI_P20–01. The SPORTs generate SDI internally.

Thermal Diode

The processors incorporate thermal diode/s to monitor the die temperature. The thermal diode is a grounded collector, PNP bipolar junction transistor (BJT). The THD_P pin is connected to the emitter, and the THD_M pin is connected to the base of the transistor. These pins can be used by an external temperature sensor (such as ADM1021A or LM86 or others) to read the die temperature of the chip.

The technique used by the external temperature sensor is to measure the change in VBE when the thermal diode is operated at two different currents. This is shown in the following equation:

$$\Delta V_{BE} = n \times \frac{kT}{q} \times ln(N)$$

where:

n = multiplication factor close to 1, depending on process variations

k = Boltzmann constant

T = temperature (°C)

q = charge of the electron

N = ratio of the two currents

The two currents are usually in the range of 10 µA to 300 µA for the common temperature sensor chips available.

Table 60 contains the thermal diode specifications using the transistor model.

Table 60. Thermal Diode Parameters—Transistor Model[1]

Symbol	Parameter	Min	Typ	Max	Unit
I_{FW}[2]	Forward Bias Current	10		300	µA
I_E	Emitter Current	10		300	µA
n_Q[3, 4]	Transistor Ideality	1.012	1.015	1.017	
R_T[3, 5]	Series Resistance	0.12	0.2	0.28	Ω

[1] Analog Devices does not recommend operation of the thermal diode under reverse bias.
[2] Analog Devices does not recommend operation of the thermal diode under reverse bias.
[3] Specified by design characterization.
[4] The ideality factor, nQ, represents the deviation from ideal diode behavior as exemplified by the diode equation: $I_C = I_S \times (e^{qVBE/nqkT} - 1)$ where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the diode, k = Boltzmann constant, and T = absolute temperature (Kelvin).
[5] The series resistance (R_T) can be used for more accurate readings as needed.

88-LFCSP_VQ LEAD ASSIGNMENT

Table 61 lists the 88-Lead LFCSP_VQ package lead names.

Table 61. 88-Lead LFCSP_VQ Lead Assignments (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
CLK_CFG1	1	V_{DD_EXT}	23	DAI_P10	45	V_{DD_INT}	67
BOOT_CFG0	2	DPI_P08	24	V_{DD_INT}	46	FLAG0	68
V_{DD_EXT}	3	DPI_P07	25	V_{DD_EXT}	47	V_{DD_INT}	69
V_{DD_INT}	4	DPI_P09	26	DAI_P20	48	FLAG1	70
BOOT_CFG1	5	DPI_P10	27	V_{DD_INT}	49	FLAG2	71
GND	6	DPI_P11	28	DAI_P08	50	FLAG3	72
CLK_CFG0	7	DPI_P12	29	DAI_P04	51	GND	73
V_{DD_INT}	8	DPI_P13	30	DAI_P14	52	GND	74
CLKIN	9	DAI_P03	31	DAI_P18	53	V_{DD_EXT}	75
XTAL	10	DPI_P14	32	DAI_P17	54	GND	76
V_{DD_EXT}	11	V_{DD_INT}	33	DAI_P16	55	V_{DD_INT}	77
V_{DD_INT}	12	DAI_P13	34	DAI_P15	56	$\overline{TRST}$	78
V_{DD_INT}	13	DAI_P07	35	DAI_P12	57	$\overline{EMU}$	79
$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	14	DAI_P19	36	DAI_P11	58	TDO	80
V_{DD_INT}	15	DAI_P01	37	V_{DD_INT}	59	V_{DD_EXT}	81
DPI_P01	16	DAI_P02	38	GND	60	V_{DD_INT}	82
DPI_P02	17	V_{DD_INT}	39	THD_M	61	TDI	83
DPI_P03	18	V_{DD_EXT}	40	THD_P	62	TCK	84
V_{DD_INT}	19	V_{DD_INT}	41	V_{DD_THD}	63	V_{DD_INT}	85
DPI_P05	20	DAI_P06	42	V_{DD_INT}	64	$\overline{RESET}$	86
DPI_P04	21	DAI_P05	43	V_{DD_INT}	65	TMS	87
DPI_P06	22	DAI_P09	44	V_{DD_INT}	66	V_{DD_INT}	88
						GND	89*

* Lead no. 89 is the GND supply (see Figure 53 and Figure 54) for the processor; this pad must be **robustly** connected to GND in order for the processor to function.

Figure 53 shows the top view of the 88-lead LFCSP_VQ pin configuration. Figure 54 shows the bottom view.

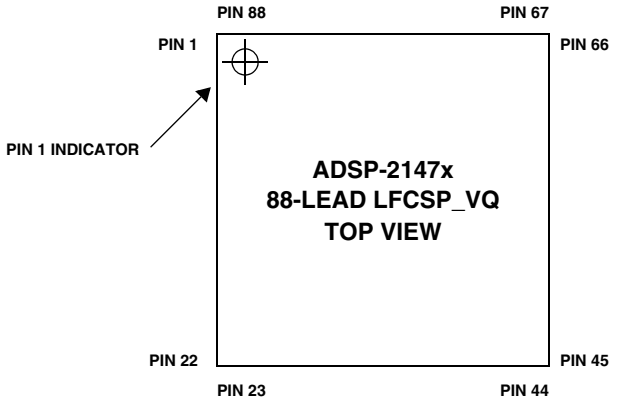

Figure 53. 88-Lead LFCSP_VQ Lead Configuration (Top View)

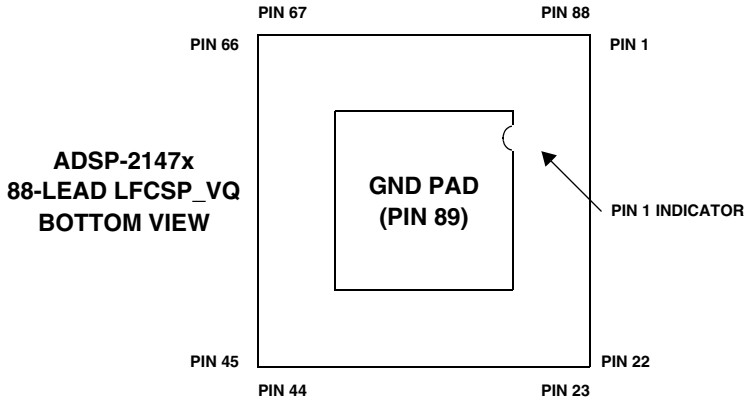

Figure 54. 88-Lead LFCSP_VQ Lead Configuration (Bottom View)

Figure 55 shows the top view configuration of the 100-lead LQFP_EP package. Figure 56 shows the bottom view configuration of the 100-lead LQFP_EP package.

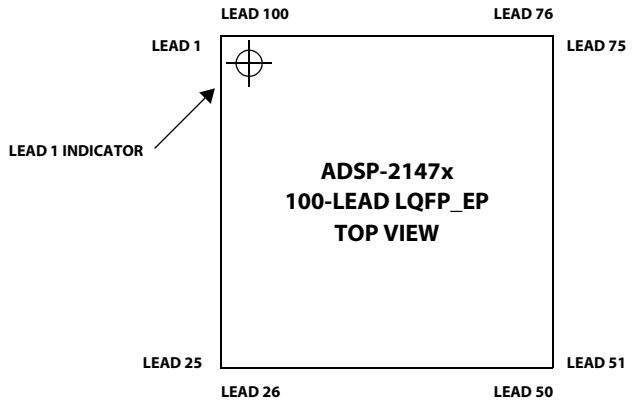

Figure 55. 100-Lead LQFP_EP Lead Configuration (Top View)

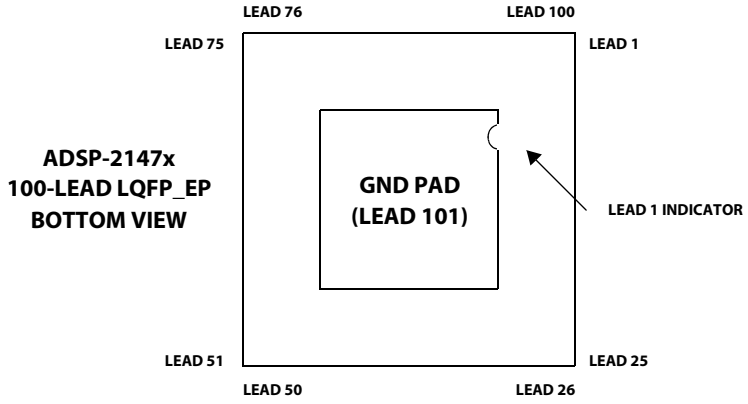

Figure 56. 100-Lead LQFP_EP Lead Configuration (Bottom View)

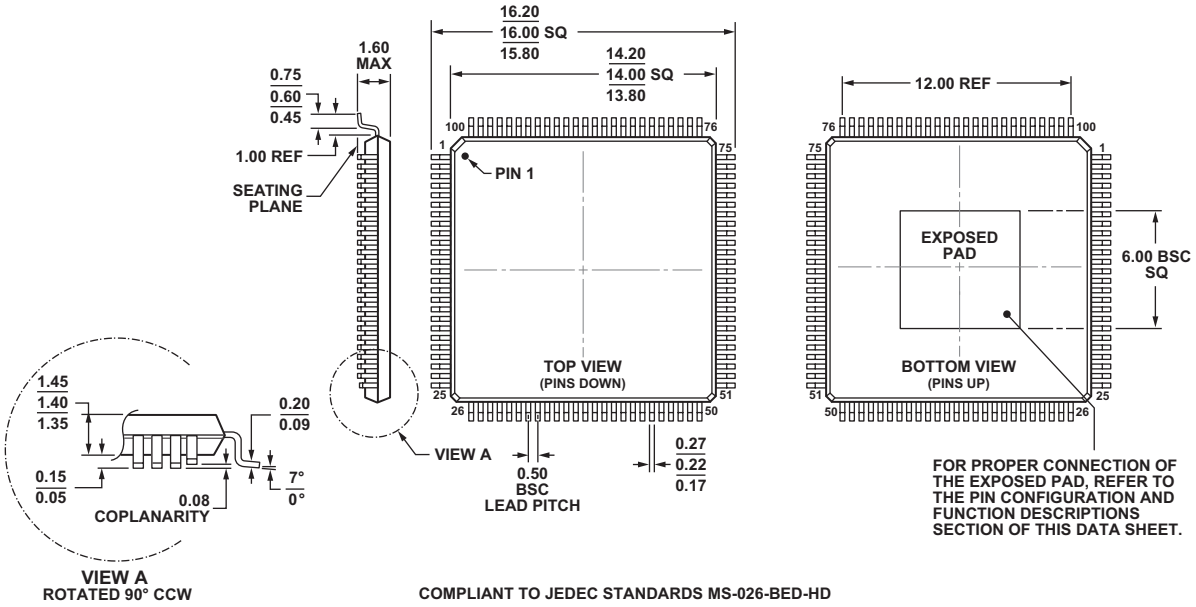

Figure 58. 100-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP[1]]
(SW-100-2)
Dimensions shown in millimeters

[1] For information relating to the exposed pad on the SW-100-2 package, see the table endnote on Page 70.

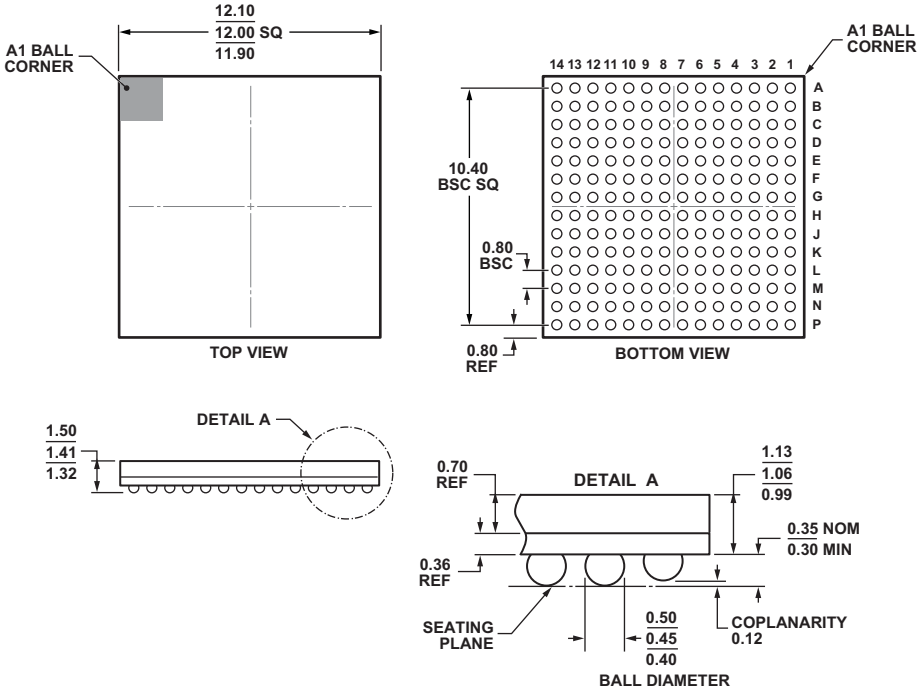

Figure 59. 196-Ball Chip Scale Package, Ball Grid Array [CSP_BGA]
(BC-196-8)
Dimensions shown in millimeters