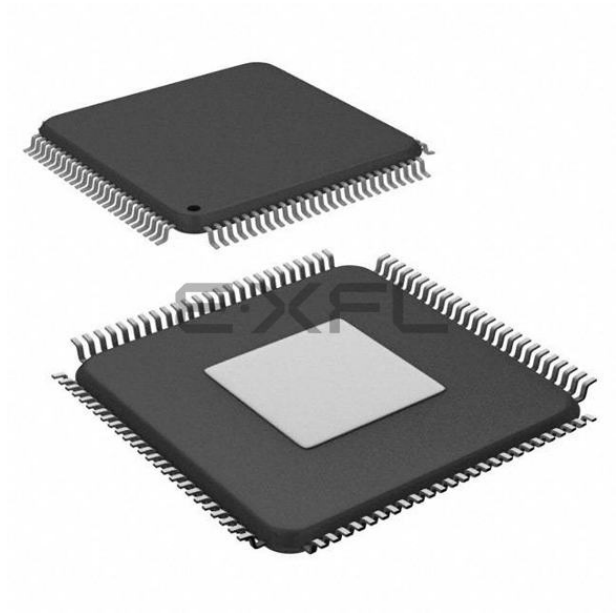

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI, I²C, SPI, SPORT, UART/USART
Clock Rate	200MHz
Non-Volatile Memory	-
On-Chip RAM	2Mbit
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	100-LQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21477kswz-1a

Table 4. ADSP-21478 Internal Memory Space (3M bits)[1]

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 3FFF
Block 0 SRAM 0x0004 9000–0x0004 CFFF	Block 0 SRAM 0x0008 C000–0x0009 1554	Block 0 SRAM 0x0009 2000–0x0009 9FFF	Block 0 SRAM 0x0012 4000–0x0013 3FFF
Reserved 0x0004 D000–0x0004 FFFF	Reserved 0x0009 1555–0x0009 FFFF	Reserved 0x0009 A000–0x0009 FFFF	Reserved 0x0013 4000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 CFFF	Block 1 SRAM 0x000A C000–0x000B 1554	Block 1 SRAM 0x000B 2000–0x000B 9FFF	Block 1 SRAM 0x0016 4000–0x0017 3FFF
Reserved 0x0005 D000–0x0005 FFFF	Reserved 0x000B 1555–0x000B FFFF	Reserved 0x000B A000–0x000B FFFF	Reserved 0x0017 4000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 1FFF	Block 2 SRAM 0x000C 0000–0x000C 2AA9	Block 2 SRAM 0x000C 0000–0x000C 3FFF	Block 2 SRAM 0x0018 0000–0x0018 7FFF
Reserved 0x0006 2000– 0x0006 FFFF	Reserved 0x000C 2AAA–0x000D FFFF	Reserved 0x000C 4000–0x000D FFFF	Reserved 0x0018 8000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 1FFF	Block 3 SRAM 0x000E 0000–0x000E 2AA9	Block 3 SRAM 0x000E 0000–0x000E 3FFF	Block 3 SRAM 0x001C 0000–0x001C 7FFF
Reserved 0x0007 2000–0x0007 FFFF	Reserved 0x000E 2AAA–0x000F FFFF	Reserved 0x000E 4000–0x000F FFFF	Reserved 0x001C 8000–0x001F FFFF

[1] Some processors include a customer-definable ROM block. ROM addresses on these models are not reserved as shown in this table. Please contact your Analog Devices sales representative for additional details.

seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

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For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

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Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

Table 11. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
THD_P	I		**Thermal Diode Anode.** When not used, this pin can be left floating.
THD_M	O		**Thermal Diode Cathode.** When not used, this pin can be left floating.
MLBCLK	I		**Media Local Bus Clock.** This clock is generated by the MLB controller that is synchronized to the MOST network and provides the timing for the entire MLB interface at 49.152 MHz at FS = 48 kHz. When the MLB controller is not used, this pin should be grounded.
MLBDAT	I/O/T in 3 pin mode. I in 5 pin mode.	High-Z	**Media Local Bus Data.** The MLBDAT line is driven by the transmitting MLB device and is received by all other MLB devices including the MLB controller. The MLBDAT line carries the actual data. In 5-pin MLB mode, this pin is an input only. When the MLB controller is not used, this pin should be grounded.
MLBSIG	I/O/T in 3 pin mode. I in 5 pin mode	High-Z	**Media Local Bus Signal.** This is a multiplexed signal which carries the Channel/Address generated by the MLB Controller, as well as the Command and RxStatus bytes from MLB devices. In 5-pin mode, this pin is input only. When the MLB controller is not used, this pin should be grounded.
MLBDO	O/T	High-Z	**Media Local Bus Data Output (in 5 Pin Mode).** This pin is used only in 5-pin MLB mode and serves as the output data pin. When the MLB controller is not used, this pin should be grounded.
MLBSO	O/T	High-Z	**Media Local Bus Signal Output (in 5 Pin Mode).** This pin is used only in 5-pin MLB mode and serves as the output signal pin. When the MLB controller is not used, this pin should be grounded.
SR_SCLK	I (ipu)		**Shift Register Serial Clock.** (Active high, rising edge sensitive)
$\overline{\text{SR\_CLR}}$	I (ipu)		**Shift Register Reset.** (Active low)
SR_SDI	I (ipu)		**Shift Register Serial Data Input.**
SR_SDO	O (ipu)	Driven Low	**Shift Register Serial Data Output.**
SR_LAT	I (ipu)		**Shift Register Latch Clock Input.** (Active high, rising edge sensitive)
SR_LDO_{17-0}	O/T (ipu)	High-Z	**Shift Register Parallel Data Output.**
RTXI	I		**RTC Crystal Input.** If RTC is not used, then this pin can be NC (no connect) or grounded and the RTC_PDN and RTC_BUSDIS bits of the RTC_INIT register must be set to 1.
RTXO	O		**RTC Crystal Output.** If RTC is not used, then this pin needs to be NC (No Connect).
RTCLKOUT	O (ipd)		**RTC Clock Output.** For calibration purposes. The clock runs at 1 Hz. If RTC is not used, then this pin needs to be NC (No Connect).

The following symbols appear in the Type column of Table 11: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be 26 kΩ to 63 kΩ. The range of an ipd resistor can be 31 kΩ to 85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.

Not all pins are available in the 88-lead LFCSP_VQ and 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 62 on Page 70.

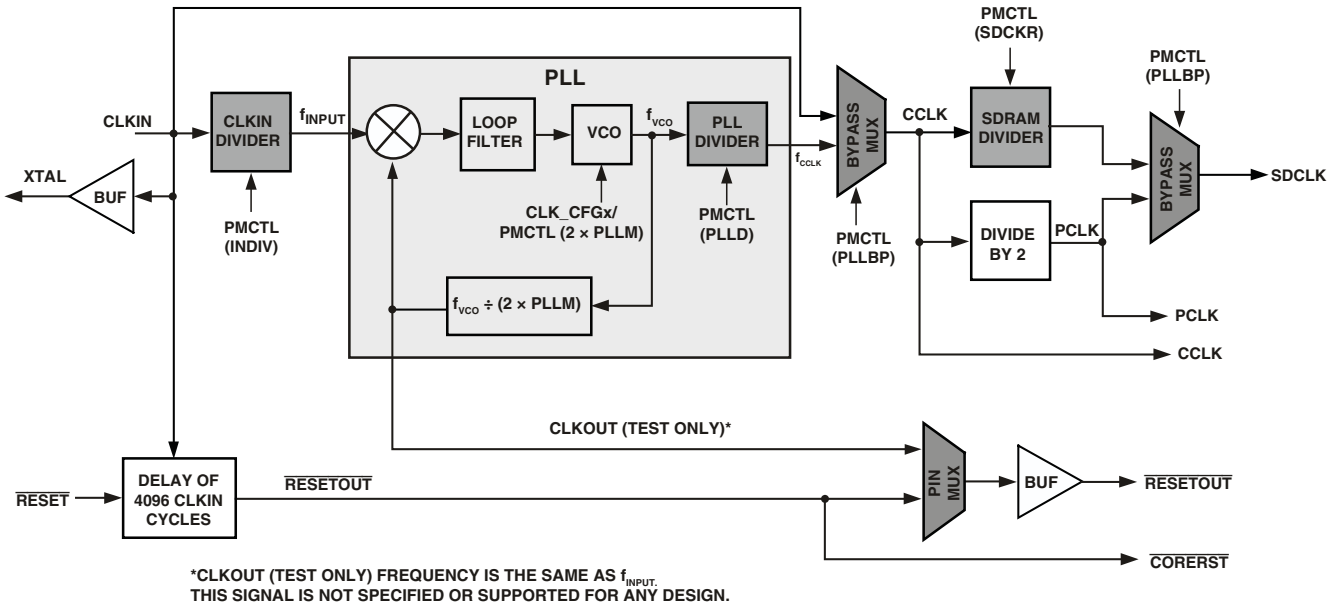

Figure 5. Core Clock and System Clock Relationship to CLKIN

Clock Signals

The processors can use an external clock or a crystal. See the CLKIN pin description in Table 11. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 8 shows the component connections used for a crystal operating in fundamental mode. Note that the clock rate is achieved using a 16.67 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 266 MHz). To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

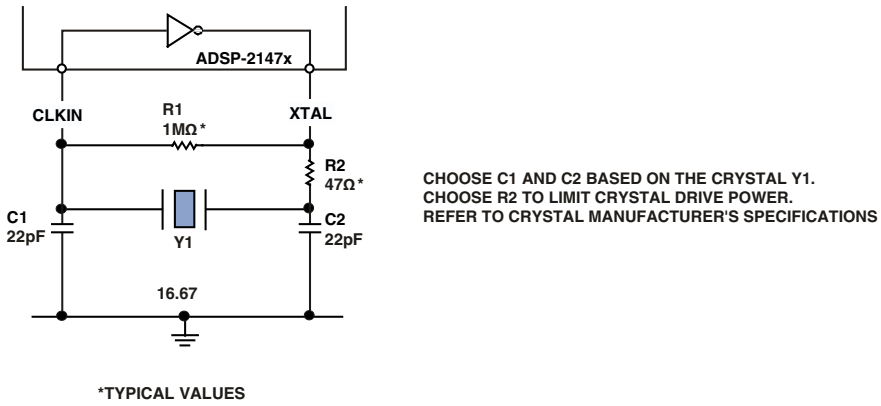

Figure 8. 266 MHz Operation (Fundamental Mode Crystal)

Reset

Table 21. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}[1]	$\overline{\text{RESET}}$ Pulse Width Low	$4 \times t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	8		ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

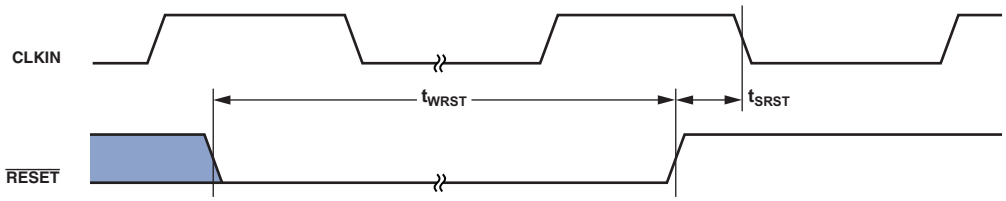

Figure 9. Reset

Timer WDTH_CAP Timing

The following timing specification applies to timer0 and timer1, and in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the timing specification provided below is valid at the DPI_P14–1 pins.

Table 26. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{PWI}	Timer Pulse Width	$2 \times t_{PCLK}$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

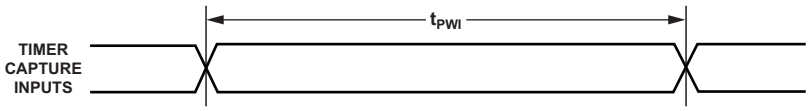

Figure 14. Timer Width Capture Timing

Watchdog Timer Timing

Table 27. Watchdog Timer Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{WDTCLKPER}$		100	1000	ns
Switching Characteristics				
t_{RST}	WDT Clock Rising Edge to Watchdog Timer $\overline{\text{RESET}}$ Falling Edge	3	7.6	ns
t_{RSTPW}	Reset Pulse Width	$64 \times t_{WDTCLKPER}$[1]		ns

[1] When the internal oscillator is used, the $1/t_{WDTCLKPER}$ varies from 1.5 MHz to 2.5 MHz and the WDT_CLKIN pin should be pulled low.

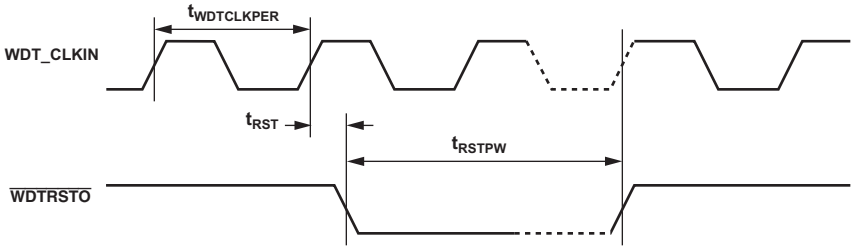

Figure 15. Watchdog Timer Timing

AMI Read

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 32. AMI Read

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}[1, 2, 3]	Address Selects Delay to Data Valid		W + t_{SDCLK} – 6.32	ns
t_{DRLD}[1, 3]	$\overline{\text{AMI\_RD}}$ Low to Data Valid		W – 3	ns
t_{SDS}[4, 5]	Data Setup to $\overline{\text{AMI\_RD}}$ High	2.6		ns
t_{HDRH}	Data Hold from $\overline{\text{AMI\_RD}}$ High	0.4		ns
t_{DAAK}[2, 6]	AMI_ACK Delay from Address Selects		t_{SDCLK} – 10 + W	ns
t_{DSAK}[4]	AMI_ACK Delay from $\overline{\text{AMI\_RD}}$ Low		W – 7.0	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{\text{AMI\_RD}}$ High	RHC + 0.38		ns
t_{DARL}[2]	Address Selects to $\overline{\text{AMI\_RD}}$ Low	t_{SDCLK} – 5		ns
t_{RW}	$\overline{\text{AMI\_RD}}$ Pulse Width	W – 1.4		ns
t_{RWR}	$\overline{\text{AMI\_RD}}$ High to $\overline{\text{AMI\_RD}}$ Low	HI + t_{SDCLK} – 1.2		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
RHC = (number of Read Hold Cycles specified in AMICTLx register) × t_{SDCLK}
Where PREDIS = 0
HI = RHC (if IC = 0): Read to Read from same bank
HI = RHC+ t_{SDCLK} (if IC > 0): Read to Read from same bank
HI = RHC + IC: Read to Read from different bank
HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank
Where PREDIS = 1
HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank
HI = RHC + (3 × t_{SDCLK}): Read to Read from same bank
HI = RHC + Max (IC, (3 × t_{SDCLK})): Read to Read from different bank
IC = (number of idle cycles specified in AMICTLx register) × t_{SDCLK}
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}.

[1] Data delay/setup: System must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{\text{AMI_MS}}$x, is referenced.
[3] The maximum limit of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.
[4] Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.
[5] Data hold: User must meet t_{HDRH} in asynchronous access mode. See Test Conditions for the calculation of hold times given capacitive and dc loads.
[6] AMI_ACK delay/setup: User must meet t_{daak}, or t_{dsak}, for deassertion of AMI_ACK (low).

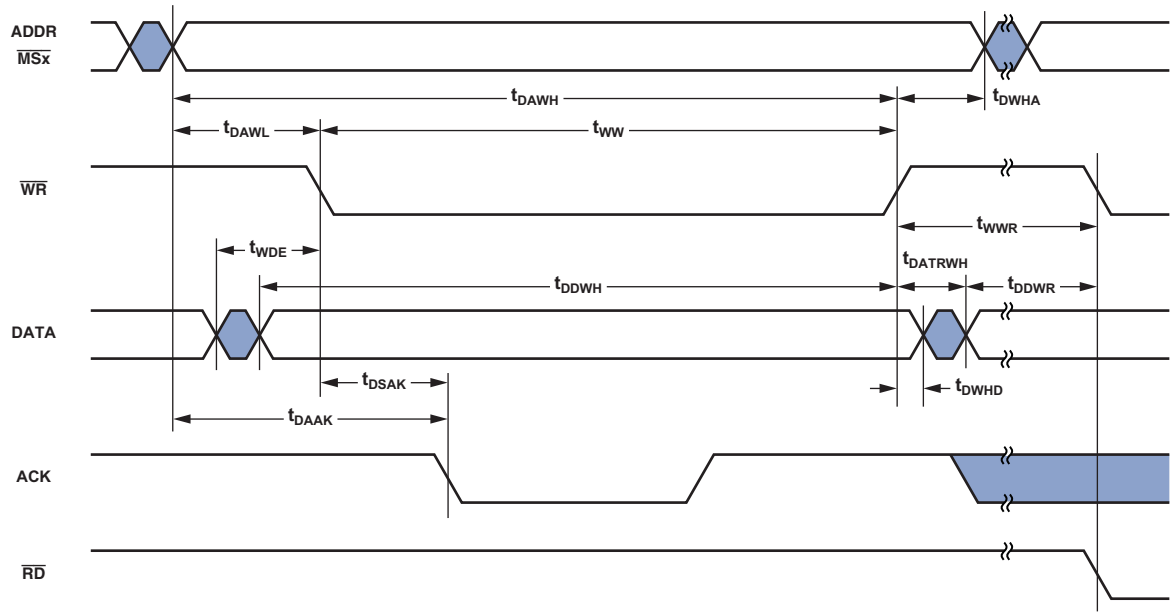

Figure 21. AMI Write

The SPORTx_TDV_O output signal (routing unit) becomes active in SPORT multichannel/packed mode. During transmit slots (enabled with active channel selection registers), the SPORTx_TDV_O is asserted for communication with external devices.

Table 38. Serial Ports—TDV (Transmit Data Valid)

Parameter		88-Lead LFCSP Package		All Other Packages		Unit
		Min	Max	Min	Max	
Switching Characteristics[1]						
t_{DRDVEN}	TDV Assertion Delay from Drive Edge of External Clock	3		3		ns
t_{DFDVEN}	TDV Deassertion Delay from Drive Edge of External Clock		$2 \times t_{PCLK}$		13.25	ns
t_{DRDVIN}	TDV Assertion Delay from Drive Edge of Internal Clock	–0.1		–0.1		ns
t_{DFDVIN}	TDV Deassertion Delay from Drive Edge of Internal Clock		3.5		3.5	ns

[1] Referenced to drive edge.

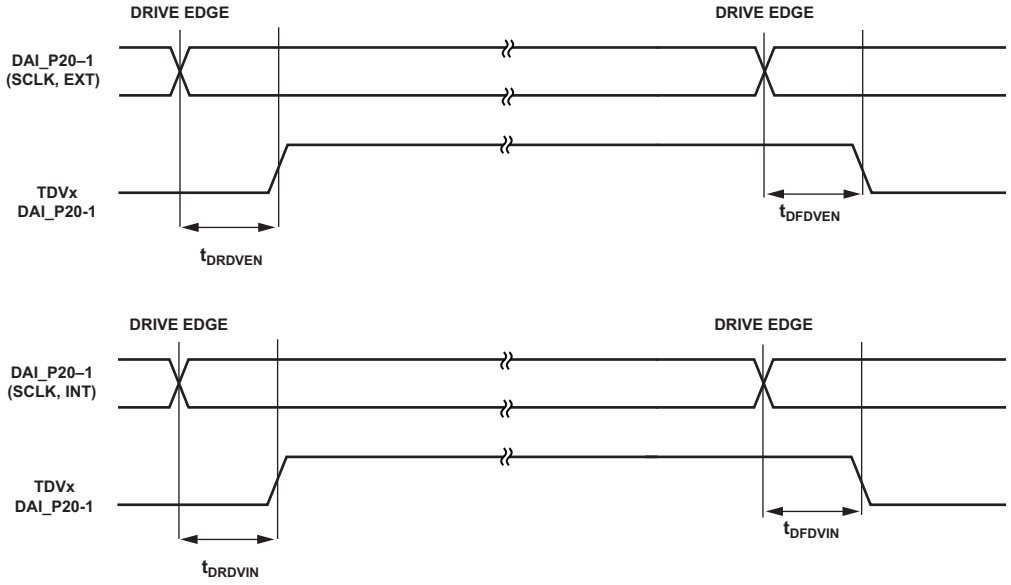

Figure 25. Serial Ports—TDV Internal and External Clock

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left-justified, I²S, or right-justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 31 shows the right-justified mode. Frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed the minimum in 24-bit output mode or the maximum in 16-bit output mode from a frame sync transition, so that when there are 64 serial clock periods per frame sync period, the LSB of the data is right-justified to the next frame sync transition.

Figure 32 shows the default I²S-justified mode. The frame sync is low for the left channel and high for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition but with a delay.

Table 44. S/PDIF Transmitter Right-Justified Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{RJD}	FS to MSB Delay in Right-Justified Mode		
	16-Bit Word Mode	16	SCLK
	18-Bit Word Mode	14	SCLK
	20-Bit Word Mode	12	SCLK
	24-Bit Word Mode	8	SCLK

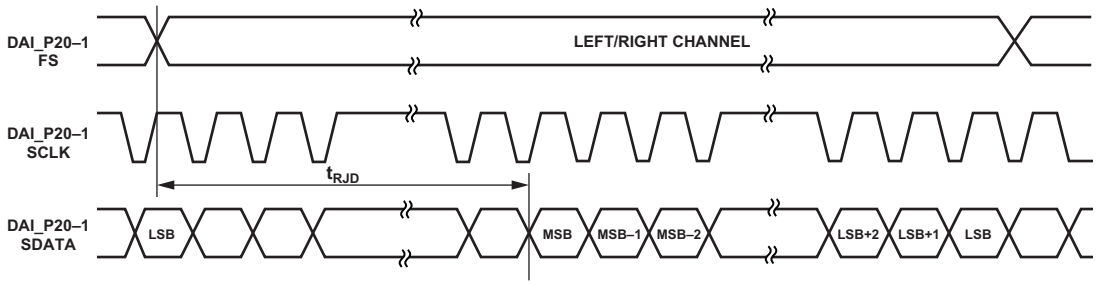

Figure 31. Right-Justified Mode

Table 45. S/PDIF Transmitter I²S Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{I2SD}	FS to MSB Delay in I²S Mode	1	SCLK

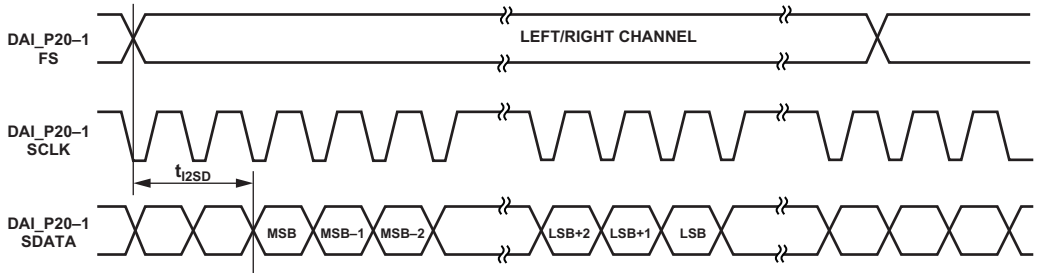

Figure 32. I²S-Justified Mode

Figure 33 shows the left-justified mode. The frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition with no delay.

Table 46. S/PDIF Transmitter Left-Justified Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{LJD}	FS to MSB Delay in Left-Justified Mode	0	SCLK

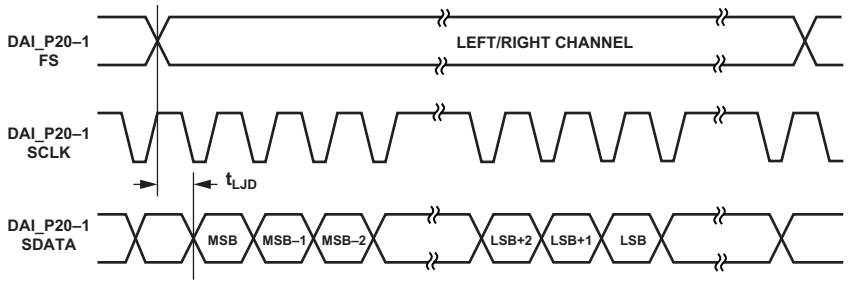

Figure 33. Left-Justified Mode

Media Local Bus

All the numbers given are applicable for all speed modes (1024 FS, 512 FS, and 256 FS for 3-pin; 512 FS and 256 FS for 5-pin) unless otherwise specified. Please refer to MediaLB specification document rev 3.0 for more details.

Table 52. MLB Interface, 3-Pin Specifications

Parameter		Min	Typ	Max	Unit
3-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	1024 FS		20.3		ns
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	1024 FS	6.1			ns
	512 FS	14			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	1024 FS	9.3			ns
	512 FS	14			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})				
	1024 FS			1	ns
	512 FS/256 FS			3	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})				
	1024 FS			1	ns
	512 FS/256 FS			3	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation				
	1024 FS			0.7	ns p-p
	512 FS/256			2.0	ns p-p
t_{DSMCF}	DAT/SIG Input Setup Time	1			ns
t_{DHMCF}	DAT/SIG Input Hold Time	1.2			ns
t_{MCFDZ}	DAT/SIG Output Time to Three-State	0		15	ns
t_{MCDRV}	DAT/SIG Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MDZH}[2]	Bus Hold Time				
	1024 FS	2			ns
	512 FS/256	4			ns
C_{MLB}	DAT/SIG Pin Load				
	1024 FS			40	pf
	512 FS/256			60	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (p-p).
[2] The board must be designed to ensure that the high impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

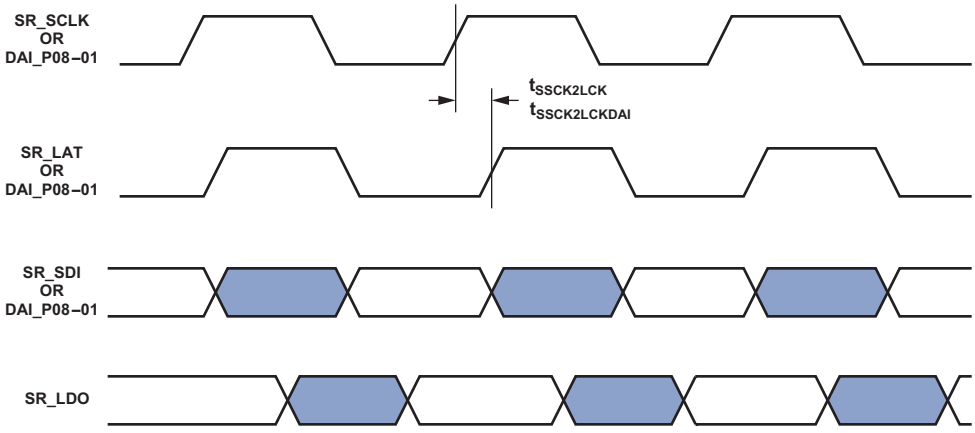

Figure 44. SR_SCLK to SR_LAT Setup, Clocks Pulse Width and Maximum Frequency

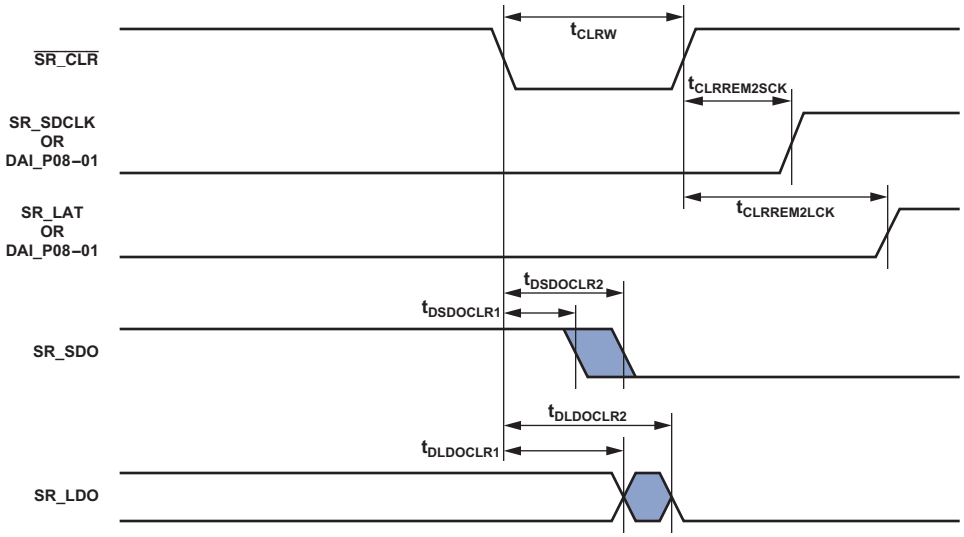

Figure 45. Shift Register Reset Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the *ADSP-214xx SHARC Hardware Reference Manual*.

2-Wire Interface (TWI)—Receive and Transmit Timing

For information on the TWI receive and transmit operations, see the *ADSP-214xx SHARC Hardware Reference Manual*.

JTAG Test Access Port and Emulation

Table 55. JTAG Test Access Port and Emulation

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{TCK}	TCK Period	20		20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		$4 \times t_{CK}$		ns
Switching Characteristics						
t_{DTDO}	TDO Delay from TCK Low		11.5		10.5	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = DATA15–0, CLK_CFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, DAI_Px, DPI_Px, FLAG3–0, MLBCLK, MLBDAT, MLBSIG, SR_SCLK, $\overline{\text{SR_CLR}}$, SR_SDI, and SR_LAT.

[2] System Outputs = DAI_Px, DPI_Px, ADDR23–0, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, FLAG3–0, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, SDCKE, SDA10, SDDQM, SDCLK, MLBDAT, MLBSIG, MLBDO, MLBSO, SR_SDO, SR_LDO, and $\overline{\text{EMU}}$.

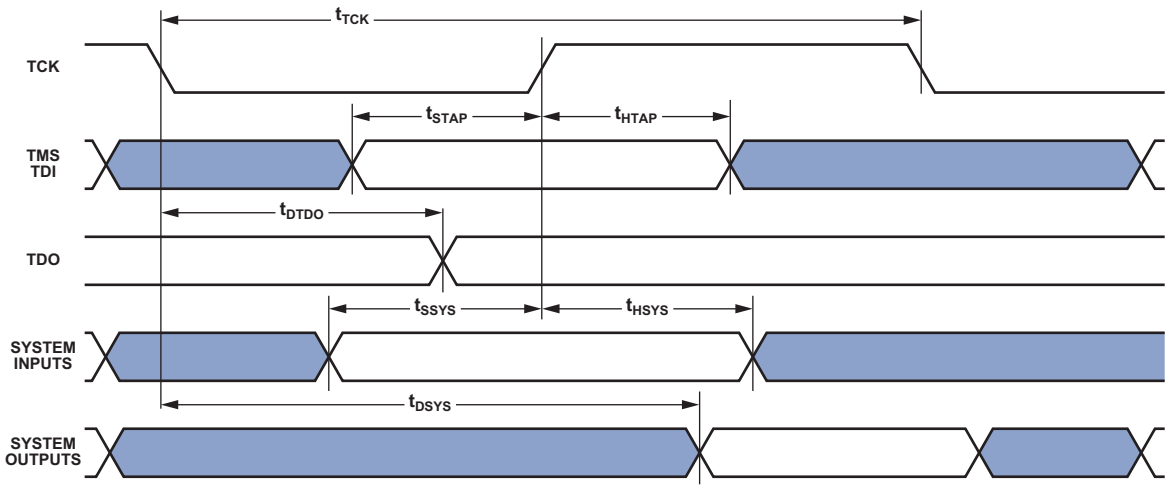

Figure 46. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Table 56 shows the driver types and the pins associated with each driver. Figure 47 shows typical I-V characteristics for each driver. The curves represent the current drive capability of the output drivers as a function of output voltage.

Table 56. Driver Types

Driver Type	Associated Pins
A	FLAG[0–3], AMI_ADDR[23–0], DATA[15–0], $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, AMI_ACK, $\overline{\text{MS}}$[1-0], $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, SDDQM, SDCKE, SDA10, $\overline{\text{EMU}}$, TDO, $\overline{\text{RESETOUT}}$, DPI[1–14], DAI[1–20], $\overline{\text{WDTRSTO}}$, MLBDAT, MLBSIG, MLBSO, MLBDO, MLBCLK, $\overline{\text{SR\_CLR}}$, SR_LAT, SR_LDO[17–0], SR_SCLK, SR_SDI
B	SDCLK, RTCLKOUT

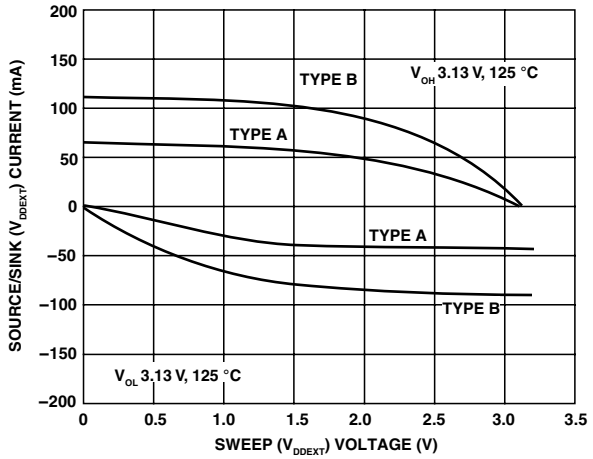

Figure 47. Typical Drive at Junction Temperature

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 21 through Table 55. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 48.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 49. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

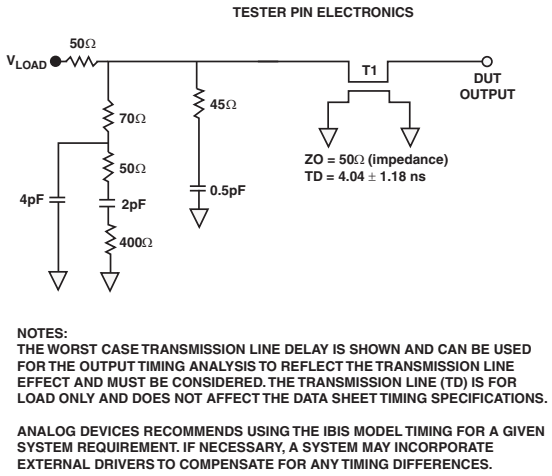

Figure 48. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

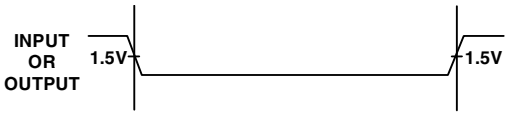

Figure 49. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 48). Figure 52 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 50, Figure 51, and Figure 52 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

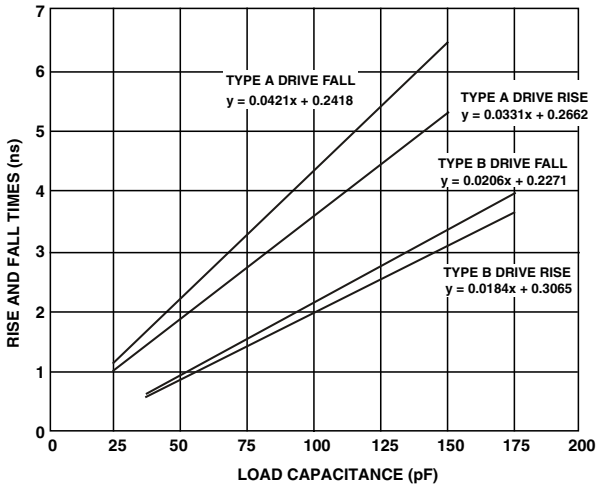

Figure 50. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Max)

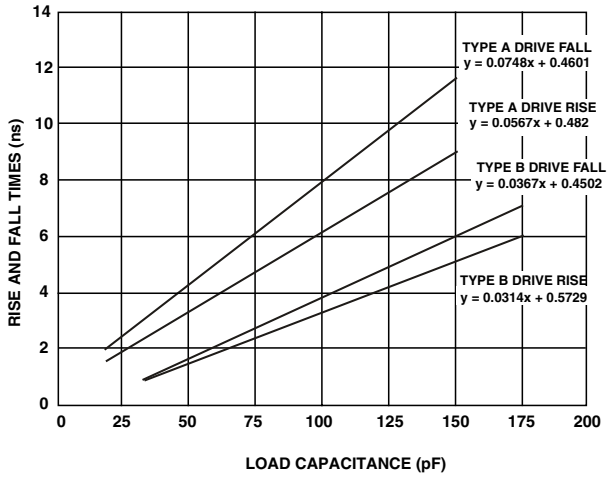

Figure 51. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Min)

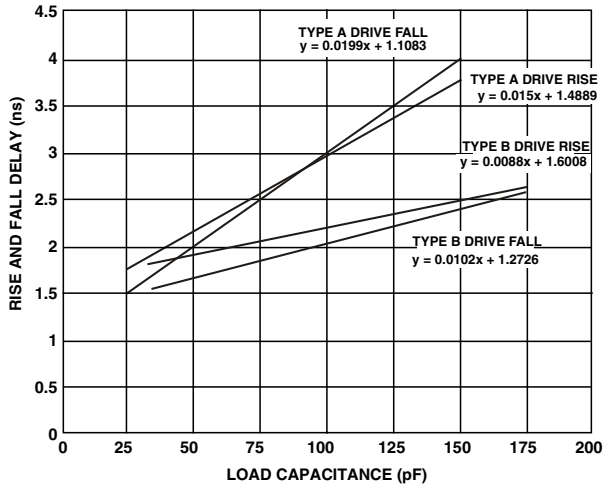

Figure 52. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

THERMAL CHARACTERISTICS

The processor is rated for performance over the temperature range specified in Operating Conditions.

Table 58 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-7 (PBGA). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the typical value from Table 58

P_D = power dissipation

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

Note that the thermal characteristics values provided in Table 58 are modeled values.

Table 57. Thermal Characteristics for 88-Lead LFCSP_VQ

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	22.6	°C/W
θ_{JMA}	Airflow = 1 m/s	18.2	°C/W
θ_{JMA}	Airflow = 2 m/s	17.3	°C/W
θ_{JC}		7.9	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.22	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.36	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.44	°C/W

Table 58. Thermal Characteristics for 100-Lead LQFP_EP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	18.1	°C/W
θ_{JMA}	Airflow = 1 m/s	15.5	°C/W
θ_{JMA}	Airflow = 2 m/s	14.6	°C/W
θ_{JC}		2.4	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.22	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.36	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.50	°C/W

Table 59. Thermal Characteristics for 196-Ball CSP_BGA

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	29.0	°C/W
θ_{JMA}	Airflow = 1 m/s	26.1	°C/W
θ_{JMA}	Airflow = 2 m/s	25.1	°C/W
θ_{JC}		8.8	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.23	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.42	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.52	°C/W

Thermal Diode

The processors incorporate thermal diode/s to monitor the die temperature. The thermal diode is a grounded collector, PNP bipolar junction transistor (BJT). The THD_P pin is connected to the emitter, and the THD_M pin is connected to the base of the transistor. These pins can be used by an external temperature sensor (such as ADM1021A or LM86 or others) to read the die temperature of the chip.

The technique used by the external temperature sensor is to measure the change in VBE when the thermal diode is operated at two different currents. This is shown in the following equation:

$$\Delta V_{BE} = n \times \frac{kT}{q} \times ln(N)$$

where:

n = multiplication factor close to 1, depending on process variations

k = Boltzmann constant

T = temperature (°C)

q = charge of the electron

N = ratio of the two currents

The two currents are usually in the range of 10 µA to 300 µA for the common temperature sensor chips available.

Table 60 contains the thermal diode specifications using the transistor model.

Table 60. Thermal Diode Parameters—Transistor Model[1]

Symbol	Parameter	Min	Typ	Max	Unit
I_{FW}[2]	Forward Bias Current	10		300	µA
I_E	Emitter Current	10		300	µA
n_Q[3, 4]	Transistor Ideality	1.012	1.015	1.017	
R_T[3, 5]	Series Resistance	0.12	0.2	0.28	Ω

[1] Analog Devices does not recommend operation of the thermal diode under reverse bias.
[2] Analog Devices does not recommend operation of the thermal diode under reverse bias.
[3] Specified by design characterization.
[4] The ideality factor, nQ, represents the deviation from ideal diode behavior as exemplified by the diode equation: $I_C = I_S \times (e^{qVBE/nqkT} - 1)$ where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the diode, k = Boltzmann constant, and T = absolute temperature (Kelvin).
[5] The series resistance (R_T) can be used for more accurate readings as needed.

88-LFCSP_VQ LEAD ASSIGNMENT

Table 61 lists the 88-Lead LFCSP_VQ package lead names.

Table 61. 88-Lead LFCSP_VQ Lead Assignments (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
CLK_CFG1	1	V_{DD_EXT}	23	DAI_P10	45	V_{DD_INT}	67
BOOT_CFG0	2	DPI_P08	24	V_{DD_INT}	46	FLAG0	68
V_{DD_EXT}	3	DPI_P07	25	V_{DD_EXT}	47	V_{DD_INT}	69
V_{DD_INT}	4	DPI_P09	26	DAI_P20	48	FLAG1	70
BOOT_CFG1	5	DPI_P10	27	V_{DD_INT}	49	FLAG2	71
GND	6	DPI_P11	28	DAI_P08	50	FLAG3	72
CLK_CFG0	7	DPI_P12	29	DAI_P04	51	GND	73
V_{DD_INT}	8	DPI_P13	30	DAI_P14	52	GND	74
CLKIN	9	DAI_P03	31	DAI_P18	53	V_{DD_EXT}	75
XTAL	10	DPI_P14	32	DAI_P17	54	GND	76
V_{DD_EXT}	11	V_{DD_INT}	33	DAI_P16	55	V_{DD_INT}	77
V_{DD_INT}	12	DAI_P13	34	DAI_P15	56	$\overline{TRST}$	78
V_{DD_INT}	13	DAI_P07	35	DAI_P12	57	$\overline{EMU}$	79
$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	14	DAI_P19	36	DAI_P11	58	TDO	80
V_{DD_INT}	15	DAI_P01	37	V_{DD_INT}	59	V_{DD_EXT}	81
DPI_P01	16	DAI_P02	38	GND	60	V_{DD_INT}	82
DPI_P02	17	V_{DD_INT}	39	THD_M	61	TDI	83
DPI_P03	18	V_{DD_EXT}	40	THD_P	62	TCK	84
V_{DD_INT}	19	V_{DD_INT}	41	V_{DD_THD}	63	V_{DD_INT}	85
DPI_P05	20	DAI_P06	42	V_{DD_INT}	64	$\overline{RESET}$	86
DPI_P04	21	DAI_P05	43	V_{DD_INT}	65	TMS	87
DPI_P06	22	DAI_P09	44	V_{DD_INT}	66	V_{DD_INT}	88
						GND	89*

* Lead no. 89 is the GND supply (see Figure 53 and Figure 54) for the processor; this pad must be **robustly** connected to GND in order for the processor to function.

SURFACE-MOUNT DESIGN

For industry-standard design recommendations, refer to IPC-7351, Generic Requirements for Surface-Mount Design and Land Pattern Standard.

AUTOMOTIVE PRODUCTS

The ADSP-21477, ADSP-21478, and ADSP-21479 are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models, and designers should review the product Specifications section of this data sheet carefully.

Only the automotive grade products shown in Table 64 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 64. Automotive Product Models

Model[1]	Temperature Range[2]	On-Chip SRAM	Processor Instruction Rate (Max)	Package Description	Package Option	Notes
AD21477WYCPZ1Axx	–40°C to +105°C	2M bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5	
AD21477WYSWZ1Axx	–40°C to +105°C	2M bits	200 MHz	100-Lead LQFP_EP	SW-100-2	
AD21478WYBCZ2Axx	–40°C to +105°C	3M bits	200 MHz	196-Ball CSP_BGA	BC-196-8	
AD21478WYCPZ1Axx	–40°C to +105°C	3M bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5	
AD21478WYSWZ2Axx	–40°C to +105°C	3M bits	266 MHz	100-Lead LQFP_EP	SW-100-2	
AD21478WYSWZ2Bxx	–40°C to +105°C	3M bits	266 MHz	100-Lead LQFP_EP	SW-100-2	3, 4
AD21479WYCPZ1Axx	–40°C to +105°C	5M bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5	
AD21479WYCPZ1Bxx	–40°C to +105°C	5M bits	200MHz	88-Lead LFCSP_VQ	CP-88-5	3, 4
AD21479WYSWZ2Axx	–40°C to +105°C	5M bits	266 MHz	100-Lead LQFP_EP	SW-100-2	
AD21479WYSWZ2Bxx	–40°C to +105°C	5M bits	266 MHz	100-Lead LQFP_EP	SW-100-2	3, 4

[1] Z = RoHS compliant part.
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions for junction temperature (T_J) specification, which is the only temperature specification.
[3] Contains multichannel audio decoders from Dolby and DTS. Users must have current licenses from Dolby and DTS to order this product.
[4] Contains Digital Transmission Content Protection (DTCP) from DTLA. User must have current license from DTLA to order this product.

ORDERING GUIDE

Model[1]	Temperature Range[2]	On-Chip SRAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21477KCPZ-1A	0°C to +70°C	2M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21477KSWZ-1A	0°C to +70°C	2M Bits	200 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21477BCPZ-1A	–40°C to +85°C	2M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21478KCPZ-1A	0°C to +70°C	3M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21478BCPZ-1A	–40°C to +85°C	3M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21478BBCZ-2A	–40°C to +85°C	3M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478BSWZ-2A	–40°C to +85°C	3M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21478KBCZ-1A	0°C to +70°C	3M Bits	200 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478KBCZ-2A	0°C to +70°C	3M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478KBCZ-3A	0°C to +70°C	3M Bits	300 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478KSWZ-1A	0°C to +70°C	3M Bits	200 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21478KSWZ-2A	0°C to +70°C	3M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21479KCPZ-1A	0°C to +70°C	5M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21479BCPZ-1A	–40°C to +85°C	5M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21479BBCZ-2A	–40°C to +85°C	5M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479BSWZ-2A	–40°C to +85°C	5M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21479KBCZ-1A	0°C to +70°C	5M Bits	200 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479KBCZ-2A	0°C to +70°C	5M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479KBCZ-3A	0°C to +70°C	5M Bits	300 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479KSWZ-1A	0°C to +70°C	5M Bits	200 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21479KSWZ-2A	0°C to +70°C	5M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2

[1] Z =RoHS compliant part.
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions for junction temperature (T_J) specification, which is the only temperature specification.