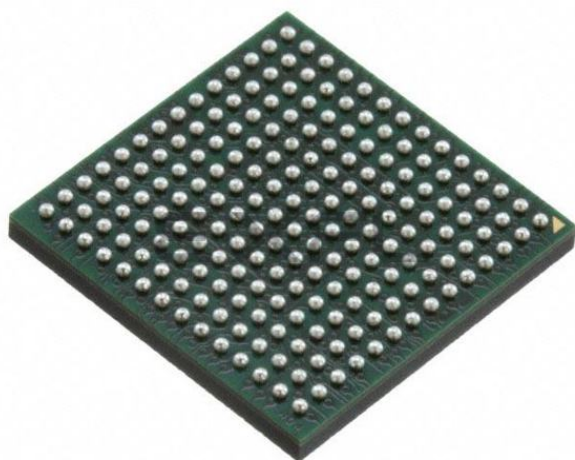




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Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

Details

Product Status	Active
Type	Floating Point
Interface	DAI, DPI, EBI/EMI, I ² C, SPI, SPORT, UART/USART
Clock Rate	200MHz
Non-Volatile Memory	ROM (4Mbit)
On-Chip RAM	3Mbit
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LFBGA, CSPBGA
Supplier Device Package	196-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21478kbcz-1a

ADSP-21477/ADSP-21478/ADSP-21479

TABLE OF CONTENTS

General Description	3	Absolute Maximum Ratings	24
Family Core Architecture	4	Timing Specifications	25
Family Peripheral Architecture	8	Output Drive Currents	65
I/O Processor Features	12	Test Conditions	65
System Design	13	Capacitive Loading	65
Development Tools	13	Thermal Characteristics	66
Additional Information	15	88-LFCSP_VQ Lead Assignment	68
Related Signal Chains	15	100-LQFP_EP Lead Assignment	70
Pin Function Descriptions	16	196-BGA Ball Assignment	72
Specifications	21	Outline Dimensions	73
Operating Conditions	21	Surface-Mount Design	75
Electrical Characteristics	22	Automotive Products	75
Maximum Power Dissipation	24	Ordering Guide	76
Package Information	24		
ESD Sensitivity	24		

REVISION HISTORY

4/2017—Rev. C to Rev. D

Change to RTXI Description in Table 11 of Pin Function Descriptions	16
Changes to Operating Conditions	21
Change to Figure 5 of Core Clock Requirements	25
Changes to AMI Read	37
Change to t_{WDE} Switching Characteristic in AMI Write ...	39
Change to Table 64 of Automotive Products	75

PRODUCT APPLICATION RESTRICTION

Not for use in in-vivo applications for body fluid constituent monitoring, including monitoring one or more of the components that form, or may be a part of, or contaminate human blood or other body fluids, such as, but not limited to, carboxyhemoglobin, methemoglobin total hemoglobin, oxygen saturation, oxygen content, fractional arterial oxygen saturation, bilirubin, glucose, drugs, lipids, water, protein, and pH.

buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

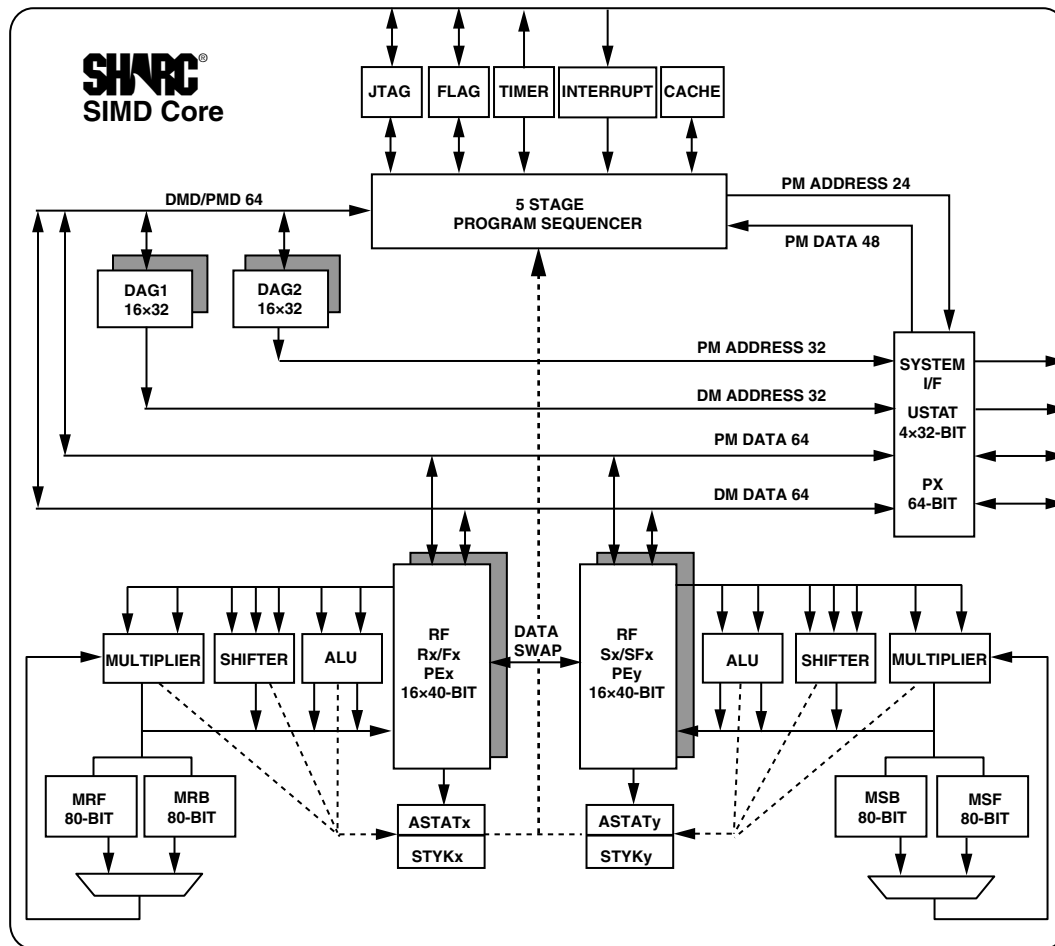


Figure 2. SHARC Core Block Diagram

Instruction Cache

The processor includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full speed execution of core looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators with Zero-Overhead Hardware Circular Buffer Support

The processor's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the processors contain sufficient registers to allow the creation of up to 32 circular buffers (16

primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the processors can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

Variable Instruction Set Architecture (VISA)

In addition to supporting the standard 48-bit instructions from previous SHARC processors, the processors support new instructions of 16 and 32 bits. This feature, called Variable Instruction Set Architecture (VISA), drops redundant/unused

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface ports (SPI), one universal asynchronous receiver-transmitter (UART), 12 flags, a 2-wire interface (TWI), three PWM modules (PWM3–1), and two general-purpose timers.

Serial Peripheral (Compatible) Interface (SPI)

The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible port to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multi-master environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The SPI-compatible port uses open drain drivers to support a multi-master configuration and to avoid data contention.

UART Port

The processors provide a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Support for bit rates ranging from ($f_{\text{CLK}}/1,048,576$) to ($f_{\text{CLK}}/16$) bits per second.
- Support for data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

In conjunction with the general-purpose timer functions, auto-baud detection is supported.

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs generating 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

PWM signals can be mapped to the external port address lines or to the DPI pins.

Timers

The processors have a total of three timers: a core timer that can generate periodic software interrupts and two general-purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watch dog mode

The core timer can be configured to use FLAG3 as a timer expired signal, and the general-purpose timers have one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables the general-purpose timer.

2-Wire Interface Port (TWI)

The TWI is a bidirectional 2-wire serial bus used to move 8-bit data while maintaining compliance with the I²C bus protocol. The TWI master incorporates the following features:

- 7-bit addressing
- Simultaneous master and slave operation on multiple device systems with support for multi-master data arbitration
- Digital filtering and timed event processing
- 100 kbps and 400 kbps data rates
- Low interrupt rate

ADSP-21477/ADSP-21478/ADSP-21479

Shift Register

The shift register can be used as a serial to parallel data converter. The shift register module consists of an 18-stage serial shift register, 18-bit latch, and three-state output buffers. The shift register and latch have separate clocks. Data is shifted into the serial shift register on the positive-going transitions of the shift register serial clock (SR_SCLK) input. The data in each flip-flop is transferred to the respective latch on a positive-going transition of the shift register latch clock (SR_LAT) input.

The shift register's signals can be configured as follows.

- The SR_SCLK can come from any of the SPORT0–7 SCLK outputs, PCGA/B clock, any of the DAI pins (1–8), and one dedicated pin (SR_SCLK).
- The SR_LAT can come from any of SPORT0–7 frame sync outputs, PCGA/B frame sync, any of the DAI pins (1–8), and one dedicated pin (SR_LAT).
- The SR_SDI input can from any of SPORT0–7 serial data outputs, any of the DAI pins (1–8), and one dedicated pin (SR_SDI).

Note that the SR_SCLK, SR_LAT, and SR_SDI inputs must come from same source except in the case of where SR_SCLK comes from PCGA/B or SR_SCLK and SR_LAT come from PCGA/B.

If SR_SCLK comes from PCGA/B, then SPORT0–7 generates the SR_LAT and SR_SDI signals. If SR_SCLK and SR_LAT come from PCGA/B, then SPORT0–7 generates the SR_SDI signal.

I/O PROCESSOR FEATURES

The I/O processor provides up to 65 channels of DMA as well as an extensive set of peripherals.

DMA Controller

The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the processor's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP) or the UART.

Up to 65 channels of DMA are available on the processors as shown in [Table 9](#).

Programs can be downloaded using DMA transfers. Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

Table 9. DMA Channels

Peripheral	DMA Channels
SPORTs	16
PDAP	8
SPI	2
UART	2

Table 9. DMA Channels (Continued)

Peripheral	DMA Channels
External Port	2
Accelerators	2
Memory-to-Memory	2
MediaLB ¹	31

¹ Automotive models only.

Delay Line DMA

The processor provides delay line DMA functionality. This allows processor reads and writes to external delay line buffers (and therefore to external memory) with limited core interaction.

Scatter/Gather DMA

The processor provides scatter/gather DMA functionality. This allows processor DMA reads/writes to/from noncontiguous memory blocks.

FFT Accelerator

The FFT accelerator implements radix-2 complex/real input, complex output FFTs with no core intervention. The FFT accelerator runs at the peripheral clock frequency.

FIR Accelerator

The FIR (finite impulse response) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency.

IIR Accelerator

The IIR (infinite impulse response) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency.

Watchdog Timer (WDT)

The processors include a 32-bit watchdog timer that can be used to implement a software watchdog function. A software watchdog can improve system reliability by forcing the processor to a known state through generation of a system reset if the timer expires before being reloaded by software. Software initializes the count value of the timer, and then enables the timer.

The WDT is used to supervise the stability of the system software. When used in this way, software reloads the WDT in a regular manner so that the downward counting timer never expires. An expiring timer then indicates that system software might be out of control.

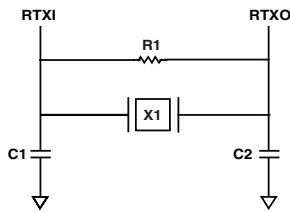
The WDT resets both the core and the internal peripherals. Software must be able to determine if the watch dog was the source of the hardware reset by interrogating a status bit in the watch dog timer control register.

The watch dog timer also has an internal RC oscillator that can be used as the clock source. The internal RC oscillator can be used as an optional alternative to using an external clock applied to the WDT_CLIN pin.

Real-Time Clock

The real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the SHARC processor. Connect RTC pins RTXI and RTXO with external components as shown in Figure 3.

The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time. An RTCLKOUT signal that operates at 1 Hz is also provided for calibration.



NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. C1 AND C2 SPECIFICATIONS ASSUME BOARD TRACE CAPACITANCE OF 3 pF.

Figure 3. External Components for RTC

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and a 32,768-day counter. When the alarm interrupt is enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms: The first alarm is for a time of day. The second alarm is for a day and time of that day.

The stopwatch function counts down from a programmed value, with one-second resolution. When the stopwatch interrupt is enabled and the counter underflows, an interrupt is generated.

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory boots at system power-up from an 8-bit EPROM via the external port, an SPI master, or an SPI slave. Booting is determined by the boot configuration (BOOT_CFG2-0) pins in Table 10.

Table 10. Boot Mode Selection

BOOT_CFG2-0 ¹	Booting Mode
000	SPI Slave Boot
001	SPI Master Boot (from Flash and Other Slaves)
010	AMI User Boot (for 8-bit Flash Boot)
011	No Boot (Processor Executes from Internal ROM After Reset)
100	Reserved
1xx	Reserved

¹ The BOOT_CFG2 pin is not available on the 100-lead or 88-lead packages.

A running reset feature is used to reset the processor core and peripherals without resetting the PLL and SDRAM controller, or performing a boot. The functionality of the RESETOUT /RUNRSTIN pin has now been extended to also act as the input for initiating a running reset. For more information, see the ADSP-214xx SHARC Processor Hardware Reference.

Power Supplies

The processors have separate power supply connections for the internal (V_{DD_INT}) and external (V_{DD_EXT}) power supplies. The internal and analog supplies must meet the V_{DD_INT} specifications. The external supply must meet the V_{DD_EXT} specification. All external supply pins must be connected to the same power supply.

To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DD_INT} and GND.

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the processors to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate emulator hardware user's guide.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio

ADSP-21477/ADSP-21478/ADSP-21479

seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on “ezkit” or “ezextender”.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is

located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2147x architecture and functionality. For detailed information on the family core architecture and instruction set, refer to the *SHARC Processor Programming Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Reference Designs page provides a link to Circuits from the Lab™ (www.analog.com/signal-chains) which contains:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

ADSP-21477/ADSP-21478/ADSP-21479

PIN FUNCTION DESCRIPTIONS

Table 11. Pin Descriptions

Name	Type	State During/ After Reset	Description
ADDR ₂₃₋₀	I/O/T (ipu)	High-Z/driven low (boot)	External Address. The processor outputs addresses for external memory and peripherals on these pins. The ADDR pins can be multiplexed to support the external memory interface address, FLAGS ₁₅₋₈ (I/O) and PWM (O). After reset, all ADDR pins are in EMIF mode, and FLAG(0-3) pins are in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the ADDR ₂₃₋₄ pins for parallel input data.
DATA ₁₅₋₀	I/O/T (ipu)	High-Z	External Data. The data pins can be multiplexed to support the external memory interface data (I/O) and FLAGS ₇₋₀ (I/O).
AMI_ACK	I (ipu)		Memory Acknowledge. External devices can deassert AMI_ACK (low) to add wait states to an external memory access. AMI_ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{MS}_{0-1}$	O/T (ipu)	High-Z	Memory Select Lines 0-1. These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{1-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, when the condition evaluates as true. The $\overline{MS}_1$ pin can be used in EPORT/FLASH boot mode. For more information on processor booting, see the ADSP-214xx SHARC Processor Hardware Reference.
$\overline{AMI_RD}$	O/T (ipu)	High-Z	AMI Port Read Enable. $\overline{AMI_RD}$ is asserted whenever the processor reads a word from external memory.
$\overline{AMI_WR}$	O/T (ipu)	High-Z	AMI Port Write Enable. $\overline{AMI_WR}$ is asserted when the processor writes a word to external memory.
FLAG0/ $\overline{IRQ0}$	I/O (ipu)	FLAG[0] INPUT	FLAG0/Interrupt Request0.
FLAG1/ $\overline{IRQ1}$	I/O (ipu)	FLAG[1] INPUT	FLAG1/Interrupt Request1.
FLAG2/ $\overline{IRQ2}/\overline{MS2}$	I/O (ipu)	FLAG[2] INPUT	FLAG2/Interrupt Request2/Memory Select2. This pin is multiplexed with $\overline{MS2}$ in the 196-ball BGA package only.
FLAG3/TMREXP/ $\overline{MS3}$	I/O (ipu)	FLAG[3] INPUT	FLAG3/Timer Expired/Memory Select3. This pin is multiplexed with $\overline{MS3}$ in the 196-ball BGA package only.

The following symbols appear in the Type column of Table 11: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be 26 k Ω to 63 k Ω . The range of an ipd resistor can be 31 k Ω to 85 k Ω . The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.

Not all pins are available in the 88-lead LFCSP_VQ and 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 62 on Page 70.

ADSP-21477/ADSP-21478/ADSP-21479

Table 12. Pin List, Power and Ground

Name	Type	Description
V _{DD_INT}	P	Internal Power Supply.
V _{DD_EXT}	P	I/O Power Supply.
V _{DD_RTC}	P	Real-Time Clock Power Supply. When RTC is not used, this pin should be connected to V _{DD_EXT} .
GND ¹	G	Ground.
V _{DD_THD}	P	Thermal Diode Power Supply. When not used, this pin can be left floating.

¹The exposed pad is required to be electrically and thermally connected to GND. Implement this by soldering the exposed pad to a GND PCB land that is the same size as the exposed pad. The GND PCB land should be *robustly* connected to the GND plane in the PCB for best electrical and thermal performance. See also [88-LFCSP_VQ Lead Assignment](#) and [100-LQFP_EP Lead Assignment](#).

ADSP-21477/ADSP-21478/ADSP-21479

ELECTRICAL CHARACTERISTICS

Parameter ¹	Description	Test Conditions	200 MHz		266 MHz		300 MHz		Unit
			Min	Max	Min	Max	Min	Max	
V_{OH}^2	High Level Output Voltage	@ $V_{DD_EXT} = \text{Min}$, $I_{OH} = -1.0 \text{ mA}^3$	2.4		2.4		2.4		V
V_{OL}^2	Low Level Output Voltage	@ $V_{DD_EXT} = \text{Min}$, $I_{OL} = 1.0 \text{ mA}^3$		0.4		0.4		0.4	V
$I_{IH}^{4,5}$	High Level Input Current	@ $V_{DD_EXT} = \text{Max}$, $V_{IN} = V_{DD_EXT} \text{ Max}$		10		10		10	μA
I_{IL}^4	Low Level Input Current	@ $V_{DD_EXT} = \text{Max}$, $V_{IN} = 0 \text{ V}$		-10		-10		-10	μA
I_{ILPU}^5	Low Level Input Current Pull-up	@ $V_{DD_EXT} = \text{Max}$, $V_{IN} = 0 \text{ V}$		200		200		200	μA
$I_{OZH}^{6,7}$	Three-State Leakage Current	@ $V_{DD_EXT} = \text{Max}$, $V_{IN} = V_{DD_EXT} \text{ Max}$		10		10		10	μA
I_{OZL}^6	Three-State Leakage Current	@ $V_{DD_EXT} = \text{Max}$, $V_{IN} = 0 \text{ V}$		-10		-10		-10	μA
I_{OZLPU}^7	Three-State Leakage Current Pull-up	@ $V_{DD_EXT} = \text{Max}$, $V_{IN} = 0 \text{ V}$		200		200		200	μA
I_{OZHDP}^8	Three-State Leakage Current Pull-down	@ $V_{DD_EXT} = \text{Max}$, $V_{IN} = V_{DD_EXT} \text{ Max}$		200		200		200	μA
I_{DD_RTC}	V_{DD_RTC} Current	@ $V_{DD_RTC} = 3.0$, $T_J = 25^\circ\text{C}$		0.76		0.76		0.76	μA
$I_{DD_INT}^9$	Supply Current (Internal)	$f_{CLK} > 0 \text{ MHz}$		Table 14 + Table 15 × ASF		Table 14 + Table 15 × ASF		Table 14 + Table 15 × ASF	mA
$C_{IN}^{10, 11}$	Input Capacitance	$T_{CASE} = 25^\circ\text{C}$		5		5		5	pF

¹ Specifications subject to change without notice.

² Applies to output and bidirectional pins: ADDR23-0, DATA15-0, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, FLAG3-0, DAI_Px, DPI_Px, $\overline{\text{EMU}}$, TDO, $\overline{\text{RESETOUT}}$, MLBSIG, MLBDAT, MLBDO, MLBSO, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, $\overline{\text{SDCKE}}$, SDA10, $\overline{\text{SDDQM}}$, MS0-1.

³ See [Output Drive Currents](#) for typical drive current capabilities.

⁴ Applies to input pins: BOOT_CFGx, CLK_CFGx, TCK, $\overline{\text{RESET}}$, CLKIN.

⁵ Applies to input pins with internal pull-ups: TRST, TMS, TDI.

⁶ Applies to three-statable pins: TDO, MLBDAT, MLBSIG, MLBDO, and MLBSO.

⁷ Applies to three-statable pins with pull-ups: DAI_Px, DPI_Px, $\overline{\text{EMU}}$.

⁸ Applies to three-statable pin with pull-down: SDCLK.

⁹ See Engineer-to-Engineer Note "Estimating Power Dissipation for ADSP-214xx SHARC Processors" for further information.

¹⁰ Applies to all signal pins.

¹¹ Guaranteed, but not tested.

ADSP-21477/ADSP-21478/ADSP-21479

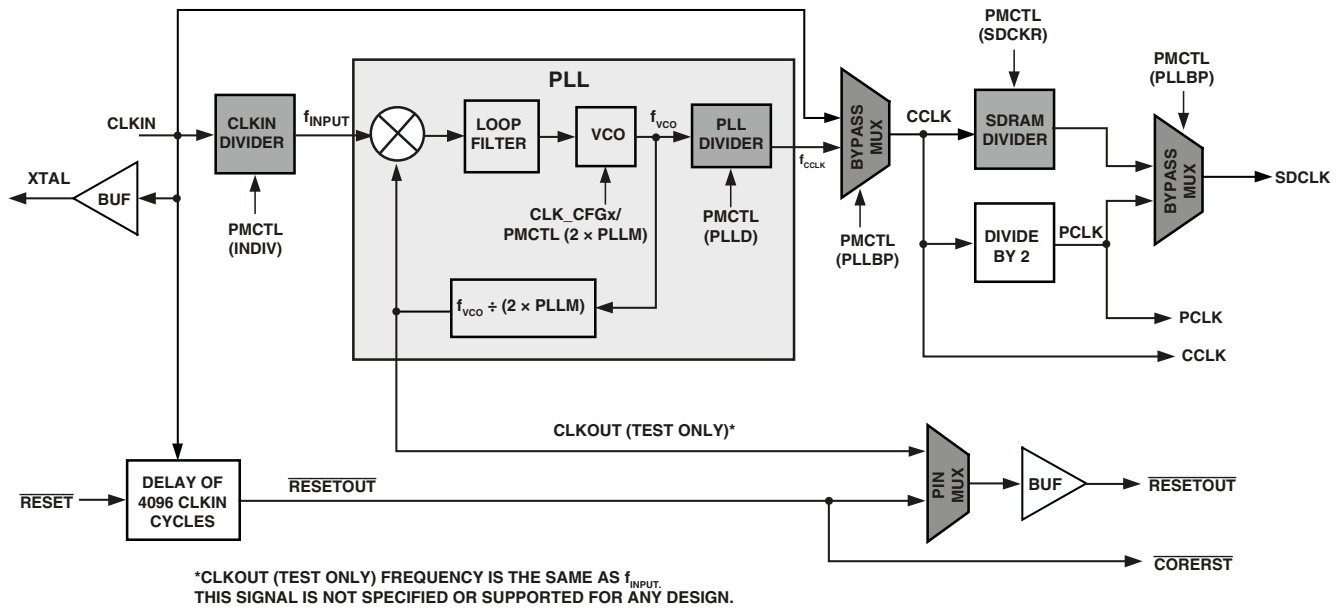


Figure 5. Core Clock and System Clock Relationship to CLKIN

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

Table 24. Core Timer

Parameter	88-Lead LFCSP Package		All Other Packages		Unit
	Min	Max	Min	Max	
<i>Switching Characteristic</i>					
t_{WCTIM} TMREXP Pulse Width	$4 \times t_{PCLK} - 1.55$		$4 \times t_{PCLK} - 1.2$		ns



Figure 12. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to timer0 and timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 25. Timer PWM_OUT Timing

Parameter	88-Lead LFCSP Package		All Other Packages		Unit
	Min	Max	Min	Max	
<i>Switching Characteristic</i>					
t_{PWMO} Timer Pulse Width Output	$2 \times t_{PCLK} - 1.65$	$2 \times (2^{31} - 1) \times t_{PCLK}$	$2 \times t_{PCLK} - 1.2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

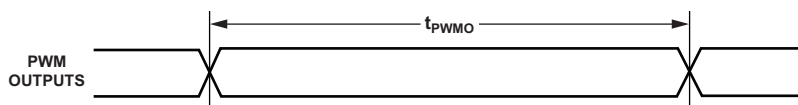


Figure 13. Timer PWM_OUT Timing

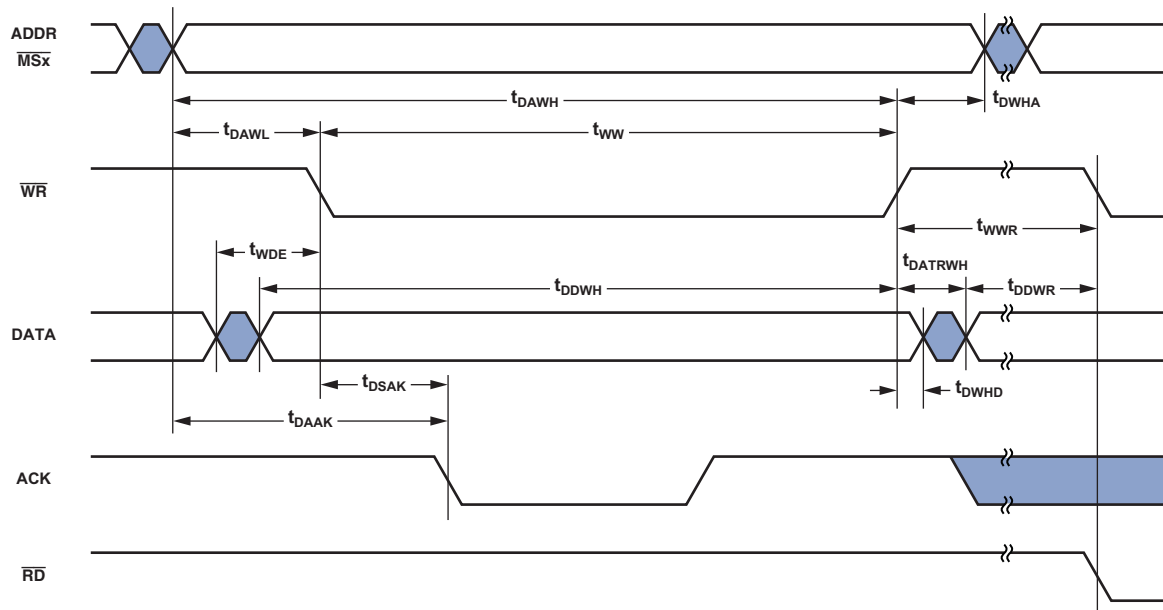


Figure 21. AMI Write

Serial Ports

In slave transmitter mode and master receiver mode, the maximum serial port frequency is $f_{PCLK}/8$. In master transmitter mode and slave receiver mode, the maximum serial port clock frequency is $f_{PCLK}/4$.

To determine whether communication is possible between two devices at clock speed, n , the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Serial port signals (SCLK, FS, Data Channel A, Data Channel B) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 34. Serial Ports—External Clock

Parameter	88-Lead LFCSP Package		All Other Packages		Unit
	Min	Max	Min	Max	
Timing Requirements					
t _{SFSE} ¹ Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	4		2.5		ns
t _{HFSE} ¹ Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	4		2.5		ns
t _{SDRE} ¹ Receive Data Setup Before Receive SCLK	4		2.5		ns
t _{HDRE} ¹ Receive Data Hold After SCLK	4		2.5		ns
t _{SCLKW} SCLK Width	(t _{PCLK} × 4) ÷ 2 – 1.5		(t _{PCLK} × 4) ÷ 2 – 1.5		ns
t _{SCLK} SCLK Period	t _{PCLK} × 4		t _{PCLK} × 4		ns
Switching Characteristics					
t _{DFSE} ² Frame Sync Delay After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)		15		15	ns
t _{HOFSE} ² Frame Sync Hold After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)	2		2		ns
t _{DDTE} ² Transmit Data Delay After Transmit SCLK		15		15	ns
t _{HDTE} ² Transmit Data Hold After Transmit SCLK	2		2		ns

¹ Referenced to sample edge.

² Referenced to drive edge.

ADSP-21477/ADSP-21478/ADSP-21479

Table 35. Serial Ports—Internal Clock

Parameter		88-Lead LFCSP Package		All Other Packages		Unit
		Min	Max	Min	Max	
Timing Requirements						
t _{SFSI} ¹	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	13		10.5		ns
t _{HFSI} ¹	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5		2.5		ns
t _{SDRI} ¹	Receive Data Setup Before SCLK	13		10.5		ns
t _{HDRI} ¹	Receive Data Hold After SCLK	2.5		2.5		ns
Switching Characteristics						
t _{DFSI} ²	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		5		5	ns
t _{HOFSI} ²	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	−1.0		−1.0		ns
t _{DFSIR} ²	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		10.7		10.7	ns
t _{HOFIR} ²	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	−1.0		−1.0		ns
t _{DDTI} ²	Transmit Data Delay After SCLK		4		4	ns
t _{HDTI} ²	Transmit Data Hold After SCLK	−1.0		−1.0		ns
t _{SCKLIW}	Transmit or Receive SCLK Width	2 × t _{PCLK} − 1.5	2 × t _{PCLK} + 1.5	2 × t _{PCLK} − 1.5	2 × t _{PCLK} + 1.5	ns

¹ Referenced to the sample edge.

² Referenced to drive edge.

Table 46. S/PDIF Transmitter Left-Justified Mode

Parameter	Nominal	Unit
<i>Timing Requirement</i>		
t_{LJD} FS to MSB Delay in Left-Justified Mode	0	SCLK

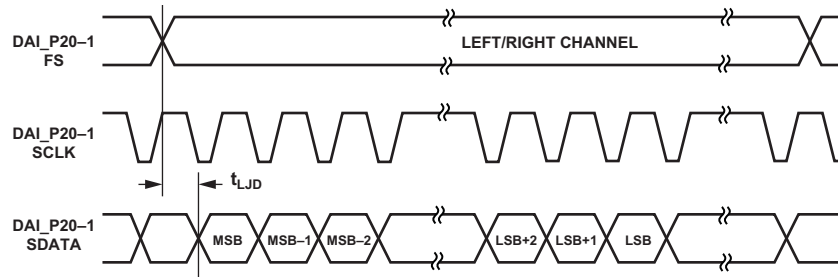


Figure 33. Left-Justified Mode

ADSP-21477/ADSP-21478/ADSP-21479

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 47. Input signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 47. S/PDIF Transmitter Input Data Timing

Parameter		88-Lead LFCSP Package		All Other Packages		Unit
		Min	Max	Min	Max	
Timing Requirements						
t _{SIFS} ¹	Frame Sync Setup Before Serial Clock Rising Edge	4.5		3		ns
t _{SIHFS} ¹	Frame Sync Hold After Serial Clock Rising Edge	3		3		ns
t _{SISD} ¹	Data Setup Before Serial Clock Rising Edge	4.5		3		ns
t _{SIHD} ¹	Data Hold After Serial Clock Rising Edge	3		3		ns
t _{SITXCLKW}	Transmit Clock Width	9		9		ns
t _{SITXCLK}	Transmit Clock Period	20		20		ns
t _{SISCLKW}	Clock Width	36		36		ns
t _{SISCLK}	Clock Period	80		80		ns

¹ The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

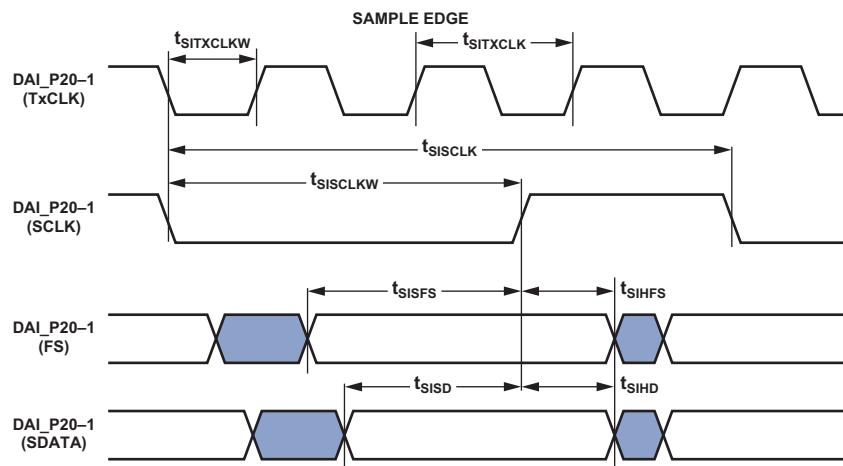


Figure 34. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

Table 48. Oversampling Clock (TxCLK) Switching Characteristics

Parameter	Max	Unit
Frequency for TxCLK = $384 \times$ Frame Sync	$\text{Oversampling Ratio} \times \text{Frame Sync} \leq 1/t_{SITXCLK}$	MHz
Frequency for TxCLK = $256 \times$ Frame Sync	49.2	MHz
Frame Rate (FS)	192.0	kHz

ADSP-21477/ADSP-21478/ADSP-21479

SPI Interface—Master

Both the primary and secondary SPIs are available through DPI only. The timing provided in Table 50 and Table 51 applies to both.

Table 50. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		88-Lead LFCSP Package		All Other Packages		Unit
		Min	Max	Min	Max	
Timing Requirements						
t _{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	10		8.6		ns
t _{HSPIDM}	SPICLK Last Sampling Edge to Data Input Not Valid	2		2		ns
Switching Characteristics						
t _{SPICLKM}	Serial Clock Cycle	8 × t _{PCLK} – 2		8 × t _{PCLK} – 2		ns
t _{SPICHM}	Serial Clock High Period	4 × t _{PCLK} – 2		4 × t _{PCLK} – 2		ns
t _{SPICLM}	Serial Clock Low Period	4 × t _{PCLK} – 2		4 × t _{PCLK} – 2		ns
t _{DDSPIDM}	SPICLK Edge to Data Out Valid (Data Out Delay time)		2.5		2.5	
t _{HDSPIDM}	SPICLK Edge to Data Out Not Valid (Data Out Hold time)	4 × t _{PCLK} – 2		4 × t _{PCLK} – 2		ns
t _{SDSCIM}	DPI Pin (SPI Device Select) Low to First SPICLK Edge	4 × t _{PCLK} – 2		4 × t _{PCLK} – 2		ns
t _{HDSM}	Last SPICLK Edge to DPI Pin (SPI Device Select) High	4 × t _{PCLK} – 2		4 × t _{PCLK} – 2		ns
t _{SPITDM}	Sequential Transfer Delay	4 × t _{PCLK} – 2		4 × t _{PCLK} – 1.4		ns

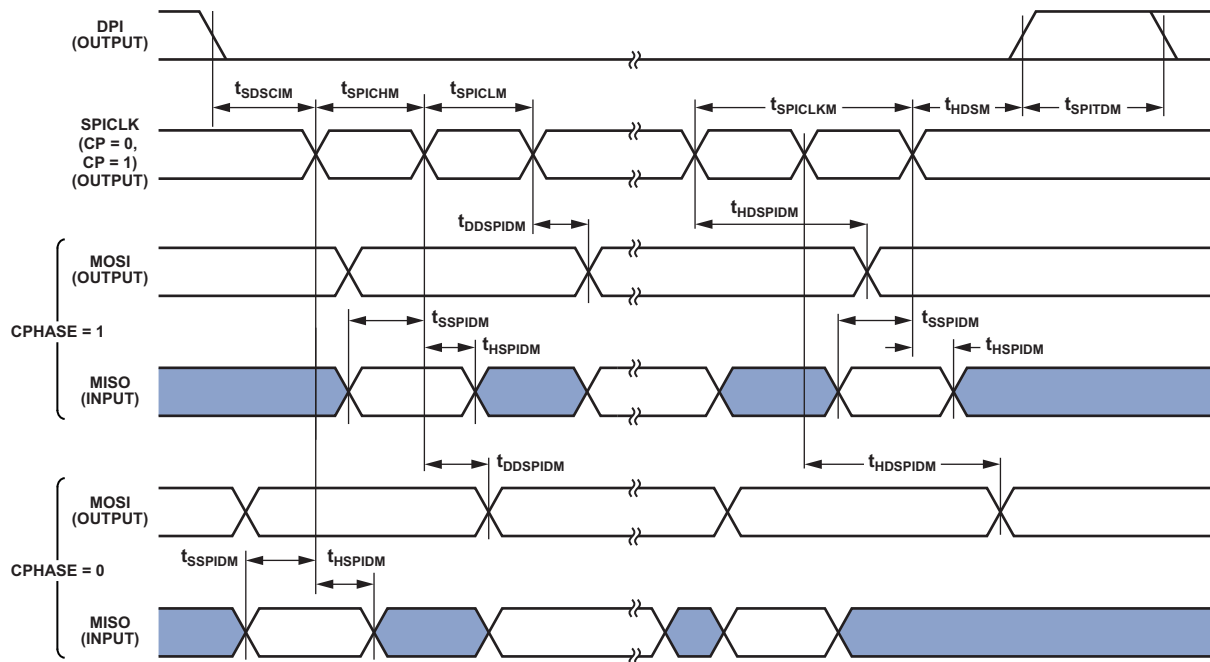


Figure 36. SPI Master Timing

ADSP-21477/ADSP-21478/ADSP-21479

Media Local Bus

All the numbers given are applicable for all speed modes (1024 FS, 512 FS, and 256 FS for 3-pin; 512 FS and 256 FS for 5-pin) unless otherwise specified. Please refer to MediaLB specification document rev 3.0 for more details.

Table 52. MLB Interface, 3-Pin Specifications

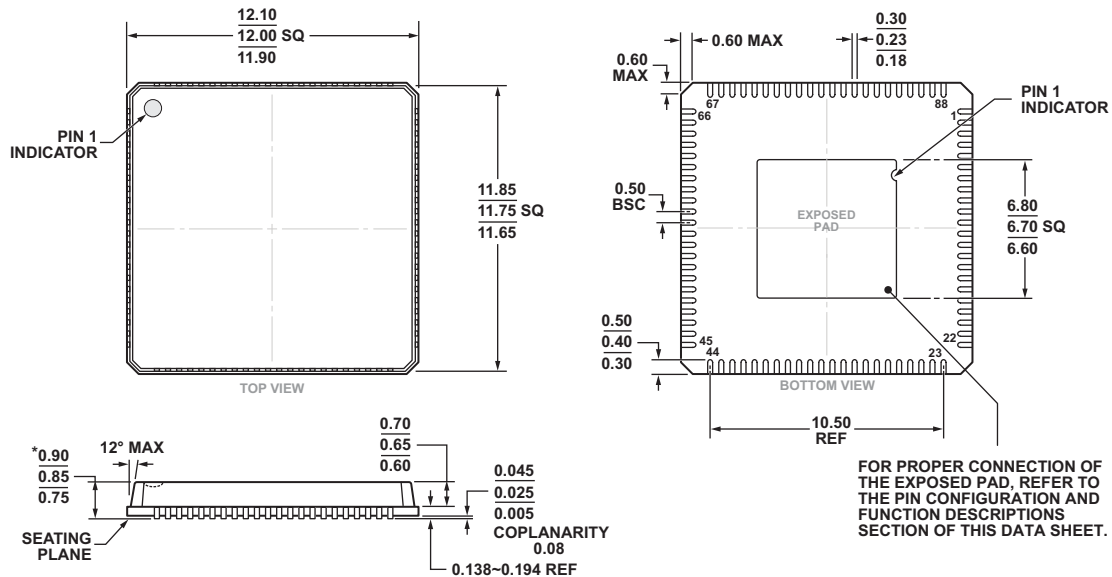
Parameter	Min	Typ	Max	Unit
<i>3-Pin Characteristics</i>				
t_{MLCLK} MLB Clock Period				
1024 FS		20.3		ns
512 FS		40		ns
256 FS		81		ns
t_{MCKL} MLBCLK Low Time				
1024 FS	6.1			ns
512 FS	14			ns
256 FS	30			ns
t_{MCKH} MLBCLK High Time				
1024 FS	9.3			ns
512 FS	14			ns
256 FS	30			ns
t_{MCKR} MLBCLK Rise Time (V_{IL} to V_{IH})				
1024 FS			1	ns
512 FS/256 FS			3	ns
t_{MCKF} MLBCLK Fall Time (V_{IH} to V_{IL})				
1024 FS			1	ns
512 FS/256 FS			3	ns
t_{MPWV}^1 MLBCLK Pulse Width Variation				
1024 FS			0.7	ns p-p
512 FS/256			2.0	ns p-p
t_{DSMCF} DAT/SIG Input Setup Time	1			ns
t_{DHMCF} DAT/SIG Input Hold Time	1.2			ns
t_{MCFDZ} DAT/SIG Output Time to Three-State	0		15	ns
t_{MCDRV} DAT/SIG Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MDZH}^2 Bus Hold Time				
1024 FS	2			ns
512 FS/256	4			ns
C_{MLB} DAT/SIG Pin Load				
1024 FS			40	pf
512 FS/256			60	pf

¹ Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (p-p).

² The board must be designed to ensure that the high impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

OUTLINE DIMENSIONS

The processors are available in 88-lead LFCSP_VQ, 100-lead LQFP_EP and 196-ball CSP_BGA RoHS compliant packages. For package assignment by model, see [Ordering Guide](#).



*COMPLIANT TO JEDEC STANDARDS MO-220-VRRD EXCEPT FOR MINIMUM THICKNESS AND LEAD COUNT.

Figure 57. 88-Lead Lead Frame Chip Scale Package [LFCSP_VQ]¹
(CP-88-5)

Dimensions Shown in Millimeters

¹ For information relating to the exposed pad on the CP-88-5 package, see the table endnote on [Page 68](#).