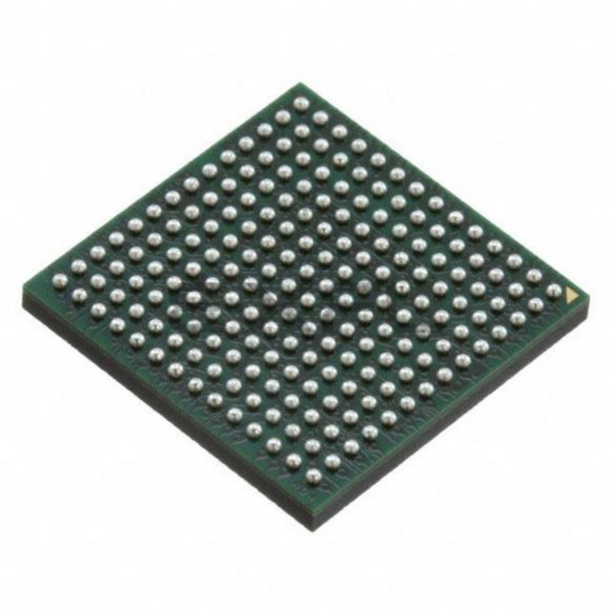

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI, EBI/EMI, I²C, SPI, SPORT, UART/USART
Clock Rate	300MHz
Non-Volatile Memory	ROM (4Mbit)
On-Chip RAM	3Mbit
Voltage - I/O	3.30V
Voltage - Core	1.30V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LFBGA, CSPBGA
Supplier Device Package	196-CSPBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21478kbcz-3a

bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external SDRAM memory. This support is not extended to the asynchronous memory interface (AMI). Source modules need to be built using the VISA option, in order to allow code generation tools to create these more efficient opcodes.

On-Chip Memory

The processors contain varying amounts of internal RAM and internal ROM which is shown in Table 3 through Table 5. Each block can be configured for different combinations of code and data storage. Each memory block supports single-cycle, independent accesses by the core processor and I/O processor.

The processor's SRAM can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5M bits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

The memory maps in Table 3 through Table 5 display the internal memory address space of the processors. The 48-bit space section describes what this address range looks like to an instruction that retrieves 48-bit memory. The 32-bit section describes what this address range looks like to an instruction that retrieves 32-bit memory.

Table 3. ADSP-21477 Internal Memory Space (2M bits)

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 FFFF
Block 0 SRAM 0x0004 9000–0x0004 BFFF	Block 0 SRAM 0x0008 C000–0x0008 FFFF	Block 0 SRAM 0x0009 2000–0x0009 7FFF	Block 0 SRAM 0x0012 4000–0x0012 FFFF
Reserved 0x0004 C000–0x0004 FFFF	Reserved 0x0009 000–0x0009 5554	Reserved 0x0009 8000–0x0009 FFFF	Reserved 0x0013 0000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000AFFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 BFFF	Block 1 SRAM 0x000A C000–0x000A FFFF	Block 1 SRAM 0x000B 2000–0x000B 7FFF	Block 1 SRAM 0x0016 4000–0x0016 FFFF
Reserved 0x0005 C000–0x0005 FFFF	Reserved 0x000B 0000–0x000B 5554	Reserved 0x000B 8000–0x000B FFFF	Reserved 0x0017 0000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 0FFF	Block 2 SRAM 0x000C 0000–0x000C 1554	Block 2 SRAM 0x000C 0000–0x000C 1FFF	Block 2 SRAM 0x0018 0000–0x0018 3FFF
Reserved 0x0006 1000– 0x0006 FFFF	Reserved 0x000C 1555–0x000D 5554	Reserved 0x000C 2000–0x000D FFFF	Reserved 0x0018 4000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 0FFF	Block 3 SRAM 0x000E 0000–0x000E 1554	Block 3 SRAM 0x000E 0000–0x000E 1FFF	Block 3 SRAM 0x001C 0000–0x001C 3FFF
Reserved 0x0007 1000–0x0007 FFFF	Reserved 0x000E 1555–0x000F 5554	Reserved 0x000E 2000–0x000F FFFF	Reserved 0x001C 4000–0x001F FFFF

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface ports (SPI), one universal asynchronous receiver-transmitter (UART), 12 flags, a 2-wire interface (TWI), three PWM modules (PWM3–1), and two general-purpose timers.

Serial Peripheral (Compatible) Interface (SPI)

The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible port to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multi-master environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The SPI-compatible port uses open drain drivers to support a multi-master configuration and to avoid data contention.

UART Port

The processors provide a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Support for bit rates ranging from (f_{PCLK}/1,048,576) to (f_{PCLK}/16) bits per second.
- Support for data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs generating 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

PWM signals can be mapped to the external port address lines or to the DPI pins.

Timers

The processors have a total of three timers: a core timer that can generate periodic software interrupts and two general-purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watch dog mode

The core timer can be configured to use FLAG3 as a timer expired signal, and the general-purpose timers have one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables the general-purpose timer.

2-Wire Interface Port (TWI)

The TWI is a bidirectional 2-wire serial bus used to move 8-bit data while maintaining compliance with the I^2C bus protocol. The TWI master incorporates the following features:

- 7-bit addressing
- Simultaneous master and slave operation on multiple device systems with support for multi-master data arbitration
- Digital filtering and timed event processing
- 100 kbps and 400 kbps data rates
- Low interrupt rate

PIN FUNCTION DESCRIPTIONS

Table 11. Pin Descriptions

Name	Type	State During/ After Reset	Description
$ADDR_{23-0}$	I/O/T (ipu)	High-Z/driven low (boot)	**External Address.** The processor outputs addresses for external memory and peripherals on these pins. The ADDR pins can be multiplexed to support the external memory interface address, FLAGS15–8 (I/O) and PWM (O). After reset, all ADDR pins are in EMIF mode, and FLAG(0–3) pins are in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the $ADDR_{23-4}$ pins for parallel input data.
$DATA_{15-0}$	I/O/T (ipu)	High-Z	**External Data.** The data pins can be multiplexed to support the external memory interface data (I/O) and $FLAGS_{7-0}$ (I/O).
AMI_ACK	I (ipu)		**Memory Acknowledge.** External devices can deassert AMI_ACK (low) to add wait states to an external memory access. AMI_ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{MS}_{0-1}$	O/T (ipu)	High-Z	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{1-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, when the condition evaluates as true. The $\overline{MS1}$ pin can be used in EPORT/FLASH boot mode. For more information on processor booting, see the *ADSP-214xx SHARC Processor Hardware Reference*.
$\overline{AMI\_RD}$	O/T (ipu)	High-Z	**AMI Port Read Enable.** $\overline{AMI\_RD}$ is asserted whenever the processor reads a word from external memory.
$\overline{AMI\_WR}$	O/T (ipu)	High-Z	**AMI Port Write Enable.** $\overline{AMI\_WR}$ is asserted when the processor writes a word to external memory.
FLAG0/$\overline{IRQ0}$	I/O (ipu)	FLAG[0] INPUT	**FLAG0/Interrupt Request0.**
FLAG1/$\overline{IRQ1}$	I/O (ipu)	FLAG[1] INPUT	**FLAG1/Interrupt Request1.**
FLAG2/$\overline{IRQ2}$/$\overline{MS2}$	I/O (ipu)	FLAG[2] INPUT	**FLAG2/Interrupt Request2/Memory Select2.** This pin is multiplexed with $\overline{MS2}$ in the 196-ball BGA package only.
FLAG3/TMREXP/$\overline{MS3}$	I/O (ipu)	FLAG[3] INPUT	**FLAG3/Timer Expired/Memory Select3.** This pin is multiplexed with $\overline{MS3}$ in the 196-ball BGA package only.

The following symbols appear in the Type column of Table 11: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be 26 kΩ to 63 kΩ. The range of an ipd resistor can be 31 kΩ to 85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.

Not all pins are available in the 88-lead LFCSP_VQ and 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 62 on Page 70.

Power-Up Sequencing

The timing requirements for processor startup are given in Table 19. While no specific power-up sequencing is required between V_{DD_EXT} and V_{DD_INT}, there are some considerations that the system designs should take into account.

- No power supply should be powered up for an extended period of time (>200 ms) before another supply starts to ramp up.
- If the V_{DD_INT} power supply comes up after V_{DD_EXT}, any pin, such as $\overline{\text{RESETOUT}}$ and $\overline{\text{RESET}}$, may actually drive momentarily until the V_{DD_INT} rail has powered up. Systems sharing these signals on the board must determine if there are any issues that need to be addressed based on this behavior.

Note that during power-up, when the V_{DD_INT} power supply comes up after V_{DD_EXT}, a leakage current of the order of three-state leakage current pull-up, pull-down, may be observed on any pin, even if that is an input only (for example, the $\overline{\text{RESET}}$ pin), until the V_{DD_INT} rail has powered up.

Table 19. Power-Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DD_EXT} or V_{DD_INT} On	0		ms
$t_{IVDDEVDD}$	V_{DD_INT} On Before V_{DD_EXT}	–200	+200	ms
t_{CLKVDD}[1]	CLKIN Valid After V_{DD_INT} and V_{DD_EXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		μs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20[3]		μs
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096 \times t_{CK} + 2 \times t_{CCLK}$ [4, 5]		

[1] Valid V_{DD_INT} and V_{DD_EXT} assumes that the supplies are fully ramped to their nominal values (it does not matter which supply comes up first). Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.
[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.
[3] Based on CLKIN cycles.
[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.
[5] The 4096 cycle count depends on t_{SRST} specification in Table 21. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

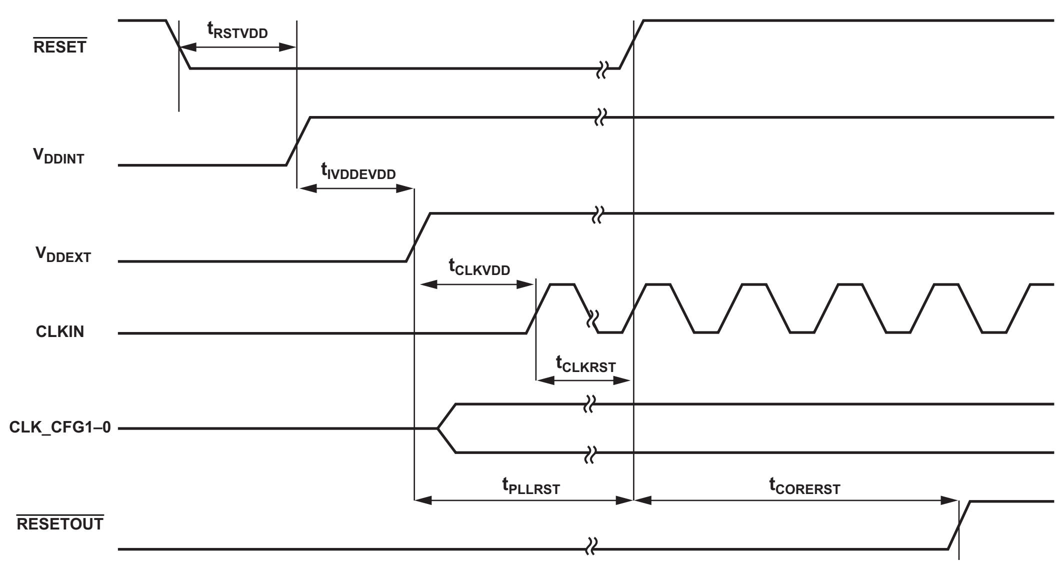

Figure 6. Power-Up Sequencing

Clock Input

Table 20. Clock Input

Parameter		200 MHz Min	200 MHz Max	266 MHz Min	266 MHz Max	300 MHz Min	300 MHz Max	Unit
Timing Requirements								
t_{CK}	CLKIN Period	40	100	30[1]	100	26.66[1]	100	ns
t_{CKL}	CLKIN Width Low	20	45	15	45	13.33	45	ns
t_{CKH}	CLKIN Width High	20	45	15	45	13.33	45	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3	ns
t_{CCLK}[2]	CCLK Period	5	10	3.75	10	3.33	10	ns
f_{VCO}[3]	VCO Frequency	200	600	200	600	200	600	MHz
t_{CKJ}[4, 5]	CLKIN Jitter Tolerance	–250	+250	–250	+250	–250	+250	ps

[1] Applies only for CLKCFG1–0 = 00 and default values for PLL control bits in PMCTL.
[2] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{cclk}.
[3] See Figure 5 for VCO diagram.
[4] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[5] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

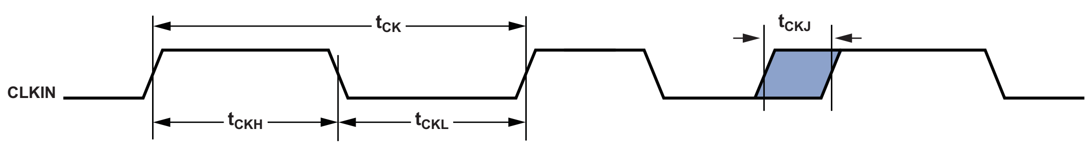

Figure 7. Clock Input

Running Reset

The following timing specification applies to RESETOUT/RUNRSTIN pin when it is configured as RUNRSTIN.

Table 22. Running Reset

Parameter		Min	Max	Unit
Timing Requirements				
$t_{WRUNRST}$	Running RESET Pulse Width Low	$4 \times t_{CK}$		ns
$t_{SRUNRST}$	Running RESET Setup Before CLKIN High	8		ns

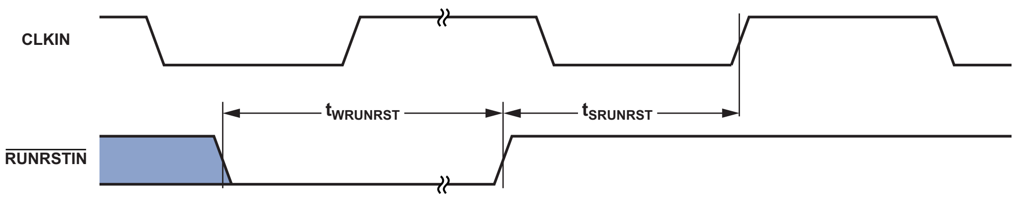

Figure 10. Running Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as IRQ0, IRQ1, and IRQ2 interrupts, as well as the DAI_P20–1 and DPI_P14–1 pins when they are configured as interrupts.

Table 23. Interrupts

Parameter		Min	Max	Unit
Timing Requirement				
t_{IPW}	IRQx Pulse Width	$2 \times t_{PCLK} + 2$		ns

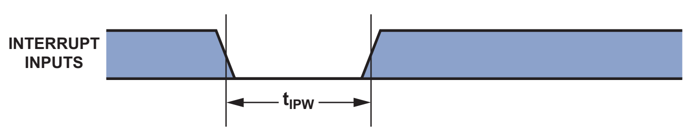

Figure 11. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

Table 24. Core Timer

Parameter		88-Lead LFCSP Package Min	Max	All Other Packages Min	Max	Unit
Switching Characteristic						
t_{WCTIM}	TMREXP Pulse Width	$4 \times t_{PCLK} - 1.55$		$4 \times t_{PCLK} - 1.2$		ns

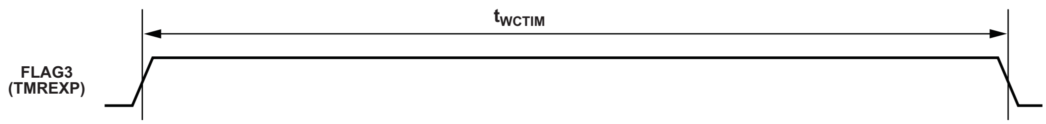

Figure 12. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to timer0 and timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 25. Timer PWM_OUT Timing

Parameter		88-Lead LFCSP Package Min	Max	All Other Packages Min	Max	Unit
Switching Characteristic						
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 1.65$	$2 \times (2^{31} - 1) \times t_{PCLK}$	$2 \times t_{PCLK} - 1.2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

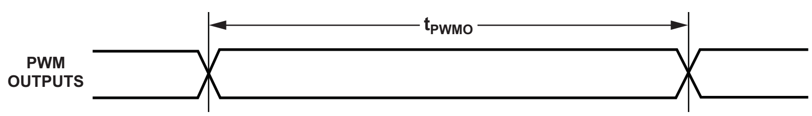

Figure 13. Timer PWM_OUT Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 28. DAI/DPI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid	1.5	10	ns

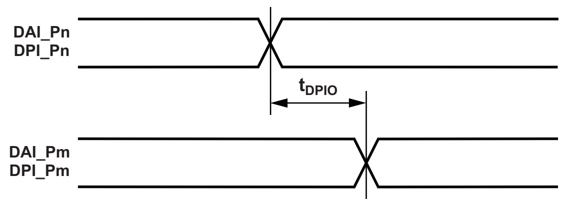

Figure 16. DAI Pin to Pin Direct Routing

AMI Read

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 32. AMI Read

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}[1, 2, 3]	Address Selects Delay to Data Valid		$W + t_{SDCLK} - 6.32$	ns
t_{DRLD}[1, 3]	$\overline{\text{AMI\_RD}}$ Low to Data Valid		$W - 3$	ns
t_{SDS}[4, 5]	Data Setup to $\overline{\text{AMI\_RD}}$ High	2.6		ns
t_{HDRH}	Data Hold from $\overline{\text{AMI\_RD}}$ High	0.4		ns
t_{DAAK}[2, 6]	AMI_ACK Delay from Address Selects		$t_{SDCLK} - 10 + W$	ns
t_{DSAK}[4]	AMI_ACK Delay from $\overline{\text{AMI\_RD}}$ Low		$W - 7.0$	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{\text{AMI\_RD}}$ High	$RHC + 0.38$		ns
t_{DARL}[2]	Address Selects to $\overline{\text{AMI\_RD}}$ Low	$t_{SDCLK} - 5$		ns
t_{RW}	$\overline{\text{AMI\_RD}}$ Pulse Width	$W - 1.4$		ns
t_{RWR}	$\overline{\text{AMI\_RD}}$ High to $\overline{\text{AMI\_RD}}$ Low	$HI + t_{SDCLK} - 1.2$		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
RHC = (number of Read Hold Cycles specified in AMICTLx register) × t_{SDCLK}
Where PREDIS = 0
HI = RHC (if IC = 0): Read to Read from same bank
HI = RHC+ t_{SDCLK} (if IC > 0): Read to Read from same bank
HI = RHC + IC: Read to Read from different bank
HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank
Where PREDIS = 1
HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank
HI = RHC + (3 × t_{SDCLK}): Read to Read from same bank
HI = RHC + Max (IC, (3 × t_{SDCLK})): Read to Read from different bank
IC = (number of idle cycles specified in AMICTLx register) × t_{SDCLK}
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}.

[1] Data delay/setup: System must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{\text{AMI\_MSx}}$, is referenced.
[3] The maximum limit of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.
[4] Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.
[5] Data hold: User must meet t_{HDRH} in asynchronous access mode. See Test Conditions for the calculation of hold times given capacitive and dc loads.
[6] AMI_ACK delay/setup: User must meet t_{daak}, or t_{dsak}, for deassertion of AMI_ACK (low).

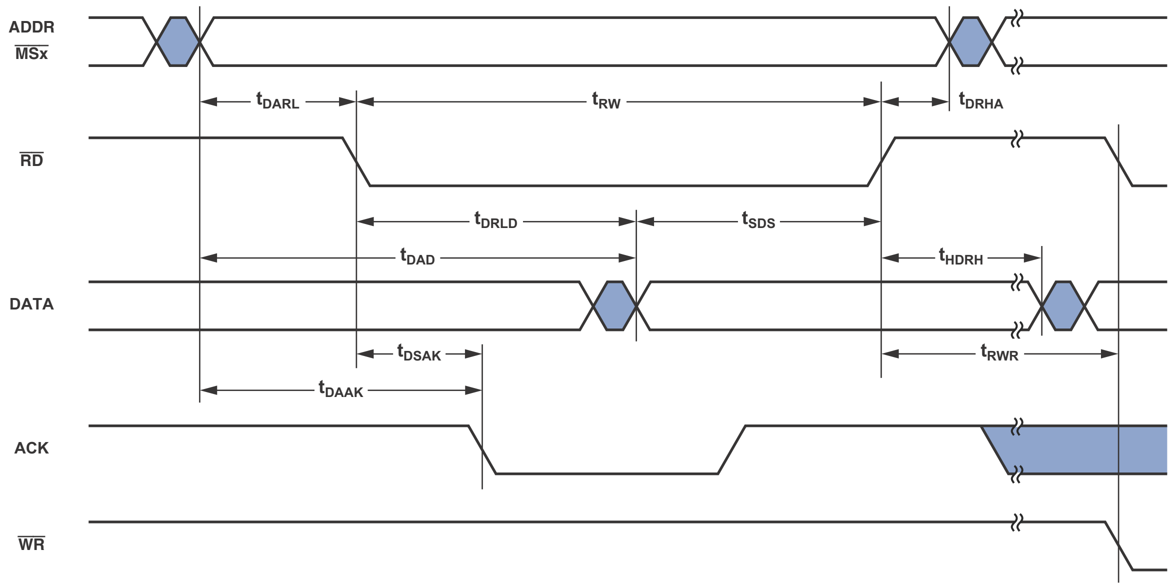

Figure 20. AMI Read

AMI Write

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 33. AMI Write

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	AMI_ACK Delay from Address Selects[1, 2]		$t_{SDCLK} - 10.1 + W$	ns
t_{DSAK}	AMI_ACK Delay from $\overline{\text{AMI\_WR}}$ Low[1, 3]		$W - 7.1$	ns
Switching Characteristics				
t_{DAWH}	Address Selects to $\overline{\text{AMI\_WR}}$ Deasserted[2]	$t_{SDCLK} - 4.4 + W$		ns
t_{DAWL}	Address Selects to $\overline{\text{AMI\_WR}}$ Low[2]	$t_{SDCLK} - 4.5$		ns
t_{WW}	$\overline{\text{AMI\_WR}}$ Pulse Width	$W - 1.3$		ns
t_{DDWH}	Data Setup Before $\overline{\text{AMI\_WR}}$ High	$t_{SDCLK} - 4.3 + W$		ns
t_{DWHA}	Address Hold After $\overline{\text{AMI\_WR}}$ Deasserted	H		ns
t_{DWHD}	Data Hold After $\overline{\text{AMI\_WR}}$ Deasserted	H		ns
t_{DATRWH}	Data Disable After $\overline{\text{AMI\_WR}}$ Deasserted[4]	$t_{SDCLK} - 1.37 + H$	$t_{SDCLK} + 6.75 + H$	ns
t_{WWR}	$\overline{\text{AMI\_WR}}$ High to $\overline{\text{AMI\_WR}}$ Low[5]	$t_{SDCLK} - 1.5 + H$		ns
t_{DDWR}	Data Disable Before $\overline{\text{AMI\_RD}}$ Low	$2 \times t_{SDCLK} - 7.1$		ns
t_{WDE}	Data Enabled to $\overline{\text{AMI\_WR}}$ Low	$t_{SDCLK} - 4.5$		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}

[1] AMI_ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low).
[2] The falling edge of $\overline{\text{AMI\_MSx}}$ is referenced.
[3] Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only applies to asynchronous access mode.
[4] See Test Conditions for calculation of hold times given capacitive and dc loads.
[5] For Write to Write: t_{SDCLK} + H, for both same bank and different bank. For Write to Read: 3 × t_{SDCLK} + H, for the same bank and different banks.

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 40. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the *ADSP-214xx SHARC Processor Hardware Reference*. Note that the 20 bits of external PDAP data can be provided through the ADDR23–0 pins or over the DAI pins.

Table 40. Parallel Data Acquisition Port (PDAP)

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{SPHOLD}[1]	PDAP_HOLD Setup Before PDAP_CLK Sample Edge	4		2.5		ns
t_{HPHOLD}[1]	PDAP_HOLD Hold After PDAP_CLK Sample Edge	4		2.5		ns
t_{PDSD}[1]	PDAP_DAT Setup Before SCLK PDAP_CLK Sample Edge	5		3.85		ns
t_{PDHD}[1]	PDAP_DAT Hold After SCLK PDAP_CLK Sample Edge	4		2.5		ns
t_{PDCLKW}	Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$		$(t_{PCLK} \times 4) \div 2 - 3$		ns
t_{PDCLK}	Clock Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns
Switching Characteristics						
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} + 3$		$2 \times t_{PCLK} + 3$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1.5$		$2 \times t_{PCLK} - 1.5$		ns

[1] Source pins of DATA and control are ADDR23–0 or DAI pins. Source pins for SCLK and FS are: 1) DAI pins, 2) CLKIN through PCG, or 3) DAI pins through PCG.

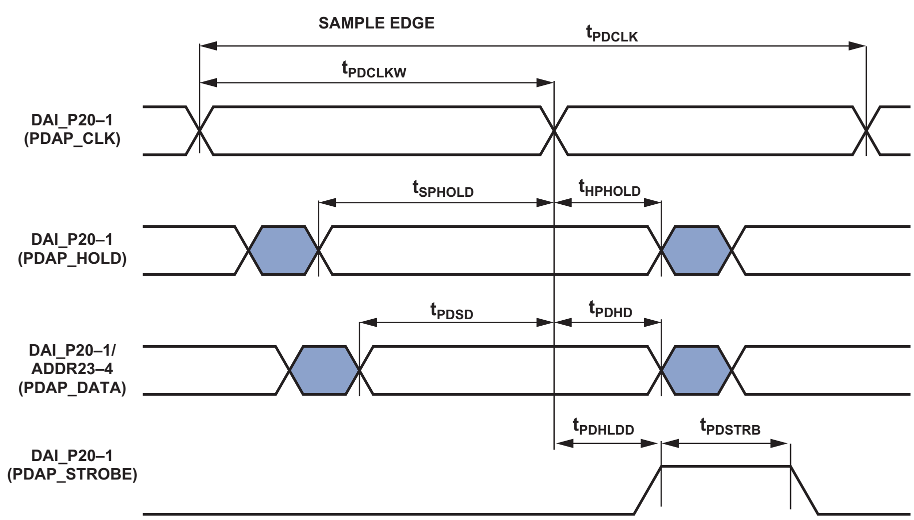

Figure 27. PDAP Timing

Pulse-Width Modulation Generators (PWM)

The following timing specifications apply when the ADDR23–8/DPI_14–1 pins are configured as PWM.

Table 43. Pulse-Width Modulation (PWM) Timing

Parameter		88-Lead LFCSP Package		All Other Packages		Unit
		Min	Max	Min	Max	
Switching Characteristics						
t_{PWMW}	PWM Output Pulse Width	$t_{PCLK} - 2$	$(2^{16} - 2) \times t_{PCLK}$	$t_{PCLK} - 2$	$(2^{16} - 2) \times t_{PCLK}$	ns
t_{PWMP}	PWM Output Period	$2 \times t_{PCLK} - 2$	$(2^{16} - 1) \times t_{PCLK}$	$2 \times t_{PCLK} - 1.5$	$(2^{16} - 1) \times t_{PCLK}$	ns

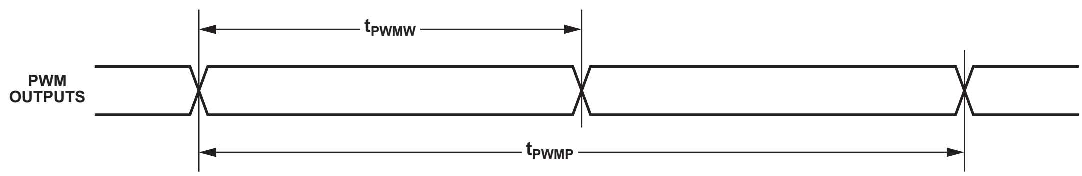

Figure 30. PWM Timing

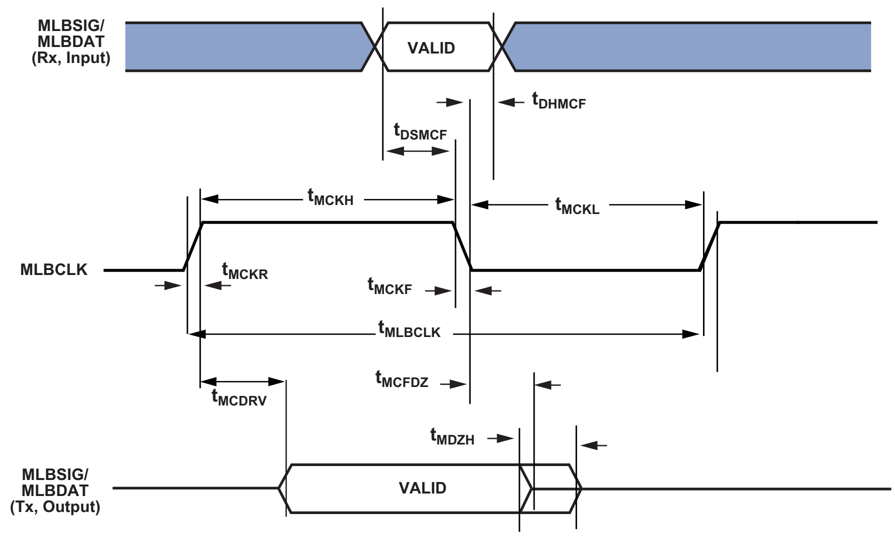

Figure 38. MLB Timing (3-Pin Interface)

Table 53. MLB Interface, 5-Pin Specifications

Parameter		Min	Typ	Max	Unit
5-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})			6	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})			6	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation			2	ns p-p
t_{DSMCF}[2]	DAT/SIG Input Setup Time	3			ns
t_{DHMCF}	DAT/SIG Input Hold Time	5			ns
t_{MCDRV}	DS/DO Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MCRDL}[3]	DO/SO Low From MLBCLK High				
	512 FS			10	ns
	256 FS			20	ns
C_{mlb}	DS/DO Pin Load			40	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (p-p).
[2] Gate delays due to OR'ing logic on the pins must be accounted for.
[3] When a node is not driving valid data onto the bus, the MLBSO and MLBDO output lines shall remain low. If the output lines can float at anytime, including while in reset, external pull-down resistors are required to keep the outputs from corrupting the MediaLB signal lines when not being driven.

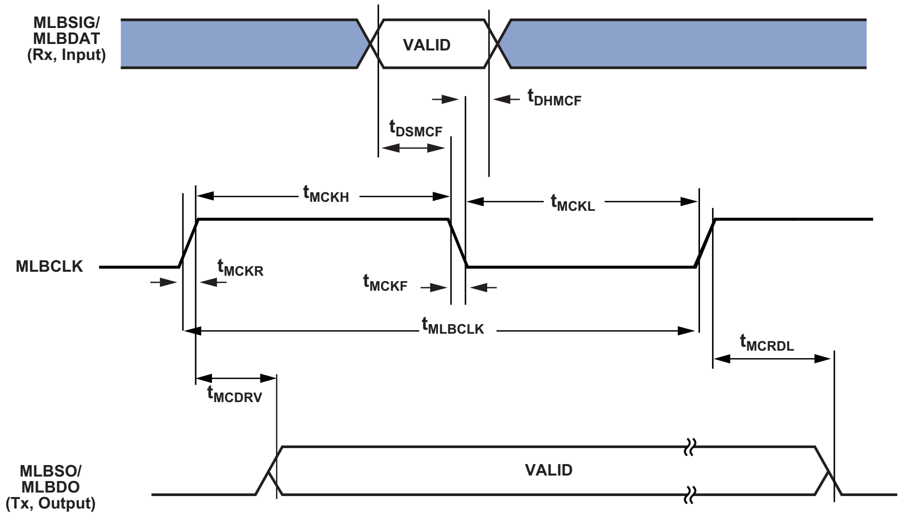

Figure 39. MLB Timing (5-Pin Interface)

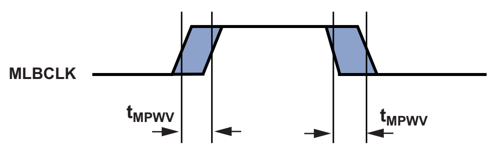

Figure 40. MLB 3-Pin and 5-Pin MLBCLK Pulse Width Variation Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the *ADSP-214xx SHARC Hardware Reference Manual*.

2-Wire Interface (TWI)—Receive and Transmit Timing

For information on the TWI receive and transmit operations, see the *ADSP-214xx SHARC Hardware Reference Manual*.

JTAG Test Access Port and Emulation

Table 55. JTAG Test Access Port and Emulation

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{TCK}	TCK Period	20		20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		$4 \times t_{CK}$		ns
Switching Characteristics						
t_{DTDO}	TDO Delay from TCK Low		11.5		10.5	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = DATA15–0, CLK_CFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, DAI_Px, DPI_Px, FLAG3–0, MLBCLK, MLBDAT, MLBSIG, SR_SCLK, $\overline{\text{SR\_CLR}}$, SR_SDI, and SR_LAT.

[2] System Outputs = DAI_Px, DPI_Px, ADDR23–0, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, FLAG3–0, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, SDCKE, SDA10, SDDQM, SDCLK, MLBDAT, MLBSIG, MLBDO, MLBSO, SR_SDO, SR_LDO, and $\overline{\text{EMU}}$.

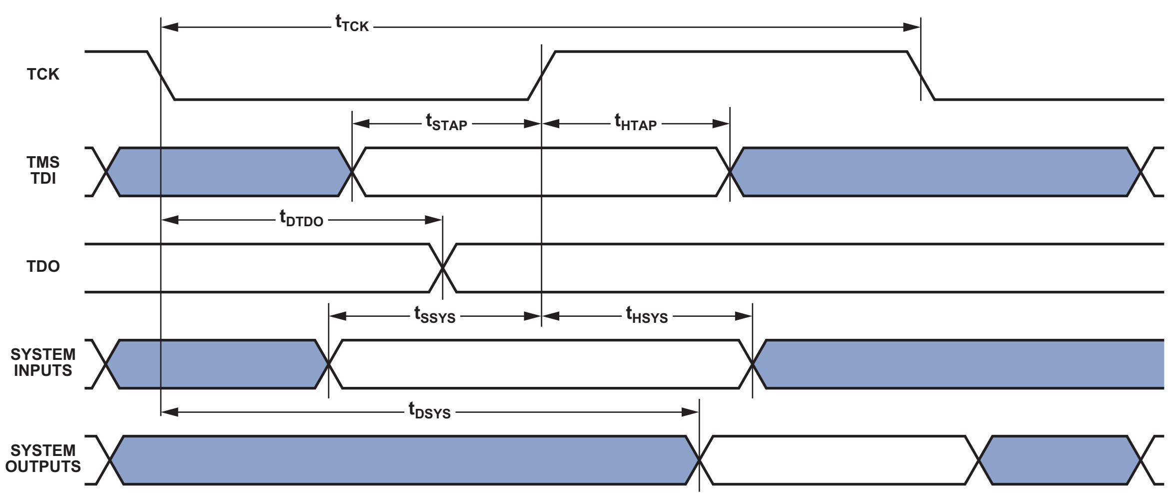

Figure 46. IEEE 1149.1 JTAG Test Access Port

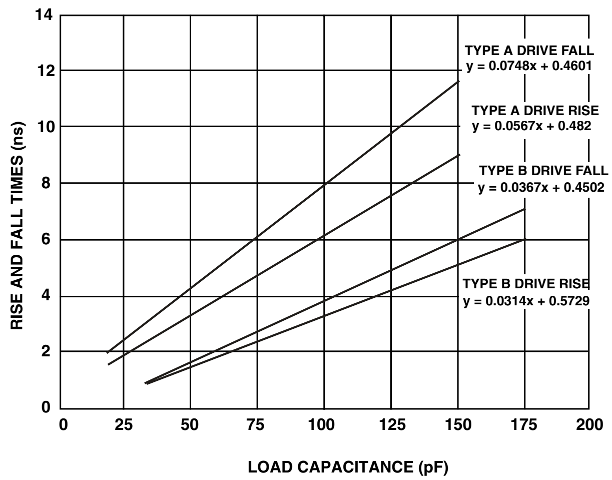

Figure 51. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Min)

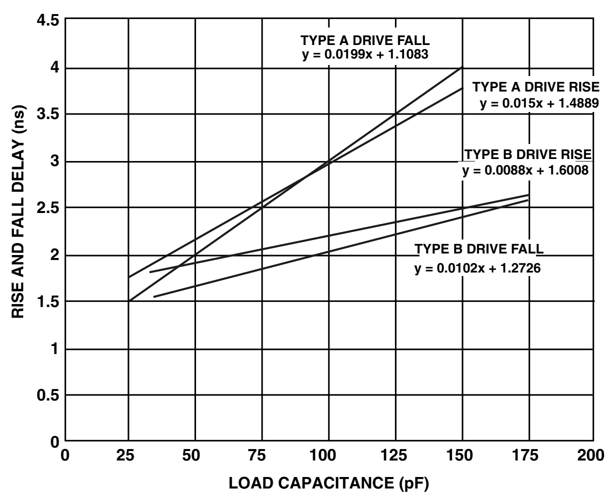

Figure 52. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

THERMAL CHARACTERISTICS

The processor is rated for performance over the temperature range specified in Operating Conditions.

Table 58 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-7 (PBGA). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the typical value from Table 58

P_D = power dissipation

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

Note that the thermal characteristics values provided in Table 58 are modeled values.

Table 57. Thermal Characteristics for 88-Lead LFCSP_VQ

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	22.6	°C/W
θ_{JMA}	Airflow = 1 m/s	18.2	°C/W
θ_{JMA}	Airflow = 2 m/s	17.3	°C/W
θ_{JC}		7.9	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.22	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.36	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.44	°C/W

Table 58. Thermal Characteristics for 100-Lead LQFP_EP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	18.1	°C/W
θ_{JMA}	Airflow = 1 m/s	15.5	°C/W
θ_{JMA}	Airflow = 2 m/s	14.6	°C/W
θ_{JC}		2.4	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.22	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.36	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.50	°C/W

Table 59. Thermal Characteristics for 196-Ball CSP_BGA

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	29.0	°C/W
θ_{JMA}	Airflow = 1 m/s	26.1	°C/W
θ_{JMA}	Airflow = 2 m/s	25.1	°C/W
θ_{JC}		8.8	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.23	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.42	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.52	°C/W

88-LFCSP_VQ LEAD ASSIGNMENT

Table 61 lists the 88-Lead LFCSP_VQ package lead names.

Table 61. 88-Lead LFCSP_VQ Lead Assignments (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
CLK_CFG1	1	V_{DD_EXT}	23	DAI_P10	45	V_{DD_INT}	67
BOOT_CFG0	2	DPI_P08	24	V_{DD_INT}	46	FLAG0	68
V_{DD_EXT}	3	DPI_P07	25	V_{DD_EXT}	47	V_{DD_INT}	69
V_{DD_INT}	4	DPI_P09	26	DAI_P20	48	FLAG1	70
BOOT_CFG1	5	DPI_P10	27	V_{DD_INT}	49	FLAG2	71
GND	6	DPI_P11	28	DAI_P08	50	FLAG3	72
CLK_CFG0	7	DPI_P12	29	DAI_P04	51	GND	73
V_{DD_INT}	8	DPI_P13	30	DAI_P14	52	GND	74
CLKIN	9	DAI_P03	31	DAI_P18	53	V_{DD_EXT}	75
XTAL	10	DPI_P14	32	DAI_P17	54	GND	76
V_{DD_EXT}	11	V_{DD_INT}	33	DAI_P16	55	V_{DD_INT}	77
V_{DD_INT}	12	DAI_P13	34	DAI_P15	56	$\overline{\text{TRST}}$	78
V_{DD_INT}	13	DAI_P07	35	DAI_P12	57	$\overline{\text{EMU}}$	79
$\overline{\text{RESETOUT}}$/RUNRSTIN	14	DAI_P19	36	DAI_P11	58	TDO	80
V_{DD_INT}	15	DAI_P01	37	V_{DD_INT}	59	V_{DD_EXT}	81
DPI_P01	16	DAI_P02	38	GND	60	V_{DD_INT}	82
DPI_P02	17	V_{DD_INT}	39	THD_M	61	TDI	83
DPI_P03	18	V_{DD_EXT}	40	THD_P	62	TCK	84
V_{DD_INT}	19	V_{DD_INT}	41	V_{DD_THD}	63	V_{DD_INT}	85
DPI_P05	20	DAI_P06	42	V_{DD_INT}	64	$\overline{\text{RESET}}$	86
DPI_P04	21	DAI_P05	43	V_{DD_INT}	65	TMS	87
DPI_P06	22	DAI_P09	44	V_{DD_INT}	66	V_{DD_INT}	88
						GND	89*

* Lead no. 89 is the GND supply (see Figure 53 and Figure 54) for the processor; this pad must be **robustly** connected to GND in order for the processor to function.

100-LQFP_EP LEAD ASSIGNMENT

Table 62 lists the 100-Lead LQFP_EP lead names.

Table 62. 100-Lead LQFP_EP Lead Assignments (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
V_{DD_INT}	1	V_{DD_EXT}	26	DAI_P10	51	V_{DD_INT}	76
CLK_CFG1	2	DPI_P08	27	V_{DD_INT}	52	FLAG0	77
BOOT_CFG0	3	DPI_P07	28	V_{DD_EXT}	53	V_{DD_INT}	78
V_{DD_EXT}	4	V_{DD_INT}	29	DAI_P20	54	V_{DD_INT}	79
V_{DD_INT}	5	DPI_P09	30	V_{DD_INT}	55	FLAG1	80
BOOT_CFG1	6	DPI_P10	31	DAI_P08	56	FLAG2	81
GND	7	DPI_P11	32	DAI_P04	57	FLAG3	82
NC	8	DPI_P12	33	DAI_P14	58	MLBCLK	83
NC	9	DPI_P13	34	DAI_P18	59	MLBDAT	84
CLK_CFG0	10	DAI_P03	35	DAI_P17	60	MLBDO	85
V_{DD_INT}	11	DPI_P14	36	DAI_P16	61	V_{DD_EXT}	86
CLKIN	12	V_{DD_INT}	37	DAI_P15	62	MLBSIG	87
XTAL	13	V_{DD_INT}	38	DAI_P12	63	V_{DD_INT}	88
V_{DD_EXT}	14	V_{DD_INT}	39	V_{DD_INT}	64	MLBSO	89
V_{DD_INT}	15	DAI_P13	40	DAI_P11	65	$\overline{\text{TRST}}$	90
V_{DD_INT}	16	DAI_P07	41	V_{DD_INT}	66	$\overline{\text{EMU}}$	91
$\overline{\text{RESETOUT}}/\overline{\text{RUNRSTIN}}$	17	DAI_P19	42	V_{DD_INT}	67	TDO	92
V_{DD_INT}	18	DAI_P01	43	GND	68	V_{DD_EXT}	93
DPI_P01	19	DAI_P02	44	THD_M	69	V_{DD_INT}	94
DPI_P02	20	V_{DD_INT}	45	THD_P	70	TDI	95
DPI_P03	21	V_{DD_EXT}	46	V_{DD_THD}	71	TCK	96
V_{DD_INT}	22	V_{DD_INT}	47	V_{DD_INT}	72	V_{DD_INT}	97
DPI_P05	23	DAI_P06	48	V_{DD_INT}	73	$\overline{\text{RESET}}$	98
DPI_P04	24	DAI_P05	49	V_{DD_INT}	74	TMS	99
DPI_P06	25	DAI_P09	50	V_{DD_INT}	75	V_{DD_INT}	100
						GND	101*

* Lead no. 101 is the GND supply (see Figure 55 and Figure 56) for the processor; this pad must be **robustly** connected to GND.
MLB pins (pins 83, 84, 85, 87, and 89) are available for automotive models only. For non-automotive models, these pins should be connected to ground (GND).

Figure 55 shows the top view configuration of the 100-lead LQFP_EP package. Figure 56 shows the bottom view configuration of the 100-lead LQFP_EP package.

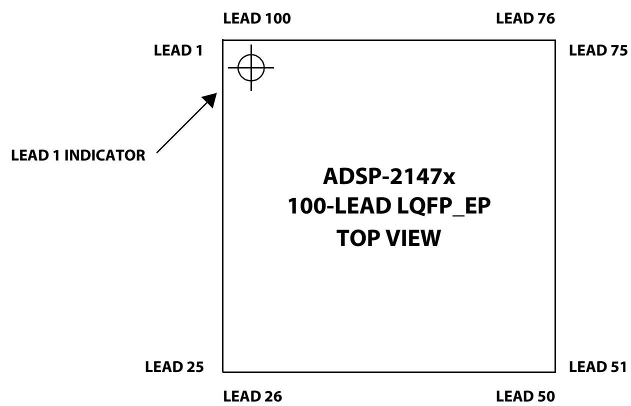

Figure 55. 100-Lead LQFP_EP Lead Configuration (Top View)

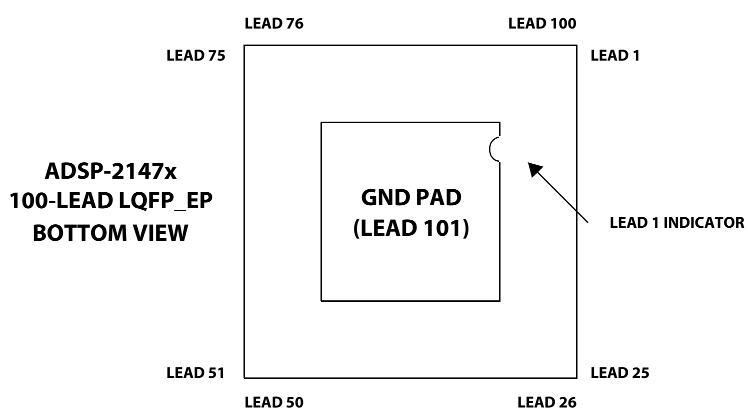

Figure 56. 100-Lead LQFP_EP Lead Configuration (Bottom View)