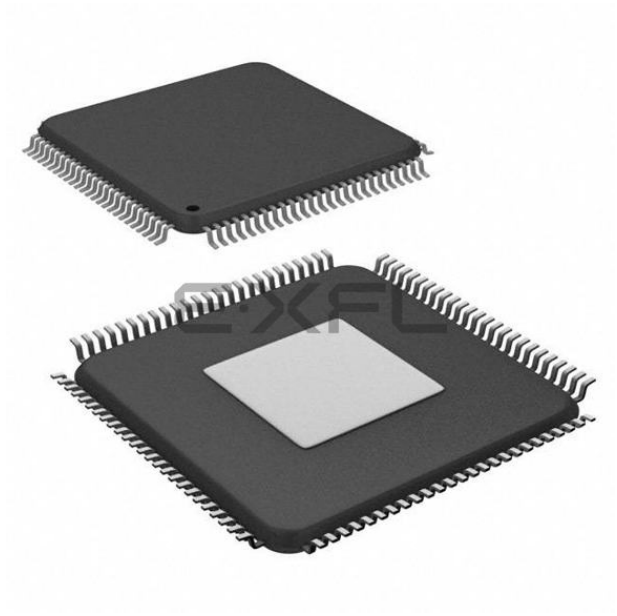

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI, EBI/EMI, I²C, SPI, SPORT, UART/USART
Clock Rate	200MHz
Non-Volatile Memory	ROM (4Mbit)
On-Chip RAM	3Mbit
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	100-LQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21478kswz-1a

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REVISION HISTORY

4/2017—Rev. C to Rev. D

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PRODUCT APPLICATION RESTRICTION

Not for use in in-vivo applications for body fluid constituent monitoring, including monitoring one or more of the components that form, or may be a part of, or contaminate human blood or other body fluids, such as, but not limited to, carboxyhemoglobin, methemoglobin total hemoglobin, oxygen saturation, oxygen content, fractional arterial oxygen saturation, bilirubin, glucose, drugs, lipids, water, protein, and pH.

GENERAL DESCRIPTION

The ADSP-2147x SHARC® processors are members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. The processors are source code compatible with the ADSP-2126x, ADSP-2136x, ADSP-2137x, ADSP-2146x, and ADSP-2116x DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. These processors are 32-bit/40-bit floating-point processors optimized for high performance audio applications with a large on-chip SRAM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

Table 1 shows performance benchmarks for the ADSP-2147x processors. Table 2 shows the features of the individual product offerings.

Table 1. Processor Benchmarks

Benchmark Algorithm	Speed (at 300 MHz)	Speed (at 200 MHz)
1024 Point Complex FFT (Radix 4, with Reversal)	30.59 µs	45.885 µs
FIR Filter (per Tap)[1]	1.66 ns	2.49 ns
IIR Filter (per Biquad)[1]	6.65 ns	9.975 ns
Matrix Multiply (Pipelined)		
[3 × 3] × [3 × 1]	14.99 ns	22.485 ns
[4 × 4] × [4 × 1]	26.66 ns	39.99 ns
Divide (y/x)	11.61 ns	17.41 ns
Inverse Square Root	18.08 ns	27.12 ns

[1] Assumes two files in multichannel SIMD mode.

Table 2. ADSP-2147x Family Features

Feature	ADSP-21477	ADSP-21478	ADSP-21479
Frequency	200 MHz	Up to 300 MHz	
RAM	2M bits	3M bits	5M bits
ROM	N/A	4M bits	
Pulse-Width Modulation	3	4 units (3 in 100-lead package)	
External Port Interface (SDRAM, AMI)[1]	No	Yes, 16-Bit	
Serial Ports	8		
Direct DMA from SPORTs to External Memory	No	Yes	
FIR, IIR, FFT Accelerator	Yes		
MediaLB Interface	No	Automotive models only	
Watch Dog Timer[2]	No	Yes	
Real-Time Clock[2, 3]	No	Yes	
Shift Register[2]	No	Yes	
IDP/PDAP	Yes		
UART	1		
DAI (SRU)/DPI (SRU2)	20/14 Pins		
S/PDIF Transceiver	1		
SPI	2		
TWI	1		
SRC SNR Performance	–128 dB		
Thermal Diode[4]	Yes		
VISA Support	Yes		
Package[1]	100-Lead LQFP 88-Lead LFCSP_VQ	196-Ball CSP_BGA 100-Lead LQFP 88-lead LFCSP_VQ	

[1] The 100-lead and 88-lead packages of the processors do not contain an external port. The SDRAM controller pins must be disabled when using this package. For more information, see Pin Function Descriptions.
[2] Available on the 196-ball CSP_BGA package only.
[3] Real Time Clock (RTC) is supported only for products with a temperature range of 0°C to +70°C and not supported for all other temperature grades.
[4] Available on the 88-lead and 100-lead packages only.

The diagram on Page 1 shows the two clock domains (core and I/O processor) that make up the ADSP-2147x processors. The core clock domain contains the following features.

- Two processing elements (PEx, PEy), each of which comprises an ALU, multiplier, shifter, and data register file
- Two data address generators (DAG1, DAG2)
- A program sequencer with instruction cache
- PM and DM buses capable of supporting 2 × 64-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (up to 5M bit)
- A JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints, which allows flexible exception handling.

bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external SDRAM memory. This support is not extended to the asynchronous memory interface (AMI). Source modules need to be built using the VISA option, in order to allow code generation tools to create these more efficient opcodes.

On-Chip Memory

The processors contain varying amounts of internal RAM and internal ROM which is shown in Table 3 through Table 5. Each block can be configured for different combinations of code and data storage. Each memory block supports single-cycle, independent accesses by the core processor and I/O processor.

The processor's SRAM can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5M bits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

The memory maps in Table 3 through Table 5 display the internal memory address space of the processors. The 48-bit space section describes what this address range looks like to an instruction that retrieves 48-bit memory. The 32-bit section describes what this address range looks like to an instruction that retrieves 32-bit memory.

Table 3. ADSP-21477 Internal Memory Space (2M bits)

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 FFFF
Block 0 SRAM 0x0004 9000–0x0004 BFFF	Block 0 SRAM 0x0008 C000–0x0008 FFFF	Block 0 SRAM 0x0009 2000–0x0009 7FFF	Block 0 SRAM 0x0012 4000–0x0012 FFFF
Reserved 0x0004 C000–0x0004 FFFF	Reserved 0x0009 000–0x0009 5554	Reserved 0x0009 8000–0x0009 FFFF	Reserved 0x0013 0000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000AFFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 BFFF	Block 1 SRAM 0x000A C000–0x000A FFFF	Block 1 SRAM 0x000B 2000–0x000B 7FFF	Block 1 SRAM 0x0016 4000–0x0016 FFFF
Reserved 0x0005 C000–0x0005 FFFF	Reserved 0x000B 0000–0x000B 5554	Reserved 0x000B 8000–0x000B FFFF	Reserved 0x0017 0000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 0FFF	Block 2 SRAM 0x000C 0000–0x000C 1554	Block 2 SRAM 0x000C 0000–0x000C 1FFF	Block 2 SRAM 0x0018 0000–0x0018 3FFF
Reserved 0x0006 1000– 0x0006 FFFF	Reserved 0x000C 1555–0x000D 5554	Reserved 0x000C 2000–0x000D FFFF	Reserved 0x0018 4000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 0FFF	Block 3 SRAM 0x000E 0000–0x000E 1554	Block 3 SRAM 0x000E 0000–0x000E 1FFF	Block 3 SRAM 0x001C 0000–0x001C 3FFF
Reserved 0x0007 1000–0x0007 FFFF	Reserved 0x000E 1555–0x000F 5554	Reserved 0x000E 2000–0x000F FFFF	Reserved 0x001C 4000–0x001F FFFF

PIN FUNCTION DESCRIPTIONS

Table 11. Pin Descriptions

Name	Type	State During/ After Reset	Description
$ADDR_{23-0}$	I/O/T (ipu)	High-Z/driven low (boot)	**External Address.** The processor outputs addresses for external memory and peripherals on these pins. The ADDR pins can be multiplexed to support the external memory interface address, FLAGS15–8 (I/O) and PWM (O). After reset, all ADDR pins are in EMIF mode, and FLAG(0–3) pins are in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the $ADDR_{23-4}$ pins for parallel input data.
$DATA_{15-0}$	I/O/T (ipu)	High-Z	**External Data.** The data pins can be multiplexed to support the external memory interface data (I/O) and $FLAGS_{7-0}$ (I/O).
AMI_ACK	I (ipu)		**Memory Acknowledge.** External devices can deassert AMI_ACK (low) to add wait states to an external memory access. AMI_ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{MS}_{0-1}$	O/T (ipu)	High-Z	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{1-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, when the condition evaluates as true. The $\overline{MS1}$ pin can be used in EPORT/FLASH boot mode. For more information on processor booting, see the *ADSP-214xx SHARC Processor Hardware Reference*.
$\overline{AMI\_RD}$	O/T (ipu)	High-Z	**AMI Port Read Enable.** $\overline{AMI\_RD}$ is asserted whenever the processor reads a word from external memory.
$\overline{AMI\_WR}$	O/T (ipu)	High-Z	**AMI Port Write Enable.** $\overline{AMI\_WR}$ is asserted when the processor writes a word to external memory.
FLAG0/$\overline{IRQ0}$	I/O (ipu)	FLAG[0] INPUT	**FLAG0/Interrupt Request0.**
FLAG1/$\overline{IRQ1}$	I/O (ipu)	FLAG[1] INPUT	**FLAG1/Interrupt Request1.**
FLAG2/$\overline{IRQ2}$/$\overline{MS2}$	I/O (ipu)	FLAG[2] INPUT	**FLAG2/Interrupt Request2/Memory Select2.** This pin is multiplexed with $\overline{MS2}$ in the 196-ball BGA package only.
FLAG3/TMREXP/$\overline{MS3}$	I/O (ipu)	FLAG[3] INPUT	**FLAG3/Timer Expired/Memory Select3.** This pin is multiplexed with $\overline{MS3}$ in the 196-ball BGA package only.

The following symbols appear in the Type column of Table 11: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be 26 kΩ to 63 kΩ. The range of an ipd resistor can be 31 kΩ to 85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.

Not all pins are available in the 88-lead LFCSP_VQ and 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 62 on Page 70.

Table 11. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
THD_P	I		**Thermal Diode Anode.** When not used, this pin can be left floating.
THD_M	O		**Thermal Diode Cathode.** When not used, this pin can be left floating.
MLBCLK	I		**Media Local Bus Clock.** This clock is generated by the MLB controller that is synchronized to the MOST network and provides the timing for the entire MLB interface at 49.152 MHz at FS = 48 kHz. When the MLB controller is not used, this pin should be grounded.
MLBDAT	I/O/T in 3 pin mode. I in 5 pin mode.	High-Z	**Media Local Bus Data.** The MLBDAT line is driven by the transmitting MLB device and is received by all other MLB devices including the MLB controller. The MLBDAT line carries the actual data. In 5-pin MLB mode, this pin is an input only. When the MLB controller is not used, this pin should be grounded.
MLBSIG	I/O/T in 3 pin mode. I in 5 pin mode	High-Z	**Media Local Bus Signal.** This is a multiplexed signal which carries the Channel/Address generated by the MLB Controller, as well as the Command and RxStatus bytes from MLB devices. In 5-pin mode, this pin is input only. When the MLB controller is not used, this pin should be grounded.
MLBDO	O/T	High-Z	**Media Local Bus Data Output (in 5 Pin Mode).** This pin is used only in 5-pin MLB mode and serves as the output data pin. When the MLB controller is not used, this pin should be grounded.
MLBSO	O/T	High-Z	**Media Local Bus Signal Output (in 5 Pin Mode).** This pin is used only in 5-pin MLB mode and serves as the output signal pin. When the MLB controller is not used, this pin should be grounded.
SR_SCLK	I (ipu)		**Shift Register Serial Clock.** (Active high, rising edge sensitive)
$\overline{\text{SR\_CLR}}$	I (ipu)		**Shift Register Reset.** (Active low)
SR_SDI	I (ipu)		**Shift Register Serial Data Input.**
SR_SDO	O (ipu)	Driven Low	**Shift Register Serial Data Output.**
SR_LAT	I (ipu)		**Shift Register Latch Clock Input.** (Active high, rising edge sensitive)
SR_LDO_{17-0}	O/T (ipu)	High-Z	**Shift Register Parallel Data Output.**
RTXI	I		**RTC Crystal Input.** If RTC is not used, then this pin can be NC (no connect) or grounded and the RTC_PDN and RTC_BUSDIS bits of the RTC_INIT register must be set to 1.
RTXO	O		**RTC Crystal Output.** If RTC is not used, then this pin needs to be NC (No Connect).
RTCLKOUT	O (ipd)		**RTC Clock Output.** For calibration purposes. The clock runs at 1 Hz. If RTC is not used, then this pin needs to be NC (No Connect).

The following symbols appear in the Type column of Table 11: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be 26 kΩ to 63 kΩ. The range of an ipd resistor can be 31 kΩ to 85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.

Not all pins are available in the 88-lead LFCSP_VQ and 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 62 on Page 70.

Table 12. Pin List, Power and Ground

Name	Type	Description
V_{DD_INT}	P	**Internal Power Supply.**
V_{DD_EXT}	P	**I/O Power Supply.**
V_{DD_RTC}	P	**Real-Time Clock Power Supply.** When RTC is not used, this pin should be connected to V_{DD_EXT}.
GND[1]	G	**Ground.**
V_{DD_THD}	P	**Thermal Diode Power Supply**. When not used, this pin can be left floating.

[1] The exposed pad is required to be electrically and thermally connected to GND. Implement this by soldering the exposed pad to a GND PCB land that is the same size as the exposed pad. The GND PCB land should be *robustly* connected to the GND plane in the PCB for best electrical and thermal performance. See also 88-LFCSP_VQ Lead Assignment and 100-LQFP_EP Lead Assignment.

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 28. DAI/DPI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid	1.5	10	ns

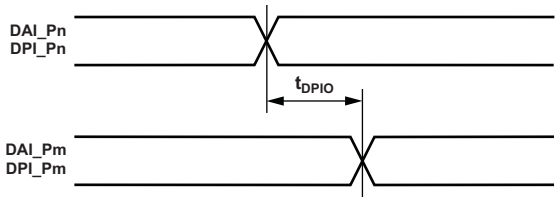

Figure 16. DAI Pin to Pin Direct Routing

AMI Write

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 33. AMI Write

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	AMI_ACK Delay from Address Selects[1, 2]		t_{SDCLK} – 10.1 + W	ns
t_{DSAK}	AMI_ACK Delay from $\overline{\text{AMI\_WR}}$ Low[1, 3]		W – 7.1	ns
Switching Characteristics				
t_{DAWH}	Address Selects to $\overline{\text{AMI\_WR}}$ Deasserted[2]	t_{SDCLK} – 4.4 + W		ns
t_{DAWL}	Address Selects to $\overline{\text{AMI\_WR}}$ Low[2]	t_{SDCLK} – 4.5		ns
t_{WW}	$\overline{\text{AMI\_WR}}$ Pulse Width	W – 1.3		ns
t_{DDWH}	Data Setup Before $\overline{\text{AMI\_WR}}$ High	t_{SDCLK} – 4.3 + W		ns
t_{DWHA}	Address Hold After $\overline{\text{AMI\_WR}}$ Deasserted	H		ns
t_{DWHD}	Data Hold After $\overline{\text{AMI\_WR}}$ Deasserted	H		ns
t_{DATRWH}	Data Disable After $\overline{\text{AMI\_WR}}$ Deasserted[4]	t_{SDCLK} – 1.37 + H	t_{SDCLK} + 6.75 + H	ns
t_{WWR}	$\overline{\text{AMI\_WR}}$ High to $\overline{\text{AMI\_WR}}$ Low[5]	t_{SDCLK} – 1.5 + H		ns
t_{DDWR}	Data Disable Before $\overline{\text{AMI\_RD}}$ Low	2 × t_{SDCLK} – 7.1		ns
t_{WDE}	Data Enabled to $\overline{\text{AMI\_WR}}$ Low	t_{SDCLK} – 4.5		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}

[1] AMI_ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low).
[2] The falling edge of $\overline{\text{AMI\_MSx}}$ is referenced.
[3] Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only applies to asynchronous access mode.
[4] See Test Conditions for calculation of hold times given capacitive and dc loads.
[5] For Write to Write: t_{SDCLK} + H, for both same bank and different bank. For Write to Read: 3 × t_{SDCLK} + H, for the same bank and different banks.

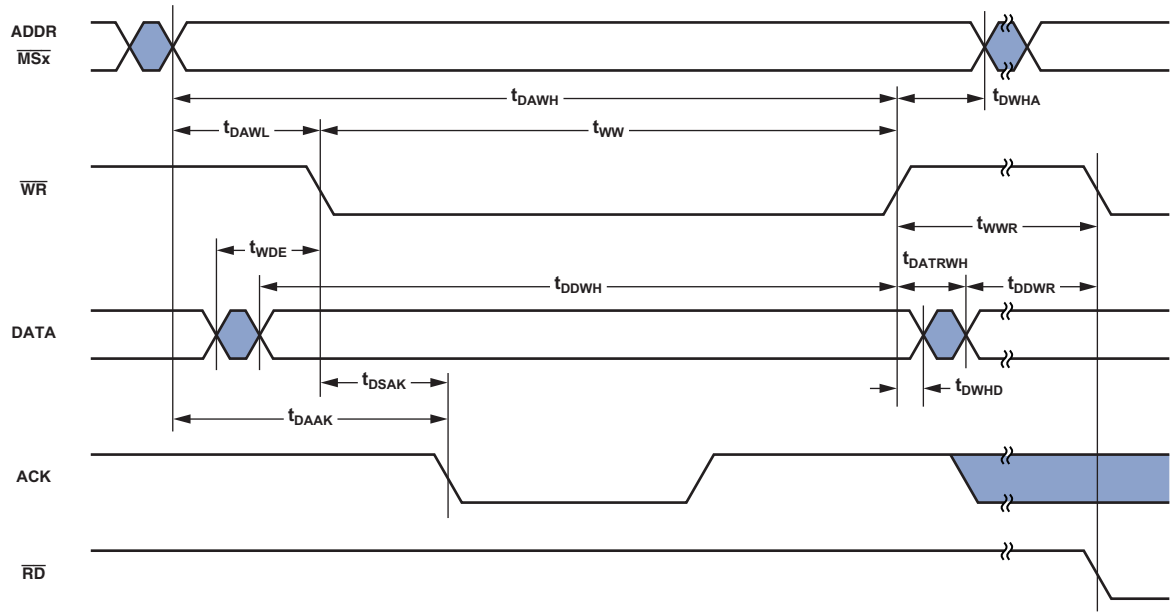

Figure 21. AMI Write

Table 35. Serial Ports—Internal Clock

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	13		10.5		ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5		2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	13		10.5		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		2.5		ns
Switching Characteristics						
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		5		5	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1.0		–1.0		ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		10.7		10.7	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1.0		–1.0		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		4		4	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0		–1.0		ns
t_{SCKLIW}	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

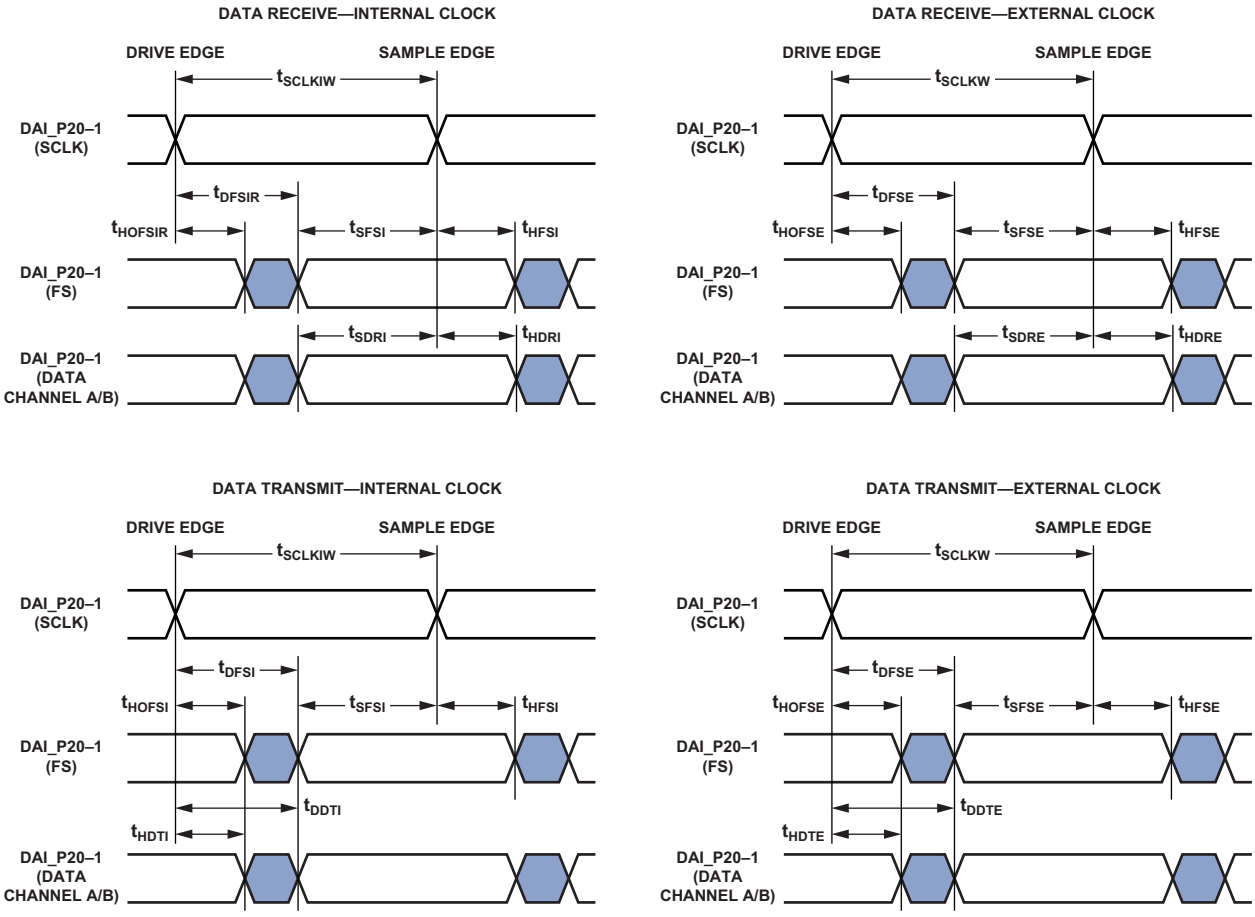

Figure 22. Serial Ports

Table 36. Serial Ports—External Late Frame Sync

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Switching Characteristics						
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0		2 × t_{PCLK}		13.5	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5		0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified as well as DSP serial mode, and MCE = 1, MFD = 0.

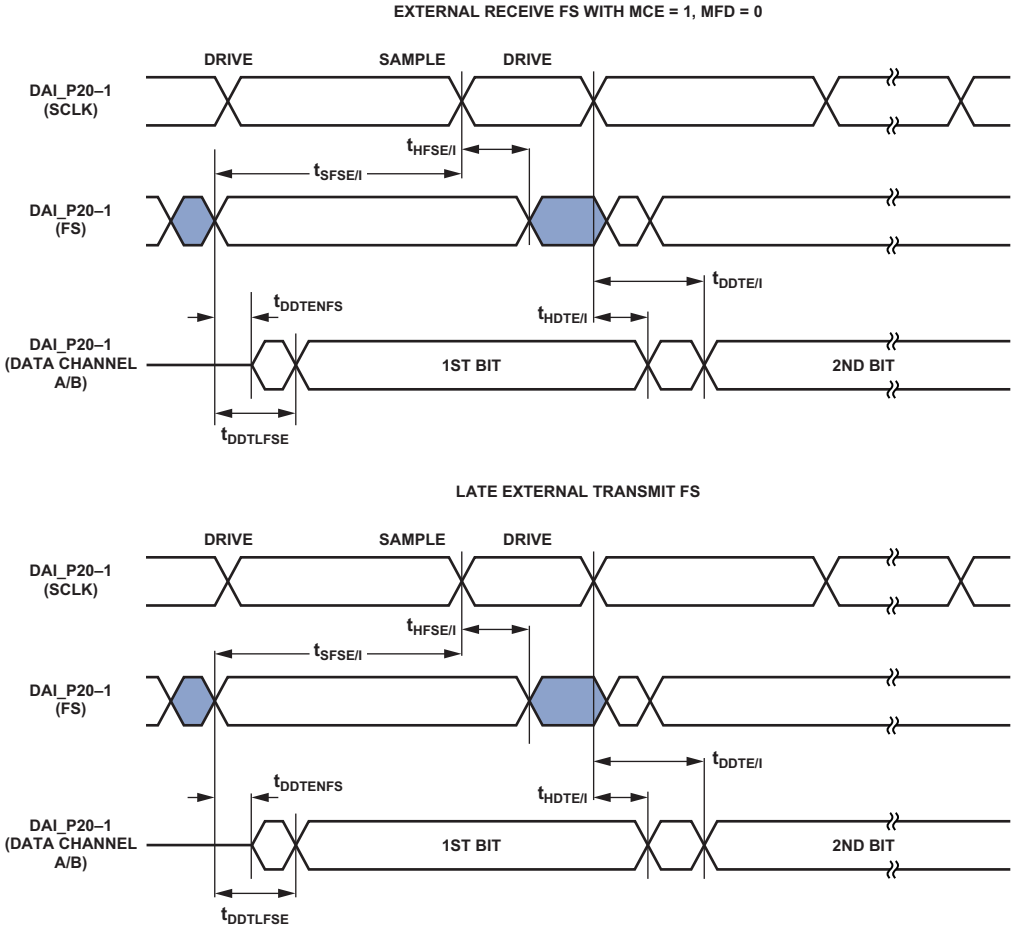

Figure 23. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified mode.

The SPORTx_TDV_O output signal (routing unit) becomes active in SPORT multichannel/packed mode. During transmit slots (enabled with active channel selection registers), the SPORTx_TDV_O is asserted for communication with external devices.

Table 38. Serial Ports—TDV (Transmit Data Valid)

Parameter		88-Lead LFCSP Package		All Other Packages		Unit
		Min	Max	Min	Max	
Switching Characteristics[1]						
t_{DRDVEN}	TDV Assertion Delay from Drive Edge of External Clock	3		3		ns
t_{DFDVEN}	TDV Deassertion Delay from Drive Edge of External Clock		$2 \times t_{PCLK}$		13.25	ns
t_{DRDVIN}	TDV Assertion Delay from Drive Edge of Internal Clock	–0.1		–0.1		ns
t_{DFDVIN}	TDV Deassertion Delay from Drive Edge of Internal Clock		3.5		3.5	ns

[1] Referenced to drive edge.

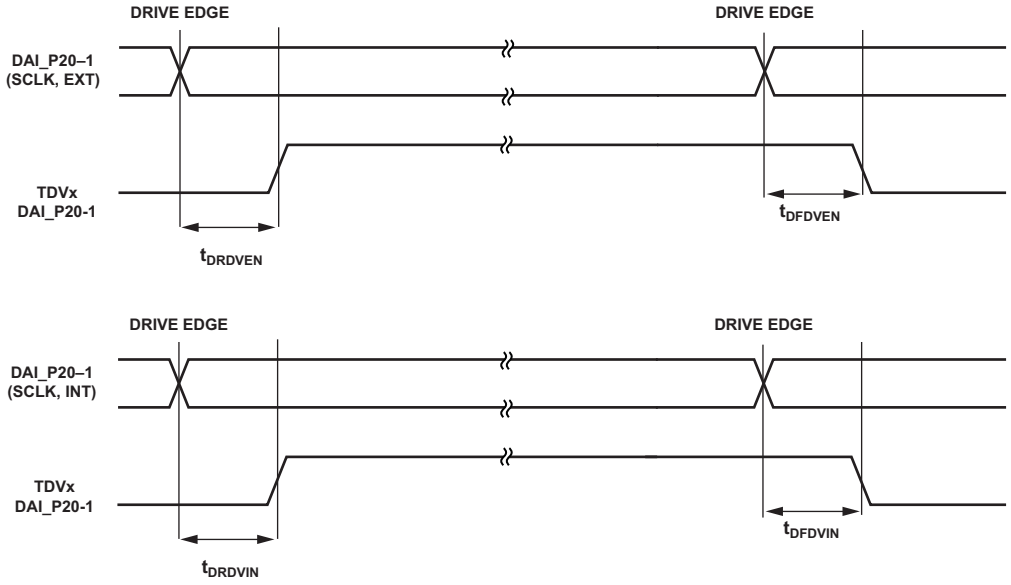

Figure 25. Serial Ports—TDV Internal and External Clock

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the 512 × FS clock.

Table 49. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	FS Delay After Serial Clock		5	ns
t_{HOFSI}	FS Hold After Serial Clock	–2		ns
t_{DDTI}	Transmit Data Delay After Serial Clock		5	ns
t_{HDTI}	Transmit Data Hold After Serial Clock	–2		ns
t_{SCLKIW}[1]	Transmit Serial Clock Width	38.5		ns

[1] The serial clock frequency is 64 × frame sync (FS) where FS = the frequency of LRCLK.

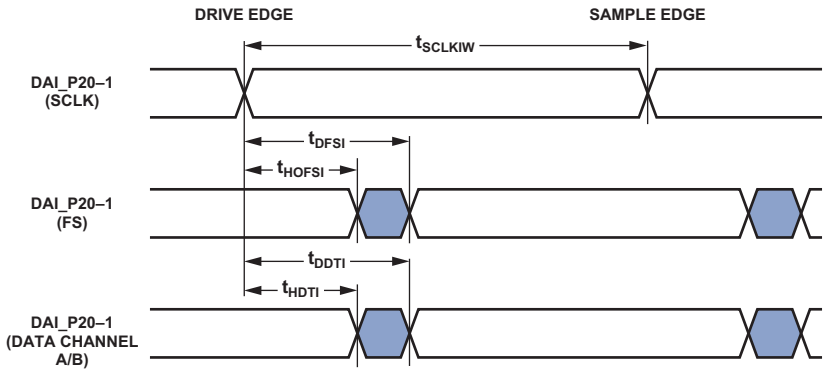

Figure 35. S/PDIF Receiver Internal Digital PLL Mode Timing

SPI Interface—Slave

Table 51. SPI Interface Protocol—Slave Switching and Timing Specifications

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
$t_{SPICLKS}$	Serial Clock Cycle	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SPICHS}	Serial Clock High Period	$2 \times t_{PCLK} - 2$		$2 \times t_{PCLK} - 2$		ns
t_{SPICLS}	Serial Clock Low Period	$2 \times t_{PCLK} - 2$		$2 \times t_{PCLK} - 2$		ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge, CPHASE = 0 or CPHASE = 1	$2 \times t_{PCLK}$		$2 \times t_{PCLK}$		ns
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0	$2 \times t_{PCLK}$		$2 \times t_{PCLK}$		ns
t_{SSPIDS}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	2		2		ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	2		2		ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE = 0)	$2 \times t_{PCLK}$		$2 \times t_{PCLK}$		ns
Switching Characteristics						
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	0	13	0	10.25	ns
t_{DSOE}[1]	$\overline{SPIDS}$ Assertion to Data Out Active (SPI2)	0	13	0	10.25	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	0	$2 \times t_{PCLK}$	0	13.25	ns
t_{DSDHI}[1]	$\overline{SPIDS}$ Deassertion to Data High Impedance (SPI2)	0	$2 \times t_{PCLK}$	0	13.25	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		13		11.5	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$2 \times t_{PCLK}$		$2 \times t_{PCLK}$		ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$5 \times t_{PCLK}$		$5 \times t_{PCLK}$	ns

[1] The timing for these parameters applies when the SPI is routed through the signal routing unit. For more information, see the processor hardware reference, "Serial Peripheral Interface Port (SPI)" chapter.

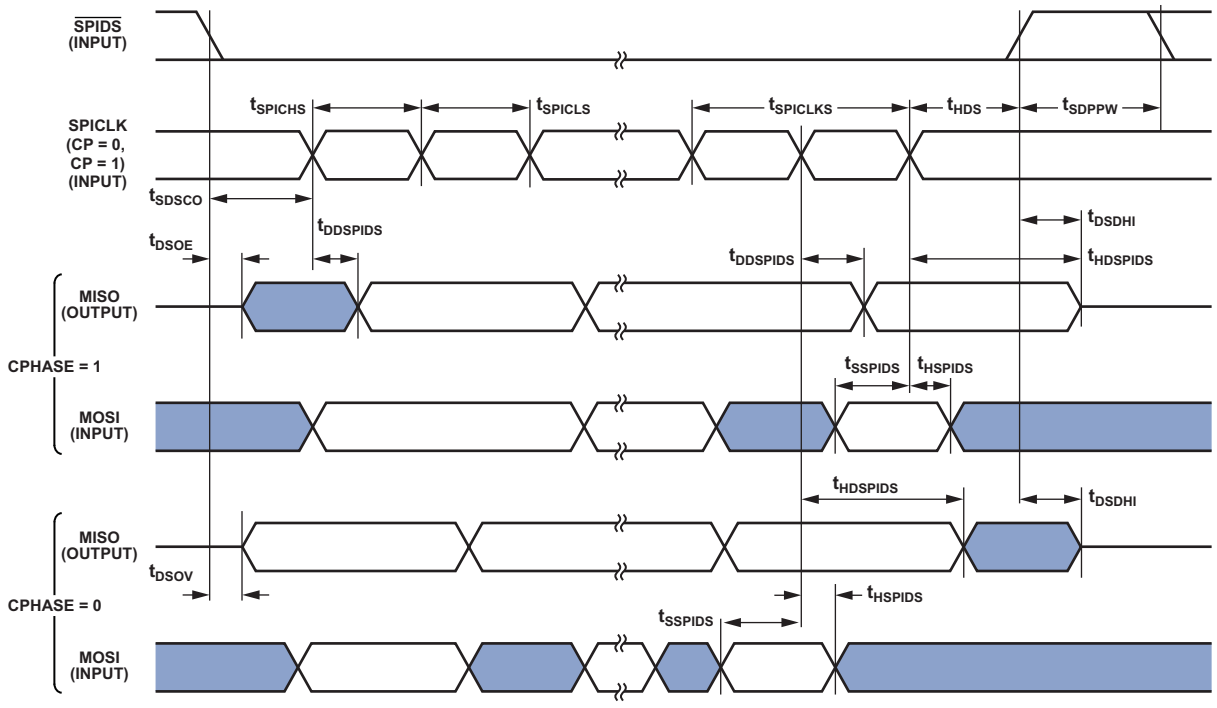

Figure 37. SPI Slave Timing

OUTPUT DRIVE CURRENTS

Table 56 shows the driver types and the pins associated with each driver. Figure 47 shows typical I-V characteristics for each driver. The curves represent the current drive capability of the output drivers as a function of output voltage.

Table 56. Driver Types

Driver Type	Associated Pins
A	FLAG[0–3], AMI_ADDR[23–0], DATA[15–0], $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, AMI_ACK, $\overline{\text{MS}}$[1-0], $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, SDDQM, SDCKE, SDA10, $\overline{\text{EMU}}$, TDO, $\overline{\text{RESETOUT}}$, DPI[1–14], DAI[1–20], $\overline{\text{WDTRSTO}}$, MLBDAT, MLBSIG, MLBSO, MLBDO, MLBCLK, $\overline{\text{SR\_CLR}}$, SR_LAT, SR_LDO[17–0], SR_SCLK, SR_SDI
B	SDCLK, RTCLKOUT

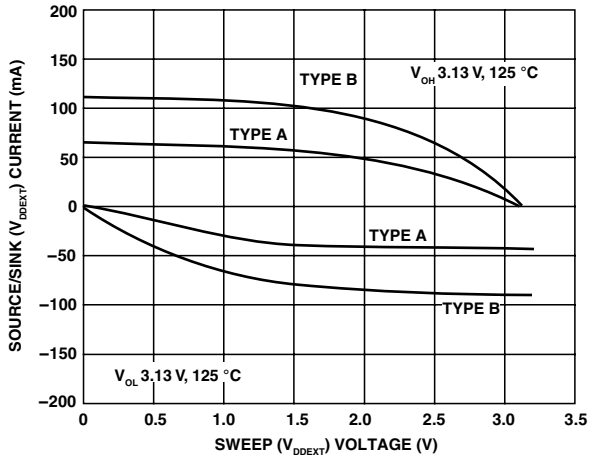

Figure 47. Typical Drive at Junction Temperature

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 21 through Table 55. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 48.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 49. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

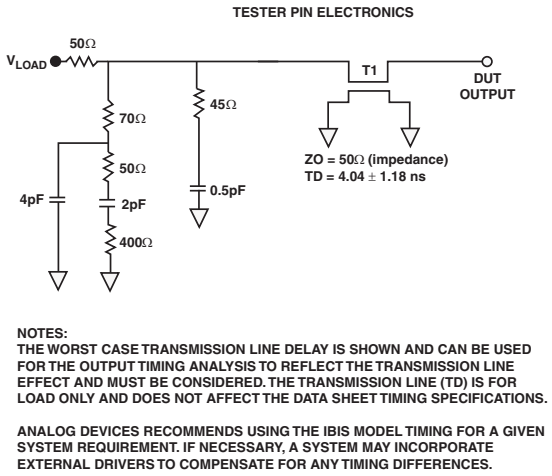

Figure 48. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

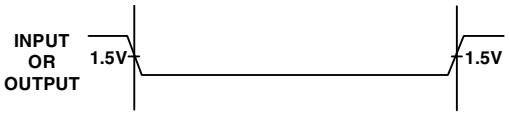

Figure 49. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 48). Figure 52 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 50, Figure 51, and Figure 52 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

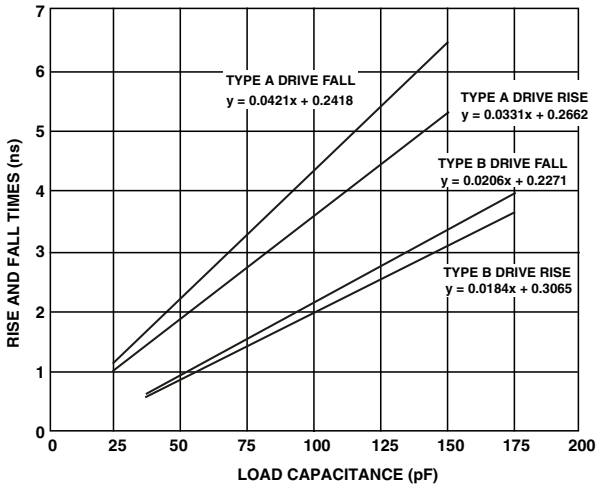

Figure 50. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Max)

88-LFCSP_VQ LEAD ASSIGNMENT

Table 61 lists the 88-Lead LFCSP_VQ package lead names.

Table 61. 88-Lead LFCSP_VQ Lead Assignments (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
CLK_CFG1	1	V_{DD_EXT}	23	DAI_P10	45	V_{DD_INT}	67
BOOT_CFG0	2	DPI_P08	24	V_{DD_INT}	46	FLAG0	68
V_{DD_EXT}	3	DPI_P07	25	V_{DD_EXT}	47	V_{DD_INT}	69
V_{DD_INT}	4	DPI_P09	26	DAI_P20	48	FLAG1	70
BOOT_CFG1	5	DPI_P10	27	V_{DD_INT}	49	FLAG2	71
GND	6	DPI_P11	28	DAI_P08	50	FLAG3	72
CLK_CFG0	7	DPI_P12	29	DAI_P04	51	GND	73
V_{DD_INT}	8	DPI_P13	30	DAI_P14	52	GND	74
CLKIN	9	DAI_P03	31	DAI_P18	53	V_{DD_EXT}	75
XTAL	10	DPI_P14	32	DAI_P17	54	GND	76
V_{DD_EXT}	11	V_{DD_INT}	33	DAI_P16	55	V_{DD_INT}	77
V_{DD_INT}	12	DAI_P13	34	DAI_P15	56	$\overline{TRST}$	78
V_{DD_INT}	13	DAI_P07	35	DAI_P12	57	$\overline{EMU}$	79
$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	14	DAI_P19	36	DAI_P11	58	TDO	80
V_{DD_INT}	15	DAI_P01	37	V_{DD_INT}	59	V_{DD_EXT}	81
DPI_P01	16	DAI_P02	38	GND	60	V_{DD_INT}	82
DPI_P02	17	V_{DD_INT}	39	THD_M	61	TDI	83
DPI_P03	18	V_{DD_EXT}	40	THD_P	62	TCK	84
V_{DD_INT}	19	V_{DD_INT}	41	V_{DD_THD}	63	V_{DD_INT}	85
DPI_P05	20	DAI_P06	42	V_{DD_INT}	64	$\overline{RESET}$	86
DPI_P04	21	DAI_P05	43	V_{DD_INT}	65	TMS	87
DPI_P06	22	DAI_P09	44	V_{DD_INT}	66	V_{DD_INT}	88
						GND	89*

* Lead no. 89 is the GND supply (see Figure 53 and Figure 54) for the processor; this pad must be **robustly** connected to GND in order for the processor to function.

OUTLINE DIMENSIONS

The processors are available in 88-lead LFCSP_VQ, 100-lead LQFP_EP and 196-ball CSP_BGA RoHS compliant packages. For package assignment by model, see Ordering Guide.

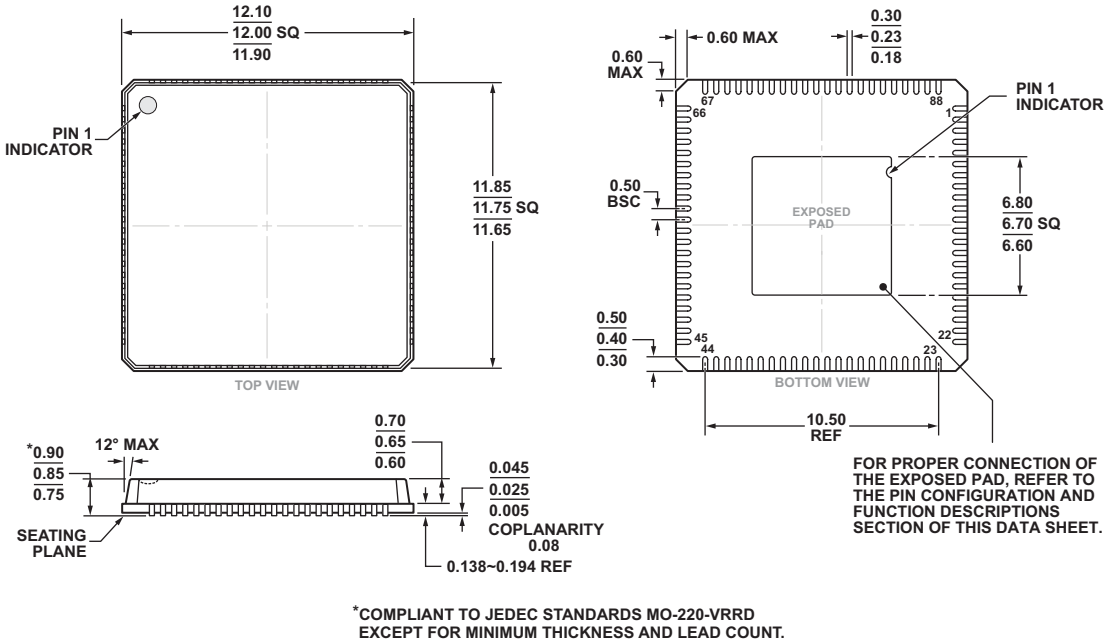

Figure 57. 88-Lead Lead Frame Chip Scale Package [LFCSP_VQ[1]]
(CP-88-5)
Dimensions Shown in Millimeters

[1] For information relating to the exposed pad on the CP-88-5 package, see the table endnote on Page 68.

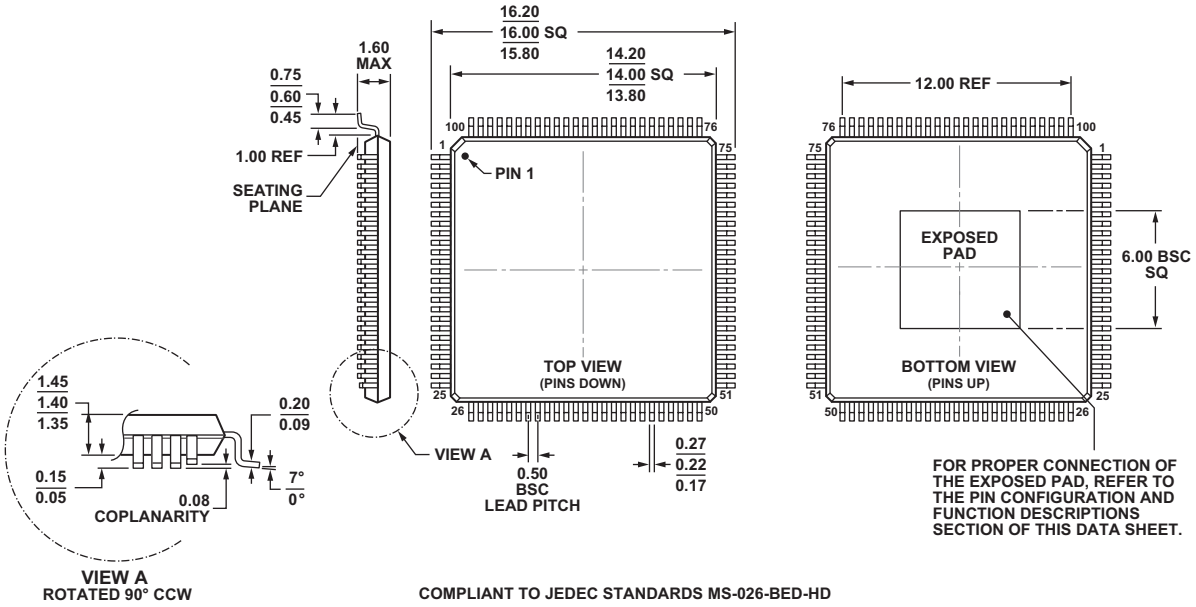

Figure 58. 100-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP[1]]
(SW-100-2)
Dimensions shown in millimeters

[1] For information relating to the exposed pad on the SW-100-2 package, see the table endnote on Page 70.

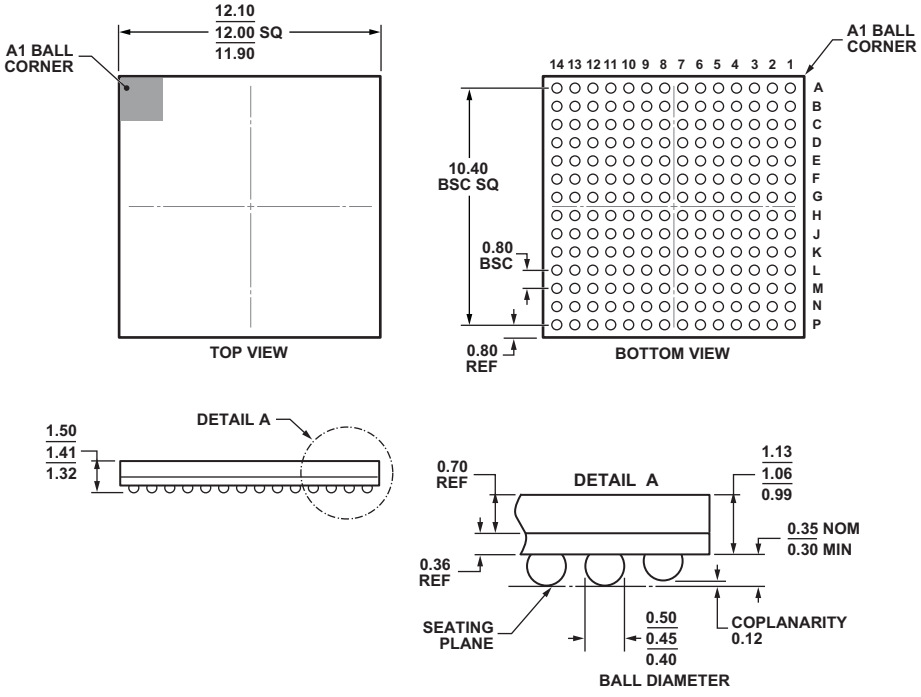

Figure 59. 196-Ball Chip Scale Package, Ball Grid Array [CSP_BGA]
(BC-196-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range[2]	On-Chip SRAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21477KCPZ-1A	0°C to +70°C	2M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21477KSWZ-1A	0°C to +70°C	2M Bits	200 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21477BCPZ-1A	–40°C to +85°C	2M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21478KCPZ-1A	0°C to +70°C	3M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21478BCPZ-1A	–40°C to +85°C	3M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21478BBCZ-2A	–40°C to +85°C	3M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478BSWZ-2A	–40°C to +85°C	3M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21478KBCZ-1A	0°C to +70°C	3M Bits	200 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478KBCZ-2A	0°C to +70°C	3M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478KBCZ-3A	0°C to +70°C	3M Bits	300 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478KSWZ-1A	0°C to +70°C	3M Bits	200 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21478KSWZ-2A	0°C to +70°C	3M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21479KCPZ-1A	0°C to +70°C	5M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21479BCPZ-1A	–40°C to +85°C	5M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21479BBCZ-2A	–40°C to +85°C	5M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479BSWZ-2A	–40°C to +85°C	5M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21479KBCZ-1A	0°C to +70°C	5M Bits	200 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479KBCZ-2A	0°C to +70°C	5M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479KBCZ-3A	0°C to +70°C	5M Bits	300 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479KSWZ-1A	0°C to +70°C	5M Bits	200 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21479KSWZ-2A	0°C to +70°C	5M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2

[1] Z =RoHS compliant part.
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions for junction temperature (T_J) specification, which is the only temperature specification.