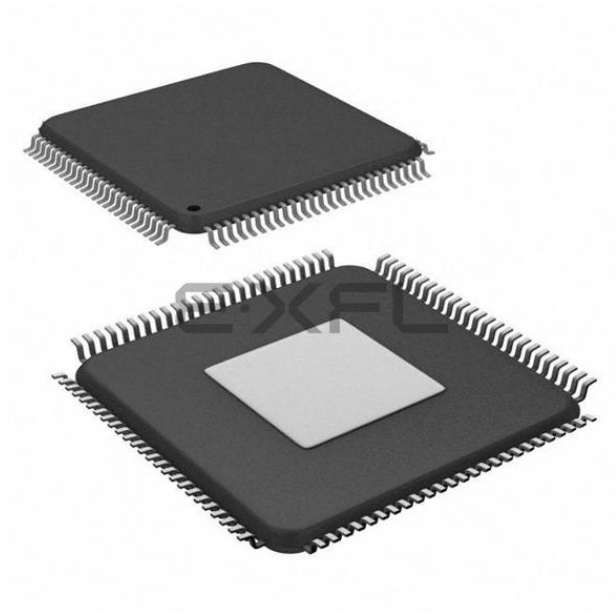

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI, EBI/EMI, I²C, SPI, SPORT, UART/USART
Clock Rate	266MHz
Non-Volatile Memory	ROM (4Mbit)
On-Chip RAM	3Mbit
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	100-LQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21478kswz-2a

buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

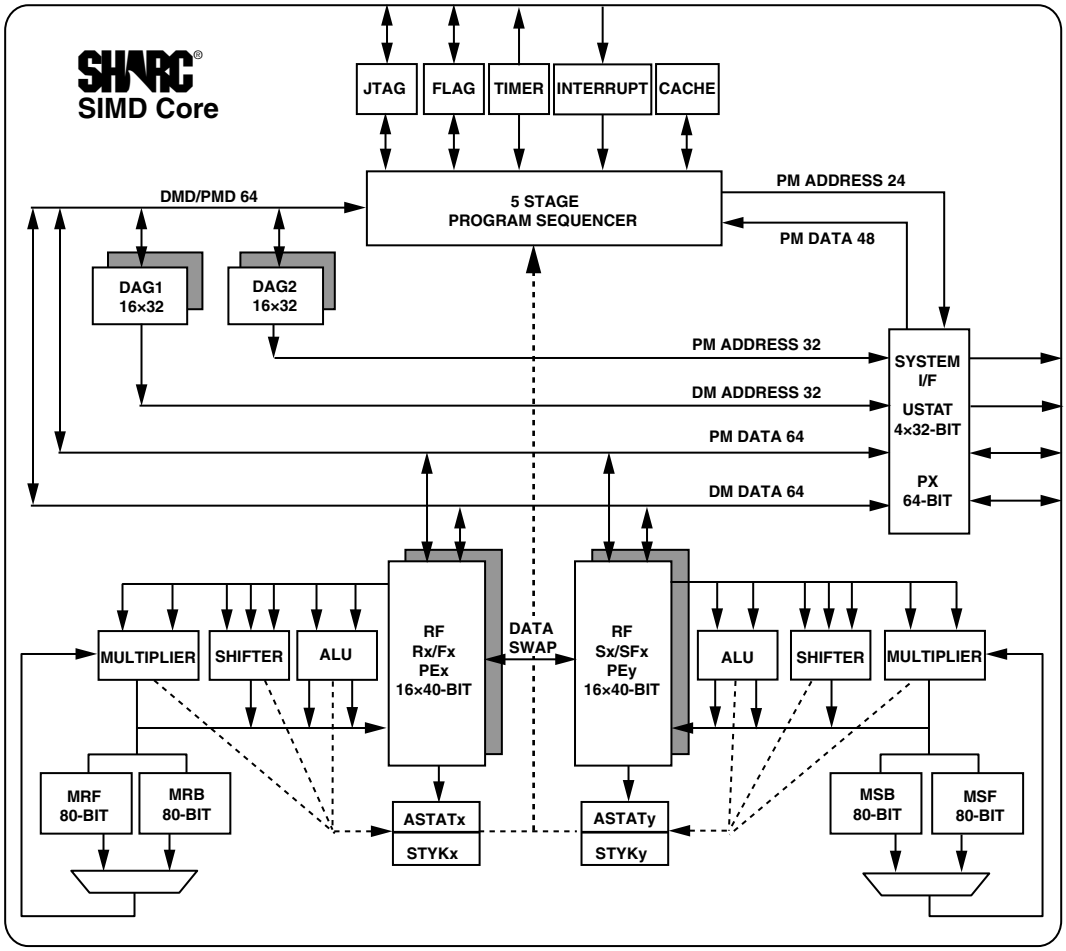

Figure 2. SHARC Core Block Diagram

Instruction Cache

The processor includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full speed execution of core looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators with Zero-Overhead Hardware Circular Buffer Support

The processor's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the processors contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the processors can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

Variable Instruction Set Architecture (VISA)

In addition to supporting the standard 48-bit instructions from previous SHARC processors, the processors support new instructions of 16 and 32 bits. This feature, called Variable Instruction Set Architecture (VISA), drops redundant/unused

Table 4. ADSP-21478 Internal Memory Space (3M bits)[1]

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 3FFF
Block 0 SRAM 0x0004 9000–0x0004 CFFF	Block 0 SRAM 0x0008 C000–0x0009 1554	Block 0 SRAM 0x0009 2000–0x0009 9FFF	Block 0 SRAM 0x0012 4000–0x0013 3FFF
Reserved 0x0004 D000–0x0004 FFFF	Reserved 0x0009 1555–0x0009 FFFF	Reserved 0x0009 A000–0x0009 FFFF	Reserved 0x0013 4000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000A FFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 CFFF	Block 1 SRAM 0x000A C000–0x000B 1554	Block 1 SRAM 0x000B 2000–0x000B 9FFF	Block 1 SRAM 0x0016 4000–0x0017 3FFF
Reserved 0x0005 D000–0x0005 FFFF	Reserved 0x000B 1555–0x000B FFFF	Reserved 0x000B A000–0x000B FFFF	Reserved 0x0017 4000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 1FFF	Block 2 SRAM 0x000C 0000–0x000C 2AA9	Block 2 SRAM 0x000C 0000–0x000C 3FFF	Block 2 SRAM 0x0018 0000–0x0018 7FFF
Reserved 0x0006 2000– 0x0006 FFFF	Reserved 0x000C 2AAA–0x000D FFFF	Reserved 0x000C 4000–0x000D FFFF	Reserved 0x0018 8000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 1FFF	Block 3 SRAM 0x000E 0000–0x000E 2AA9	Block 3 SRAM 0x000E 0000–0x000E 3FFF	Block 3 SRAM 0x001C 0000–0x001C 7FFF
Reserved 0x0007 2000–0x0007 FFFF	Reserved 0x000E 2AAA–0x000F FFFF	Reserved 0x000E 4000–0x000F FFFF	Reserved 0x001C 8000–0x001F FFFF

[1] Some processors include a customer-definable ROM block. ROM addresses on these models are not reserved as shown in this table. Please contact your Analog Devices sales representative for additional details.

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface ports (SPI), one universal asynchronous receiver-transmitter (UART), 12 flags, a 2-wire interface (TWI), three PWM modules (PWM3–1), and two general-purpose timers.

Serial Peripheral (Compatible) Interface (SPI)

The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible port to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multi-master environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The SPI-compatible port uses open drain drivers to support a multi-master configuration and to avoid data contention.

UART Port

The processors provide a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Support for bit rates ranging from (f_{PCLK}/1,048,576) to (f_{PCLK}/16) bits per second.
- Support for data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs generating 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

PWM signals can be mapped to the external port address lines or to the DPI pins.

Timers

The processors have a total of three timers: a core timer that can generate periodic software interrupts and two general-purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watch dog mode

The core timer can be configured to use FLAG3 as a timer expired signal, and the general-purpose timers have one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables the general-purpose timer.

2-Wire Interface Port (TWI)

The TWI is a bidirectional 2-wire serial bus used to move 8-bit data while maintaining compliance with the I^2C bus protocol. The TWI master incorporates the following features:

- 7-bit addressing
- Simultaneous master and slave operation on multiple device systems with support for multi-master data arbitration
- Digital filtering and timed event processing
- 100 kbps and 400 kbps data rates
- Low interrupt rate

PIN FUNCTION DESCRIPTIONS

Table 11. Pin Descriptions

Name	Type	State During/ After Reset	Description
$ADDR_{23-0}$	I/O/T (ipu)	High-Z/driven low (boot)	**External Address.** The processor outputs addresses for external memory and peripherals on these pins. The ADDR pins can be multiplexed to support the external memory interface address, FLAGS15–8 (I/O) and PWM (O). After reset, all ADDR pins are in EMIF mode, and FLAG(0–3) pins are in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the $ADDR_{23-4}$ pins for parallel input data.
$DATA_{15-0}$	I/O/T (ipu)	High-Z	**External Data.** The data pins can be multiplexed to support the external memory interface data (I/O) and $FLAGS_{7-0}$ (I/O).
AMI_ACK	I (ipu)		**Memory Acknowledge.** External devices can deassert AMI_ACK (low) to add wait states to an external memory access. AMI_ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{MS}_{0-1}$	O/T (ipu)	High-Z	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{1-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, when the condition evaluates as true. The $\overline{MS1}$ pin can be used in EPORT/FLASH boot mode. For more information on processor booting, see the *ADSP-214xx SHARC Processor Hardware Reference*.
$\overline{AMI\_RD}$	O/T (ipu)	High-Z	**AMI Port Read Enable.** $\overline{AMI\_RD}$ is asserted whenever the processor reads a word from external memory.
$\overline{AMI\_WR}$	O/T (ipu)	High-Z	**AMI Port Write Enable.** $\overline{AMI\_WR}$ is asserted when the processor writes a word to external memory.
FLAG0/$\overline{IRQ0}$	I/O (ipu)	FLAG[0] INPUT	**FLAG0/Interrupt Request0.**
FLAG1/$\overline{IRQ1}$	I/O (ipu)	FLAG[1] INPUT	**FLAG1/Interrupt Request1.**
FLAG2/$\overline{IRQ2}$/$\overline{MS2}$	I/O (ipu)	FLAG[2] INPUT	**FLAG2/Interrupt Request2/Memory Select2.** This pin is multiplexed with $\overline{MS2}$ in the 196-ball BGA package only.
FLAG3/TMREXP/$\overline{MS3}$	I/O (ipu)	FLAG[3] INPUT	**FLAG3/Timer Expired/Memory Select3.** This pin is multiplexed with $\overline{MS3}$ in the 196-ball BGA package only.

The following symbols appear in the Type column of Table 11: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be 26 kΩ to 63 kΩ. The range of an ipd resistor can be 31 kΩ to 85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.

Not all pins are available in the 88-lead LFCSP_VQ and 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 62 on Page 70.

Table 11. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
THD_P	I		**Thermal Diode Anode.** When not used, this pin can be left floating.
THD_M	O		**Thermal Diode Cathode.** When not used, this pin can be left floating.
MLBCLK	I		**Media Local Bus Clock.** This clock is generated by the MLB controller that is synchronized to the MOST network and provides the timing for the entire MLB interface at 49.152 MHz at FS = 48 kHz. When the MLB controller is not used, this pin should be grounded.
MLBDAT	I/O/T in 3 pin mode. I in 5 pin mode.	High-Z	**Media Local Bus Data.** The MLBDAT line is driven by the transmitting MLB device and is received by all other MLB devices including the MLB controller. The MLBDAT line carries the actual data. In 5-pin MLB mode, this pin is an input only. When the MLB controller is not used, this pin should be grounded.
MLBSIG	I/O/T in 3 pin mode. I in 5 pin mode	High-Z	**Media Local Bus Signal.** This is a multiplexed signal which carries the Channel/Address generated by the MLB Controller, as well as the Command and RxStatus bytes from MLB devices. In 5-pin mode, this pin is input only. When the MLB controller is not used, this pin should be grounded.
MLBDO	O/T	High-Z	**Media Local Bus Data Output (in 5 Pin Mode).** This pin is used only in 5-pin MLB mode and serves as the output data pin. When the MLB controller is not used, this pin should be grounded.
MLBSO	O/T	High-Z	**Media Local Bus Signal Output (in 5 Pin Mode).** This pin is used only in 5-pin MLB mode and serves as the output signal pin. When the MLB controller is not used, this pin should be grounded.
SR_SCLK	I (ipu)		**Shift Register Serial Clock.** (Active high, rising edge sensitive)
$\overline{\text{SR\_CLR}}$	I (ipu)		**Shift Register Reset.** (Active low)
SR_SDI	I (ipu)		**Shift Register Serial Data Input.**
SR_SDO	O (ipu)	Driven Low	**Shift Register Serial Data Output.**
SR_LAT	I (ipu)		**Shift Register Latch Clock Input.** (Active high, rising edge sensitive)
SR_LDO_{17-0}	O/T (ipu)	High-Z	**Shift Register Parallel Data Output.**
RTXI	I		**RTC Crystal Input.** If RTC is not used, then this pin can be NC (no connect) or grounded and the RTC_PDN and RTC_BUSDIS bits of the RTC_INIT register must be set to 1.
RTXO	O		**RTC Crystal Output.** If RTC is not used, then this pin needs to be NC (No Connect).
RTCLKOUT	O (ipd)		**RTC Clock Output.** For calibration purposes. The clock runs at 1 Hz. If RTC is not used, then this pin needs to be NC (No Connect).

The following symbols appear in the Type column of Table 11: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be 26 kΩ to 63 kΩ. The range of an ipd resistor can be 31 kΩ to 85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.

Not all pins are available in the 88-lead LFCSP_VQ and 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 62 on Page 70.

Table 12. Pin List, Power and Ground

Name	Type	Description
V_{DD_INT}	P	**Internal Power Supply.**
V_{DD_EXT}	P	**I/O Power Supply.**
V_{DD_RTC}	P	**Real-Time Clock Power Supply.** When RTC is not used, this pin should be connected to V_{DD_EXT}.
GND[1]	G	**Ground.**
V_{DD_THD}	P	**Thermal Diode Power Supply**. When not used, this pin can be left floating.

[1] The exposed pad is required to be electrically and thermally connected to GND. Implement this by soldering the exposed pad to a GND PCB land that is the same size as the exposed pad. The GND PCB land should be *robustly* connected to the GND plane in the PCB for best electrical and thermal performance. See also 88-LFCSP_VQ Lead Assignment and 100-LQFP_EP Lead Assignment.

Running Reset

The following timing specification applies to $\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$ pin when it is configured as $\overline{\text{RUNRSTIN}}$.

Table 22. Running Reset

Parameter		Min	Max	Unit
Timing Requirements				
$t_{WRUNRST}$	Running $\overline{\text{RESET}}$ Pulse Width Low	$4 \times t_{CK}$		ns
$t_{SRUNRST}$	Running $\overline{\text{RESET}}$ Setup Before CLKIN High	8		ns

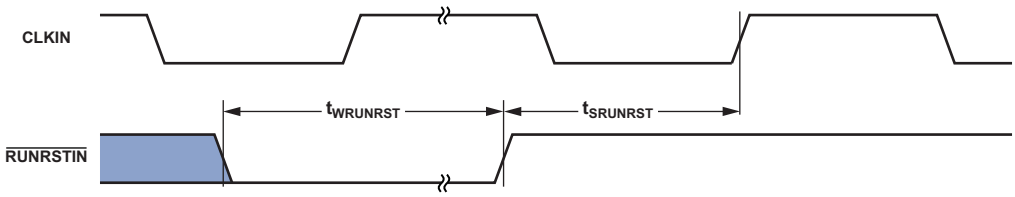

Figure 10. Running Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts, as well as the DAI_P20–1 and DPI_P14–1 pins when they are configured as interrupts.

Table 23. Interrupts

Parameter		Min	Max	Unit
Timing Requirement				
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	$2 \times t_{PCLK} + 2$		ns

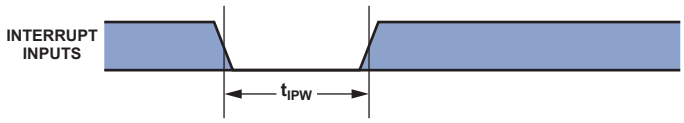

Figure 11. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

Table 24. Core Timer

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Switching Characteristic						
t_{WCTIM}	TMREXP Pulse Width	$4 \times t_{PCLK} - 1.55$		$4 \times t_{PCLK} - 1.2$		ns

Figure 12. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to timer0 and timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 25. Timer PWM_OUT Timing

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Switching Characteristic						
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 1.65$	$2 \times (2^{31} - 1) \times t_{PCLK}$	$2 \times t_{PCLK} - 1.2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

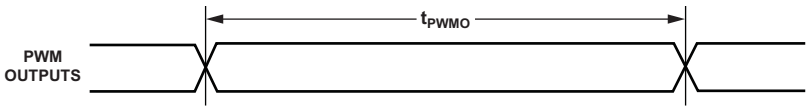

Figure 13. Timer PWM_OUT Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example, DAI_PB01_I to DAI_PB02_O).

Table 28. DAI/DPI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid	1.5	10	ns

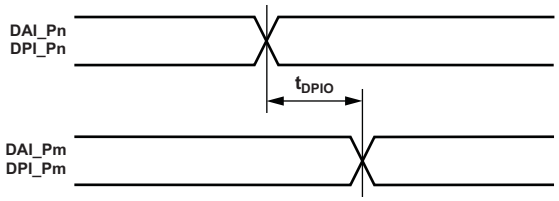

Figure 16. DAI Pin to Pin Direct Routing

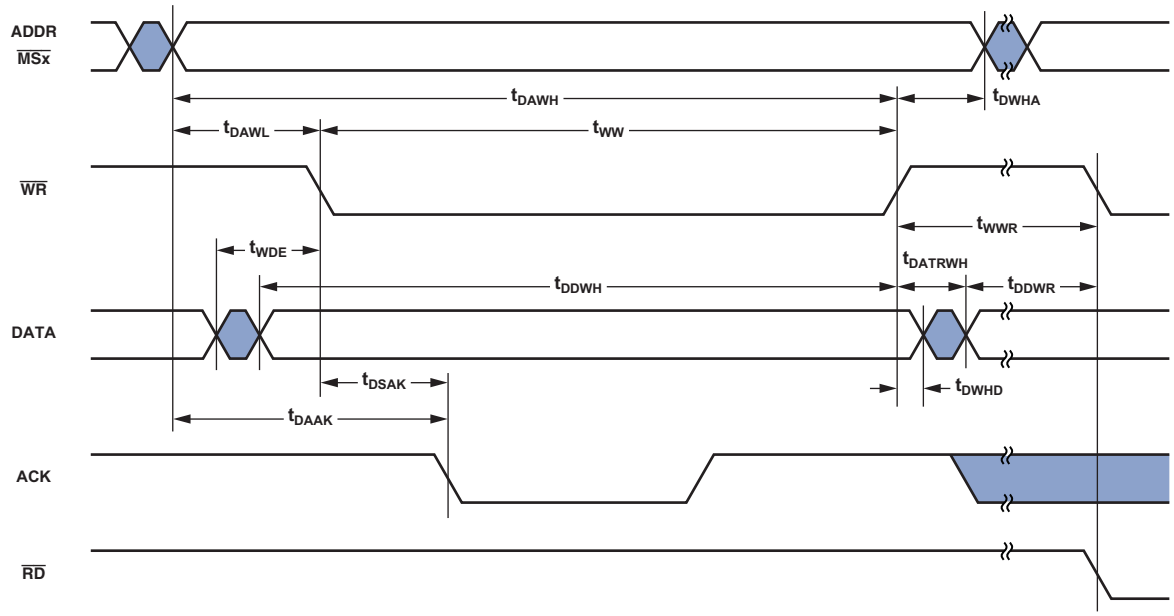

Figure 21. AMI Write

Serial Ports

In slave transmitter mode and master receiver mode, the maximum serial port frequency is $f_{PCLK}/8$. In master transmitter mode and slave receiver mode, the maximum serial port clock frequency is $f_{PCLK}/4$.

To determine whether communication is possible between two devices at clock speed, n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Serial port signals (SCLK, FS, Data Channel A, Data Channel B) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 34. Serial Ports—External Clock

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{SFSE}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	4		2.5		ns
t_{HFSE}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	4		2.5		ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	4		2.5		ns
t_{HDRE}[1]	Receive Data Hold After SCLK	4		2.5		ns
t_{SCLKW}	SCLK Width	$(t_{PCLK} \times 4) \div 2 - 1.5$		$(t_{PCLK} \times 4) \div 2 - 1.5$		ns
t_{SCLK}	SCLK Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns
Switching Characteristics						
t_{DFSE}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)		15		15	ns
t_{HOFSE}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)	2		2		ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK		15		15	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	2		2		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 36. Serial Ports—External Late Frame Sync

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Switching Characteristics						
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0		2 × t_{PCLK}		13.5	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5		0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified as well as DSP serial mode, and MCE = 1, MFD = 0.

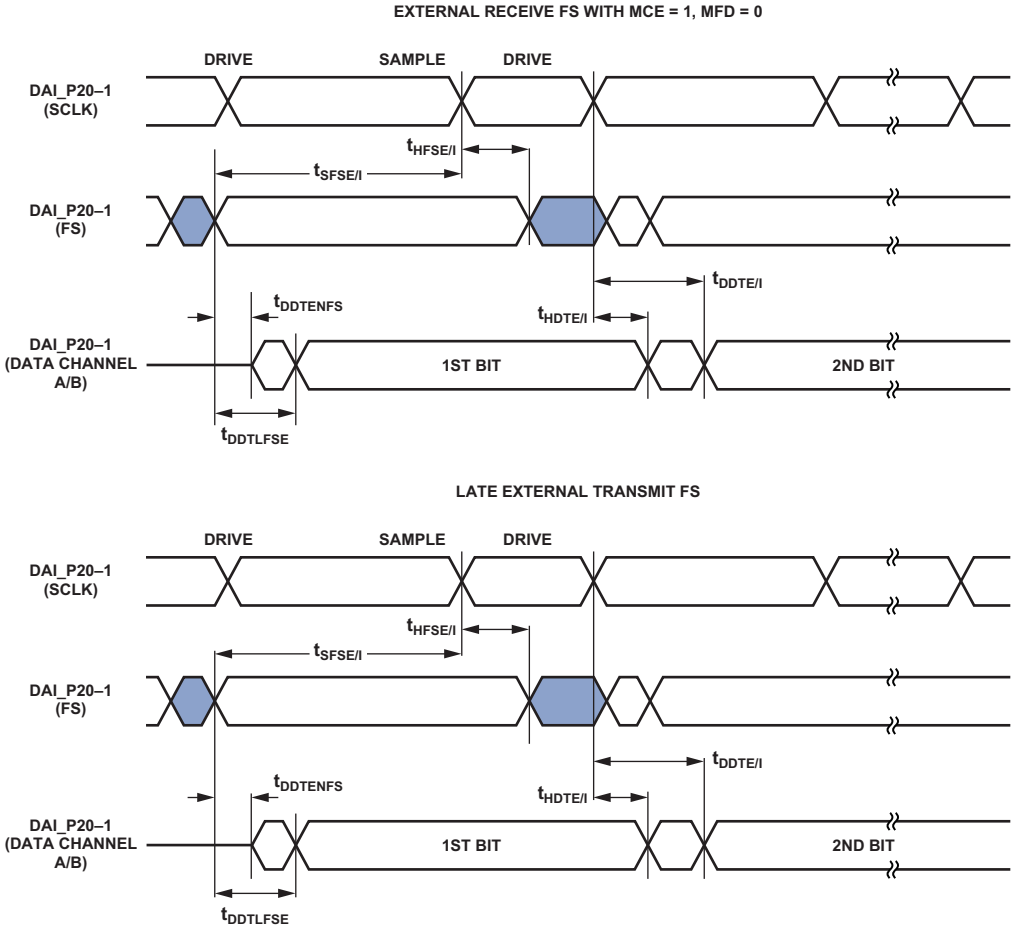

Figure 23. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified mode.

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 39. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 39. Input Data Port (IDP)

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4.5		3.8		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		2.5		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	4		2.5		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		2.5		ns
$t_{IDPCLKW}$	Clock Width	$(t_{PCLK} \times 4) \div 2 - 1$		$(t_{PCLK} \times 4) \div 2 - 1$		ns
t_{IDPCLK}	Clock Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The PCG's input can be either CLKIN or any of the DAI pins.

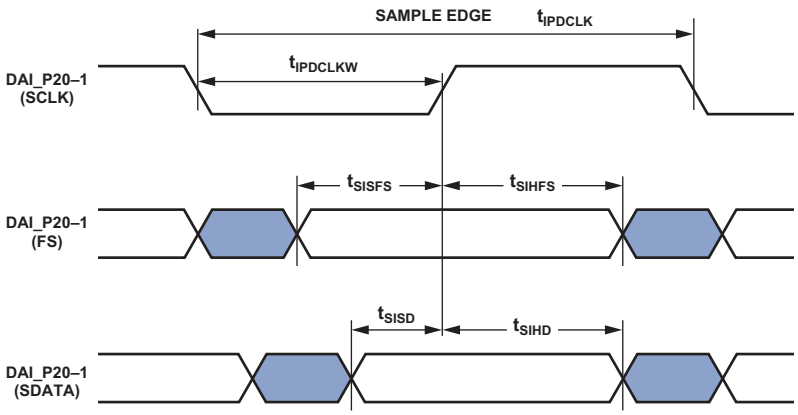

Figure 26. IDP Master Timing

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 40. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the *ADSP-214xx SHARC Processor Hardware Reference*. Note that the 20 bits of external PDAP data can be provided through the ADDR23–0 pins or over the DAI pins.

Table 40. Parallel Data Acquisition Port (PDAP)

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{SPHOLD}[1]	PDAP_HOLD Setup Before PDAP_CLK Sample Edge	4		2.5		ns
t_{HPHOLD}[1]	PDAP_HOLD Hold After PDAP_CLK Sample Edge	4		2.5		ns
t_{PDSD}[1]	PDAP_DAT Setup Before SCLK PDAP_CLK Sample Edge	5		3.85		ns
t_{PDHD}[1]	PDAP_DAT Hold After SCLK PDAP_CLK Sample Edge	4		2.5		ns
t_{PDCLKW}	Clock Width	$(t_{PCLK} \times 4) \div 2 - 3$		$(t_{PCLK} \times 4) \div 2 - 3$		ns
t_{PDCLK}	Clock Period	$t_{PCLK} \times 4$		$t_{PCLK} \times 4$		ns
Switching Characteristics						
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	$2 \times t_{PCLK} + 3$		$2 \times t_{PCLK} + 3$		ns
t_{PDSTRB}	PDAP Strobe Pulse Width	$2 \times t_{PCLK} - 1.5$		$2 \times t_{PCLK} - 1.5$		ns

[1] Source pins of DATA and control are ADDR23–0 or DAI pins. Source pins for SCLK and FS are: 1) DAI pins, 2) CLKIN through PCG, or 3) DAI pins through PCG.

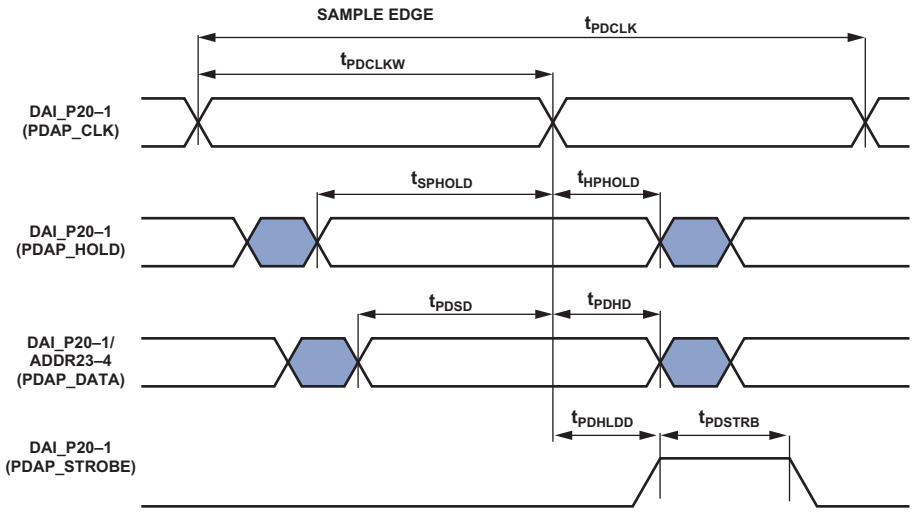

Figure 27. PDAP Timing

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 47. Input signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 47. S/PDIF Transmitter Input Data Timing

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4.5		3		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		3		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	4.5		3		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		3		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		9		ns
$t_{SITXCLK}$	Transmit Clock Period	20		20		ns
$t_{SISCLKW}$	Clock Width	36		36		ns
t_{SISCLK}	Clock Period	80		80		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

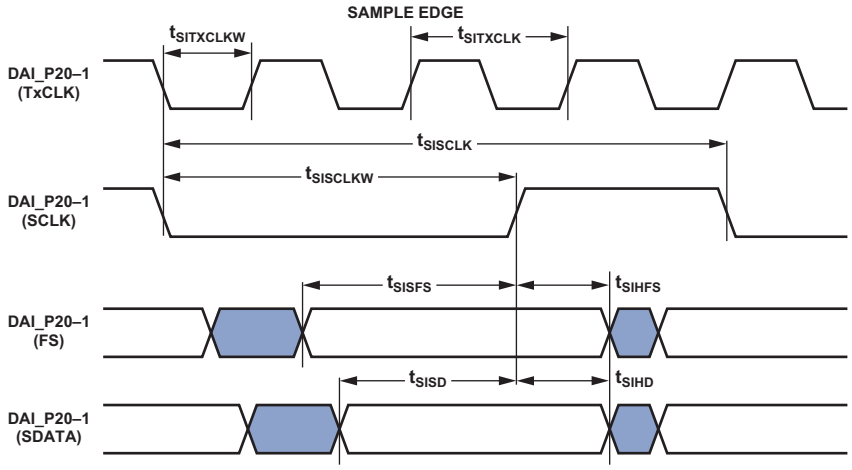

Figure 34. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

Table 48. Oversampling Clock (TxCLK) Switching Characteristics

Parameter	Max	Unit
Frequency for TxCLK = 384 × Frame Sync	Oversampling Ratio × Frame Sync ≤ $1/t_{SITXCLK}$	MHz
Frequency for TxCLK = 256 × Frame Sync	49.2	MHz
Frame Rate (FS)	192.0	kHz

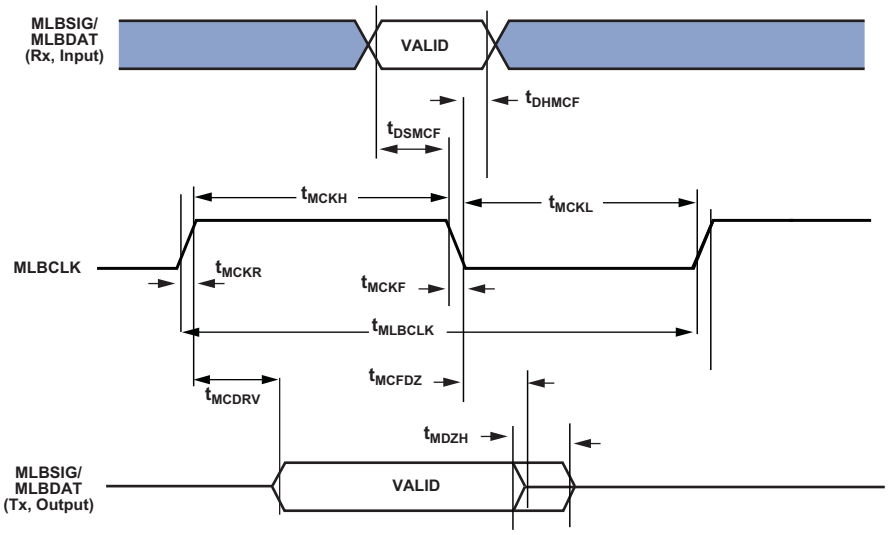

Figure 38. MLB Timing (3-Pin Interface)

Table 53. MLB Interface, 5-Pin Specifications

Parameter		Min	Typ	Max	Unit
5-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})			6	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})			6	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation			2	ns p-p
t_{DSMCF}[2]	DAT/SIG Input Setup Time	3			ns
t_{DHMCF}	DAT/SIG Input Hold Time	5			ns
t_{MCDRV}	DS/DO Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MCRDL}[3]	DO/SO Low From MLBCLK High				
	512 FS			10	ns
	256 FS			20	ns
C_{mlb}	DS/DO Pin Load			40	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (p-p).
[2] Gate delays due to OR'ing logic on the pins must be accounted for.
[3] When a node is not driving valid data onto the bus, the MLBSO and MLBDO output lines shall remain low. If the output lines can float at anytime, including while in reset, external pull-down resistors are required to keep the outputs from corrupting the MediaLB signal lines when not being driven.

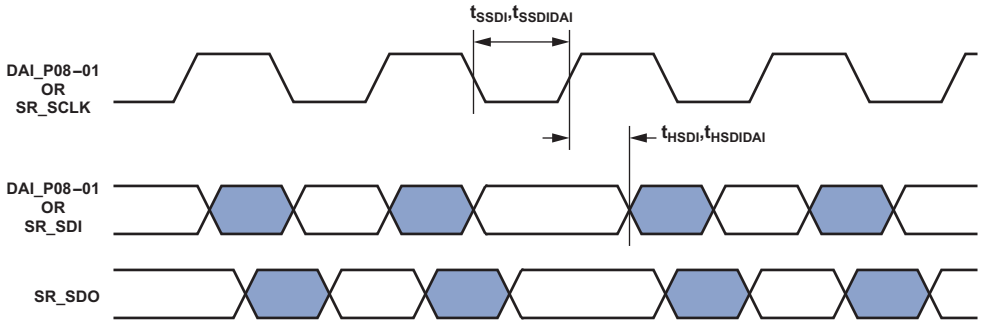

Figure 41. SR_SDI Setup, Hold

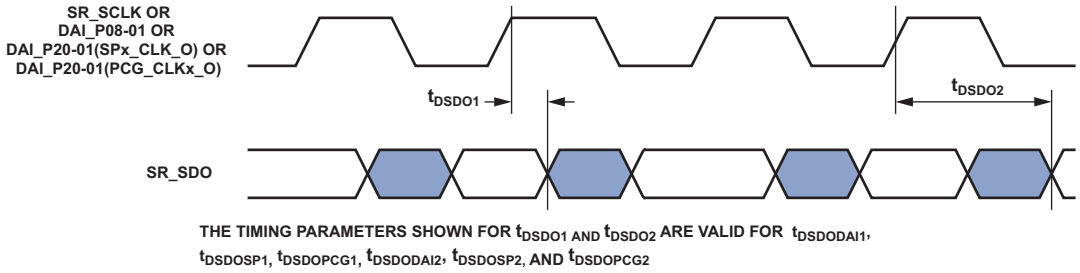

Figure 42. SR_ SDO Delay

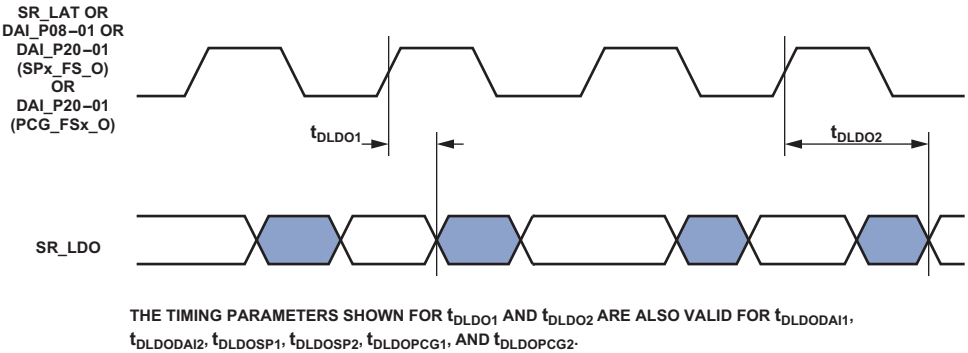

Figure 43. SR_LDO Delay

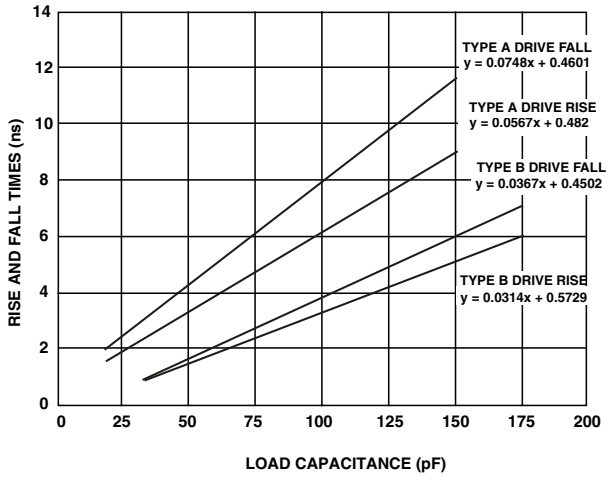

Figure 51. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Min)

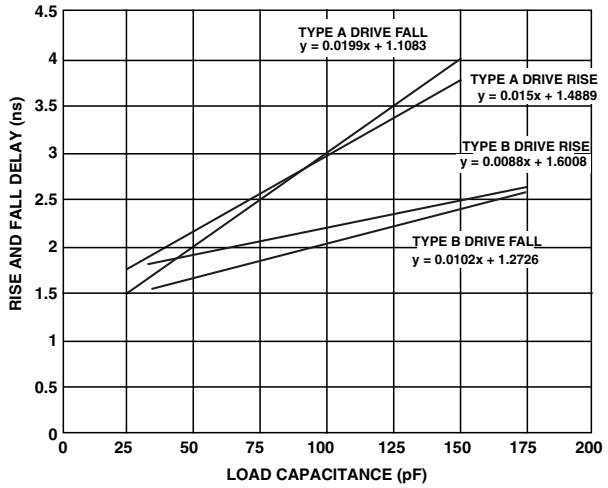

Figure 52. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

THERMAL CHARACTERISTICS

The processor is rated for performance over the temperature range specified in Operating Conditions.

Table 58 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-7 (PBGA). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the typical value from Table 58

P_D = power dissipation

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

Note that the thermal characteristics values provided in Table 58 are modeled values.

Table 57. Thermal Characteristics for 88-Lead LFCSP_VQ

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	22.6	°C/W
θ_{JMA}	Airflow = 1 m/s	18.2	°C/W
θ_{JMA}	Airflow = 2 m/s	17.3	°C/W
θ_{JC}		7.9	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.22	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.36	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.44	°C/W

Table 58. Thermal Characteristics for 100-Lead LQFP_EP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	18.1	°C/W
θ_{JMA}	Airflow = 1 m/s	15.5	°C/W
θ_{JMA}	Airflow = 2 m/s	14.6	°C/W
θ_{JC}		2.4	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.22	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.36	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.50	°C/W

Table 59. Thermal Characteristics for 196-Ball CSP_BGA

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	29.0	°C/W
θ_{JMA}	Airflow = 1 m/s	26.1	°C/W
θ_{JMA}	Airflow = 2 m/s	25.1	°C/W
θ_{JC}		8.8	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.23	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.42	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.52	°C/W

88-LFCSP_VQ LEAD ASSIGNMENT

Table 61 lists the 88-Lead LFCSP_VQ package lead names.

Table 61. 88-Lead LFCSP_VQ Lead Assignments (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
CLK_CFG1	1	V_{DD_EXT}	23	DAI_P10	45	V_{DD_INT}	67
BOOT_CFG0	2	DPI_P08	24	V_{DD_INT}	46	FLAG0	68
V_{DD_EXT}	3	DPI_P07	25	V_{DD_EXT}	47	V_{DD_INT}	69
V_{DD_INT}	4	DPI_P09	26	DAI_P20	48	FLAG1	70
BOOT_CFG1	5	DPI_P10	27	V_{DD_INT}	49	FLAG2	71
GND	6	DPI_P11	28	DAI_P08	50	FLAG3	72
CLK_CFG0	7	DPI_P12	29	DAI_P04	51	GND	73
V_{DD_INT}	8	DPI_P13	30	DAI_P14	52	GND	74
CLKIN	9	DAI_P03	31	DAI_P18	53	V_{DD_EXT}	75
XTAL	10	DPI_P14	32	DAI_P17	54	GND	76
V_{DD_EXT}	11	V_{DD_INT}	33	DAI_P16	55	V_{DD_INT}	77
V_{DD_INT}	12	DAI_P13	34	DAI_P15	56	$\overline{TRST}$	78
V_{DD_INT}	13	DAI_P07	35	DAI_P12	57	$\overline{EMU}$	79
$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	14	DAI_P19	36	DAI_P11	58	TDO	80
V_{DD_INT}	15	DAI_P01	37	V_{DD_INT}	59	V_{DD_EXT}	81
DPI_P01	16	DAI_P02	38	GND	60	V_{DD_INT}	82
DPI_P02	17	V_{DD_INT}	39	THD_M	61	TDI	83
DPI_P03	18	V_{DD_EXT}	40	THD_P	62	TCK	84
V_{DD_INT}	19	V_{DD_INT}	41	V_{DD_THD}	63	V_{DD_INT}	85
DPI_P05	20	DAI_P06	42	V_{DD_INT}	64	$\overline{RESET}$	86
DPI_P04	21	DAI_P05	43	V_{DD_INT}	65	TMS	87
DPI_P06	22	DAI_P09	44	V_{DD_INT}	66	V_{DD_INT}	88
						GND	89*

* Lead no. 89 is the GND supply (see Figure 53 and Figure 54) for the processor; this pad must be **robustly** connected to GND in order for the processor to function.

ORDERING GUIDE

Model[1]	Temperature Range[2]	On-Chip SRAM	Processor Instruction Rate (Max)	Package Description	Package Option
ADSP-21477KCPZ-1A	0°C to +70°C	2M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21477KSWZ-1A	0°C to +70°C	2M Bits	200 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21477BCPZ-1A	–40°C to +85°C	2M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21478KCPZ-1A	0°C to +70°C	3M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21478BCPZ-1A	–40°C to +85°C	3M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21478BBCZ-2A	–40°C to +85°C	3M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478BSWZ-2A	–40°C to +85°C	3M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21478KBCZ-1A	0°C to +70°C	3M Bits	200 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478KBCZ-2A	0°C to +70°C	3M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478KBCZ-3A	0°C to +70°C	3M Bits	300 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21478KSWZ-1A	0°C to +70°C	3M Bits	200 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21478KSWZ-2A	0°C to +70°C	3M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21479KCPZ-1A	0°C to +70°C	5M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21479BCPZ-1A	–40°C to +85°C	5M Bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5
ADSP-21479BBCZ-2A	–40°C to +85°C	5M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479BSWZ-2A	–40°C to +85°C	5M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21479KBCZ-1A	0°C to +70°C	5M Bits	200 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479KBCZ-2A	0°C to +70°C	5M Bits	266 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479KBCZ-3A	0°C to +70°C	5M Bits	300 MHz	196-Ball CSP_BGA	BC-196-8
ADSP-21479KSWZ-1A	0°C to +70°C	5M Bits	200 MHz	100-Lead LQFP_EP	SW-100-2
ADSP-21479KSWZ-2A	0°C to +70°C	5M Bits	266 MHz	100-Lead LQFP_EP	SW-100-2

[1] Z =RoHS compliant part.
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions for junction temperature (T_J) specification, which is the only temperature specification.