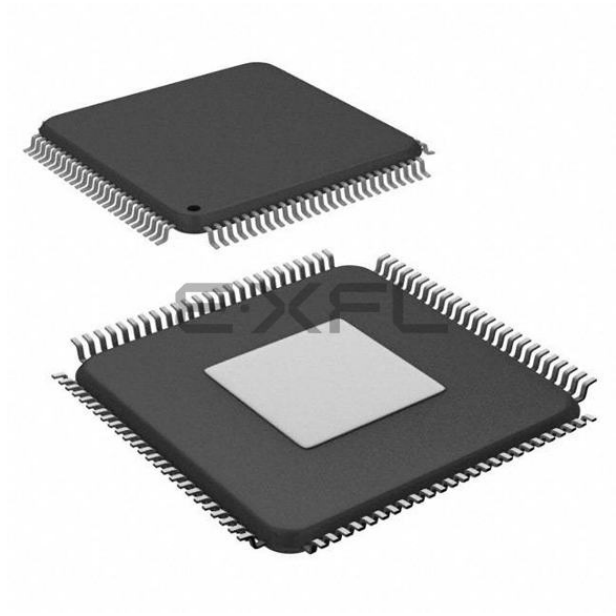

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI, EBI/EMI, I²C, SPI, SPORT, UART/USART
Clock Rate	266MHz
Non-Volatile Memory	ROM (4Mbit)
On-Chip RAM	5Mbit
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	100-LQFP-EP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21479bswz-2a

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REVISION HISTORY

4/2017—Rev. C to Rev. D

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PRODUCT APPLICATION RESTRICTION

Not for use in in-vivo applications for body fluid constituent monitoring, including monitoring one or more of the components that form, or may be a part of, or contaminate human blood or other body fluids, such as, but not limited to, carboxyhemoglobin, methemoglobin total hemoglobin, oxygen saturation, oxygen content, fractional arterial oxygen saturation, bilirubin, glucose, drugs, lipids, water, protein, and pH.

bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external SDRAM memory. This support is not extended to the asynchronous memory interface (AMI). Source modules need to be built using the VISA option, in order to allow code generation tools to create these more efficient opcodes.

On-Chip Memory

The processors contain varying amounts of internal RAM and internal ROM which is shown in Table 3 through Table 5. Each block can be configured for different combinations of code and data storage. Each memory block supports single-cycle, independent accesses by the core processor and I/O processor.

The processor's SRAM can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5M bits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

The memory maps in Table 3 through Table 5 display the internal memory address space of the processors. The 48-bit space section describes what this address range looks like to an instruction that retrieves 48-bit memory. The 32-bit section describes what this address range looks like to an instruction that retrieves 32-bit memory.

Table 3. ADSP-21477 Internal Memory Space (2M bits)

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 Bits)	**Extended Precision Normal or Instruction Word (48 Bits)**	**Normal Word (32 Bits)**	**Short Word (16 Bits)**
Block 0 ROM (Reserved) 0x0004 0000–0x0004 7FFF	Block 0 ROM (Reserved) 0x0008 0000–0x0008 AAA9	Block 0 ROM (Reserved) 0x0008 0000–0x0008 FFFF	Block 0 ROM (Reserved) 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0008 AAAA–0x0008 BFFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 FFFF
Block 0 SRAM 0x0004 9000–0x0004 BFFF	Block 0 SRAM 0x0008 C000–0x0008 FFFF	Block 0 SRAM 0x0009 2000–0x0009 7FFF	Block 0 SRAM 0x0012 4000–0x0012 FFFF
Reserved 0x0004 C000–0x0004 FFFF	Reserved 0x0009 000–0x0009 5554	Reserved 0x0009 8000–0x0009 FFFF	Reserved 0x0013 0000–0x0013 FFFF
Block 1 ROM (Reserved) 0x0005 0000–0x0005 7FFF	Block 1 ROM (Reserved) 0x000A 0000–0x000A AAA9	Block 1 ROM (Reserved) 0x000A 0000–0x000AFFFF	Block 1 ROM (Reserved) 0x0014 0000–0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000A AAAA–0x000A BFFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000–0x0016 3FFF
Block 1 SRAM 0x0005 9000–0x0005 BFFF	Block 1 SRAM 0x000A C000–0x000A FFFF	Block 1 SRAM 0x000B 2000–0x000B 7FFF	Block 1 SRAM 0x0016 4000–0x0016 FFFF
Reserved 0x0005 C000–0x0005 FFFF	Reserved 0x000B 0000–0x000B 5554	Reserved 0x000B 8000–0x000B FFFF	Reserved 0x0017 0000–0x0017 FFFF
Block 2 SRAM 0x0006 0000–0x0006 0FFF	Block 2 SRAM 0x000C 0000–0x000C 1554	Block 2 SRAM 0x000C 0000–0x000C 1FFF	Block 2 SRAM 0x0018 0000–0x0018 3FFF
Reserved 0x0006 1000– 0x0006 FFFF	Reserved 0x000C 1555–0x000D 5554	Reserved 0x000C 2000–0x000D FFFF	Reserved 0x0018 4000–0x001B FFFF
Block 3 SRAM 0x0007 0000–0x0007 0FFF	Block 3 SRAM 0x000E 0000–0x000E 1554	Block 3 SRAM 0x000E 0000–0x000E 1FFF	Block 3 SRAM 0x001C 0000–0x001C 3FFF
Reserved 0x0007 1000–0x0007 FFFF	Reserved 0x000E 1555–0x000F 5554	Reserved 0x000E 2000–0x000F FFFF	Reserved 0x001C 4000–0x001F FFFF

occupy a 8M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic.

External Port Throughput

The throughput for the external port, based on 133 MHz clock and 16-bit data bus, is 88 Mbytes/sec for the AMI and 266 Mbytes/sec for SDRAM.

MediaLB

The automotive models of the processors have an MLB interface which allows the processor to function as a media local bus device. It includes support for both 3-pin and 5-pin MLB protocols. It supports speeds up to 1024 FS (49.25M bits/sec, FS = 48.1 kHz) and up to 31 logical channels, with up to 124 bytes of data per media local bus frame. For a list of automotive products, see Automotive Products.

Digital Applications Interface (DAI)

The digital applications interface (DAI) provides the ability to connect various peripherals to any of the DAI pins (DAI_P20–1).

Programs make these connections using the signal routing unit (SRU), shown in Figure 1.

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with non configurable signal paths.

The associated peripherals include eight serial ports, four precision clock generators (PCG), a S/PDIF transceiver, four ASRCs, and an input data port (IDP). The IDP provides an additional input path to the SHARC core, configurable as either eight channels of serial data, or a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

Serial Ports (SPORTs)

The processors feature eight synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports can support up to 16 transmit or 16 receive DMA channels of audio data when all eight SPORTs are enabled, or four full duplex TDM streams of 128 channels per frame.

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified mode

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a bi phase encoded signal. The serial data input to the receiver/transmitter can be formatted as left justified, I^2S or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources, such as the SPORTs, external pins, the precision clock generators (PCGs), and are controlled by the SRU control registers.

Asynchronous Sample Rate Converter (SRC)

The sample rate converter contains four blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter. The SRC block provides up to 128 dB SNR and is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Input Data Port

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in I^2S, left-justified sample pair, or right-justified mode.

The IDP also provides a parallel data acquisition port (PDAP) which can be used for receiving parallel data. The PDAP port has a clock input and a hold input. The data for the PDAP can be received from DAI pins or from the external port pins. The PDAP supports a maximum of 20-bit data and four different packing modes to receive the incoming data.

Precision Clock Generators

The precision clock generators (PCG) consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A B, C, and D are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

The outputs of PCG A and B can be routed through the DAI pins and the outputs of PCG C and D can be driven on to the DAI as well as the DPI pins.

Table 11. Pin Descriptions (Continued)

Name	Type	State During/ After Reset	Description
$\overline{\text{SDRAS}}$	O/T (ipu)	High-Z/ driven high	**SDRAM Row Address Strobe.** Connect to SDRAM's RAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDCAS}}$	O/T (ipu)	High-Z/ driven high	**SDRAM Column Address Select.** Connect to SDRAM's CAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform.
$\overline{\text{SDWE}}$	O/T (ipu)	High-Z/ driven high	**SDRAM Write Enable.** Connect to SDRAM's WE or W buffer pin.
SDCKE	O/T (ipu)	High-Z/ driven high	**SDRAM Clock Enable.** Connect to SDRAM's CKE pin. Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	O/T (ipu)	High-Z/ driven high	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with non-SDRAM accesses. This pin replaces the DSP's ADDR10 pin only during SDRAM accesses.
SDDQM	O/T (ipu)	High-Z/ driven high	**DQM Data Mask.** SDRAM input mask signal for write accesses and output enable signal for read accesses. Input data is masked when DQM is sampled high during a write cycle. The SDRAM output buffers are placed in a High-Z state when DQM is sampled high during a read cycle. SDDQM is driven high from reset de-assertion until SDRAM initialization completes. Afterwards, it is driven low irrespective of whether any SDRAM accesses occur or not.
SDCLK	O/T (ipd)	High-Z/ driving	**SDRAM Clock Output.** Clock driver for this pin differs from all other clock drivers. See Figure 47. For models in the 100-lead package, the SDRAM interface should be disabled to avoid unnecessary power switching by setting the DSDCTL bit in SDCTL register. For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*.
DAI _P_{20-1}	I/O/T (ipu)	High-Z	**Digital Applications Interface**. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audio-centric peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins.
DPI _P_{14-1}	I/O/T (ipu)	High-Z	**Digital Peripheral Interface.** These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determine the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins.
WDT_CLKIN	I		**Watch Dog Timer Clock Input.** This pin should be pulled low when not used.
WDT_CLKO	O		**Watch Dog Resonator Pad Output.**
$\overline{\text{WDTRSTO}}$	O (ipu)		**Watch Dog Timer Reset Out.**

The following symbols appear in the Type column of Table 11: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.

The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be 26 kΩ to 63 kΩ. The range of an ipd resistor can be 31 kΩ to 85 kΩ. The three-state voltage of ipu pads will not reach to full the V_{DD_EXT} level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.

In this table, all pins are LVTTL compliant with the exception of the thermal diode, shift register, and real-time clock (RTC) pins.

Not all pins are available in the 88-lead LFCSP_VQ and 100-lead LQFP package. For more information, see Table 2 on Page 3 and Table 62 on Page 70.

Table 12. Pin List, Power and Ground

Name	Type	Description
V_{DD_INT}	P	**Internal Power Supply.**
V_{DD_EXT}	P	**I/O Power Supply.**
V_{DD_RTC}	P	**Real-Time Clock Power Supply.** When RTC is not used, this pin should be connected to V_{DD_EXT}.
GND[1]	G	**Ground.**
V_{DD_THD}	P	**Thermal Diode Power Supply**. When not used, this pin can be left floating.

[1] The exposed pad is required to be electrically and thermally connected to GND. Implement this by soldering the exposed pad to a GND PCB land that is the same size as the exposed pad. The GND PCB land should be *robustly* connected to the GND plane in the PCB for best electrical and thermal performance. See also 88-LFCSP_VQ Lead Assignment and 100-LQFP_EP Lead Assignment.

SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter[1]	Description	200 MHz			266 MHz			300 MHz			Unit
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{DD_INT}	Internal (Core) Supply Voltage	1.14	1.2	1.26	1.14	1.2	1.26	1.25	1.3	1.35	V
V_{DD_EXT}	External (I/O) Supply Voltage	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
V_{DD_THD}	Thermal Diode Supply Voltage	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
V_{DD_RTC}	Real-Time Clock Power Supply Voltage	2.0	3.0	3.6	2.0	3.0	3.6	2.0	3.0	3.6	V
V_{IH}[2]	High Level Input Voltage @ V_{DD_EXT} = Max	2.0			2.0			2.0			V
V_{IL}[3]	Low Level Input Voltage @ V_{DD_EXT} = Min			0.8			0.8			0.8	V
V_{IH_CLKIN}[3]	High Level Input Voltage @ V_{DD_EXT} = Max	2.2		V_{DD_EXT}	2.2		V_{DD_EXT}	2.2		V_{DD_EXT}	V
V_{IL_CLKIN}	Low Level Input Voltage @ V_{DD_EXT} = Max	–0.3		+0.8	–0.3		+0.8	–0.3		+0.8	V
T_J	Junction Temperature 88-Lead LFCSP_VQ @ $T_{AMBIENT}$ 0°C to +70°C	0		105	N/A		N/A	N/A		N/A	°C
T_J	Junction Temperature 88-Lead LFCSP_VQ @ $T_{AMBIENT}$ –40°C to +85°C	–40		+115	N/A		N/A	N/A		N/A	°C
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C	0		105	0		105	N/A		N/A	°C
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	N/A		N/A	–40		+125	N/A		N/A	°C
T_J[4]	Junction Temperature 196-Ball CSP_BGA @ $T_{AMBIENT}$ 0°C to +70°C	N/A		N/A	0		105	0		100	°C
T_J	Junction Temperature 196-Ball CSP_BGA @ $T_{AMBIENT}$ –40°C to +85°C	N/A		N/A	–40		+125	N/A		N/A	°C
AUTOMOTIVE USE ONLY											
T_J	Junction Temperature 88-Lead LFCSP_VQ @ $T_{AMBIENT}$ –40°C to +105°C (Automotive Grade)	–40		+125[5]	N/A		N/A	N/A		N/A	°C
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +105°C (Automotive Grade)	–40		+125[5]	–40		+125	N/A		N/A	°C
T_J[4]	Junction Temperature 196-Ball CSP_BGA @ $T_{AMBIENT}$ –40°C to +105°C (Automotive Grade)	–40		+125[5]	N/A		N/A	N/A		N/A	°C

[1] Specifications subject to change without notice.

[2] Applies to input and bidirectional pins: ADDR23–0, DATA15–0, FLAG3–0, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{\text{RUNRSTIN}}$, $\overline{\text{RESET}}$, TCK, TMS, TDI, $\overline{\text{TRST}}$, SDA10, AMI_ACK, MLBCLK, MLBDAT, MLBSIG.

[3] Applies to input pin CLKIN, WDT_CLKIN.

[4] Real Time Clock (RTC) is supported only for products in the BGA package with a temperature range of 0°C to +70°C. For the status of unused RTC pins please see Table 11.

[5] Automotive application use profile only. Not supported for nonautomotive use. Contact Analog Devices for more information.

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	200 MHz Min	200 MHz Max	266 MHz Min	266 MHz Max	300 MHz Min	300 MHz Max	Unit
V_{OH}[2]	High Level Output Voltage	@ V_{DD_EXT} = Min, I_{OH} = –1.0 mA[3]	2.4		2.4		2.4		V
V_{OL}[2]	Low Level Output Voltage	@ V_{DD_EXT} = Min, I_{OL} = 1.0 mA[3]		0.4		0.4		0.4	V
I_{IH}[4, 5]	High Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max		10		10		10	µA
I_{IL}[4]	Low Level Input Current	@ V_{DD_EXT} = Max, V_{IN} = 0 V		–10		–10		–10	µA
I_{ILPU}[5]	Low Level Input Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V		200		200		200	µA
I_{OZH}[6, 7]	Three-State Leakage Current	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max		10		10		10	µA
I_{OZL}[6]	Three-State Leakage Current	@ V_{DD_EXT} = Max, V_{IN} = 0 V		–10		–10		–10	µA
I_{OZLPU}[7]	Three-State Leakage Current Pull-up	@ V_{DD_EXT} = Max, V_{IN} = 0 V		200		200		200	µA
I_{OZHPD}[8]	Three-State Leakage Current Pull-down	@ V_{DD_EXT} = Max, V_{IN} = V_{DD_EXT} Max		200		200		200	µA
I_{DD_RTC}	V_{DD_RTC} Current	@ V_{DD_RTC} = 3.0, T_J = 25°C		0.76		0.76		0.76	µA
I_{DD_INT}[9]	Supply Current (Internal)	f_{CCLK} > 0 MHz		Table 14 + Table 15 × ASF		Table 14 + Table 15 × ASF		Table 14 + Table 15 × ASF	mA
C_{IN}[10, 11]	Input Capacitance	T_{CASE} = 25°C		5		5		5	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: ADDR23-0, DATA15-0, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, FLAG3–0, DAI_Px, DPI_Px, $\overline{\text{EMU}}$, TDO, $\overline{\text{RESETOUT}}$,MLBSIG, MLBDAT, MLBDO, MLBSO, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, SDCKE, SDA10, SDDQM, MS0-1.
[3] See Output Drive Currents for typical drive current capabilities.
[4] Applies to input pins: BOOT_CFGx, CLK_CFGx, TCK, $\overline{\text{RESET}}$, CLKIN.
[5] Applies to input pins with internal pull-ups: $\overline{\text{TRST}}$, TMS, TDI.
[6] Applies to three-statable pins: TDO, MLBDAT, MLBSIG, MLBDO, and MLBSO.
[7] Applies to three-statable pins with pull-ups: DAI_Px, DPI_Px, $\overline{\text{EMU}}$.
[8] Applies to three-statable pin with pull-down: SDCLK.
[9] See Engineer-to-Engineer Note “Estimating Power Dissipation for ADSP-214xx SHARC Processors” for further information.
[10] Applies to all signal pins.
[11] Guaranteed, but not tested.

Total Power Dissipation

The information in this section should be augmented with *Estimating Power for ADSP-214xx SHARC Processors (EE-348)*. Total power dissipation has two components:

1. Internal power consumption is additionally comprised of two components:
   - Static current due to leakage. Table 14 shows the static current consumption ($I_{DD\_INT\_STATIC}$) as a function of junction temperature (T_J) and core voltage (V_{DD_INT}).
   - Dynamic current ($I_{DD\_INT\_DYNAMIC}$), due to transistor switching characteristics and activity level of the processor. The activity level is reflected by the Activity Scaling Factor (ASF), which represents the activity level of the application code running on the processor core and having various levels of peripheral and external port activity (Table 13). Dynamic current consumption is calculated by selecting the ASF that corresponds most closely with the user application and then multiplying that with the dynamic current consumption (Table 15).
2. External power consumption is due to the switching activity of the external pins.

Table 13. Activity Scaling Factors (ASF)[1]

Activity	Scaling Factor (ASF)
Idle	0.31
Low	0.53
Medium Low	0.62
Medium High	0.78
Peak-Typical (50:50)[2]	0.85
Peak-Typical (60:40)[2]	0.93
Peak-Typical (70:30)[2]	1.00
High Typical	1.18
High	1.28
Peak	1.34

[1] See *Estimating Power for ADSP-214xx SHARC Processors (EE-348)* for more information on the explanation of the power vectors specific to the ASF table.
[2] Ratio of continuous instruction loop (core) to SDRAM control code reads and writes.

Table 14. Static Current—$I_{DD\_INT\_STATIC}$ (mA)[1]

	Voltage (V_{DD_INT})						
T_J (°C)	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V
–45	< 0.1	< 0.1	0.4	0.8	1.3	2.1	3.3
–35	< 0.1	< 0.1	0.4	0.7	1.1	1.7	2.9
–25	< 0.1	0.2	0.4	0.8	1.2	1.7	2.9
–15	< 0.1	0.4	0.6	1.0	1.4	1.9	3.2
–5	0.2	0.6	0.9	1.3	1.8	2.3	3.7
+5	0.5	0.9	1.3	1.8	2.3	3.0	4.4
+15	0.8	1.4	1.8	2.3	3.0	3.7	5.1
+25	1.3	1.9	2.5	3.1	3.9	4.7	6.2
+35	2.0	2.8	3.4	4.2	5.1	6.0	8.0
+45	3.0	3.9	4.7	5.7	6.7	7.8	10.1
+55	4.3	5.4	6.3	7.6	8.8	10.3	12.9
+65	6.0	7.3	8.6	10.1	11.7	13.5	16.4
+75	8.3	9.9	11.5	13.3	15.3	17.4	21.2
+85	11.2	13.2	15.3	17.5	19.9	22.6	27.1
+95	15.2	17.6	20.1	22.9	26.1	29.4	34.6
+100	17.4	20.2	22.9	25.9	29.4	33.0	39.2
+105	20.0	23.0	26.1	29.5	33.4	N/A	N/A
+115	26.3	30.0	33.9	38.2	42.9	N/A	N/A
+125	34.4	38.9	43.6	48.8	54.8	N/A	N/A

[1] Valid temperature and voltage ranges are model-specific. See Operating Conditions.

TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See Figure 49 under Test Conditions for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see Figure 5). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Voltage Controlled Oscillator (VCO)

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in Table 20.

- The product of CLKIN and PLLM must never exceed 1/2 of f_{VCO} (max) in Table 20 if the input divider is not enabled (INDIV = 0).
- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in Table 20 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$$f_{VCO} = 2 \times PLLM \times f_{INPUT}$$
$$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div PLLD$$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLD = 2, 4, 8, or 16 based on the divider value programmed on the PMCTL register. During reset this value is 2.

f_{INPUT} is the input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled, or CLKIN ÷ 2 when the input divider is enabled.

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in Table 20. All of the timing specifications for the peripherals are defined in relation to t_{PCLK}. See the peripheral specific section for each peripheral's timing information.

Table 18. Clock Periods

Timing Requirements	Description
t_{CK}	CLKIN Clock Period
t_{CCLK}	Processor Core Clock Period
t_{PCLK}	Peripheral Clock Period = 2 × t_{CCLK}
t_{SDCLK}	SDRAM Clock Period = (t_{CCLK}) × SDCKR

Figure 5 shows core to CLKIN relationships with an external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*.

AMI Read

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 32. AMI Read

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}[1, 2, 3]	Address Selects Delay to Data Valid		W + t_{SDCLK} – 6.32	ns
t_{DRLD}[1, 3]	$\overline{\text{AMI\_RD}}$ Low to Data Valid		W – 3	ns
t_{SDS}[4, 5]	Data Setup to $\overline{\text{AMI\_RD}}$ High	2.6		ns
t_{HDRH}	Data Hold from $\overline{\text{AMI\_RD}}$ High	0.4		ns
t_{DAAK}[2, 6]	AMI_ACK Delay from Address Selects		t_{SDCLK} – 10 + W	ns
t_{DSAK}[4]	AMI_ACK Delay from $\overline{\text{AMI\_RD}}$ Low		W – 7.0	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{\text{AMI\_RD}}$ High	RHC + 0.38		ns
t_{DARL}[2]	Address Selects to $\overline{\text{AMI\_RD}}$ Low	t_{SDCLK} – 5		ns
t_{RW}	$\overline{\text{AMI\_RD}}$ Pulse Width	W – 1.4		ns
t_{RWR}	$\overline{\text{AMI\_RD}}$ High to $\overline{\text{AMI\_RD}}$ Low	HI + t_{SDCLK} – 1.2		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
RHC = (number of Read Hold Cycles specified in AMICTLx register) × t_{SDCLK}
Where PREDIS = 0
HI = RHC (if IC = 0): Read to Read from same bank
HI = RHC+ t_{SDCLK} (if IC > 0): Read to Read from same bank
HI = RHC + IC: Read to Read from different bank
HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank
Where PREDIS = 1
HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank
HI = RHC + (3 × t_{SDCLK}): Read to Read from same bank
HI = RHC + Max (IC, (3 × t_{SDCLK})): Read to Read from different bank
IC = (number of idle cycles specified in AMICTLx register) × t_{SDCLK}
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}.

[1] Data delay/setup: System must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{\text{AMI_MS}}$x, is referenced.
[3] The maximum limit of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.
[4] Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.
[5] Data hold: User must meet t_{HDRH} in asynchronous access mode. See Test Conditions for the calculation of hold times given capacitive and dc loads.
[6] AMI_ACK delay/setup: User must meet t_{daak}, or t_{dsak}, for deassertion of AMI_ACK (low).

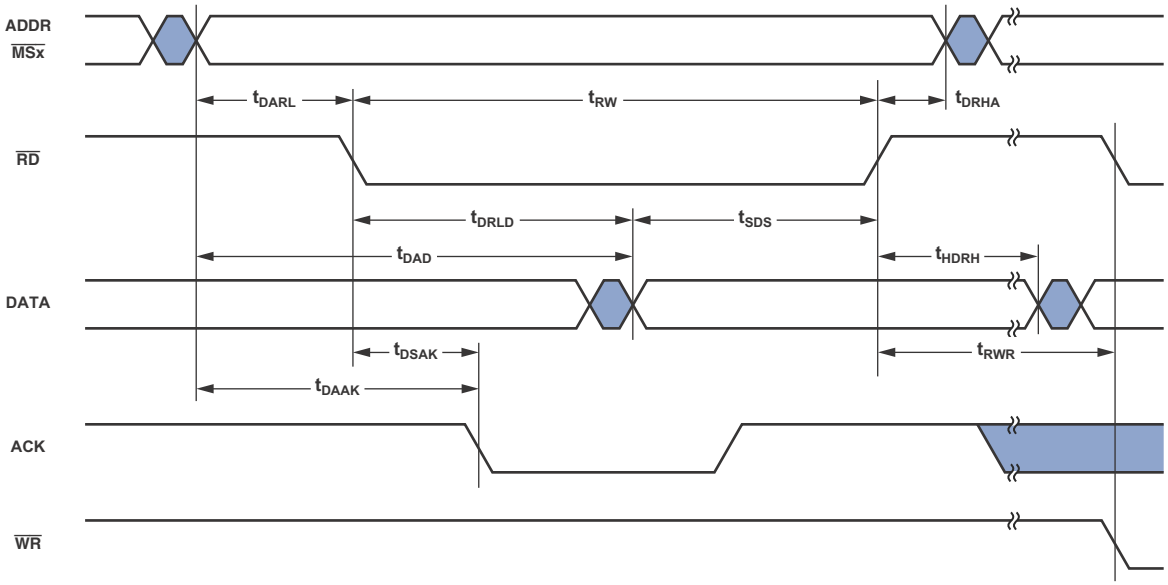

Figure 20. AMI Read

AMI Write

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 33. AMI Write

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	AMI_ACK Delay from Address Selects[1, 2]		t_{SDCLK} – 10.1 + W	ns
t_{DSAK}	AMI_ACK Delay from $\overline{\text{AMI\_WR}}$ Low[1, 3]		W – 7.1	ns
Switching Characteristics				
t_{DAWH}	Address Selects to $\overline{\text{AMI\_WR}}$ Deasserted[2]	t_{SDCLK} – 4.4 + W		ns
t_{DAWL}	Address Selects to $\overline{\text{AMI\_WR}}$ Low[2]	t_{SDCLK} – 4.5		ns
t_{WW}	$\overline{\text{AMI\_WR}}$ Pulse Width	W – 1.3		ns
t_{DDWH}	Data Setup Before $\overline{\text{AMI\_WR}}$ High	t_{SDCLK} – 4.3 + W		ns
t_{DWHA}	Address Hold After $\overline{\text{AMI\_WR}}$ Deasserted	H		ns
t_{DWHD}	Data Hold After $\overline{\text{AMI\_WR}}$ Deasserted	H		ns
t_{DATRWH}	Data Disable After $\overline{\text{AMI\_WR}}$ Deasserted[4]	t_{SDCLK} – 1.37 + H	t_{SDCLK} + 6.75 + H	ns
t_{WWR}	$\overline{\text{AMI\_WR}}$ High to $\overline{\text{AMI\_WR}}$ Low[5]	t_{SDCLK} – 1.5 + H		ns
t_{DDWR}	Data Disable Before $\overline{\text{AMI\_RD}}$ Low	2 × t_{SDCLK} – 7.1		ns
t_{WDE}	Data Enabled to $\overline{\text{AMI\_WR}}$ Low	t_{SDCLK} – 4.5		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}

[1] AMI_ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low).
[2] The falling edge of $\overline{\text{AMI\_MSx}}$ is referenced.
[3] Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only applies to asynchronous access mode.
[4] See Test Conditions for calculation of hold times given capacitive and dc loads.
[5] For Write to Write: t_{SDCLK} + H, for both same bank and different bank. For Write to Read: 3 × t_{SDCLK} + H, for the same bank and different banks.

The SPORTx_TDV_O output signal (routing unit) becomes active in SPORT multichannel/packed mode. During transmit slots (enabled with active channel selection registers), the SPORTx_TDV_O is asserted for communication with external devices.

Table 38. Serial Ports—TDV (Transmit Data Valid)

Parameter		88-Lead LFCSP Package		All Other Packages		Unit
		Min	Max	Min	Max	
Switching Characteristics[1]						
t_{DRDVEN}	TDV Assertion Delay from Drive Edge of External Clock	3		3		ns
t_{DFDVEN}	TDV Deassertion Delay from Drive Edge of External Clock		$2 \times t_{PCLK}$		13.25	ns
t_{DRDVIN}	TDV Assertion Delay from Drive Edge of Internal Clock	–0.1		–0.1		ns
t_{DFDVIN}	TDV Deassertion Delay from Drive Edge of Internal Clock		3.5		3.5	ns

[1] Referenced to drive edge.

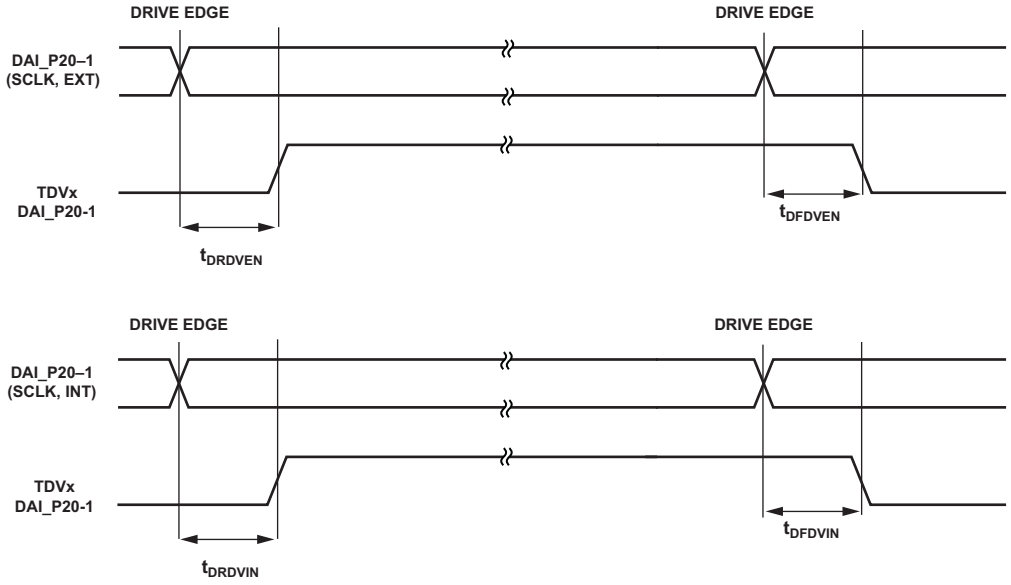

Figure 25. Serial Ports—TDV Internal and External Clock

Table 46. S/PDIF Transmitter Left-Justified Mode

Parameter		Nominal	Unit
Timing Requirement			
t_{LJD}	FS to MSB Delay in Left-Justified Mode	0	SCLK

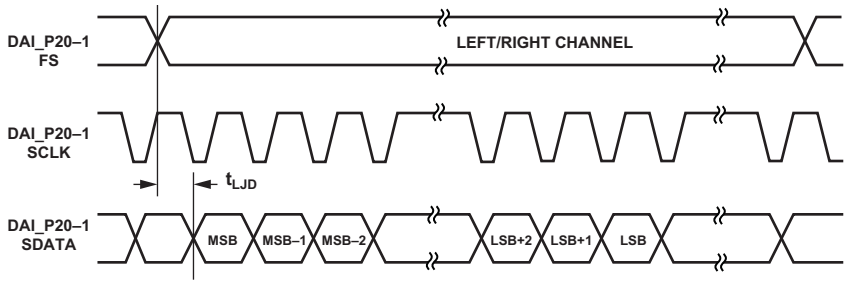

Figure 33. Left-Justified Mode

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the 512 × FS clock.

Table 49. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	FS Delay After Serial Clock		5	ns
t_{HOFSI}	FS Hold After Serial Clock	–2		ns
t_{DDTI}	Transmit Data Delay After Serial Clock		5	ns
t_{HDTI}	Transmit Data Hold After Serial Clock	–2		ns
t_{SCLKIW}[1]	Transmit Serial Clock Width	38.5		ns

[1] The serial clock frequency is 64 × frame sync (FS) where FS = the frequency of LRCLK.

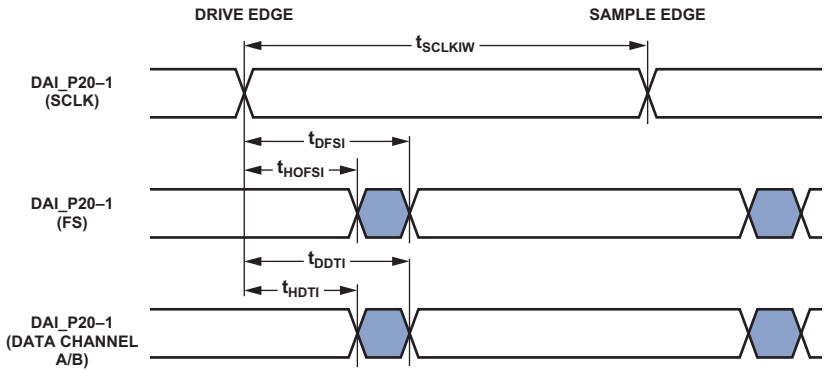

Figure 35. S/PDIF Receiver Internal Digital PLL Mode Timing

SPI Interface—Master

Both the primary and secondary SPIs are available through DPI only. The timing provided in Table 50 and Table 51 applies to both.

Table 50. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	10		8.6		ns
t_{HSPIDM}	SPICLK Last Sampling Edge to Data Input Not Valid	2		2		ns
Switching Characteristics						
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay time)		2.5		2.5	
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold time)	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	DPI Pin (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK Edge to DPI Pin (SPI Device Select) High	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 1.4$		ns

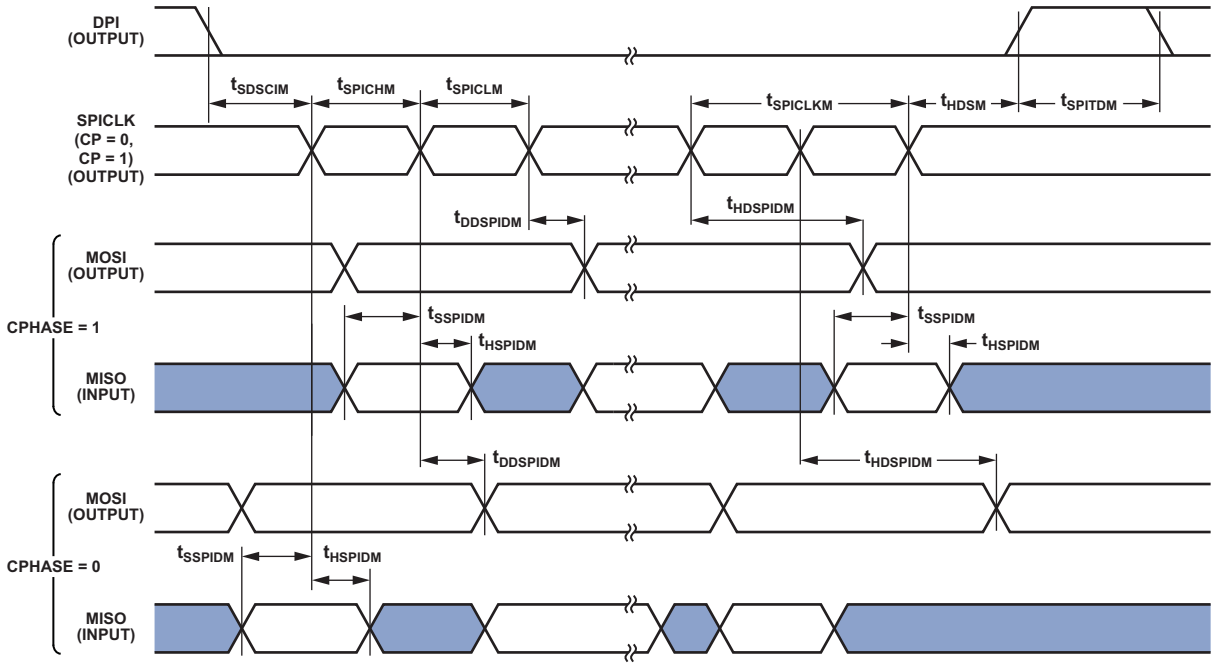

Figure 36. SPI Master Timing

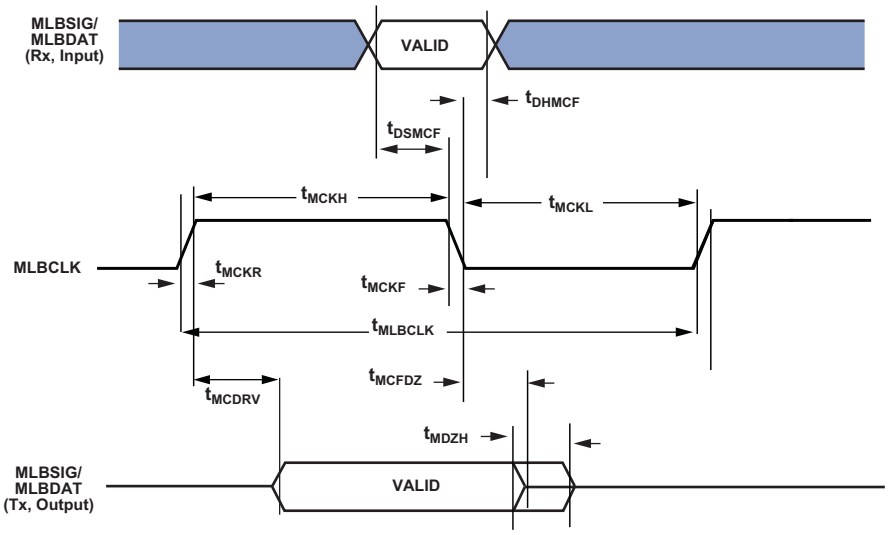

Figure 38. MLB Timing (3-Pin Interface)

Table 53. MLB Interface, 5-Pin Specifications

Parameter		Min	Typ	Max	Unit
5-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})			6	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})			6	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation			2	ns p-p
t_{DSMCF}[2]	DAT/SIG Input Setup Time	3			ns
t_{DHMCF}	DAT/SIG Input Hold Time	5			ns
t_{MCDRV}	DS/DO Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MCRDL}[3]	DO/SO Low From MLBCLK High				
	512 FS			10	ns
	256 FS			20	ns
C_{mlb}	DS/DO Pin Load			40	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (p-p).
[2] Gate delays due to OR'ing logic on the pins must be accounted for.
[3] When a node is not driving valid data onto the bus, the MLBSO and MLBDO output lines shall remain low. If the output lines can float at anytime, including while in reset, external pull-down resistors are required to keep the outputs from corrupting the MediaLB signal lines when not being driven.

Figure 53 shows the top view of the 88-lead LFCSP_VQ pin configuration. Figure 54 shows the bottom view.

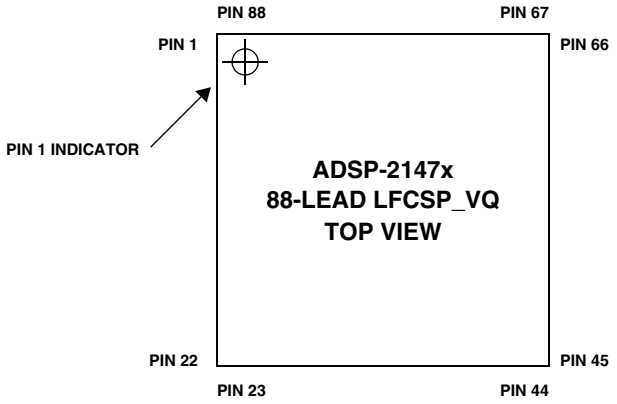

Figure 53. 88-Lead LFCSP_VQ Lead Configuration (Top View)

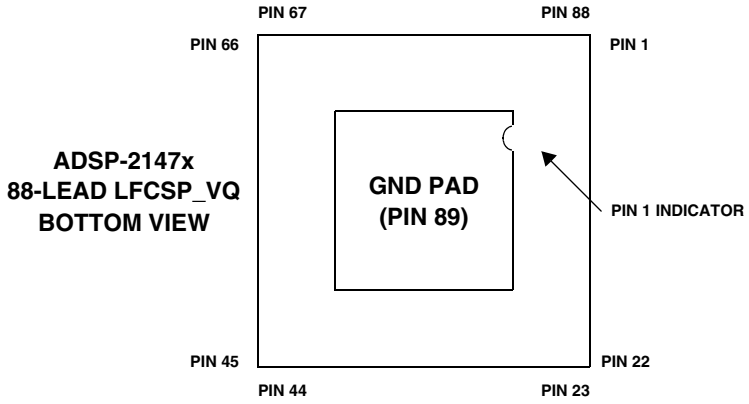

Figure 54. 88-Lead LFCSP_VQ Lead Configuration (Bottom View)

196-BGA BALL ASSIGNMENT

Table 63. 196-Ball CSP_BGA Ball Assignment (Numerical by Ball No.)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	GND	D1	ADDR6	G1	XTAL	K1	DPI_P02	N1	DPI_P14
A2	SDCKE	D2	ADDR4	G2	SDA10	K2	DPI_P04	N2	SR_LDO1
A3	SDDQM	D3	ADDR1	G3	ADDR11	K3	DPI_P05	N3	SR_LDO4
A4	$\overline{\text{SDRAS}}$	D4	CLK_CFG0	G4	GND	K4	DPI_P09	N4	SR_LDO8
A5	$\overline{\text{SDWE}}$	D5	V_{DD_EXT}	G5	V_{DD_INT}	K5	V_{DD_INT}	N5	SR_LDO10
A6	DATA12	D6	V_{DD_EXT}	G6	GND	K6	GND	N6	DAI_P01
A7	DATA13	D7	V_{DD_EXT}	G7	GND	K7	GND	N7	SR_LDO9
A8	DATA10	D8	V_{DD_EXT}	G8	GND	K8	GND	N8	DAI_P02
A9	DATA9	D9	V_{DD_EXT}	G9	GND	K9	GND	N9	SR_LDO13
A10	DATA7	D10	V_{DD_EXT}	G10	V_{DD_INT}	K10	V_{DD_INT}	N10	SR_SCLK
A11	DATA3	D11	V_{DD_EXT}	G11	V_{DD_EXT}	K11	GND	N11	DAI_P09
A12	DATA1	D12	ADDR14	G12	ADDR21	K12	DAI_P16	N12	SR_SDI
A13	DATA2	D13	ADDR20	G13	ADDR19	K13	DAI_P18	N13	SR_LDO17
A14	GND	D14	WDT_CLKO	G14	RTXO	K14	DAI_P15	N14	DAI_P14
B1	ADDR0	E1	ADDR8	H1	ADDR13	L1	DAI_P03	P1	GND
B2	CLK_CFG1	E2	ADDR7	H2	ADDR12	L2	DPI_P10	P2	SR_LDO3
B3	BOOT_CFG0	E3	ADDR5	H3	ADDR10	L3	DPI_P08	P3	SR_LDO2
B4	TMS	E4	V_{DD_EXT}	H4	ADDR17	L4	DPI_P06	P4	SR_LDO6
B5	$\overline{\text{RESET}}$	E5	V_{DD_INT}	H5	V_{DD_INT}	L5	V_{DD_INT}	P5	$\overline{\text{WDTRSTO}}$
B6	DATA14	E6	V_{DD_INT}	H6	GND	L6	V_{DD_INT}	P6	DAI_P19
B7	DATA11	E7	V_{DD_INT}	H7	GND	L7	V_{DD_INT}	P7	DAI_P13
B8	DATA4	E8	V_{DD_INT}	H8	GND	L8	V_{DD_INT}	P8	SR_LDO11
B9	DATA8	E9	V_{DD_INT}	H9	GND	L9	V_{DD_INT}	P9	SR_LDO15
B10	DATA6	E10	V_{DD_INT}	H10	V_{DD_INT}	L10	V_{DD_INT}	P10	$\overline{\text{SR\_CLR}}$
B11	DATA5	E11	V_{DD_EXT}	H11	V_{DD_EXT}	L11	DAI_P10	P11	SR_LAT
B12	$\overline{\text{TRST}}$	E12	$\overline{\text{AMI\_RD}}$	H12	BOOT_CFG2	L12	DAI_P20	P12	SR_LDO14
B13	FLAG1	E13	ADDR22	H13	ADDR23	L13	DAI_P17	P13	SR_LDO12
B14	DATA0	E14	FLAG2	H14	RTXI	L14	DAI_P04	P14	GND
C1	ADDR2	F1	CLKIN	J1	DPI_P01	M1	DPI_P13		
C2	ADDR3	F2	ADDR9	J2	DPI_P03	M2	DPI_P12		
C3	RTCLKOUT	F3	BOOT_CFG1	J3	ADDR18	M3	SR_LDO0		
C4	$\overline{\text{MS0}}$	F4	NC	J4	$\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$	M4	DPI_P07		
C5	$\overline{\text{SDCAS}}$	F5	NC	J5	V_{DD_INT}	M5	DPI_P11		
C6	DATA15	F6	GND	J6	GND	M6	SR_LDO5		
C7	TCK	F7	GND	J7	GND	M7	SR_LDO7		
C8	TDI	F8	GND	J8	GND	M8	DAI_P07		
C9	SDCLK	F9	GND	J9	GND	M9	SR_LDO16		
C10	$\overline{\text{EMU}}$	F10	V_{DD_INT}	J10	V_{SS_RTC}	M10	SR_SDO		
C11	TDO	F11	V_{DD_EXT}	J11	V_{DD_RTC}	M11	DAI_P06		
C12	FLAG3	F12	ADDR15	J12	DAI_P11	M12	DAI_P05		
C13	ADDR16	F13	FLAG0	J13	AMI_ACK	M13	DAI_P08		
C14	WDT_CLKIN	F14	$\overline{\text{AMI\_WR}}$	J14	$\overline{\text{MS1}}$	M14	DAI_P12		

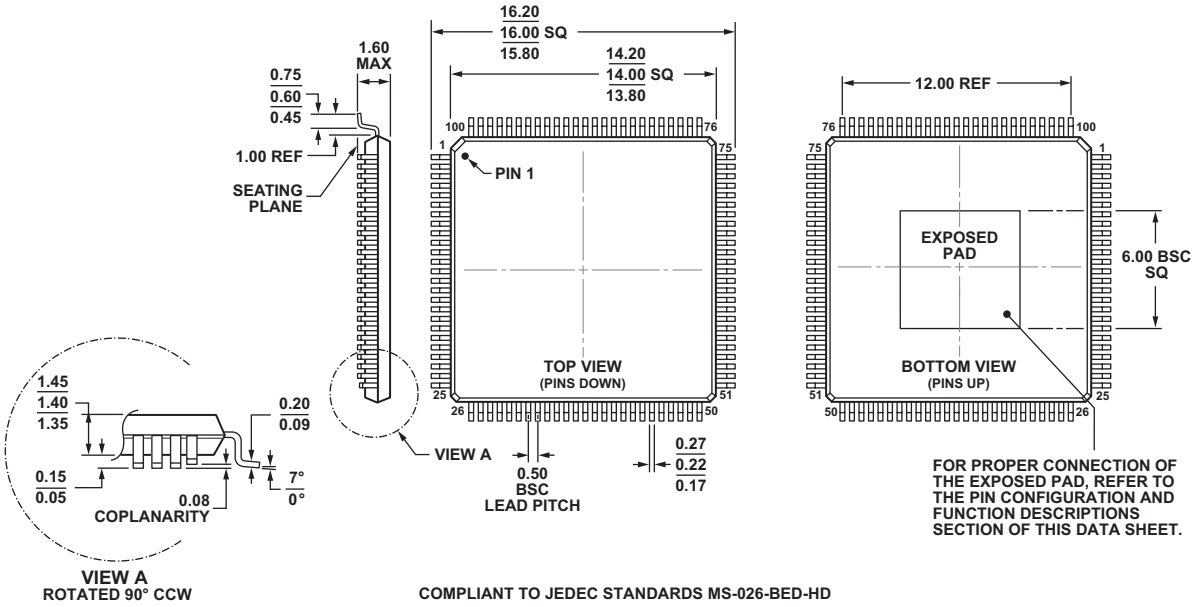

Figure 58. 100-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP[1]]
(SW-100-2)
Dimensions shown in millimeters

[1] For information relating to the exposed pad on the SW-100-2 package, see the table endnote on Page 70.

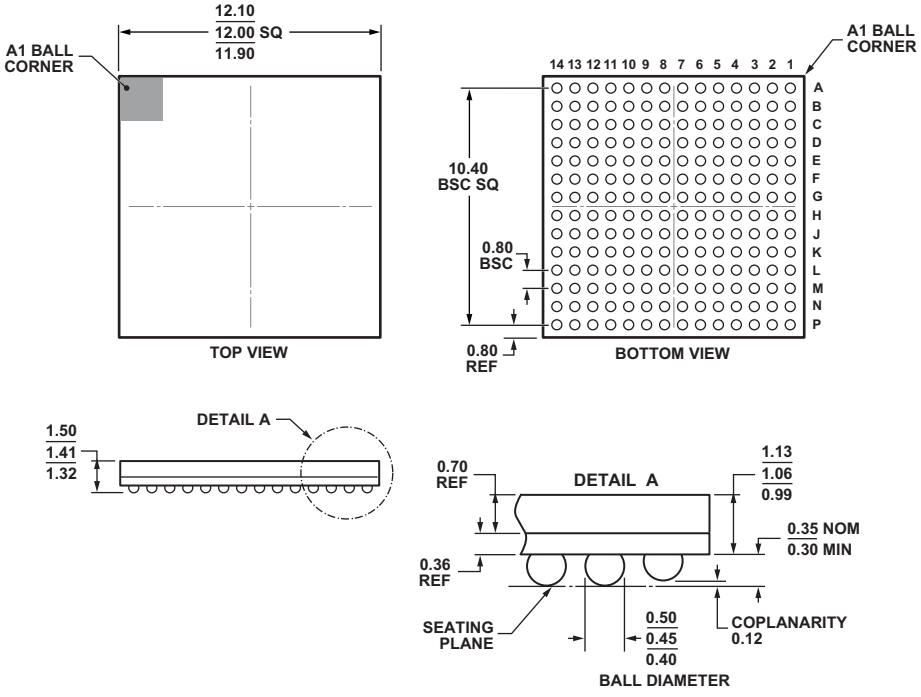

Figure 59. 196-Ball Chip Scale Package, Ball Grid Array [CSP_BGA]
(BC-196-8)
Dimensions shown in millimeters