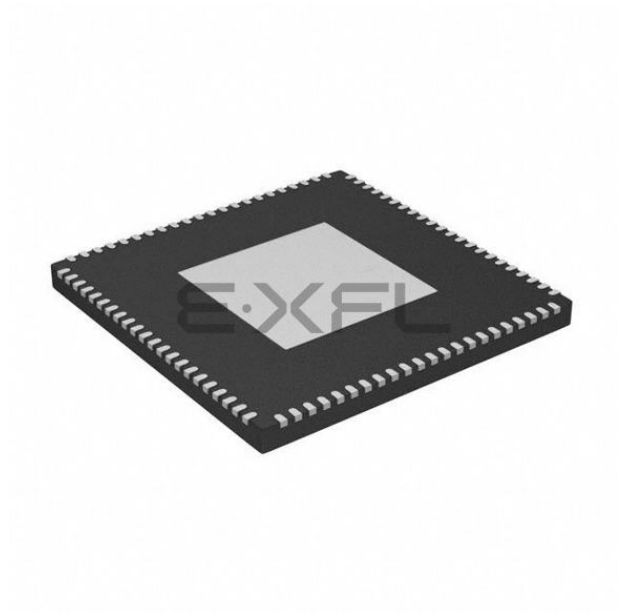

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	DAI, DPI, EBI/EMI, I²C, SPI, SPORT, UART/USART
Clock Rate	200MHz
Non-Volatile Memory	ROM (4Mbit)
On-Chip RAM	5Mbit
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	88-VFQFN Exposed Pad, CSP
Supplier Device Package	88-LFCSP-VQ (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21479kcpz-1a

External Memory

The external memory interface supports access to the external memory through core and DMA accesses. The external memory address space is divided into four banks. Any bank can be programmed as either asynchronous or synchronous memory. The external ports are comprised of the following modules.

- An AMI which communicates with SRAM, FLASH, and other devices that meet the standard asynchronous SRAM access protocol. The AMI supports 6M words of external memory in Bank 0 and 8M words of external memory in Bank 1, Bank 2, and Bank 3.
- An SDRAM controller that supports a glueless interface with any of the standard SDRAMs. The SDC supports 62M words of external memory in Bank 0, and 64M words of external memory in Bank 1, Bank 2, and Bank 3.
- Arbitration logic to coordinate core and DMA transfers between internal and external memory over the external port.

External Port

The external port provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The external port, available on the 196-ball CSP_BGA, may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers. The first is an SDRAM controller for connection of industry-standard synchronous DRAM devices while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types. Non-SDRAM external memory address space is shown in Table 6.

Table 6. External Memory for Non-SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	6M	0x0020 0000–0x007F FFFF
Bank 1	8M	0x0400 0000–0x047F FFFF
Bank 2	8M	0x0800 0000–0x087F FFFF
Bank 3	8M	0x0C00 0000–0x0C7F FFFF

SIMD Access to External Memory

The SDRAM controller supports SIMD access on the 64-bit external port data bus (EPD) which allows access to the complementary registers on the PEy unit in the normal word space (NW). This improves performance since there is no need to explicitly load the complementary registers (as in SISD mode).

VISA and ISA Access to External Memory

The SDRAM controller supports VISA code operation which reduces the memory load since the VISA instructions are compressed. Moreover, bus fetching is reduced because, in the best case, one 48-bit fetch contains three valid instructions. Code execution from the traditional ISA operation is also supported. Note that code execution is only supported from Bank 0 regardless of VISA/ISA. Table 7 shows the address ranges for instruction fetch in each mode.

Table 7. External Bank 0 Instruction Fetch

Access Type	Size in Words	Address Range
ISA (NW)	4M	0x0020 0000–0x005F FFFF
VISA (SW)	10M	0x0060 0000–0x00FF FFFF

SDRAM Controller

The SDRAM controller, available on the ADSP-2147x in the 196-ball CSP_BGA package, provides an interface of up to four separate banks of industry-standard SDRAM devices or DIMMs, at speeds up to f_{SDCLK}. Fully compliant with the SDRAM standard, each bank has its own memory select line ($\overline{MS0}$–$\overline{MS3}$), and can be configured to contain between 4 Mbytes and 256 Mbytes of memory. SDRAM external memory address space is shown in Table 8.

Table 8. External Memory for SDRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000–0x03FF FFFF
Bank 1	64M	0x0400 0000–0x07FF FFFF
Bank 2	64M	0x0800 0000–0x0BFF FFFF
Bank 3	64M	0x0C00 0000–0x0FFF FFFF

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. The SDRAM and the AMI interface do not support 32-bit wide devices.

The SDRAM controller address, data, clock, and control pins can drive loads up to distributed 30 pF. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

Note that the external memory bank addresses shown are for normal-word (32-bit) accesses. If 48-bit instructions as well as 32-bit data are both placed in the same external memory bank, care must be taken while mapping them to avoid overlap.

Asynchronous Memory Controller

The asynchronous memory controller, available on the ADSP-2147x in the 196-ball CSP_BGA package, provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 6M word window and Banks 1, 2, and 3

Table 12. Pin List, Power and Ground

Name	Type	Description
V_{DD_INT}	P	**Internal Power Supply.**
V_{DD_EXT}	P	**I/O Power Supply.**
V_{DD_RTC}	P	**Real-Time Clock Power Supply.** When RTC is not used, this pin should be connected to V_{DD_EXT}.
GND[1]	G	**Ground.**
V_{DD_THD}	P	**Thermal Diode Power Supply**. When not used, this pin can be left floating.

[1] The exposed pad is required to be electrically and thermally connected to GND. Implement this by soldering the exposed pad to a GND PCB land that is the same size as the exposed pad. The GND PCB land should be *robustly* connected to the GND plane in the PCB for best electrical and thermal performance. See also 88-LFCSP_VQ Lead Assignment and 100-LQFP_EP Lead Assignment.

SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter[1]	Description	200 MHz			266 MHz			300 MHz			Unit
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{DD_INT}	Internal (Core) Supply Voltage	1.14	1.2	1.26	1.14	1.2	1.26	1.25	1.3	1.35	V
V_{DD_EXT}	External (I/O) Supply Voltage	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
V_{DD_THD}	Thermal Diode Supply Voltage	3.13	3.3	3.47	3.13	3.3	3.47	3.13	3.3	3.47	V
V_{DD_RTC}	Real-Time Clock Power Supply Voltage	2.0	3.0	3.6	2.0	3.0	3.6	2.0	3.0	3.6	V
V_{IH}[2]	High Level Input Voltage @ V_{DD_EXT} = Max	2.0			2.0			2.0			V
V_{IL}[3]	Low Level Input Voltage @ V_{DD_EXT} = Min			0.8			0.8			0.8	V
V_{IH_CLKIN}[3]	High Level Input Voltage @ V_{DD_EXT} = Max	2.2		V_{DD_EXT}	2.2		V_{DD_EXT}	2.2		V_{DD_EXT}	V
V_{IL_CLKIN}	Low Level Input Voltage @ V_{DD_EXT} = Max	–0.3		+0.8	–0.3		+0.8	–0.3		+0.8	V
T_J	Junction Temperature 88-Lead LFCSP_VQ @ $T_{AMBIENT}$ 0°C to +70°C	0		105	N/A		N/A	N/A		N/A	°C
T_J	Junction Temperature 88-Lead LFCSP_VQ @ $T_{AMBIENT}$ –40°C to +85°C	–40		+115	N/A		N/A	N/A		N/A	°C
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C	0		105	0		105	N/A		N/A	°C
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C	N/A		N/A	–40		+125	N/A		N/A	°C
T_J[4]	Junction Temperature 196-Ball CSP_BGA @ $T_{AMBIENT}$ 0°C to +70°C	N/A		N/A	0		105	0		100	°C
T_J	Junction Temperature 196-Ball CSP_BGA @ $T_{AMBIENT}$ –40°C to +85°C	N/A		N/A	–40		+125	N/A		N/A	°C
AUTOMOTIVE USE ONLY											
T_J	Junction Temperature 88-Lead LFCSP_VQ @ $T_{AMBIENT}$ –40°C to +105°C (Automotive Grade)	–40		+125[5]	N/A		N/A	N/A		N/A	°C
T_J	Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +105°C (Automotive Grade)	–40		+125[5]	–40		+125	N/A		N/A	°C
T_J[4]	Junction Temperature 196-Ball CSP_BGA @ $T_{AMBIENT}$ –40°C to +105°C (Automotive Grade)	–40		+125[5]	N/A		N/A	N/A		N/A	°C

[1] Specifications subject to change without notice.

[2] Applies to input and bidirectional pins: ADDR23–0, DATA15–0, FLAG3–0, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{\text{RUNRSTIN}}$, $\overline{\text{RESET}}$, TCK, TMS, TDI, $\overline{\text{TRST}}$, SDA10, AMI_ACK, MLBCLK, MLBDAT, MLBSIG.

[3] Applies to input pin CLKIN, WDT_CLKIN.

[4] Real Time Clock (RTC) is supported only for products in the BGA package with a temperature range of 0°C to +70°C. For the status of unused RTC pins please see Table 11.

[5] Automotive application use profile only. Not supported for nonautomotive use. Contact Analog Devices for more information.

TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See Figure 49 under Test Conditions for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Core Clock Requirements

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see Figure 5). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

Voltage Controlled Oscillator (VCO)

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds f_{VCO} specified in Table 20.

- The product of CLKIN and PLLM must never exceed 1/2 of f_{VCO} (max) in Table 20 if the input divider is not enabled (INDIV = 0).
- The product of CLKIN and PLLM must never exceed f_{VCO} (max) in Table 20 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$$f_{VCO} = 2 \times PLLM \times f_{INPUT}$$
$$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div PLLD$$

where:

f_{VCO} = VCO output

PLLM = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

PLLD = 2, 4, 8, or 16 based on the divider value programmed on the PMCTL register. During reset this value is 2.

f_{INPUT} is the input frequency to the PLL.

f_{INPUT} = CLKIN when the input divider is disabled, or CLKIN ÷ 2 when the input divider is enabled.

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in Table 20. All of the timing specifications for the peripherals are defined in relation to t_{PCLK}. See the peripheral specific section for each peripheral's timing information.

Table 18. Clock Periods

Timing Requirements	Description
t_{CK}	CLKIN Clock Period
t_{CCLK}	Processor Core Clock Period
t_{PCLK}	Peripheral Clock Period = 2 × t_{CCLK}
t_{SDCLK}	SDRAM Clock Period = (t_{CCLK}) × SDCKR

Figure 5 shows core to CLKIN relationships with an external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*.

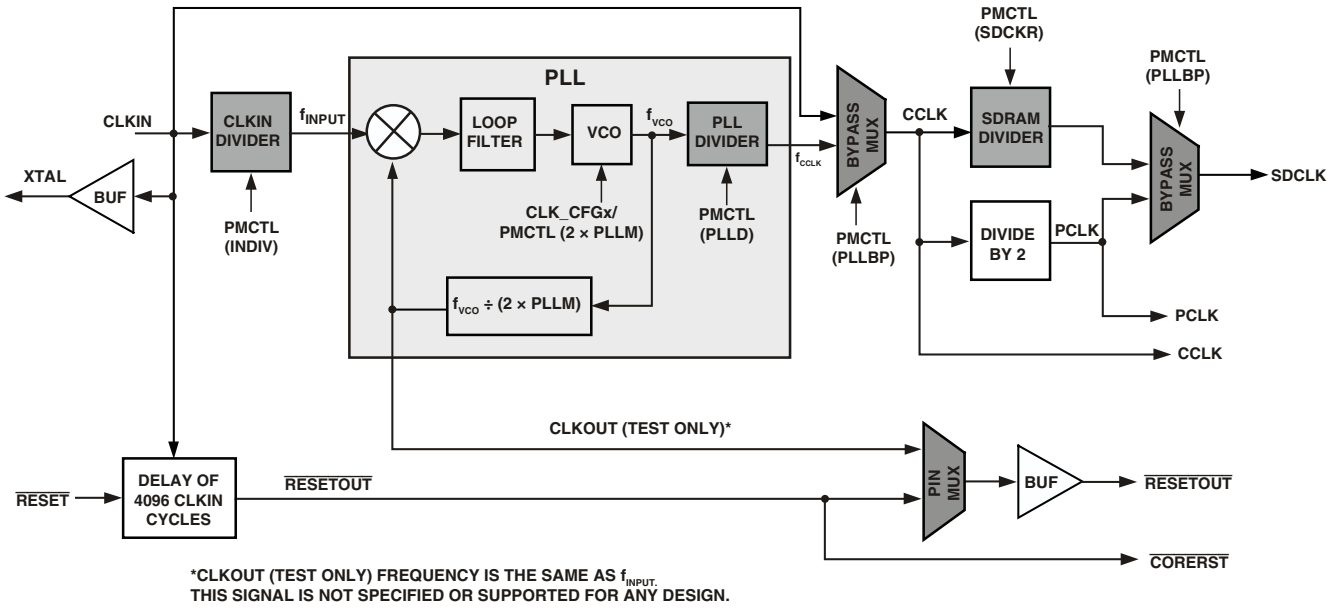

Figure 5. Core Clock and System Clock Relationship to CLKIN

Power-Up Sequencing

The timing requirements for processor startup are given in Table 19. While no specific power-up sequencing is required between V_{DD_EXT} and V_{DD_INT}, there are some considerations that the system designs should take into account.

- No power supply should be powered up for an extended period of time (>200 ms) before another supply starts to ramp up.
- If the V_{DD_INT} power supply comes up after V_{DD_EXT}, any pin, such as $\overline{\text{RESETOUT}}$ and $\overline{\text{RESET}}$, may actually drive momentarily until the V_{DD_INT} rail has powered up. Systems sharing these signals on the board must determine if there are any issues that need to be addressed based on this behavior.

Note that during power-up, when the V_{DD_INT} power supply comes up after V_{DD_EXT}, a leakage current of the order of three-state leakage current pull-up, pull-down, may be observed on any pin, even if that is an input only (for example, the $\overline{\text{RESET}}$ pin), until the V_{DD_INT} rail has powered up.

Table 19. Power-Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DD_EXT} or V_{DD_INT} On	0		ms
$t_{IVDDEVDD}$	V_{DD_INT} On Before V_{DD_EXT}	–200	+200	ms
t_{CLKVDD} [1]	CLKIN Valid After V_{DD_INT} and V_{DD_EXT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10 [2]		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20 [3]		µs
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096 \times t_{CK} + 2 \times t_{CCLK}$ [4, 5]		

[1] Valid V_{DD_INT} and V_{DD_EXT} assumes that the supplies are fully ramped to their nominal values (it does not matter which supply comes up first). Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4096 cycle count depends on t_{SRST} specification in Table 21. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

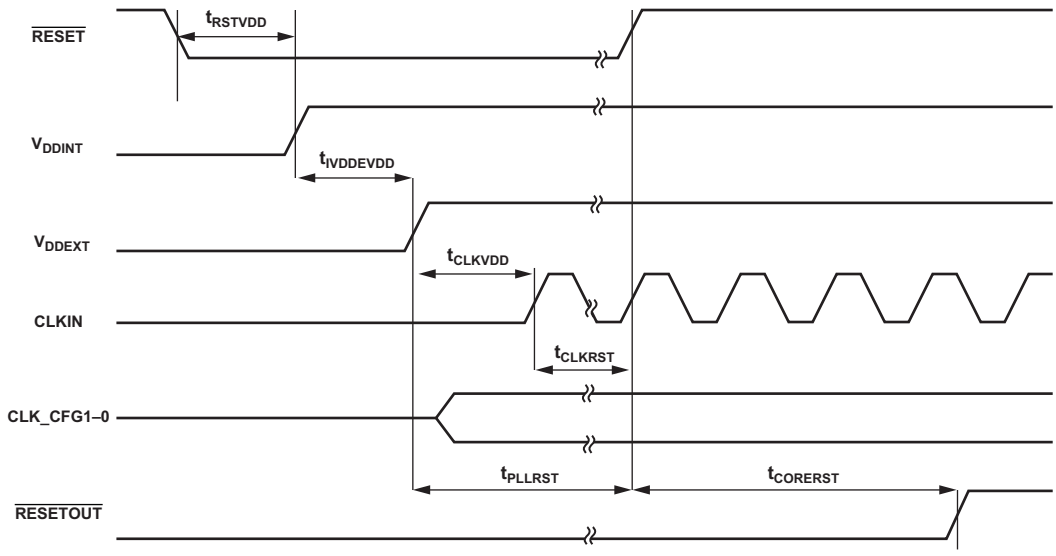

Figure 6. Power-Up Sequencing

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

Table 24. Core Timer

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Switching Characteristic						
t_{WCTIM}	TMREXP Pulse Width	$4 \times t_{PCLK} - 1.55$		$4 \times t_{PCLK} - 1.2$		ns

Figure 12. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to timer0 and timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 25. Timer PWM_OUT Timing

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Switching Characteristic						
t_{PWMO}	Timer Pulse Width Output	$2 \times t_{PCLK} - 1.65$	$2 \times (2^{31} - 1) \times t_{PCLK}$	$2 \times t_{PCLK} - 1.2$	$2 \times (2^{31} - 1) \times t_{PCLK}$	ns

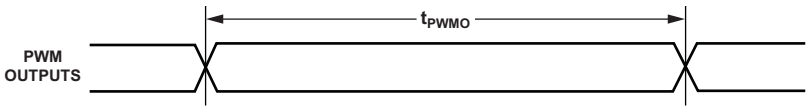

Figure 13. Timer PWM_OUT Timing

AMI Read

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 32. AMI Read

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}[1, 2, 3]	Address Selects Delay to Data Valid		W + t_{SDCLK} – 6.32	ns
t_{DRLD}[1, 3]	$\overline{\text{AMI\_RD}}$ Low to Data Valid		W – 3	ns
t_{SDS}[4, 5]	Data Setup to $\overline{\text{AMI\_RD}}$ High	2.6		ns
t_{HDRH}	Data Hold from $\overline{\text{AMI\_RD}}$ High	0.4		ns
t_{DAAK}[2, 6]	AMI_ACK Delay from Address Selects		t_{SDCLK} – 10 + W	ns
t_{DSAK}[4]	AMI_ACK Delay from $\overline{\text{AMI\_RD}}$ Low		W – 7.0	ns
Switching Characteristics				
t_{DRHA}	Address Selects Hold After $\overline{\text{AMI\_RD}}$ High	RHC + 0.38		ns
t_{DARL}[2]	Address Selects to $\overline{\text{AMI\_RD}}$ Low	t_{SDCLK} – 5		ns
t_{RW}	$\overline{\text{AMI\_RD}}$ Pulse Width	W – 1.4		ns
t_{RWR}	$\overline{\text{AMI\_RD}}$ High to $\overline{\text{AMI\_RD}}$ Low	HI + t_{SDCLK} – 1.2		ns

W = (number of wait states specified in AMICTLx register) × t_{SDCLK}.
RHC = (number of Read Hold Cycles specified in AMICTLx register) × t_{SDCLK}
Where PREDIS = 0
HI = RHC (if IC = 0): Read to Read from same bank
HI = RHC+ t_{SDCLK} (if IC > 0): Read to Read from same bank
HI = RHC + IC: Read to Read from different bank
HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank
Where PREDIS = 1
HI = RHC + Max (IC, (4 × t_{SDCLK})): Read to Write from same or different bank
HI = RHC + (3 × t_{SDCLK}): Read to Read from same bank
HI = RHC + Max (IC, (3 × t_{SDCLK})): Read to Read from different bank
IC = (number of idle cycles specified in AMICTLx register) × t_{SDCLK}
H = (number of hold cycles specified in AMICTLx register) × t_{SDCLK}.

[1] Data delay/setup: System must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{\text{AMI_MS}}$x, is referenced.
[3] The maximum limit of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.
[4] Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.
[5] Data hold: User must meet t_{HDRH} in asynchronous access mode. See Test Conditions for the calculation of hold times given capacitive and dc loads.
[6] AMI_ACK delay/setup: User must meet t_{daak}, or t_{dsak}, for deassertion of AMI_ACK (low).

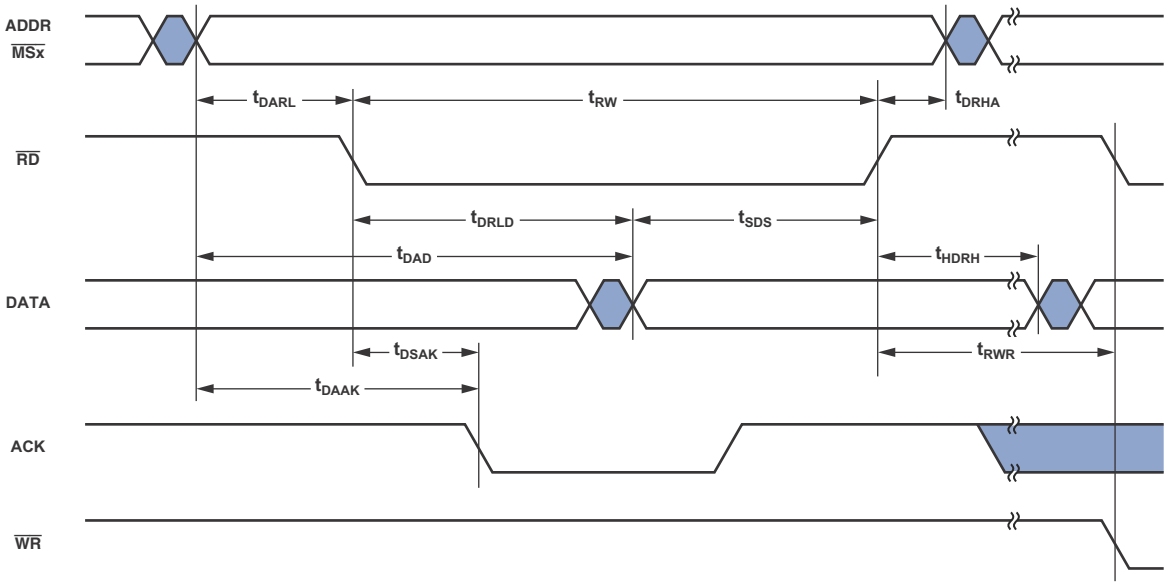

Figure 20. AMI Read

Table 35. Serial Ports—Internal Clock

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{SFSI}[1]	Frame Sync Setup Before SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	13		10.5		ns
t_{HFSI}[1]	Frame Sync Hold After SCLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)	2.5		2.5		ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	13		10.5		ns
t_{HDRI}[1]	Receive Data Hold After SCLK	2.5		2.5		ns
Switching Characteristics						
t_{DFSI}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode)		5		5	ns
t_{HOFSI}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode)	–1.0		–1.0		ns
t_{DFSIR}[2]	Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode)		10.7		10.7	ns
t_{HOFSIR}[2]	Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode)	–1.0		–1.0		ns
t_{DDTI}[2]	Transmit Data Delay After SCLK		4		4	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	–1.0		–1.0		ns
t_{SCKLIW}	Transmit or Receive SCLK Width	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	$2 \times t_{PCLK} - 1.5$	$2 \times t_{PCLK} + 1.5$	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

Table 36. Serial Ports—External Late Frame Sync

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Switching Characteristics						
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0		2 × t_{PCLK}		13.5	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	0.5		0.5		ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified as well as DSP serial mode, and MCE = 1, MFD = 0.

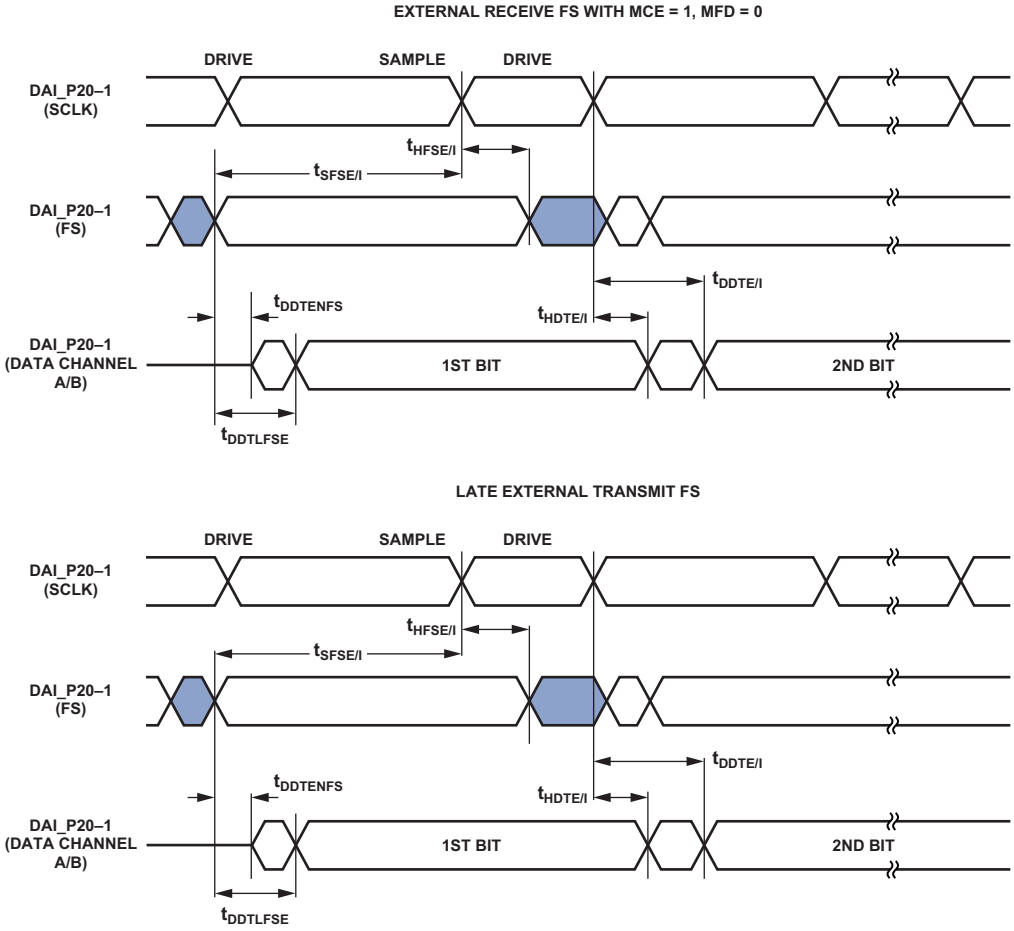

Figure 23. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified mode.

Table 37. Serial Ports—Enable and Three-State

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Switching Characteristics						
t_{DDTEN}[1]	Data Enable from External Transmit SCLK	2		2		ns
t_{DDTTE}[1]	Data Disable from External Transmit SCLK		23		20	ns
t_{DDTIN}[1]	Data Enable from Internal Transmit SCLK	–1		–1		ns

[1] Referenced to drive edge.

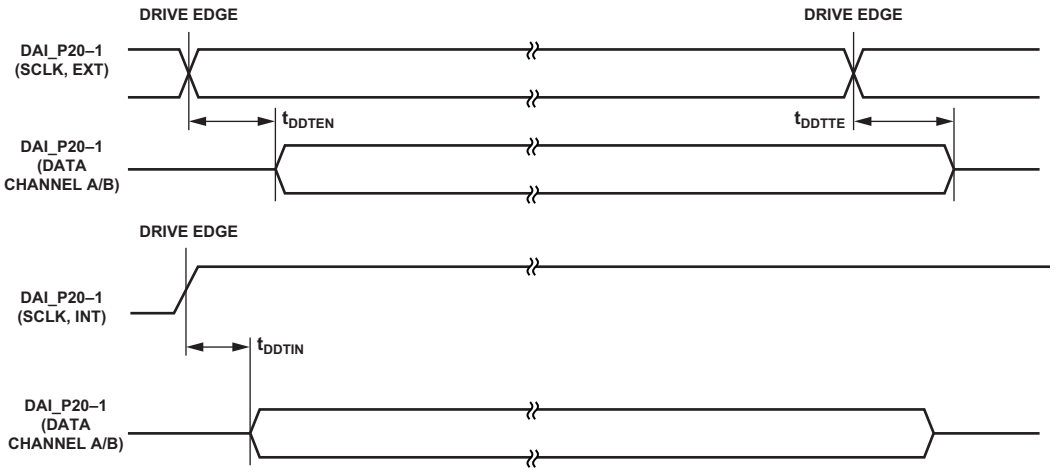

Figure 24. Enable and Three-State

SPI Interface—Master

Both the primary and secondary SPIs are available through DPI only. The timing provided in Table 50 and Table 51 applies to both.

Table 50. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{SSPIDM}	Data Input Valid to SPICLK Edge (Data Input Setup Time)	10		8.6		ns
t_{HSPIDM}	SPICLK Last Sampling Edge to Data Input Not Valid	2		2		ns
Switching Characteristics						
$t_{SPICLKM}$	Serial Clock Cycle	$8 \times t_{PCLK} - 2$		$8 \times t_{PCLK} - 2$		ns
t_{SPICHM}	Serial Clock High Period	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SPICLM}	Serial Clock Low Period	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay time)		2.5		2.5	
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold time)	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SDSCIM}	DPI Pin (SPI Device Select) Low to First SPICLK Edge	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{HDSM}	Last SPICLK Edge to DPI Pin (SPI Device Select) High	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 2$		ns
t_{SPITDM}	Sequential Transfer Delay	$4 \times t_{PCLK} - 2$		$4 \times t_{PCLK} - 1.4$		ns

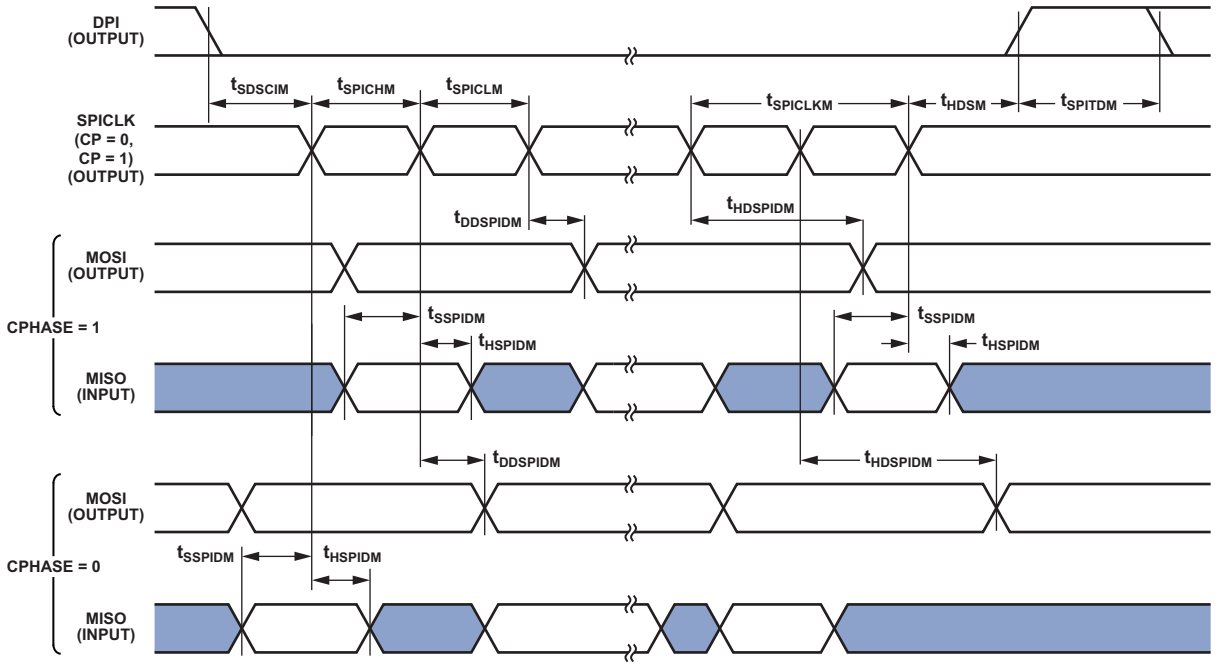

Figure 36. SPI Master Timing

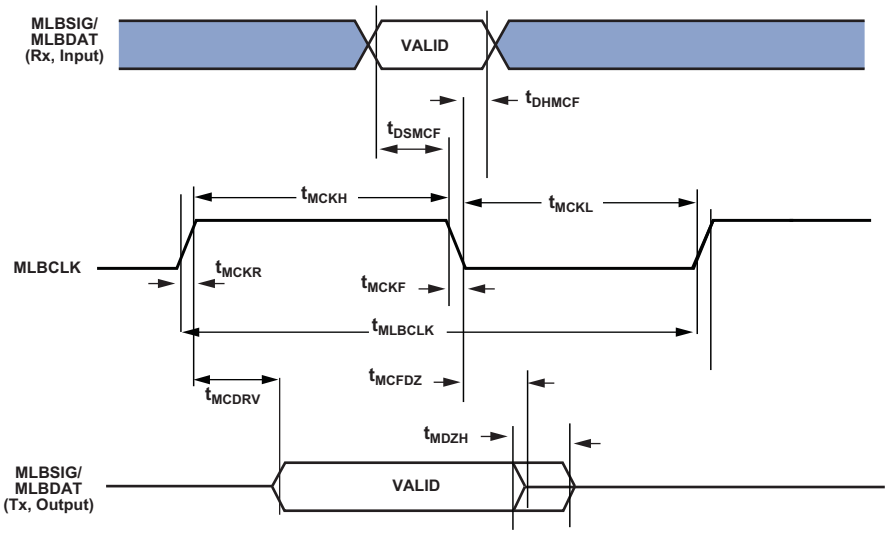

Figure 38. MLB Timing (3-Pin Interface)

Table 53. MLB Interface, 5-Pin Specifications

Parameter		Min	Typ	Max	Unit
5-Pin Characteristics					
t_{MLBCLK}	MLB Clock Period				
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	512 FS	15			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})			6	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})			6	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation			2	ns p-p
t_{DSMCF}[2]	DAT/SIG Input Setup Time	3			ns
t_{DHMCF}	DAT/SIG Input Hold Time	5			ns
t_{MCDRV}	DS/DO Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MCRDL}[3]	DO/SO Low From MLBCLK High				
	512 FS			10	ns
	256 FS			20	ns
C_{mlb}	DS/DO Pin Load			40	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (p-p).
[2] Gate delays due to OR'ing logic on the pins must be accounted for.
[3] When a node is not driving valid data onto the bus, the MLBSO and MLBDO output lines shall remain low. If the output lines can float at anytime, including while in reset, external pull-down resistors are required to keep the outputs from corrupting the MediaLB signal lines when not being driven.

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

For information on the UART port receive and transmit operations, see the *ADSP-214xx SHARC Hardware Reference Manual*.

2-Wire Interface (TWI)—Receive and Transmit Timing

For information on the TWI receive and transmit operations, see the *ADSP-214xx SHARC Hardware Reference Manual*.

JTAG Test Access Port and Emulation

Table 55. JTAG Test Access Port and Emulation

Parameter		88-Lead LFCSP Package Min	88-Lead LFCSP Package Max	All Other Packages Min	All Other Packages Max	Unit
Timing Requirements						
t_{TCK}	TCK Period	20		20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		6		ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	7		7		ns
t_{HSYS}[1]	System Inputs Hold After TCK High	18		18		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	$4 \times t_{CK}$		$4 \times t_{CK}$		ns
Switching Characteristics						
t_{DTDO}	TDO Delay from TCK Low		11.5		10.5	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low		$t_{CK} \div 2 + 7$		$t_{CK} \div 2 + 7$	ns

[1] System Inputs = DATA15–0, CLK_CFG1–0, $\overline{\text{RESET}}$, BOOT_CFG1–0, DAI_Px, DPI_Px, FLAG3–0, MLBCLK, MLBDAT, MLBSIG, SR_SCLK, $\overline{\text{SR_CLR}}$, SR_SDI, and SR_LAT.

[2] System Outputs = DAI_Px, DPI_Px, ADDR23–0, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, FLAG3–0, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, SDCKE, SDA10, SDDQM, SDCLK, MLBDAT, MLBSIG, MLBDO, MLBSO, SR_SDO, SR_LDO, and $\overline{\text{EMU}}$.

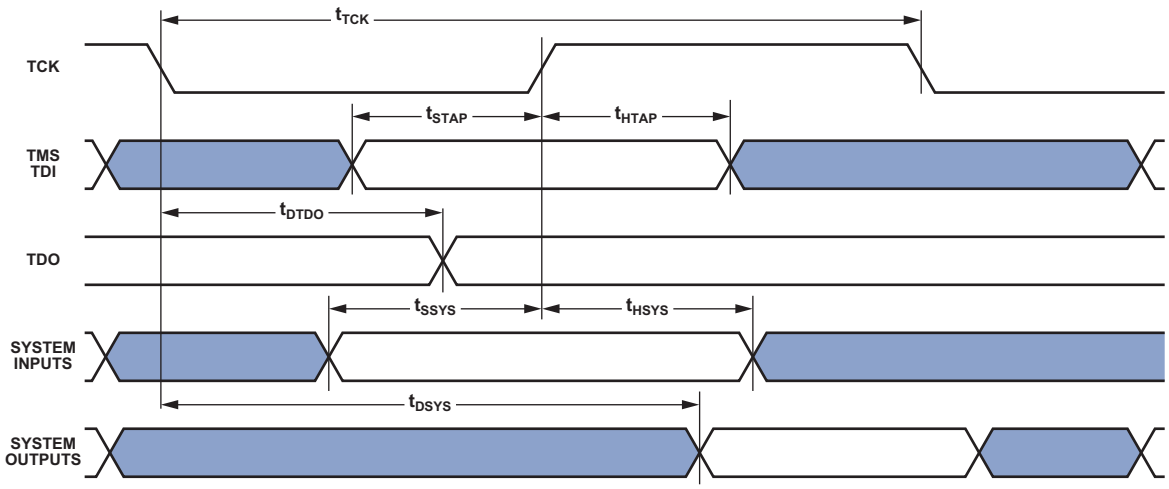

Figure 46. IEEE 1149.1 JTAG Test Access Port

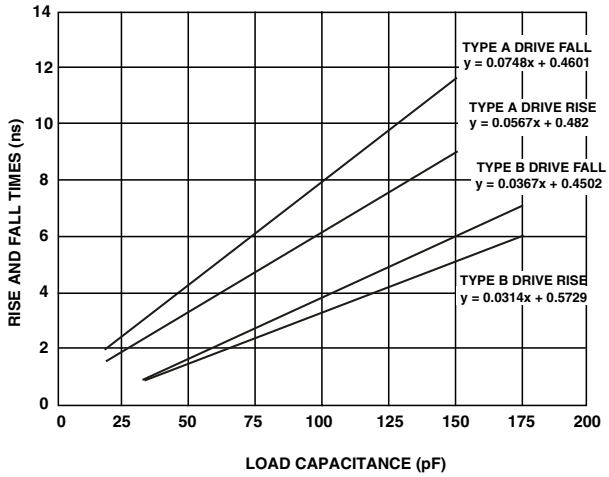

Figure 51. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Min)

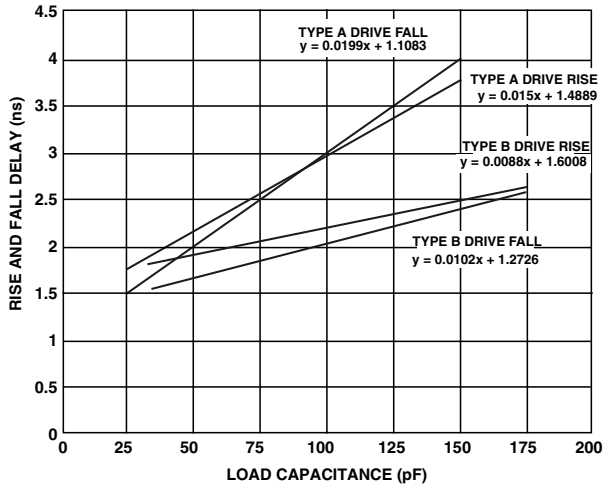

Figure 52. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

THERMAL CHARACTERISTICS

The processor is rated for performance over the temperature range specified in Operating Conditions.

Table 58 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-7 (PBGA). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the typical value from Table 58

P_D = power dissipation

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

Note that the thermal characteristics values provided in Table 58 are modeled values.

Table 57. Thermal Characteristics for 88-Lead LFCSP_VQ

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	22.6	°C/W
θ_{JMA}	Airflow = 1 m/s	18.2	°C/W
θ_{JMA}	Airflow = 2 m/s	17.3	°C/W
θ_{JC}		7.9	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.22	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.36	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.44	°C/W

Table 58. Thermal Characteristics for 100-Lead LQFP_EP

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	18.1	°C/W
θ_{JMA}	Airflow = 1 m/s	15.5	°C/W
θ_{JMA}	Airflow = 2 m/s	14.6	°C/W
θ_{JC}		2.4	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.22	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.36	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.50	°C/W

Table 59. Thermal Characteristics for 196-Ball CSP_BGA

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	29.0	°C/W
θ_{JMA}	Airflow = 1 m/s	26.1	°C/W
θ_{JMA}	Airflow = 2 m/s	25.1	°C/W
θ_{JC}		8.8	°C/W
Ψ_{JT}	Airflow = 0 m/s	0.23	°C/W
Ψ_{JMT}	Airflow = 1 m/s	0.42	°C/W
Ψ_{JMT}	Airflow = 2 m/s	0.52	°C/W

88-LFCSP_VQ LEAD ASSIGNMENT

Table 61 lists the 88-Lead LFCSP_VQ package lead names.

Table 61. 88-Lead LFCSP_VQ Lead Assignments (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
CLK_CFG1	1	V_{DD_EXT}	23	DAI_P10	45	V_{DD_INT}	67
BOOT_CFG0	2	DPI_P08	24	V_{DD_INT}	46	FLAG0	68
V_{DD_EXT}	3	DPI_P07	25	V_{DD_EXT}	47	V_{DD_INT}	69
V_{DD_INT}	4	DPI_P09	26	DAI_P20	48	FLAG1	70
BOOT_CFG1	5	DPI_P10	27	V_{DD_INT}	49	FLAG2	71
GND	6	DPI_P11	28	DAI_P08	50	FLAG3	72
CLK_CFG0	7	DPI_P12	29	DAI_P04	51	GND	73
V_{DD_INT}	8	DPI_P13	30	DAI_P14	52	GND	74
CLKIN	9	DAI_P03	31	DAI_P18	53	V_{DD_EXT}	75
XTAL	10	DPI_P14	32	DAI_P17	54	GND	76
V_{DD_EXT}	11	V_{DD_INT}	33	DAI_P16	55	V_{DD_INT}	77
V_{DD_INT}	12	DAI_P13	34	DAI_P15	56	$\overline{TRST}$	78
V_{DD_INT}	13	DAI_P07	35	DAI_P12	57	$\overline{EMU}$	79
$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	14	DAI_P19	36	DAI_P11	58	TDO	80
V_{DD_INT}	15	DAI_P01	37	V_{DD_INT}	59	V_{DD_EXT}	81
DPI_P01	16	DAI_P02	38	GND	60	V_{DD_INT}	82
DPI_P02	17	V_{DD_INT}	39	THD_M	61	TDI	83
DPI_P03	18	V_{DD_EXT}	40	THD_P	62	TCK	84
V_{DD_INT}	19	V_{DD_INT}	41	V_{DD_THD}	63	V_{DD_INT}	85
DPI_P05	20	DAI_P06	42	V_{DD_INT}	64	$\overline{RESET}$	86
DPI_P04	21	DAI_P05	43	V_{DD_INT}	65	TMS	87
DPI_P06	22	DAI_P09	44	V_{DD_INT}	66	V_{DD_INT}	88
						GND	89*

* Lead no. 89 is the GND supply (see Figure 53 and Figure 54) for the processor; this pad must be **robustly** connected to GND in order for the processor to function.

Figure 53 shows the top view of the 88-lead LFCSP_VQ pin configuration. Figure 54 shows the bottom view.

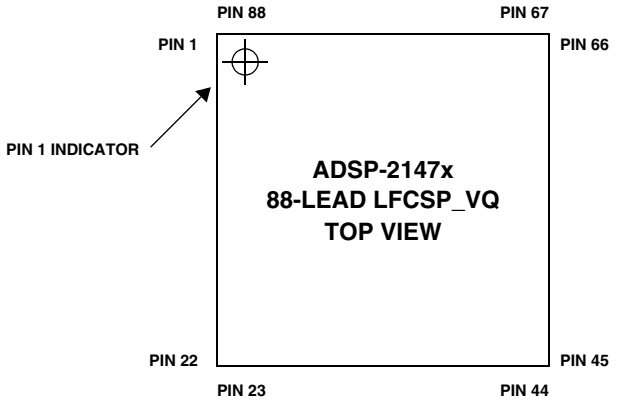

Figure 53. 88-Lead LFCSP_VQ Lead Configuration (Top View)

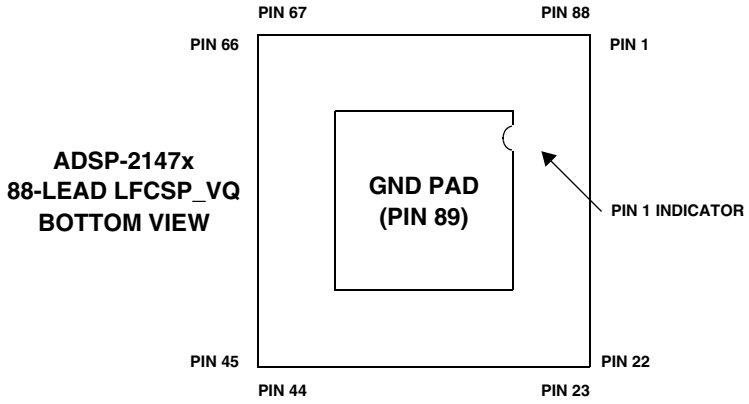

Figure 54. 88-Lead LFCSP_VQ Lead Configuration (Bottom View)

100-LQFP_EP LEAD ASSIGNMENT

Table 62 lists the 100-Lead LQFP_EP lead names.

Table 62. 100-Lead LQFP_EP Lead Assignments (Numerical by Lead Number)

Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.
V_{DD_INT}	1	V_{DD_EXT}	26	DAI_P10	51	V_{DD_INT}	76
CLK_CFG1	2	DPI_P08	27	V_{DD_INT}	52	FLAG0	77
BOOT_CFG0	3	DPI_P07	28	V_{DD_EXT}	53	V_{DD_INT}	78
V_{DD_EXT}	4	V_{DD_INT}	29	DAI_P20	54	V_{DD_INT}	79
V_{DD_INT}	5	DPI_P09	30	V_{DD_INT}	55	FLAG1	80
BOOT_CFG1	6	DPI_P10	31	DAI_P08	56	FLAG2	81
GND	7	DPI_P11	32	DAI_P04	57	FLAG3	82
NC	8	DPI_P12	33	DAI_P14	58	MLBCLK	83
NC	9	DPI_P13	34	DAI_P18	59	MLBDAT	84
CLK_CFG0	10	DAI_P03	35	DAI_P17	60	MLBDO	85
V_{DD_INT}	11	DPI_P14	36	DAI_P16	61	V_{DD_EXT}	86
CLKIN	12	V_{DD_INT}	37	DAI_P15	62	MLBSIG	87
XTAL	13	V_{DD_INT}	38	DAI_P12	63	V_{DD_INT}	88
V_{DD_EXT}	14	V_{DD_INT}	39	V_{DD_INT}	64	MLBSO	89
V_{DD_INT}	15	DAI_P13	40	DAI_P11	65	$\overline{TRST}$	90
V_{DD_INT}	16	DAI_P07	41	V_{DD_INT}	66	$\overline{EMU}$	91
$\overline{RESETOUT}$/$\overline{RUNRSTIN}$	17	DAI_P19	42	V_{DD_INT}	67	TDO	92
V_{DD_INT}	18	DAI_P01	43	GND	68	V_{DD_EXT}	93
DPI_P01	19	DAI_P02	44	THD_M	69	V_{DD_INT}	94
DPI_P02	20	V_{DD_INT}	45	THD_P	70	TDI	95
DPI_P03	21	V_{DD_EXT}	46	V_{DD_THD}	71	TCK	96
V_{DD_INT}	22	V_{DD_INT}	47	V_{DD_INT}	72	V_{DD_INT}	97
DPI_P05	23	DAI_P06	48	V_{DD_INT}	73	$\overline{RESET}$	98
DPI_P04	24	DAI_P05	49	V_{DD_INT}	74	TMS	99
DPI_P06	25	DAI_P09	50	V_{DD_INT}	75	V_{DD_INT}	100
						GND	101*

* Lead no. 101 is the GND supply (see Figure 55 and Figure 56) for the processor; this pad must be **robustly** connected to GND.
MLB pins (pins 83, 84, 85, 87, and 89) are available for automotive models only. For non-automotive models, these pins should be connected to ground (GND).

SURFACE-MOUNT DESIGN

For industry-standard design recommendations, refer to IPC-7351, Generic Requirements for Surface-Mount Design and Land Pattern Standard.

AUTOMOTIVE PRODUCTS

The ADSP-21477, ADSP-21478, and ADSP-21479 are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models, and designers should review the product Specifications section of this data sheet carefully.

Only the automotive grade products shown in Table 64 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 64. Automotive Product Models

Model[1]	Temperature Range[2]	On-Chip SRAM	Processor Instruction Rate (Max)	Package Description	Package Option	Notes
AD21477WYCPZ1Axx	–40°C to +105°C	2M bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5	
AD21477WYSWZ1Axx	–40°C to +105°C	2M bits	200 MHz	100-Lead LQFP_EP	SW-100-2	
AD21478WYBCZ2Axx	–40°C to +105°C	3M bits	200 MHz	196-Ball CSP_BGA	BC-196-8	
AD21478WYCPZ1Axx	–40°C to +105°C	3M bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5	
AD21478WYSWZ2Axx	–40°C to +105°C	3M bits	266 MHz	100-Lead LQFP_EP	SW-100-2	
AD21478WYSWZ2Bxx	–40°C to +105°C	3M bits	266 MHz	100-Lead LQFP_EP	SW-100-2	3, 4
AD21479WYCPZ1Axx	–40°C to +105°C	5M bits	200 MHz	88-Lead LFCSP_VQ	CP-88-5	
AD21479WYCPZ1Bxx	–40°C to +105°C	5M bits	200MHz	88-Lead LFCSP_VQ	CP-88-5	3, 4
AD21479WYSWZ2Axx	–40°C to +105°C	5M bits	266 MHz	100-Lead LQFP_EP	SW-100-2	
AD21479WYSWZ2Bxx	–40°C to +105°C	5M bits	266 MHz	100-Lead LQFP_EP	SW-100-2	3, 4

[1] Z = RoHS compliant part.
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions for junction temperature (T_J) specification, which is the only temperature specification.
[3] Contains multichannel audio decoders from Dolby and DTS. Users must have current licenses from Dolby and DTS to order this product.
[4] Contains Digital Transmission Content Protection (DTCP) from DTLA. User must have current license from DTLA to order this product.