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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Sigma
Interface	I²C, SPI
Clock Rate	25MHz
Non-Volatile Memory	-
On-Chip RAM	3kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adau1702jstz-rl

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SPECIFICATIONS

AVDD = 3.3 V, DVDD = 1.8 V, PVDD = 3.3 V, IOVDD = 3.3 V, master clock input = 12.288 MHz, unless otherwise noted.

ANALOG PERFORMANCE

Specifications are guaranteed at 25°C (ambient).

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC INPUTS					
Number of Channels		2			Stereo input
Resolution		24		Bits	
Full-Scale Input		100 (283)		µA rms (µA p-p)	2 V rms input with 20 kΩ (18 kΩ external + 2 kΩ internal) series resistor
Signal-to-Noise Ratio					
A-Weighted		100		dB	
Dynamic Range					−60 dB with respect to full-scale analog input
A-Weighted	95	100		dB	
Total Harmonic Distortion + Noise		−83		dB	−3 dB with respect to full-scale analog input
Interchannel Gain Mismatch		25	250	mdB	
Crosstalk		−82		dB	Analog channel-to-channel crosstalk
DC Bias	1.4	1.5	1.6	V	
Gain Error	−11		+11	%	
Group Delay		480		µs	Delay is the same across all frequencies
DAC OUTPUTS					
Number of Channels		4			Two stereo output channels
Resolution		24		Bits	
Full-Scale Analog Output		0.9 (2.5)		V rms (V p-p)	
Signal-to-Noise Ratio					
A-Weighted		104		dB	
Dynamic Range					−60 dB with respect to full-scale analog output
A-Weighted	99	104		dB	
Total Harmonic Distortion + Noise		−90		dB	−1 dB with respect to full-scale analog output
Crosstalk		−100		dB	Analog channel-to-channel crosstalk
Interchannel Gain Mismatch		25	250	mdB	
Gain Error	−10		+10	%	
DC Bias	1.4	1.5	1.6	V	
Group Delay		400		µs	Delay is the same across all frequencies
VOLTAGE REFERENCE					
Absolute Voltage (CM)	1.4	1.5	1.6	V	
AUXILIARY ADC					
Full-Scale Analog Input	2.8	3.0	3.1	V	
INL		0.5		LSB	
DNL		1.0		LSB	
Offset		15		mV	
Input Impedance	17.8	30	42	kΩ	

DIGITAL INPUT/OUTPUT

Table 2.

Parameter	Symbol	Min	Typ	Max[1]	Unit	Test Conditions/Comments
Input Voltage, High	V_{IH}	2.0		IOVDD	V	
Input Voltage, Low	V_{IL}			0.8	V	
Input Leakage, High	I_{IH}			1	µA	Excluding MCLKI
Input Leakage, Low	I_{IL}			1	µA	Excluding MCLKI and bidirectional pins
Bidirectional Pin Pull-Up Current, Low				150	µA	
MCLKI Input Leakage, High	I_{IH}			3	µA	
MCLKI Input Leakage, Low	I_{IL}			3	µA	
High Level Output Voltage	V_{OH}	2.0			V	I_{OH} = 2 mA
Low Level Output Voltage	V_{OL}			0.8	V	I_{OL} = 2 mA
Input Capacitance				5	pF	
GPIO Output Drive			2		mA	

[1] Maximum specifications are measured across a temperature range of −40°C to +130°C (case), a DVDD range of 1.62 V to 1.98 V, and an AVDD range of 2.97 V to 3.63 V.

POWER

Table 3.

Parameter	Min	Typ	Max[1]	Unit
SUPPLY VOLTAGE				
Analog Voltage		3.3		V
Digital Voltage		1.8		V
PLL Voltage		3.3		V
IOVDD Voltage		3.3		V
SUPPLY CURRENT				
Analog Current (AVDD and PVDD)		50	85	mA
Digital Current (DVDD)		40	60	mA
Analog Current, Reset		35	55	mA
Digital Current, Reset		1.5	4.5	mA
DISSIPATION				
Operation (AVDD, DVDD, PVDD)[2]		286.5		mW
Reset, All Supplies		118		mW
POWER SUPPLY REJECTION RATIO (PSRR)				
1 kHz, 200 mV p-p Signal at AVDD		50		dB

[1] Maximum specifications are measured across a temperature range of −40°C to +130°C (case), a DVDD range of 1.62 V to 1.98 V, and an AVDD range of 2.97 V to 3.63 V.
[2] Power dissipation does not include IOVDD power because the current drawn from this supply is dependent on the loads at the digital output pins.

PLL AND OSCILLATOR

Table 4. PLL and Oscillator

Parameter	Min	Typ	Max[1]	Unit
PLL Operating Range	MCLK_Nom – 20%		MCLK_Nom + 20%	MHz
PLL Lock Time			20	ms
Crystal Oscillator Transconductance (g_m)		78		mmho

[1] Maximum specifications are measured across a temperature range of −40°C to +130°C (case), a DVDD range of 1.62 V to 1.98 V, and an AVDD range of 2.97 V to 3.63 V.

REGULATOR

Table 5. Regulator

Parameter	Min[1]	Typ[1]	Max[1]	Unit
DVDD Voltage	1.7	1.8	1.84	V

[1] Regulator specifications are calculated using a Zetex Semiconductors FZT953 transistor in the circuit.

Digital Timing Diagrams

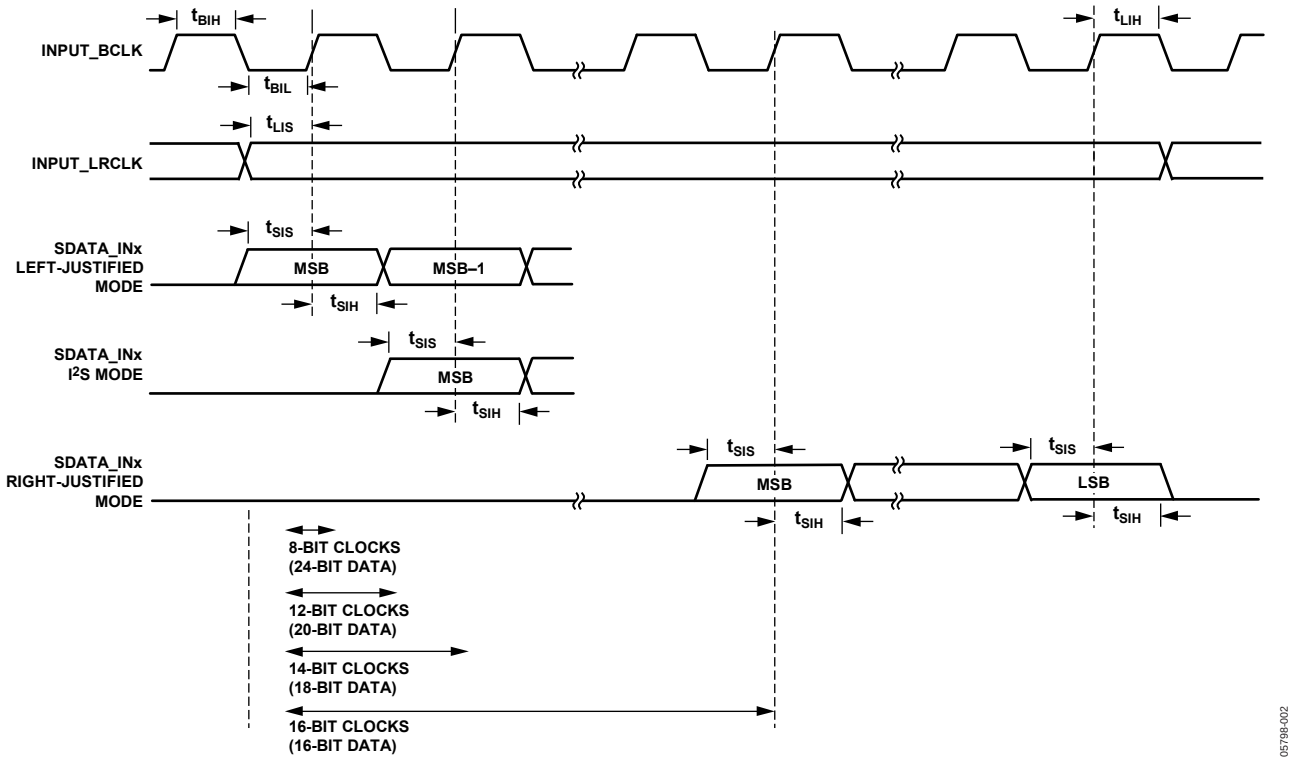

Figure 2. Serial Input Port Timing

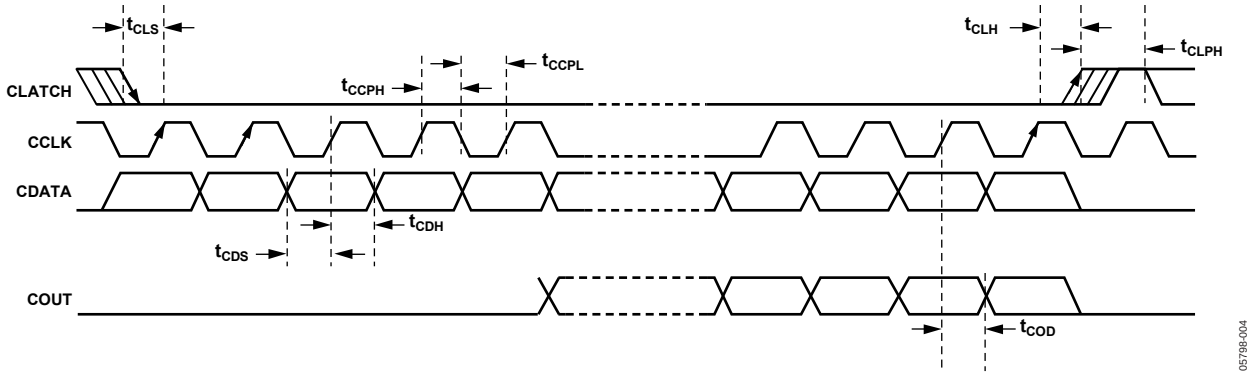

Figure 3. SPI Port Timing

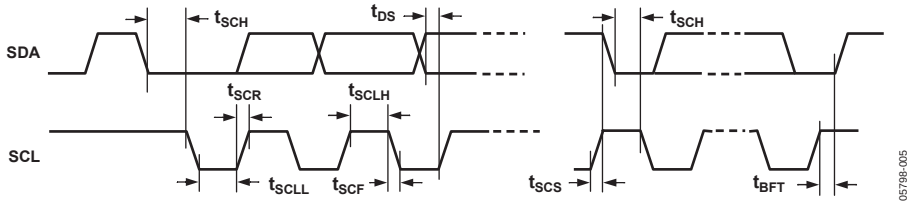

Figure 4. I²C Port Timing

Pin No.	Mnemonic	Type[1]	Description
33	PGND	PWR	PLL Ground Pin. The AGND, DGND, and PGND pins can be tied directly together in a common ground plane. Decouple PGND to PVDD with a 100 nF capacitor.
34	PVDD	PWR	3.3 V Power Supply for the PLL and the Auxiliary ADC Analog Section. Decouple this pin should to PGND with a 100 nF capacitor.
35	PLL_LF	A_OUT	PLL Loop Filter Connection. Two capacitors and a resistor need to be connected to this pin, as shown in Figure 15. See the Setting Master Clock/PLL Mode section for more details.
36, 48	AVDD	PWR	3.3 V Analog Supply. Decouple this pin to AGND with a 100 nF capacitor.
38, 39	PLL_MODE0, PLL_MODE1	D_IN	PLL Mode Setting. PLL_MODE0 and PLL_MODE1 set the output frequency of the master clock PLL. See the Setting Master Clock/PLL Mode section for more details.
40	CM	A_OUT	1.5 V Common-Mode Reference. Connect a 47 µF decoupling capacitor between this pin and ground to reduce crosstalk between the ADCs and DACs. The material of the capacitors is not critical. This pin can be used to bias external analog circuits, as long as those circuits are not drawing current from the pin (such as when CM is connected to the noninverting input of an op amp).
41	FILTD	A_OUT	DAC Filter Decoupling Pin. Connect a 10 µF capacitor between this pin and ground. The capacitor material is not critical. The voltage on this pin is 1.5 V.
43	VOUT3	A_OUT	VOUT3 DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with either an active or passive output reconstruction filter. See the Audio DACs section for details.
44	VOUT2	A_OUT	VOUT2 DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with either an active or passive output reconstruction filter. See the Audio DACs section for details.
45	VOUT1	A_OUT	VOUT1 DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with either an active or passive output reconstruction filter. See the Audio DACs section for details.
46	VOUT0	A_OUT	VOUT0 DAC Output. The full-scale output voltage is 0.9 V rms. This output can be used with either an active or passive output reconstruction filter. See the Audio DACs section for details.
47	FILTA	A_OUT	ADC Filter Decoupling Pin. Connect a 10 µF capacitor between this pin and ground. The capacitor material is not critical. The voltage on this pin is 1.5 V.

[1] PWR is power/ground, A_IN is analog input, D_IN is digital input, A_OUT is analog output, D_IO is digital input/output, D_IO is digital input/output, A_IO is analog input/output, and N/A is not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

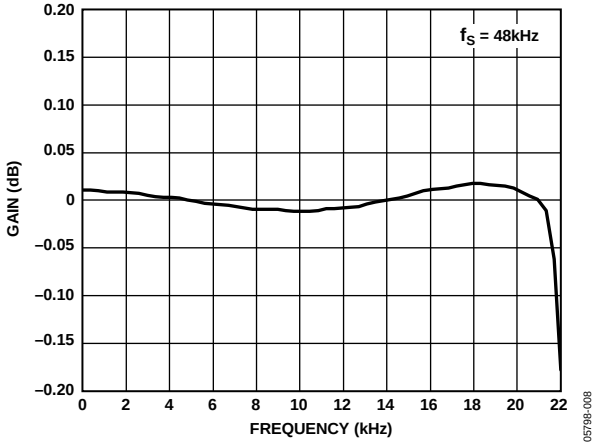

Figure 8. ADC Pass-Band Filter Response

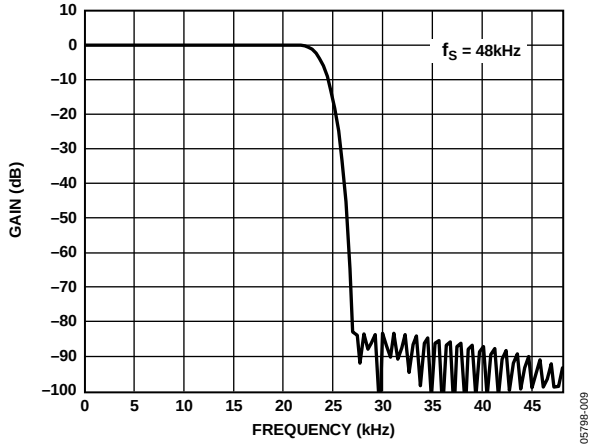

Figure 9. ADC Stop-Band Filter Response

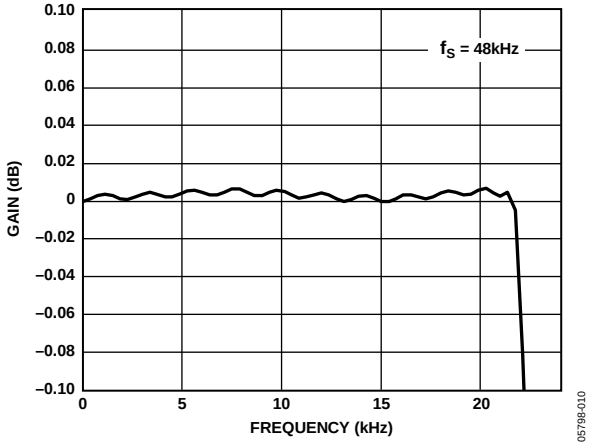

Figure 10. DAC Pass-Band Filter Response

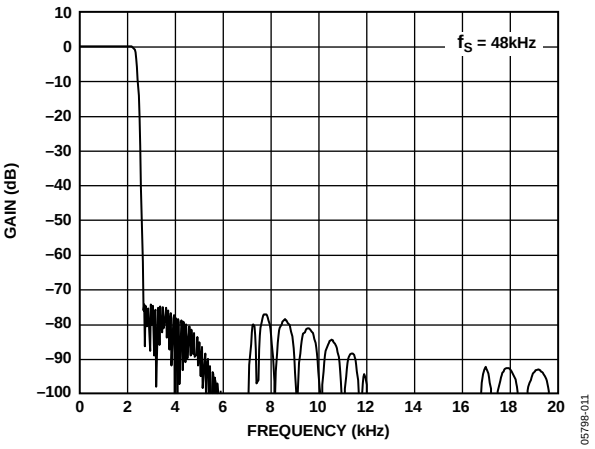

Figure 11. DAC Stop-Band Filter Response

SYSTEM BLOCK DIAGRAM

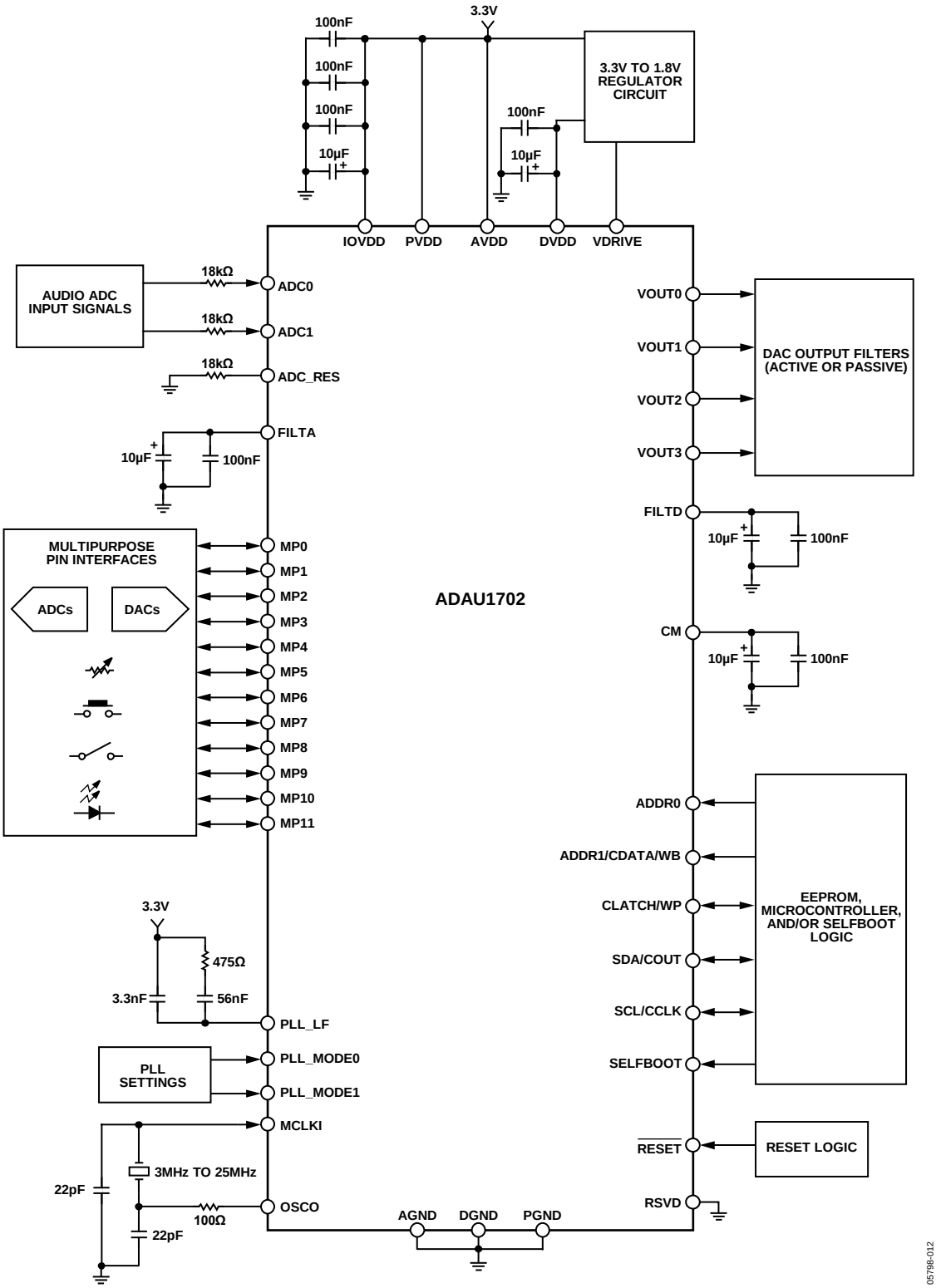

Figure 12. System Block Diagram

INITIALIZATION

This section details the procedure for properly setting up the ADAU1702. The following five-step sequence provides an overview of how to initialize the IC:

1. Apply power to ADAU1702.
2. Wait for PLL to lock.
3. Load the SigmaDSP program and parameters.
4. Set up the registers (including multipurpose pins and digital interfaces).
5. Turn off the default muting of the converters, clear the data registers, and initialize the DAC setup register (see the Control Registers Setup section for specific settings).

POWER-UP SEQUENCE

The ADAU1702 has a built-in power-up sequence that initializes the contents of all internal RAMs on power-up or when the device is brought out of a reset. On the positive edge of $\overline{\text{RESET}}$, the contents of the Internal Program Boot ROM are copied to the Internal Program RAM memory, the parameter, RAM, is filled with values (all 0s) from its associated Boot ROM, and all registers are initialized to 0s. The default Boot ROM program copies audio from the inputs to the outputs without processing it (see Figure 13). In this program, serial digital Input 0 and Input 1 are output on DAC0 and DAC1 and serial digital Output 0 and Output 1. ADC0 and ADC1 are output on DAC2 and DAC3. The data memories are also zeroed at power-up. Do not write new values to the control port until the initialization is complete.

Table 10. Power-Up Time

MCLKI Input	Init. Time	Max Program/ Parameter/Register Boot Time (I²C)	Total
3.072 MHz (64 × f_S)	85 ms	133 ms	218 ms
11.289 MHz (256 × f_S)	23 ms	133 ms	156 ms
12.288 MHz (256 × f_S)	21 ms	133 ms	154 ms
18.432 MHz (384 × f_S)	16 ms	133 ms	149 ms
24.576 MHz (512 × f_S)	11 ms	133 ms	144 ms

The PLL start-up time lasts for 2^{18} cycles of the clock on the MCLKI pin. This time ranges from 10.7 ms for a 24.576 MHz (512 × f_S) input clock to 85.3 ms for a 3.072 MHz (64 × f_S) input clock and is measured from the rising edge of $\overline{\text{RESET}}$. Following the PLL startup, the duration of the ADAU1702 boot cycle is about 42 µs for a f_S of 48 kHz. The user should avoid writing to or reading from the ADAU1702 during this start-up time.

For an MCLK input of 12.288 MHz, the full initialization sequence (PLL startup plus boot cycle) is approximately 21 ms. As the device comes out of a reset, the clock mode is immediately set by the PLL_MODE0 and PLL_MODE1 pins. The reset is synchronized to the falling edge of the internal clock.

Table 10 lists typical times to boot the ADAU1702 into an operational state of an application, assuming a 400 kHz I²C clock loading a full program, parameter set, and all registers (about 6.5 kB). In reality, most applications do not fill the RAMs and therefore boot time (Column 3 of Table 10) is less.

CONTROL REGISTERS SETUP

The following registers must be set as described in this section to initialize the ADAU1702. These settings are the basic minimum settings needed to operate the IC with an analog input/output of 48 kHz. More registers may need to be set, depending on the application. See the RAMs and Registers section for additional settings.

DSP Core Control Register (Address 2076)

Set Bits[4:2] (ADM, DAM, and CR) each to 1.

DAC Setup Register (Address 2087)

Set Bits[0:1] (DS[1:0]) to 01.

RECOMMENDED PROGRAM/PARAMETER LOADING PROCEDURE

When writing large amounts of data to the program or parameter RAM in direct write mode, the processor core should be disabled to prevent unpleasant noises from appearing in the audio output.

1. Set Bit 3 and Bit 4 (active low) of the core control register to 1 to mute the ADCs and DACs. This begins a volume ramp-down.
2. Set Bit 2 (active low) of the core control register to 1. This zeroes the SigmaDSP accumulators, the data output registers, and the data input registers.
3. Fill the program RAM using burst mode writes.
4. Fill the parameter RAM using burst mode writes.
5. Deassert Bit 2 to Bit 4 of the core control register.

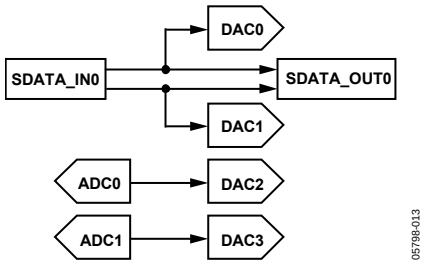

Figure 13. Default Program Signal Flow

POWER REDUCTION MODES

Sections of the ADAU1702 chip can be turned on and off as needed to reduce power consumption. These include the ADCs, DACs, and voltage reference.

The individual analog sections can be turned off by writing to the auxiliary ADC and power control register. By default, the ADCs, DACs, and reference are enabled (all bits set to 0). Each of these can be turned off by writing a 1 to the appropriate bits in this register. The ADC power-down mode powers down both ADCs, and each DAC can be powered down individually. The current savings is about 15 mA when the ADCs are powered down and about 4 mA for each DAC that is powered down. The voltage reference, which is supplied to both the ADCs and DACs, should only be powered down if all ADCs and DACs are powered down. The reference is powered down by setting both Bit 6 and Bit 7 of the control register.

USING THE OSCILLATOR

The ADAU1702 can use an on-board oscillator to generate its master clock. The oscillator is designed to work with a 256 × f_S master clock, which is 12.288 MHz for a f_S of 48 kHz and 11.2896 MHz for a f_S of 44.1 kHz. The crystal in the oscillator circuit should be an AT-cut, parallel resonator operating at its fundamental frequency. Figure 14 shows the external circuit recommended for proper operation.

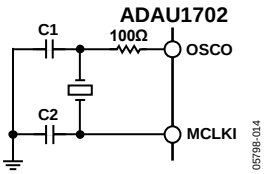

Figure 14. Crystal Oscillator Circuit

The 100 Ω damping resistor on OSCO gives the oscillator a voltage swing of approximately 2.2 V. The crystal shunt capacitance should be 7 pF. Its load capacitance should be about 18 pF, although the circuit supports values of up to 25 pF. The necessary values of the C1 and C2 load capacitors can be calculated from the crystal load capacitance as follows:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_{stray}$$

where C_{stray} is the stray capacitance in the circuit and is usually assumed to be approximately 2 pF to 5 pF.

OSCO should not be used to drive the crystal signal directly to another IC. This signal is an analog sine wave, and it is not appropriate to use it to drive a digital input. There are two options for using the ADAU1702 to provide a master clock to other ICs in the system. The first, and less recommended, method is to use a high impedance input digital buffer on the OSCO signal. If this approach is used, minimize the trace length to the buffer input. The second method is to use a clock from the serial output port. Pin MP11 can be set as an output (master) clock divided down from the internal core clock. If this pin is set to serial output port (OUTPUT_BCLK) mode in the multipurpose pin configuration register (Address 2081) and the port is set to master in the serial output control register (Address 2078), the desired output frequency can also be set in the serial output control register with the OBF[1:0] bits (see Table 47).

If the oscillator is not used in the design, it can be powered down to save power. This can be done if a system master clock is already available in the system. By default, the oscillator is powered on. The oscillator powers down when a 1 is written to the OPD bit of the oscillator power-down register (see Table 58).

SETTING MASTER CLOCK/PLL MODE

The MCLKI input of the ADAU1702 feeds a PLL, which generates the 25 MIPS SigmaDSP core clock. In normal operation, the input to MCLKI must be one of the following: 64 × f_S, 256 × f_S, 384 × f_S, or 512 × f_S, where f_S is the input sampling rate. The mode is set on PLL_MODE0 and PLL_MODE1 as described in Table 11. If the ADAU1702 is set to receive double-rate signals (by reducing the number of program steps per sample by a factor of 2 using the core control register), the master clock frequency must be 32 × f_S, 128 × f_S, 192 × f_S, or 256 × f_S. If the ADAU1702 is set to receive quad-rate signals (by reducing the number of program steps per sample by a factor of 4 using the core control register), the master clock frequency must be 16 × f_S, 64 × f_S, 96 × f_S, or 128 × f_S. On power-up, a clock signal must be present on the MCLKI pin so that the ADAU1702 can complete its initialization routine.

Table 11. PLL Modes

MCLKI Input	PLL_MODE0	PLL_MODE1
64 × f_S	0	0
256 × f_S	0	1
384 × f_S	1	0
512 × f_S	1	1

Do not change the clock mode without also resetting the ADAU1702. If the mode is changed during operation, a click or pop can result in the output signals. Change the state of the PLL_MODEx pins while holding $\overline{\text{RESET}}$ low.

Connect the PLL loop filter to the PLL_LF pin. This filter, shown in Figure 15, includes three passive components—two capacitors and a resistor. The values of these components do not need to be exact; the tolerance can be up to 10% for the resistor and up to 20% for the capacitors. The 3.3 V signal shown in Figure 15 can be connected to the AVDD supply of the chip.

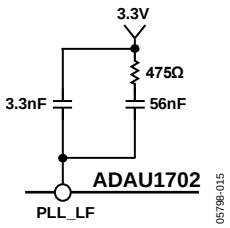

Figure 15. PLL Loop Filter

AUDIO ADCs

The ADAU1702 has two Σ-Δ ADCs. The signal-to-noise ratio (SNR) of the ADCs is 100 dB, and the THD + N is −83 dB.

The stereo audio ADCs are current input; therefore, a voltage-to-current resistor is required on the inputs. This means that the voltage level of the input signals to the system can be set to any level; only the input resistors need to be scaled to provide the proper full-scale current input. The ADC0 and ADC1 input pins, as well as ADC_RES, have an internal 2 kΩ resistor for ESD protection. The voltage seen directly on the ADC input pins is the 1.5 V common mode.

The external resistor connected to ADC_RES sets the full-scale current input of the ADCs. The full range of the ADC inputs is 100 μA rms with an external 18 kΩ resistor on ADC_RES (20 kΩ total, because it is in series with the internal 2 kΩ). The only reason to change the ADC_RES resistor is if a sampling rate other than 48 kHz is used.

The voltage-to-current resistors connected to ADC0/ADC1 set the full-scale voltage input of the ADCs. With a full-scale current input of 100 μA rms, a 2.0 V rms signal with an external 18 kΩ resistor (in series with the 2 kΩ internal resistor) results in an input using the full range of the ADC. The matching of these resistors to the ADC_RES resistor is important to the operation of the ADCs. For these three resistors, a 1% tolerance is recommended.

Either the ADC0 and/or ADC1 input pins can be left unconnected if that channel of the ADC is unused.

These calculations of resistor values assume a 48 kHz sample rate. The recommended input and current setting resistors scale linearly with the sample rate because the ADCs have a switched-capacitor input. The total value (2 kΩ internal plus external resistor) of the ADC_RES resistor with sample rate f_{S_NEW} can be calculated as follows:

$$R_{TOTAL} = 20\ \text{k}\Omega \times \frac{48{,}000}{f_{S\_NEW}}$$

The values of the resistors (internal plus external) in series with the ADC0 and ADC1 pins can be calculated as follows:

$$R_{INPUT\ TOTAL} = (rms\ Input\ Voltage) \times 10\ \text{k}\Omega \times \frac{48{,}000}{f_{S\_NEW}}$$

Table 12 lists the external and total resistor values for common signal input levels at a 48 kHz sampling rate. A full-scale rms input voltage of 0.9 V is shown in the table because a full-scale signal at this input level is equal to a full-scale output on the DACs.

Table 12. ADC Input Resistor Values

Full-Scale RMS Input Voltage (V)	ADC_RES Value (kΩ)	ADC0/ADC1 Resistor Value (kΩ)	Total ADC0/ADC1 Input Resistance (External + Internal) (kΩ)
0.9	18	7	9
1.0	18	8	10
2.0	18	18	20

Figure 17 shows a typical configuration of the ADC inputs for a 2.0 V rms input signal for a f_S of 48 kHz. The 47 μF capacitors are used to ac-couple the signals so that the inputs are biased at 1.5 V.

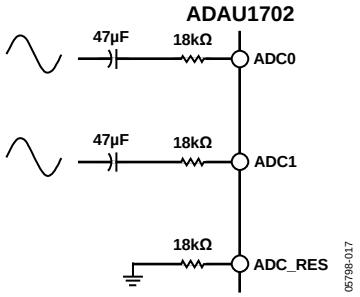

Figure 17. Audio ADC Input Configuration

AUDIO DACs

The ADAU1702 includes four Σ-Δ DACs. The SNR of the DAC is 104 dB, and the THD + N is −90 dB. A full-scale output on the DACs is 0.9 V rms (2.5 V p-p).

The DACs are in an inverting configuration. If a signal inversion from input to output is undesirable, it can be reversed either by using an inverting configuration for the output filter or by simply inverting the signal in the SigmaDSP program flow.

The DAC outputs can be filtered with either an active or a passive reconstruction filter. A single-pole, passive, low-pass filter with a 50 kHz corner frequency, as shown in Figure 18, is sufficient to filter the DAC out-of-band noise, although an active filter may provide better audio performance. Figure 19 shows a triple-pole, active, low-pass filter that provides a steeper roll-off and better stop-band attenuation than the passive filter. In this configuration, the V+ and V− pins of the AD8606 op amp are set to AVDD and ground, respectively.

To properly initialize the DACs, the DS[1:0] bits in the DAC setup register (Address 2087) should be set to 01.

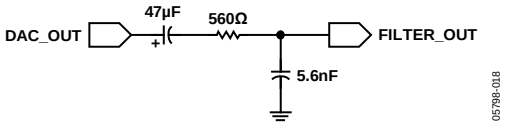

Figure 18. Passive DAC Output Filter

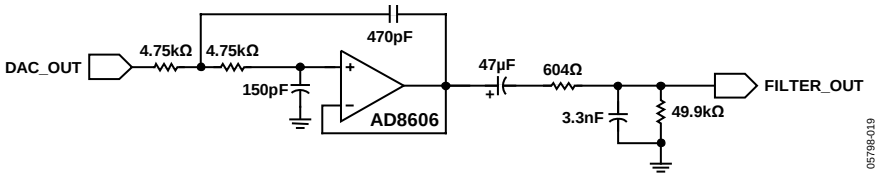

Figure 19. Active DAC Output Filter

I²C PORT

The ADAU1702 supports a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. Two pins, serial data (SDA) and serial clock (SCL), carry information between the ADAU1702 and the system I²C master controller. In I²C mode, the ADAU1702 is always a slave on the bus, meaning it cannot initiate a data transfer. Each slave device is recognized by a unique address. The address byte format is shown in Table 14. The ADAU1702 slave addresses are set with the ADDR0 and ADDR1 pins. The address resides in the first seven bits of the I²C write. The LSB of this byte sets either a read or write operation. Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation. Bit 5 and Bit 6 of the address are set by tying the ADDRx pins of the ADAU1702 to Logic Level 0 or Logic Level 1. The full byte addresses, including the pin settings and read/write (R/$\overline{W}$) bit, are shown in Table 15.

Burst mode addressing, where the subaddresses are automatically incremented at word boundaries, can be used for writing large amounts of data to contiguous memory locations. This increment happens automatically after a single-word write unless a stop condition is encountered. The registers and RAMs in the ADAU1702 range in width from one to five bytes, so the auto-increment feature knows the mapping between subaddresses and the word length of the destination register (or memory location). A data transfer is always terminated by a stop condition.

Both SDA and SCL should have 2.2 kΩ pull-up resistors on the lines connected to them. The voltage on these signal lines should not be more than IOVDD (3.3 V).

Table 14. ADAU1702 I²C Address Byte Format

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	1	1	0	1	ADDR1	ADDR0	R/$\overline{W}$

Table 15. ADAU1702 I²C Addresses

ADDR1	ADDR0	R/$\overline{W}$	Slave Address
0	0	0	0x68
0	0	1	0x69
0	1	0	0x6A
0	1	1	0x6B
1	0	0	0x6C
1	0	1	0x6D
1	1	0	0x6E
1	1	1	0x6F

Addressing

Initially, each device on the I²C bus is in an idle state monitoring the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address or an address and a data stream follow. All devices on the bus respond to the start condition and shift the next eight bits (the 7-bit address plus the R/$\overline{W}$ bit) MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition. The R/$\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means the master writes information to the peripheral, whereas a Logic 1 means the master reads infor-mation from the peripheral after writing the subaddress and repeating the start address. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. Figure 20 shows the timing of an I²C write, and Figure 21 shows an I²C read.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, the ADAU1702 immediately jumps to the idle condition. During a given SCL high period, the user should only issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADAU1702 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while in auto-increment mode, one of two actions is taken. In read mode, the ADAU1702 outputs the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth clock pulse on SCL. On the other hand, if the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADAU1702, and the part returns to the idle condition.

Table 20. Parameter RAM Read/Write Format (Single Address)

Byte 0	Byte 1	Byte 2	Byte 3	Bytes[4:6]
CHIP_ADR[6:0], $\overline{W}$/R	000000, PARAM_ADR[9:8]	PARAM_ADR[7:0]	0000, PARAM[27:24]	PARAM[23:0]

Table 21. Parameter RAM Block Read/Write Format (Burst Mode)

Byte 0	Byte 1	Byte 2	Byte 3	Bytes[4:6]	Bytes[7:10]	Bytes[11:14]
CHIP_ADR[6:0], $\overline{W}$/R	000000, PARAM_ADR[9:8]	PARAM_ADR[7:0]	0000, PARAM[27:24]	PARAM[23:0]		
			<—PARAM_ADR—>		PARAM_ADR + 1	PARAM_ADR + 2

Table 22. Program RAM Read/Write Format (Single Address)

Byte 0	Byte 1	Byte 2	Bytes[3:7]
CHIP_ADR[6:0], $\overline{W}$/R	00000, PROG_ADR[10:8]	PROG_ADR[7:0]	PROG[39:0]

Table 23. Program RAM Block Read/Write Format (Burst Mode)

Byte 0	Byte 1	Byte 2	Bytes[3:7]	Bytes[8:12]	Bytes[13:17]
CHIP_ADR[6:0], $\overline{W}$/R	00000, PROG_ADR[10:8]	PROG_ADR[7:0]	PROG[39:0]		
			<—PROG_ADR—>	PROG_ADR + 1	PROG_ADR + 2

Table 24. Control Register Read/Write Format (Core, Serial Out 0, Serial Out 1)

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
CHIP_ADR[6:0], $\overline{W}$/R	0000, REG_ADR[11:8]	REG_ADR[7:0]	Data[15:8]	Data[7:0]

Table 25. Control Register Read/Write Format (RAM Configuration, Serial Input)

Byte 0	Byte 1	Byte 2	Byte 3
CHIP_ADR[6:0], $\overline{W}$/R	0000, REG_ADR[11:8]	REG_ADR[7:0]	Data[7:0]

Table 26. Data Capture Register Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
CHIP_ADR[6:0], $\overline{W}$/R	0000, DATA_CAPTURE_ADR[11:8]	DATA_CAPTURE_ADR[7:0]	000, PROGCOUNT[10:6] [1]	PROGCOUNT[5:0][1], REGSEL[1:0] [2]

[1] PROGCOUNT[10:0] is the value of the program counter when the data capture occurs (the table of values is generated by the SigmaStudio compiler).
[2] REGSEL[1:0] selects one of four registers (see the 2074 to 2075 (0x081A to 0x081B)—Data Capture Registers section).

Table 27. Data Capture (Control Port Readback) Register Read Format

Byte 0	Byte 1	Byte 2	Bytes[3:5]
CHIP_ADR[6:0], $\overline{W}$/R	0000, DATA_CAPTURE_ADR[11:8]	DATA_CAPTURE_ADR[7:0]	Data[23:0]

Table 28. Safeload Address Register Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
CHIP_ADR[6:0], $\overline{W}$/R	0000, SAFELOAD_ADR[11:8]	SAFELOAD_ADR[7:0]	000000, PARAM_ADR[9:8]	PARAM_ADR[7:0]

Table 29. Safeload Data Register Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Bytes[5:7]
CHIP_ADR[6:0], $\overline{W}$/R	0000, SAFELOAD_ADR[11:8]	SAFELOAD_ADR[7:0]	00000000	0000, Data[27:24]	Data[23:0]

ADDRESS 2056 (0x0808)—GPIO PIN SETTING REGISTER

This register allows the user to set the GPIO pins through the control port. High or low settings can be directly written to or read from this register after setting the GPIO pin to set the register control port write (GPCW) mode in the core control register. This register is updated once every LRCLK frame ($1/f_S$).

Table 33. GPIO Pin Setting Register Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0	0	0	0	MP11	MP10	MP09	MP08	MP07	MP06	MP05	MP04	MP03	MP02	MP01	MP00	0x0000

Table 34.

Bit Name	Description
MP[11:0]	Setting of multipurpose pin when controlled through SPI or I^2C

ADDRESS 2057 TO ADDRESS 2060 (0x0809 TO 0x080C)—AUXILIARY ADC DATA REGISTERS

These registers hold the data generated by the 4-channel auxiliary ADC. The ADCs have eight bits of precision and can be extended to 12 bits if filtering is selected via Bits FIL[1:0] of the auxiliary ADC and power control register. The SigmaDSP program reads this data as a 1.11 format data-word with a range of 0 to 1.0. This data-word is mapped to the 5.23 format parameter word with the four MSBs and 12 LSBs set to 0. A full-scale code of 255 results in a value of 1.0 in 5.23 format. These registers can be written to directly if the auxiliary ADC data registers control port write (AACW) mode bit is set in the DSP core control register.

Table 35. Auxiliary ADC Data Register Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0	0	0	0	AA11	AA10	AA09	AA08	AA07	AA06	AA05	AA04	AA03	AA02	AA01	AA00	0x0000

Table 36.

Bit Name	Description
AA[11:0]	Auxiliary ADC output data, MSB first

ADDRESS 2064 TO ADDRESS 2068 (0x0810 TO 0x0814)—SAFELOAD DATA REGISTERS

Many applications require real-time microcontroller control of signal processing parameters, such as filter coefficients, mixer gains, multichannel virtualizing parameters, or dynamics processing curves. When controlling a biquad filter, for example, all of the parameters must be updated at the same time. Doing so prevents the filter from executing with a mix of old and new coefficients for one or two audio frames, thus avoiding temporary instability and transients that may take a long time to decay. To accomplish this, the ADAU1702 uses safeload data registers to simultaneously load a set of five 28-bit values to the desired parameter RAM address. Five registers are used because a biquad filter uses five coefficients and, as previously mentioned, it is desirable to do a complete update in one transaction.

The first step in performing a safeload operation is writing the parameter address to one of the safeload address registers (Address 2069 to Address 2073). The 10-bit data-word to be written is the address in parameter RAM to which the safeload is being performed. After this address is written, the 28-bit data-word can be written to the corresponding safeload data register (Address 2064 to Address 2068).

The data formats for these writes are detailed in Table 28 and Table 29. Table 37 shows how each of the five address registers maps to its corresponding data register.

After the address and data registers are loaded, set the initiate safeload transfer bit in the core control register to initiate the loading into RAM. Each of the five safeload registers takes one of the 512 core instructions to load into the parameter RAM. The total program lengths should, therefore, be limited to 507 cycles (512 minus 5) to ensure that the SigmaDSP core always has at least five cycles available. The safeload is guaranteed to occur within one LRCLK period (21 μs for a f_S of 48 kHz) of the initiate safeload transfer bit being set.

The safeload logic automatically sends data to be loaded into RAM from only those safeload registers that have been written to since the last safeload operation. For example, if two parameters are to be updated in the RAM, only two of the five safeload registers must be written. When the initiate safeload transfer bit is asserted, only data from those two registers are sent to the RAM; the other three registers are not sent to the RAM and may hold old or invalid data.

Table 37. Safeload Address and Data Register Mapping

Safeload Register	Safeload Address Register	Safeload Data Register
0	2069	2064
1	2070	2065
2	2071	2066
3	2072	2067
4	2073	2068

Table 38. Safeload Registers Bit Map

D31 D15	D30 D14	D29 D13	D28 D12	D27 D11	D26 D10	D25 D9	D24 D8	D39 D23 D7	D38 D22 D6	D37 D21 D5	D36 D20 D4	D35 D19 D3	D34 D18 D2	D33 D17 D1	D32 D16 D0	Default
								SD39	SD38	SD37	SD36	SD35	SD34	SD33	SD32	0x00
SD31	SD30	SD29	SD28	SD27	SD26	SD25	SD24	SD23	SD22	SD21	SD20	SD19	SD18	SD17	SD16	0x0000
SD15	SD14	SD13	SD12	SD11	SD10	SD09	SD08	SD07	SD06	SD05	SD04	SD03	SD02	SD01	SD00	0x0000

Table 39.

Bit Name	Description
SD[39:0]	Safeload data. Data (program, parameters, and register contents) to be loaded into the RAMs or registers.

ADDRESS 2069 TO ADDRESS 2073 (0x0815 TO 0x0819)—SAFELOAD ADDRESS REGISTERS

Table 40. Safeload Address Registers Bit Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0	0	0	0	SA11	SA10	SA09	SA08	SA07	SA06	SA05	SA04	SA03	SA02	SA01	SA00	0x0000

Table 41.

Bit Name	Description
SA[11:0]	Safeload address. Address of data that is to be loaded into the RAMs or registers.

ADDRESS 2079 (0x081F)—SERIAL INPUT CONTROL REGISTER

Table 48. Serial Input Control Register Bit Map

D7	D6	D5	D4	D3	D2	D1	D0	Default
0	0	0	ILP	IBP	M2	M1	M0	0x00

Table 49. Serial Input Control Register Bit Descriptions

Bit Name	Description	
ILP	INPUT_LRCLK polarity. When this bit is set to 0, the left channel data on the SDATA_INx pins is clocked when INPUT_LRCLK is low and the right channel data is clocked when INPUT_LRCLK is high. When this bit is set to 1, the clocking of these channels is reversed. In TDM mode, when this bit is set to 0, data is clocked in starting with the next appropriate BCLK edge (set in Bit 3 of this register) after a falling edge on the INPUT_LRCLK pin. When this bit is set to 1 and the device is running in TDM mode, the input data is valid on the BCLK edge after a rising edge on the word clock (INPUT_LRCLK). INPUT_LRCLK can also operate with a pulse input, rather than a clock; in this case, the first edge of the pulse is used by the ADAU1702 to start the data frame. When this polarity bit is set to 0, use a low pulse; when the bit it set to 1, use a high pulse.	
IBP	INPUT_BCLK polarity. This bit controls on which edge of the bit clock the input data changes and on which edge it is clocked. Data changes on the falling edge of INPUT_BCLK when this bit is set to 0 and on the rising edge when this bit is set at 1.	
M[2:0]	Serial input mode. These two bits control the data format that the input port expects to receive. Bit 3 and Bit 4 of this control register override the settings of Bits[2:0]; therefore, all four bits must be changed together for proper operation in some modes. The clock diagrams for these modes are shown in Figure 32, Figure 33, and Figure 34. Note that for left-justified and right-justified modes, the LRCLK polarity is high and then low, which is the opposite of the default setting for ILP. When these bits are set to accept a TDM input, the ADAU1702 data starts after the edge defined by ILP. Input the ADAU1702 TDM data stream on Pin SDATA_IN0. Figure 35 shows a TDM stream with a high-to-low triggered LRCLK and data changing on the falling edge of the BCLK. The ADAU1702 expects the MSB of each data slot to be delayed by one BCLK from the beginning of the slot, as it would in stereo I²S format. In TDM mode, Channel 0 to Channel 3 are in the first half of the frame, and Channel 4 to Channel 7 are in the second half. Figure 36 shows an example of a TDM stream running with a pulse word clock, which is used to interface to ADI codecs in auxiliary mode. To work in this mode with either the input or output serial ports, set the ADAU1702 to begin the frame on the rising edge of LRCLK, to change data on the falling edge of BCLK, and to delay the MSB position from the start of the word clock by one BCLK.	
	Setting	**Function**
	000	I²S
	001	Left justified
	010	TDM
	011	Right justified, 24 bits
	100	Right justified, 20 bits
	101	Right justified, 18 bits
	110	Right justified, 16 bits
	111	Reserved

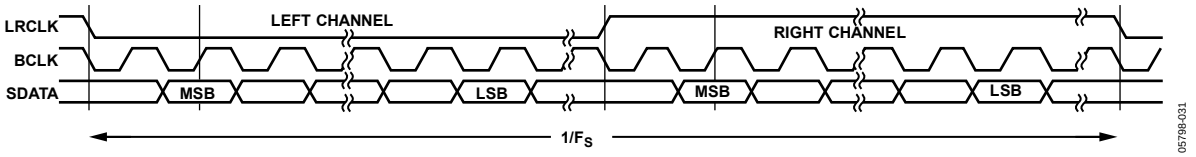

Figure 32. I²S Mode—16 Bits to 24 Bits Per Channel

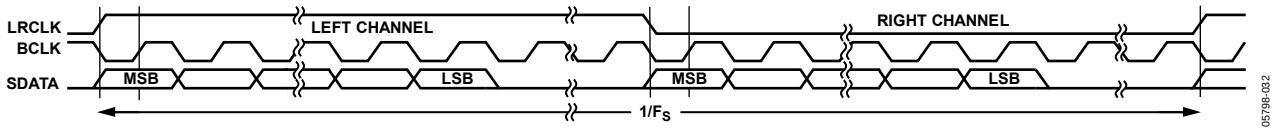

Figure 33. Left-Justified Mode—16 Bits to 24 Bits Per Channel

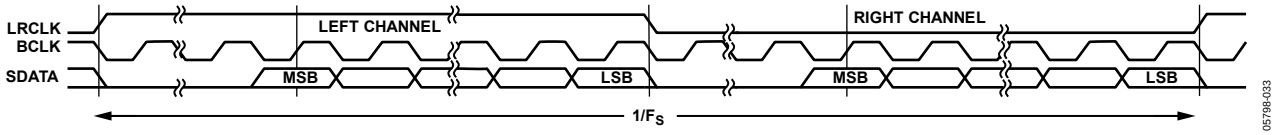

Figure 34. Right-Justified Mode—16 Bits to 24 Bits Per Channel

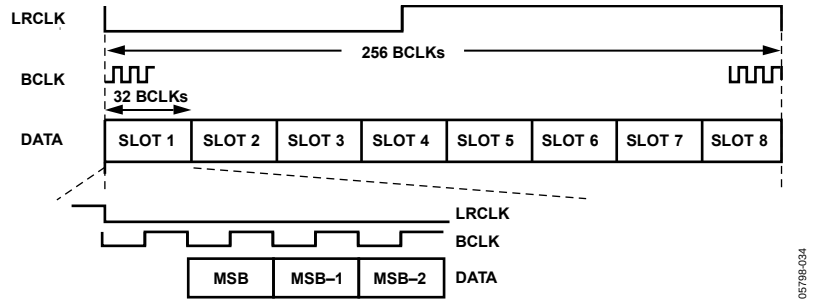

Figure 35. TDM Mode

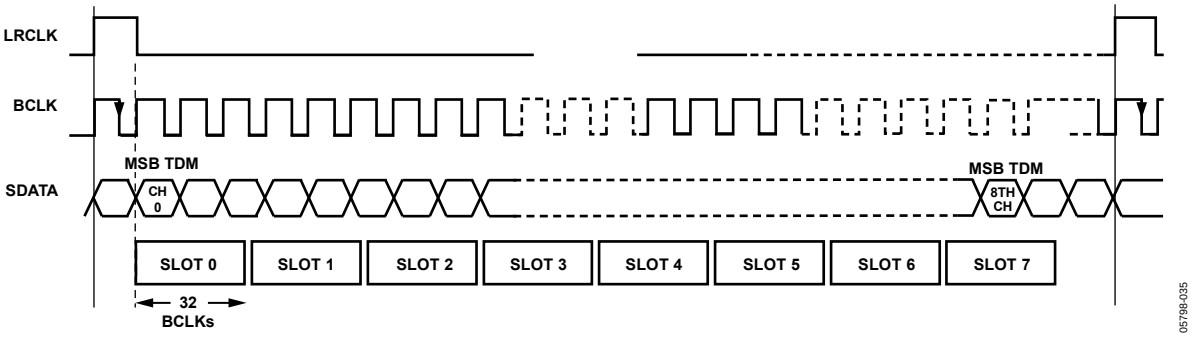

Figure 36. TDM Mode with Pulse Word Clock

SPI CONTROL

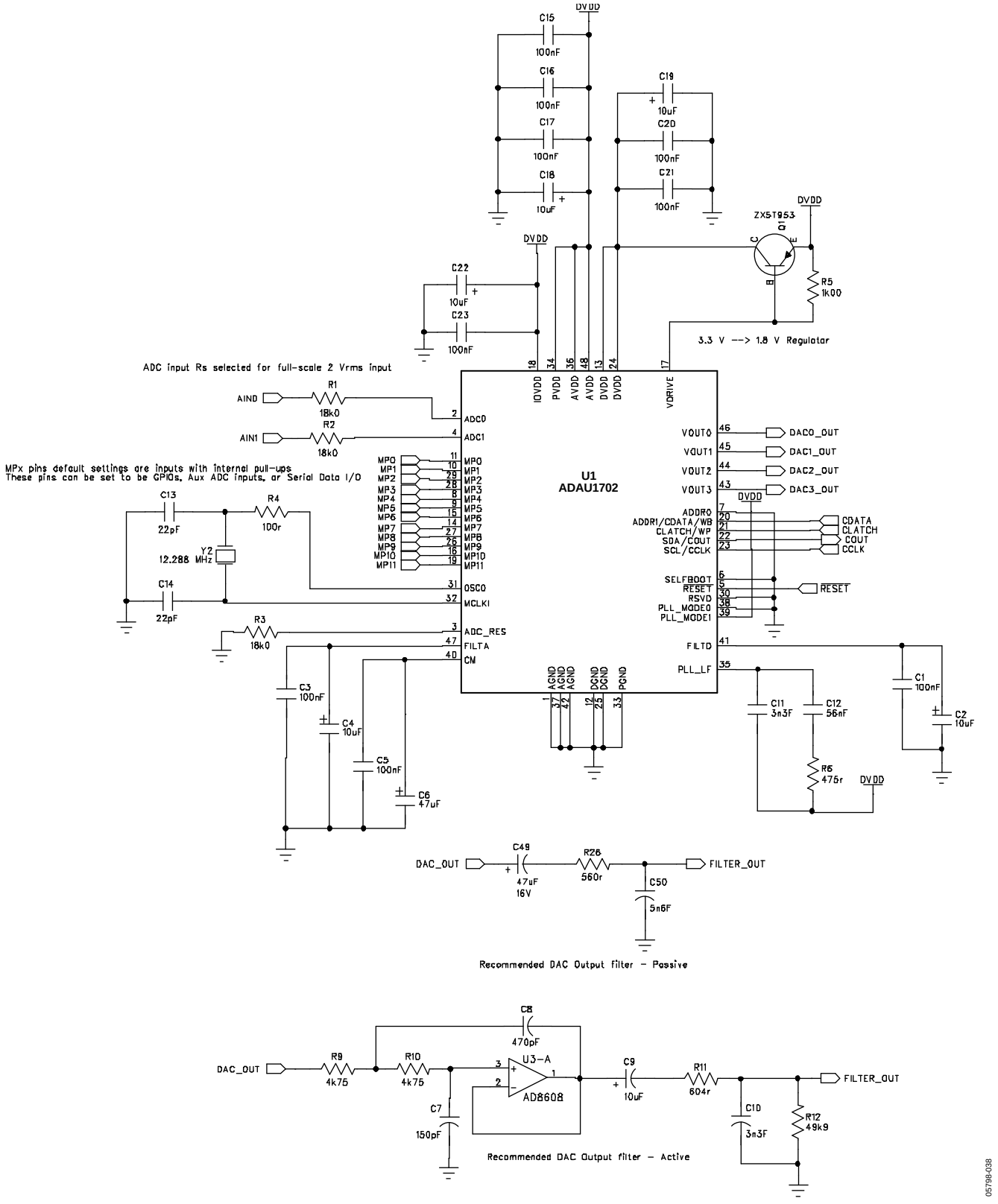

Figure 39. SPI Control Schematic

OUTLINE DIMENSIONS

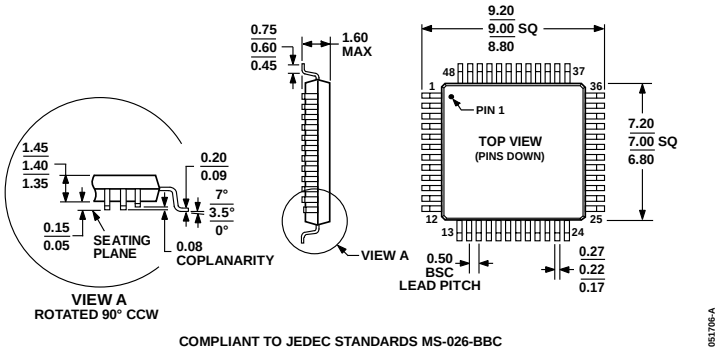

Figure 40. 48-Lead Low-Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model [1, 2]	Temperature Range	Package Description	Package Option
ADAU1702JSTZ	0°C to +70°C	48-Lead LQFP	ST-48
ADAU1702JSTZ-RL	0°C to +70°C	48-Lead LQFP in 13" Tape and Reel	ST-48
EVAL-ADAU1401EBZ		Evaluation Board	
EVAL-ADAU1701MINIZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] The EVAL-ADAU1401EBZ and the EVAL-ADAU1701MINIZ are used to evaluate the ADAU1702, ADAU1701, and the ADAU1401.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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