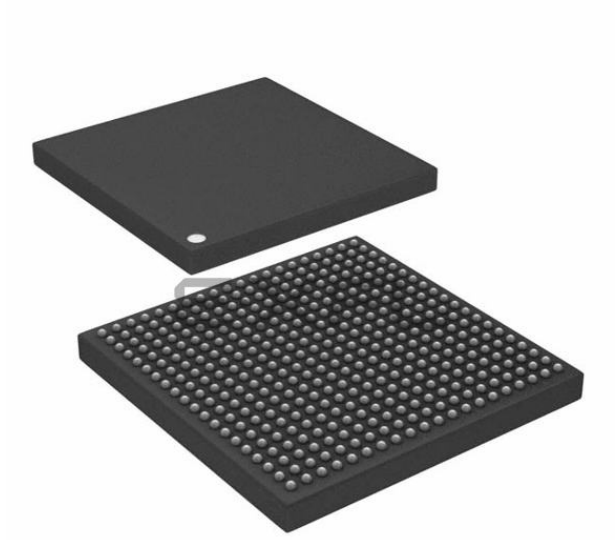

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, EBI/EMI, SD/SDIO, SPI, SPORT, TWI, UART/USART, USB OTG
Clock Rate	533MHz
Non-Volatile Memory	External
On-Chip RAM	260kB
Voltage - I/O	3.30V
Voltage - Core	1.19V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf549wbbcz504

- SIC interrupt mask registers (SIC_IMASKx). These registers control the masking and unmasking of each peripheral interrupt event. When a bit is set in a register, that peripheral event is unmasked and is processed by the system when asserted. A cleared bit in the register masks the peripheral event, preventing the processor from servicing the event.
- SIC interrupt status registers (SIC_ISRx). As multiple peripherals can be mapped to a single event, these registers allow the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt, and a cleared bit indicates the peripheral is not asserting the event.
- SIC interrupt wakeup enable registers (SIC_IWRx). By enabling the corresponding bit in this register, a peripheral can be configured to wake up the processor, should the core be idled or in Sleep mode when the event is generated. (For more information, see Dynamic Power Management on Page 15.)

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected. (Detection requires two core clock cycles.) The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC recognizes and queues the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

DMA CONTROLLERS

ADSP-BF54x Blackfin processors have multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the ADSP-BF54x processors' internal memories and any of the DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including DDR and asynchronous memory controllers.

While the USB controller and MXVR have their own dedicated DMA controllers, the other on-chip peripherals are managed by two centralized DMA controllers, called DMAC1 (32-bit) and DMAC0 (16-bit). Both operate in the SCLK domain. Each DMA controller manages 12 independent peripheral DMA channels, as well as two independent memory DMA streams. The DMAC1 controller masters high-bandwidth peripherals over a dedicated 32-bit DMA access bus (DAB32). Similarly, the DMAC0 controller masters most serial interfaces over the 16-bit DAB16 bus. Individual DMA channels have fixed access priority on the DAB buses. DMA priority of peripherals is managed by a flexible peripheral-to-DMA channel assignment scheme.

All four DMA controllers use the same 32-bit DCB bus to exchange data with L1 memory. This includes L1 ROM, but excludes scratchpad memory. Fine granulation of L1 memory and special DMA buffers minimize potential memory conflicts when the L1 memory is accessed simultaneously by the core. Similarly, there are dedicated DMA buses between the external bus interface unit (EBIU) and the three DMA controllers (DMAC1, DMAC0, and USB) that arbitrate DMA accesses to external memories and the boot ROM.

The ADSP-BF54x Blackfin processors' DMA controllers support both 1-dimensional (1D) and 2-dimensional (2D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the ADSP-BF54x Blackfin processors' DMA controllers include:

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1D or 2D DMA using a linked list of descriptors
- 2D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, the DMAC1 and DMAC0 controllers each feature two memory DMA channel pairs for transfers between the various memories of the ADSP-BF54x Blackfin processors. This enables transfers of blocks of data between any of the memories—including external DDR, ROM, SRAM, and flash memory—with minimal processor intervention. Like peripheral DMAs, memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

The memory DMA channels of the DMAC1 controller (MDMA2 and MDMA3) can be controlled optionally by the external DMA request input pins. When used in conjunction with the External Bus Interface Unit (EBIU), this handshaked memory DMA (HMDMA) scheme can be used to efficiently exchange data with block-buffered or FIFO-style devices connected externally. Users can select whether the DMA request pins control the source or the destination side of the memory DMA. It allows control of the number of data transfers for memory DMA. The number of transfers per edge is programmable. This feature can be programmed to allow memory DMA to have an increased priority on the external bus relative to the core.

includes support for five to eight data bits, one or two stop bits, and none, even, or odd parity. Each UART port supports two modes of operation:

- PIO (programmed I/O). The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access). The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. Each UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates. Flexible interrupt timing options are available on the transmit side.

Each UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{SCLK}/1,048,576) to (f_{SCLK}) bits per second.
- Supporting data formats from seven to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

The UART port's clock rate is calculated as

$$UART\ Clock\ Rate = \frac{f_{SCLK}}{16^{(1-EDBO)} \times UART\_Divisor}$$

Where the 16-bit UART divisor comes from the UARTx_DLH register (most significant 8 bits) and UARTx_DLL register (least significant eight bits), and the EDBO is a bit in the UARTx_GCTL register.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

UART1 and UART3 feature a pair of $\overline{\text{UARTxRTS}}$ (request to send) and $\overline{\text{UARTxCTS}}$ (clear to send) signals for hardware flow purposes. The transmitter hardware is automatically prevented from sending further data when the $\overline{\text{UARTxCTS}}$ input is de-asserted. The receiver can automatically de-assert its $\overline{\text{UARTxRTS}}$ output when the enhanced receive FIFO exceeds a certain high-water level. The capabilities of the UARTs are further extended with support for the Infrared Data Association (IrDA®) Serial Infrared Physical Layer Link Specification (SIR) protocol.

CONTROLLER AREA NETWORK (CAN)

The ADSP-BF54x Blackfin processors offer up to two CAN controllers that are communication controllers that implement the controller area network (CAN) 2.0B (active) protocol. This protocol is an asynchronous communications protocol used in both industrial and automotive control systems. The CAN protocol is well suited for control applications due to its capability to communicate reliably over a network since the protocol incorporates CRC checking, message error tracking, and fault node confinement.

The ADSP-BF54x Blackfin processors' CAN controllers offer the following features:

- 32 mailboxes (8 receive only, 8 transmit only, 16 configurable for receive or transmit).
- Dedicated acceptance masks for each mailbox.
- Additional data filtering on first two bytes.
- Support for both the standard (11-bit) and extended (29-bit) identifier (ID) message formats.
- Support for remote frames.
- Active or passive network support.
- CAN wakeup from hibernation mode (lowest static power consumption mode).
- Interrupts, including: TX complete, RX complete, error and global.

The electrical characteristics of each network connection are very demanding, so the CAN interface is typically divided into two parts: a controller and a transceiver. This allows a single controller to support different drivers and CAN networks. The ADSP-BF54x Blackfin processors' CAN module represents only the controller part of the interface. The controller interface supports connection to 3.3 V high speed, fault-tolerant, single-wire transceivers.

An additional crystal is not required to supply the CAN clock, as the CAN clock is derived from the processor system clock (SCLK) through a programmable divider.

TWI CONTROLLER INTERFACE

The ADSP-BF54x Blackfin processors include up to two 2-wire interface (TWI) modules for providing a simple exchange method of control data between multiple devices. The modules are compatible with the widely used I^2C bus standard. The TWI modules offer the capabilities of simultaneous master and slave operation and support for both 7-bit addressing and multimedia data arbitration. Each TWI interface uses two pins for transferring clock (SCLx) and data (SDAx), and supports the protocol at speeds up to 400K bits/sec. The TWI interface pins are compatible with 5 V logic levels.

Additionally, the ADSP-BF54x Blackfin processors' TWI modules are fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

PORTS

Because of their rich set of peripherals, the ADSP-BF54x Blackfin processors group the many peripheral signals to ten ports—referred to as Port A to Port J. Most ports contain 16 pins, though some have fewer. Many of the associated pins are shared by multiple signals. The ports function as multiplexer controls. Every port has its own set of memory-mapped registers to control port muxing and GPIO functionality.

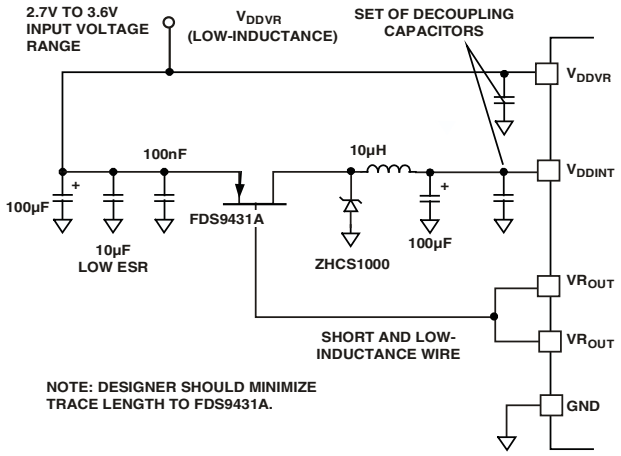


Figure 6. Voltage Regulator Circuit

CLOCK SIGNALS

The ADSP-BF54x Blackfin processors can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the ADSP-BF54x Blackfin processors include an on-chip oscillator circuit, an external crystal may be used. For fundamental frequency operation, use the circuit shown in Figure 7. A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Typically, further parallel resistors are not recommended. The two capacitors and the series resistor shown in Figure 7 fine-tune phase and amplitude of the sine frequency. The 1MOhm pull-up resistor on the XTAL pin guarantees that the clock circuit is properly held inactive when the processor is in the hibernate state.

The capacitor and resistor values shown in Figure 7 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. System designs should verify the customized values based on careful investigations on multiple devices over temperature range.

A third-overtone crystal can be used at frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit as shown in Figure 7. A design procedure for third-overtone operation is discussed in detail in an Application Note, *Using Third Overtone Crystals (EE-168)*.

The Blackfin core runs at a different clock rate than the on-chip peripherals. As shown in Figure 8 on Page 17, the core clock (CCLK) and system peripheral clock (SCLK) are derived from

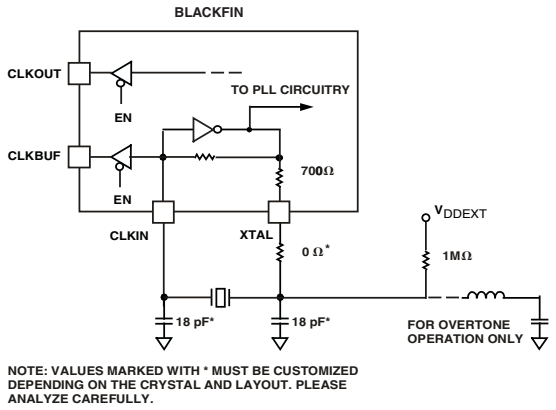
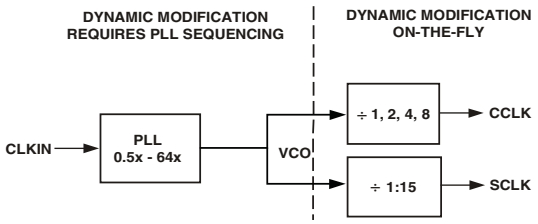


Figure 7. External Crystal Connections

the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a programmable 0.5× to 64× multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 8×, but it can be modified by a software instruction sequence. This sequence is managed by the bfrom_SysControl() function in the on-chip ROM.

On-the-fly CCLK and SCLK frequency changes can be applied by using the bfrom_SysControl() function in the on-chip ROM. Whereas the maximum allowed CCLK and SCLK rates depend on the applied voltages V_{DDINT} and V_{DDEXT}, the VCO is always permitted to run up to the frequency specified by the part's speed grade.

The CLKOUT pin reflects the SCLK frequency to the off-chip world. It functions as a reference for many timing specifications. While inactive by default, it can be enabled using the EBIU_AMGCTL register.



Note: For CCLK and SCLK specifications, see Table 15.

Figure 8. Frequency Modification Methods

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 6 illustrates typical system clock ratios. The default ratio is 4.

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
Port I: GPIO/*AMC*			
PI0/*A10*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI1/*A11*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI2/*A12*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI3/*A13*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI4/*A14*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI5/*A15*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI6/*A16*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI7/*A17*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI8/*A18*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI9/*A19*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI10/*A20*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI11/*A21*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI12/*A22*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI13/*A23*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI14/*A24*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI15/*A25/NR_CLK*[6]	I/O	GPIO/*Address Bus for Async Access/ NOR clock*	A
Port J: GPIO/*AMC/ATAPI*			
PJ0/*ARDY*/$\overline{WAIT}$	I/O	GPIO/ *Async Ready/NOR Wait*	A
PJ1/$\overline{ND\_CE}$[7]	I/O	GPIO/*NAND Chip Enable*	A
PJ2/$\overline{ND\_RB}$	I/O	GPIO/*NAND Ready Busy*	A
PJ3/$\overline{ATAPI\_DIOR}$	I/O	GPIO/*ATAPI Read*	A
PJ4/$\overline{ATAPI\_DIOW}$	I/O	GPIO/*ATAPI Write*	A
PJ5/$\overline{ATAPI\_CS0}$	I/O	GPIO/*ATAPI Chip Select/Command Block*	A
PJ6/$\overline{ATAPI\_CS1}$	I/O	GPIO/*ATAPI Chip Select*	A
PJ7/$\overline{ATAPI\_DMACK}$	I/O	GPIO/*ATAPI DMA Acknowledge*	A
PJ8/$\overline{ATAPI\_DMARQ}$	I/O	GPIO/*ATAPI DMA Request*	A
PJ9/*ATAPI_INTRQ*	I/O	GPIO/*Interrupt Request from the Device*	A
PJ10/$\overline{ATAPI\_IORDY}$	I/O	GPIO/*ATAPI Ready Handshake*	A
PJ11/$\overline{BR}$[8]	I/O	GPIO/*Bus Request*	A
PJ12/$\overline{BG}$[6]	I/O	GPIO/*Bus Grant*	A
PJ13/$\overline{BGH}$[6]	I/O	GPIO/*Bus Grant Hang*	A

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
DDR Memory Interface			
DA0–12	O	DDR Address Bus	D
DBA0–1	O	DDR Bank Active Strobe	D
DQ0–15	I/O	DDR Data Bus	D
DQS0–1	I/O	DDR Data Strobe	D
DQM0–1	O	DDR Data Mask for Reads and Writes	D
DCLK0–1	O	DDR Output Clock	D
$\overline{\text{DCLK0–1}}$	O	DDR Complementary Output Clock	D
$\overline{\text{DCS0–1}}$	O	DDR Chip Selects	D
DCLKE[9]	O	DDR Clock Enable (Requires a pull-down if hibernate with DDR self-refresh is used.)	D
$\overline{\text{DRAS}}$	O	DDR Row Address Strobe	D
$\overline{\text{DCAS}}$	O	DDR Column Address Strobe	D
$\overline{\text{DWE}}$	O	DDR Write Enable	D
DDR_VREF	I	DDR Voltage Reference	
DDR_VSSR	I	DDR Voltage Reference Shield (Must be connected to GND.)	
Asynchronous Memory Interface			
A1-3	O	Address Bus for Async and ATAPI Addresses	A
D0-15/ND_D0-15/ATAPI_D0-15	I/O	Data Bus for Async, NAND and ATAPI Accesses	A
$\overline{\text{AMS0–3}}$	O	Bank Selects (Pull high with a resistor when used as chip select. Require pull-ups if hibernate is used.)	A
$\overline{\text{ABE0}}$ / *ND_CLE*	O	Byte Enables: Data Masks for Asynchronous Access / *NAND Command Latch Enable*	A
$\overline{\text{ABE1}}$ / *ND_ALE*	O	Byte Enables: Data Masks for Asynchronous Access / *NAND Address Latch Enable*	A
$\overline{\text{AOE}}$ / *NR_ADV*	O	Output Enable / *NOR Address Data Valid*	A
$\overline{\text{ARE}}$	O	Read Enable / *NOR Output Enable*	A
$\overline{\text{AWE}}$	O	Write Enable	A
ATAPI Controller Pins			
$\overline{\text{ATAPI\_PDIAG}}$	I	Determines if an 80-pin cable is connected to the host. (Pull high or low when unused.)	
High Speed USB OTG Pins			
USB_DP	I/O	USB D+ Pin (Pull low when unused.)	
USB_DM	I/O	USB D– Pin (Pull low when unused.)	
USB_XI	C	Clock XTAL Input (Pull high or low when unused.)	
USB_XO	C	Clock XTAL Output (Leave unconnected when unused.)	
USB_ID[10]	I	USB OTG ID Pin (Pull high when unused.)	

[10]Parameter value applies to USB_DP, USB_DM, and USB_VBUS pins. See Absolute Maximum Ratings on Page 40.
[11]Parameter value applies to all input and bidirectional pins, except PB1-0, PE15-14, PG15–11, and PH7-6.
[12]Parameter value applies to pins PG15–11 and PH7-6.
[13]Parameter value applies to pins PB1-0 and PE15-14. Consult the I^2C specification version 2.1 for the proper resistor value and other open drain pin electrical parameters.
[14]T_J must be in the range: 0°C < T_J < 55°C during OTP memory programming operations.

Table 12 and Table 15 describe the voltage/frequency requirements for the ADSP-BF54x Blackfin processors' clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock. Table 14 describes the phase-locked loop operating conditions.

Table 12. Core Clock (CCLK) Requirements—533 MHz and 600 MHz Speed Grade[1]

Parameter		Min V_{DDINT}	Internal Regulator Setting[2]	Max CCLK Frequency	Unit
f_{CCLK}	Core Clock Frequency	1.30 V	N/A[2]	600	MHz
		1.188 V	1.25 V	533	MHz
		1.14 V	1.20 V	500	MHz
		1.045 V	1.10 V	444	MHz
		0.95 V	1.00 V	400	MHz
		0.90 V	0.95 V	333	MHz

[1] See the Ordering Guide on Page 101.
[2] Use of an internal voltage regulator is not supported on automotive grade and 600 MHz speed grade models. Internal regulator setting should be used as recommended nominal V_{DDINT} for external regulator.

Table 13. Core Clock (CCLK) Requirements—400 MHz Speed Grade[1]

Parameter		Min V_{DDINT}	Internal Regulator Setting[2]	Max CCLK Frequency	Unit
f_{CCLK}	Core Clock Frequency	1.14 V	1.20 V	400	MHz
		1.045 V	1.10 V	364	MHz
		0.95 V	1.00 V	333	MHz
		0.90 V	0.95 V	300	MHz

[1] See Ordering Guide on Page 101.
[2] Use of an internal voltage regulator is not supported on automotive grade models. Internal regulator setting should be used as recommended nominal V_{DDINT} for external regulator.

Table 14. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	50	Maximum f_{CCLK}	MHz

Table 15. System Clock Requirements

Parameter	Condition	DDR SDRAM Models Max	Mobile DDR SDRAM Models Min	Mobile DDR SDRAM Models Max	Unit
f_{SCLK}	$V_{DDINT} \geq 1.14$ V[1], Non-extended temperature grades	133[2]	120[3]	133[2]	MHz
f_{SCLK}	$V_{DDINT} < 1.14$ V[1], Non-extended temperature grades	100	N/A[4]	N/A[4]	MHz
f_{SCLK}	$V_{DDINT} \geq 1.0$ V[1], Extended temperature grade	100	N/A	N/A	MHz

[1] f_{SCLK} must be less than or equal to f_{CCLK}.
[2] Rounded number. Actual test specification is SCLK period of 7.5 ns. See Table 25 on Page 43.
[3] Rounded number. Actual test specification is SCLK period of 8.33 ns.
[4] V_{DDINT} must be greater than or equal to 1.14 V for mobile DDR SDRAM models. See Operating Conditions on Page 34.

Parameter		Test Conditions	Nonautomotive 400 MHz[1] Min	Typ	Max	All Other Devices[2] Min	Typ	Max	Unit
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.10 V, f_{CCLK} = 300 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00		145			178		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.20 V, f_{CCLK} = 400 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00		199			239		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.25 V, f_{CCLK} = 533 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00					301		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.35 V, f_{CCLK} = 600 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00					360		mA
$I_{DDHIBERNATE}$[13, 14]	Hibernate State Current	V_{DDEXT} = V_{DDVR} = V_{DDUSB} = 3.30 V, V_{DDDDR} = 2.5 V, T_J = 25°C, CLKIN= 0 MHz with voltage regulator off (V_{DDINT} = 0 V)		60			60		µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J = 25°C		20			20		µA
$I_{DDUSB-FS}$	V_{DDUSB} Current in Full/Low Speed Mode	V_{DDUSB} = 3.3 V, T_J = 25°C, Full Speed USB Transmit		9			9		mA
$I_{DDUSB-HS}$	V_{DDUSB} Current in High Speed Mode	V_{DDUSB} = 3.3 V, T_J = 25°C, High Speed USB Transmit		25			25		mA
$I_{DDDEEPSLEEP}$[13, 15]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz			Table 16			Table 17	mA
$I_{DDSLEEP}$[13, 15]	V_{DDINIT} Current in Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} > 0 MHz			$I_{DDDEEPSLEEP}$ + (0.77 × V_{DDINT} × f_{SCLK})[16]			$I_{DDDEEPSLEEP}$ + (0.77 × V_{DDINT} × f_{SCLK})[16]	mA[16]
I_{DDINT}[15, 17]	V_{DDINT} Current	f_{CCLK} > 0 MHz, f_{SCLK} > 0 MHz			$I_{DDSLEEP}$ + (Table 19 × ASF)			$I_{DDSLEEP}$ + (Table 19 × ASF)	mA

[1] Applies to all nonautomotive 400 MHz speed grade models and all extended temperature grade models. See Ordering Guide.
[2] Applies to all 533 MHz and 600 MHz speed grade models and automotive 400 MHz speed grade models. See Ordering Guide.
[3] Applies to output and bidirectional pins, except USB_VBUS and the pins listed in table note 4.
[4] Applies to pins DA0–12, DBA0–1, DQ0–15, DQS0–1, DQM0–1, DCLK1–2, $\overline{\text{DCLK1–2}}$, $\overline{\text{DCS0–1}}$, DCLKE, $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, and $\overline{\text{DWE}}$.
[5] Applies to all input pins except JTAG inputs.
[6] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{\text{TRST}}$).
[7] Applies to DDR_VREF pin.
[8] Absolute value.
[9] For DDR pins (DQ0-15, DQS0-1), test conditions are V_{DDDDR} = Maximum, V_{IN} = V_{DDDDR} Maximum.
[10] Applies to three-statable pins.
[11] For DDR pins (DQ0-15, DQS0-1), test conditions are V_{DDDDR} = Maximum, V_{IN} = 0 V.
[12] Guaranteed, but not tested.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 9 and Table 23 provides information related to specific product features. For a complete listing of product offerings, see the Ordering Guide on Page 101.

Figure 9. Product Information on Package

Table 23. Package Information

Brand Key	Description
BF54x	x = 2, 4, 7, 8 or 9
(M)	Mobile DDR Indicator (Optional)
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part (Optional)
cc	See Ordering Guide
vvvvvv.x-q	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

TIMING SPECIFICATIONS

Timing specifications are detailed in this section.

Clock and Reset Timing

Table 24 and Figure 10 describe Clock Input and Reset Timing.
Table 25 and Figure 11 describe Clock Out Timing.

Table 24. Clock Input and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN Period[1, 2, 3, 4]	20.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse[2]	8.0		ns
t_{CKINH}	CLKIN High Pulse[2]	8.0		ns
$t_{BUFDLAY}$	CLKIN to CLKBUF Delay		10	ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulsewidth Low[5]	11 t_{CKIN}		ns
t_{RHWFT}	RESET High to First HWAIT/HWAITA Transition (Boot Host Wait Mode)[6, 7, 8, 9]	6100 t_{CKIN} + 7900 t_{SCLK}		ns
	RESET High to First HWAIT/HWAITA Transition (Reset Output Mode)[7, 10, 11]	6100 t_{CKIN}	7000 t_{CKIN}	ns

[1] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 15 and Table 12 on Page 35.
[2] Applies to PLL bypass mode and PLL non-bypass mode.
[3] CLKIN frequency and duty cycle must not change on the fly.
[4] If the DF bit in the PLL_CTL register is set, then the maximum t_{CKIN} period is 50 ns.
[5] Applies after power-up sequence is complete. See Table 26 and Figure 12 for more information about power-up reset timing.
[6] Maximum value not specified due to variation resulting from boot mode selection and OTP memory programming.
[7] Values specified assume no invalidation preboot settings in OTP page PBS00L. Invalidating a PBS set will increase the value by 1875 t_{CKIN} (typically).
[8] Applies only to boot modes BMODE=1, 2, 4, 6, 7, 10, 11, 14, 15.
[9] Use default t_{SCLK} value unless PLL is reprogrammed during preboot. In case of PLL reprogramming use the new t_{SCLK} value and add PLL_LOCKCNT settle time.
[10] When enabled by OTP_RESETOUT_HWAIT bit. If regular HWAIT is not required in an application, the OTP_RESETOUT_HWAIT bit in the same page instructs the HWAIT or HWAITA to simulate reset output functionality. Then an external resistor is expected to pull the signal to the reset level, as the pin itself is in high performance mode during reset.
[11] Variances are mainly dominated by PLL programming instructions in PBS00L page and boot code differences between silicon revisions. The earlier is bypassed in boot mode BMODE = 0. Maximum value assumes PLL programming instructions do not cause the SCLK frequency to decrease.

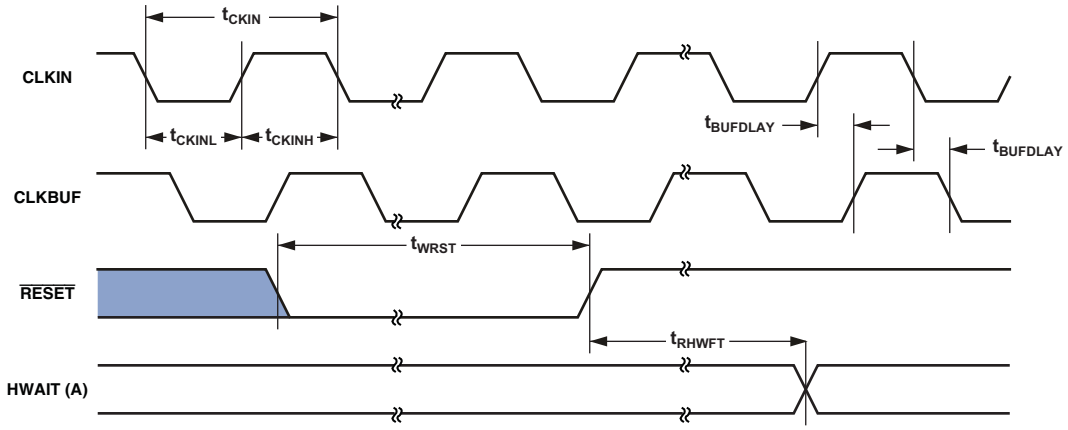


Figure 10. Clock and Reset Timing

Table 28. Asynchronous Memory Read Cycle Timing with Asynchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA15–0 Setup Before CLKOUT	5.0		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
t_{DANR}	ARDY Negated Delay from $\overline{AMSx}$ Asserted[1]		$(S + RA - 2) \times t_{SCLK}$	ns
t_{HAA}	ARDY Asserted Hold After $\overline{ARE}$ Negated	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[2]		6.0	ns
t_{HO}	Output Hold After CLKOUT[2]	0.3		ns

[1] S = number of programmed setup cycles, RA = number of programmed read access cycles.
[2] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, $\overline{AOE}$, and $\overline{ARE}$.

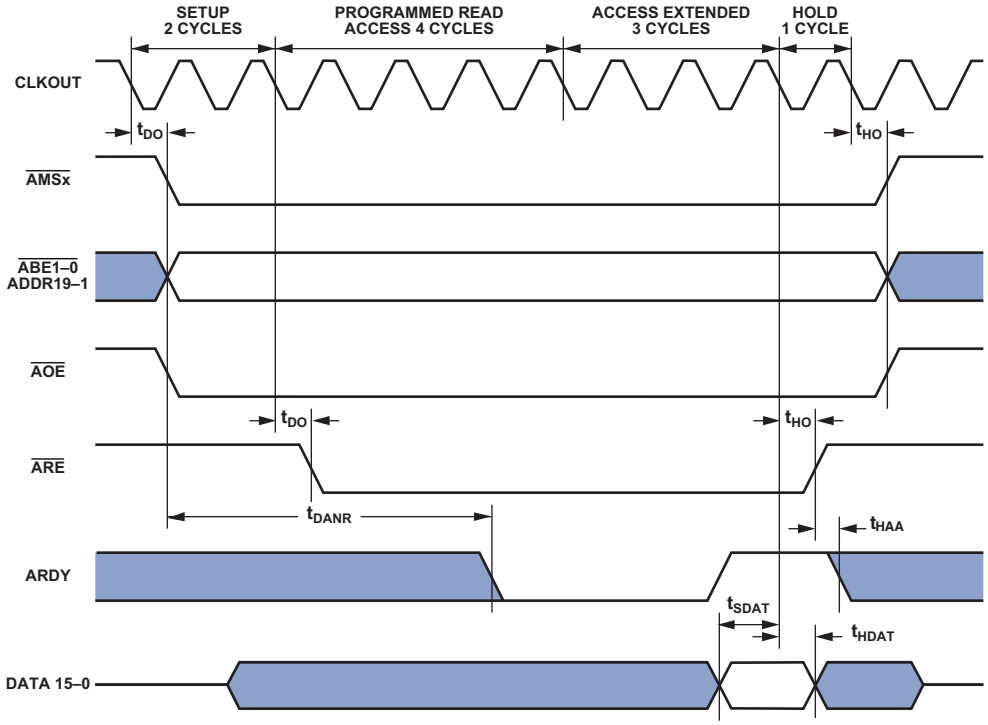


Figure 14. Asynchronous Memory Read Cycle Timing with Asynchronous ARDY

DDR SDRAM/Mobile DDR SDRAM Write Cycle Timing

Table 33 and Figure 20 describe DDR SDRAM/mobile DDR SDRAM write cycle timing.

Table 33. DDR SDRAM/Mobile DDR SDRAM Write Cycle Timing

Parameter		DDR SDRAM Min	DDR SDRAM Max	Mobile DDR SDRAM Min	Mobile DDR SDRAM Max	Unit
Switching Characteristics						
t_{DQSS}	Write CMD to First DQS0-1	0.75	1.25	0.75	1.25	t_{CK}
t_{DS}	DQ0-15/DQM0-1 Setup to DQS0-1	0.90		0.90		ns
t_{DH}	DQ0-15/DQM0-1 Hold to DQS0-1	0.90		0.90		ns
t_{DSS}	DQS0-1 Falling to DCK0-1 Rising (DQS0-1 Setup)	0.20		0.20		t_{CK}
t_{DSH}	DQS0-1 Falling from DCK0-1 Rising (DQS0-1 Hold)	0.20		0.20		t_{CK}
t_{DQSH}	DQS0-1 High Pulse Width	0.35		0.40	0.60	t_{CK}
t_{DQSL}	DQS0-1 Low Pulse Width	0.35		0.40	0.60	t_{CK}
t_{WPRE}	DQS0-1 Write Preamble	0.25		0.25		t_{CK}
t_{WPST}	DQS0-1 Write Postamble	0.40	0.60	0.40	0.60	t_{CK}
t_{DOPW}	DQ0-15 and DQM0-1 Output Pulse Width (for Each)	1.75		1.75		ns

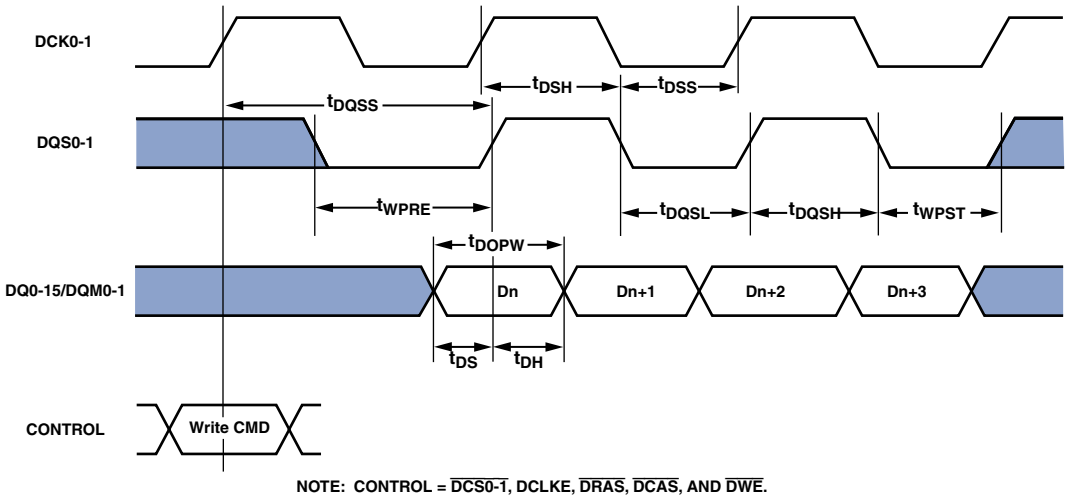


Figure 20. DDR SDRAM /Mobile DDR SDRAM Controller Write Cycle Timing

External Port Bus Request and Grant Cycle Timing

Table 34 and Table 35 on Page 52 and Figure 21 and Figure 22 on Page 52 describe external port bus request and grant cycle operations for synchronous and for asynchronous $\overline{BR}$.

Table 34. External Port Bus Request and Grant Cycle Timing with Synchronous $\overline{BR}$

Parameter		Min	Max	Unit
Timing Requirements				
t_{BS}	$\overline{BR}$ Asserted to CLKOUT Low Setup	5.0		ns
t_{BH}	CLKOUT Low to $\overline{BR}$ Deasserted Hold Time	0.0		ns
Switching Characteristics				
t_{SD}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Disable		5.0	ns
t_{SE}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Enable		5.0	ns
t_{DBG}	CLKOUT Low to $\overline{BG}$ Asserted Output Delay		4.0	ns
t_{EBG}	CLKOUT Low to $\overline{BG}$ Deasserted Output Hold		4.0	ns
t_{DBH}	CLKOUT Low to $\overline{BGH}$ Asserted Output Delay		3.6	ns
t_{EBH}	CLKOUT Low to $\overline{BGH}$ Deasserted Output Hold		3.6	ns

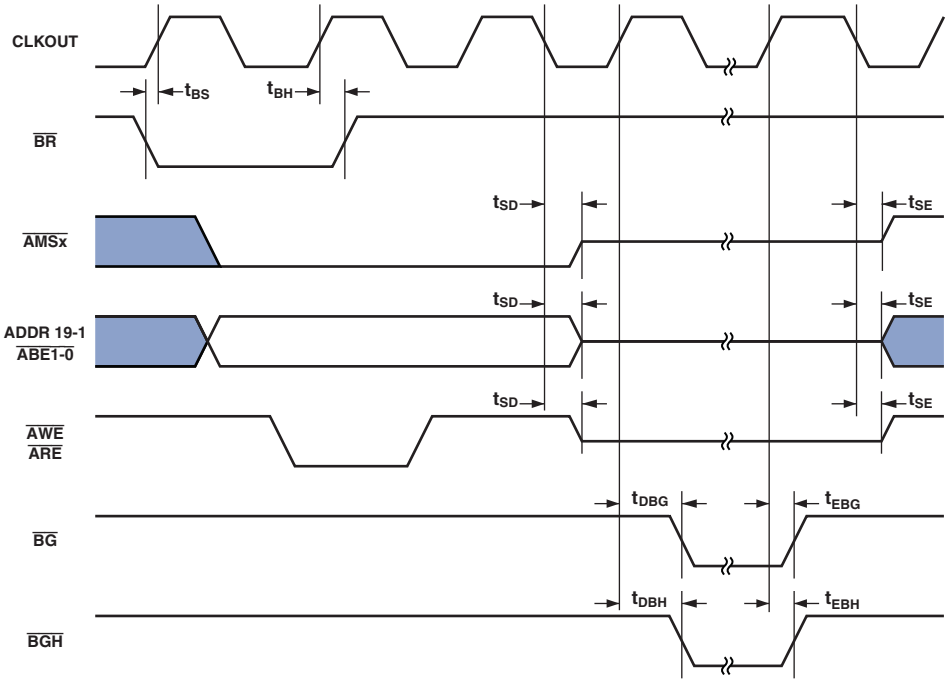


Figure 21. External Port Bus Request and Grant Cycle Timing with Synchronous $\overline{BR}$

Table 35. External Port Bus Request and Grant Cycle Timing with Asynchronous $\overline{BR}$

Parameter		Min	Max	Unit
Timing Requirement				
t_{WBR}	$\overline{BR}$ Pulsewidth	$2 \times t_{SCLK}$		ns
Switching Characteristics				
t_{SD}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}/\overline{AWE}$ Disable		5.0	ns
t_{SE}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}/\overline{AWE}$ Enable		5.0	ns
t_{DBG}	CLKOUT Low to $\overline{BG}$ Asserted Output Delay		4.0	ns
t_{EBG}	CLKOUT Low to $\overline{BG}$ Deasserted Output Hold		4.0	ns
t_{DBH}	CLKOUT Low to $\overline{BGH}$ Asserted Output Delay		3.6	ns
t_{EBH}	CLKOUT Low to $\overline{BGH}$ Deasserted Output Hold		3.6	ns

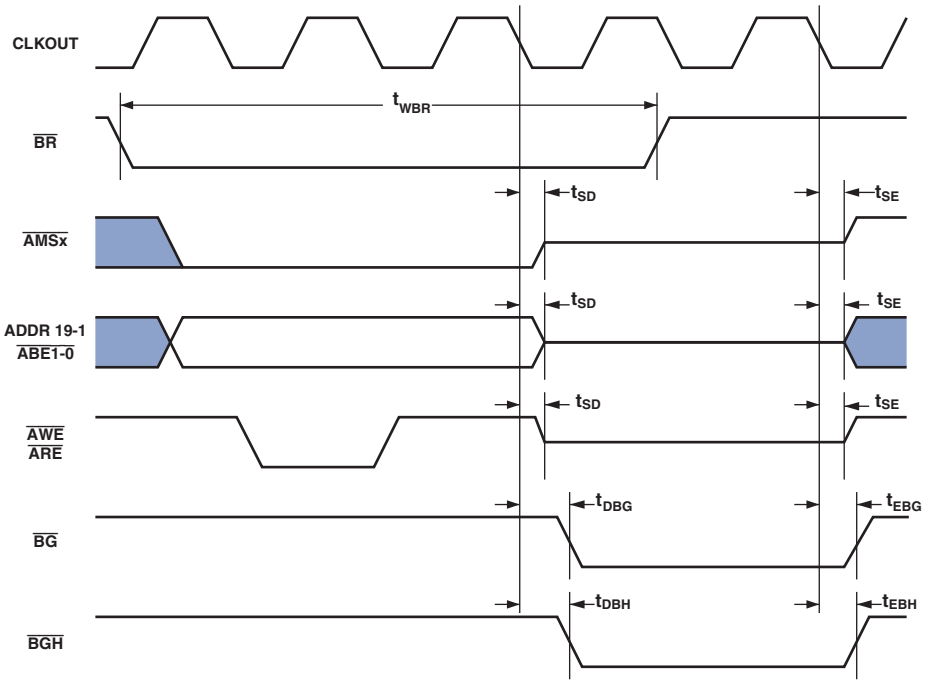


Figure 22. External Port Bus Request and Grant Cycle Timing with Asynchronous $\overline{BR}$

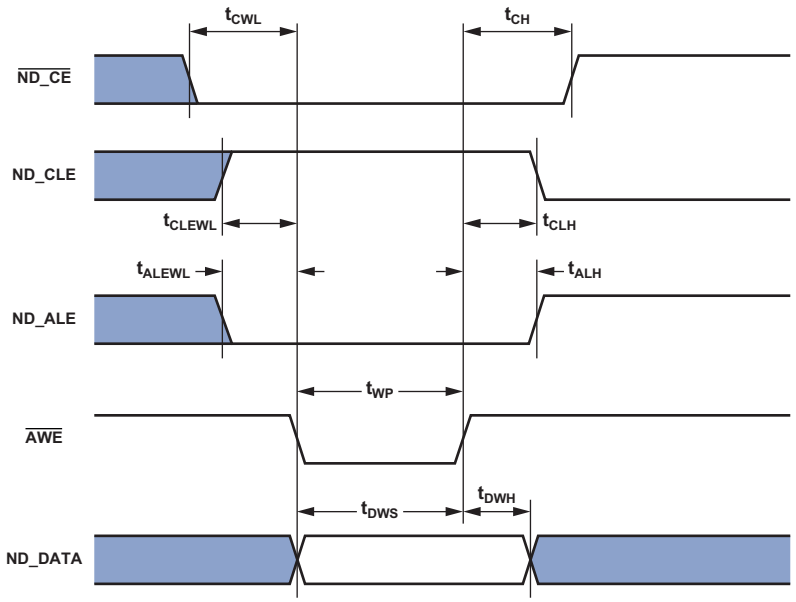


Figure 23. NAND Flash Controller Interface Timing—Command Write Cycle

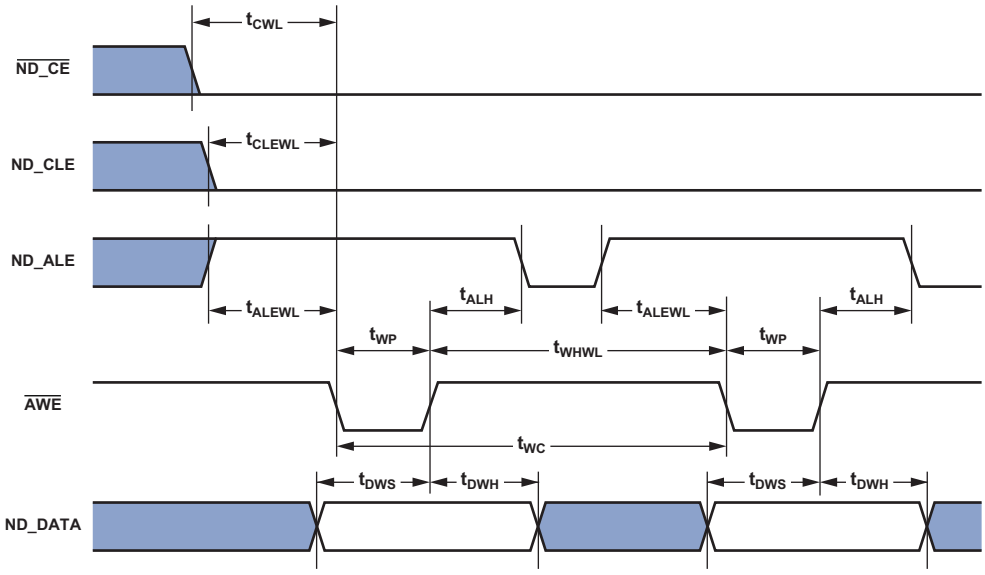


Figure 24. NAND Flash Controller Interface Timing—Address Write Cycle

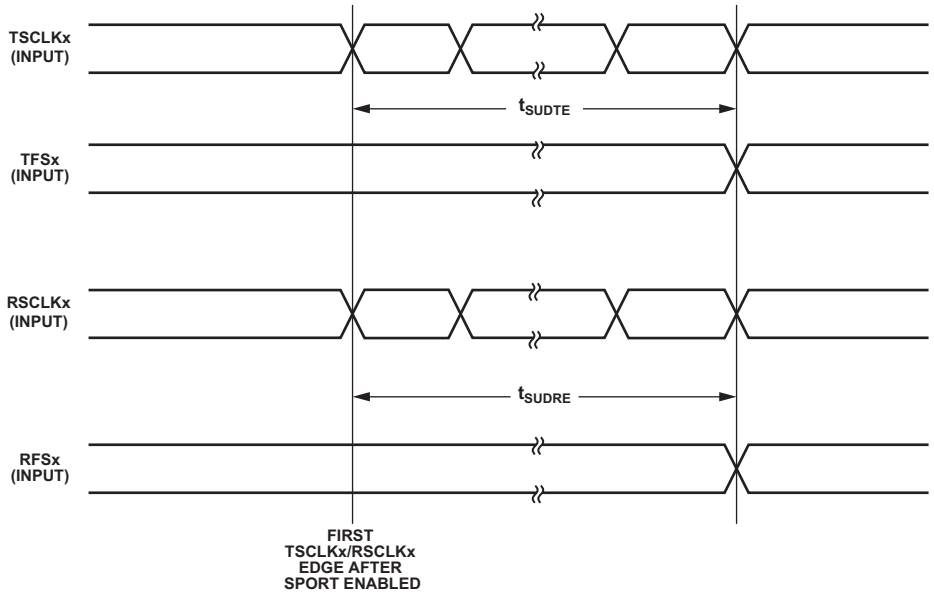


Figure 34. Serial Port Start-Up with External Clock and Frame Sync

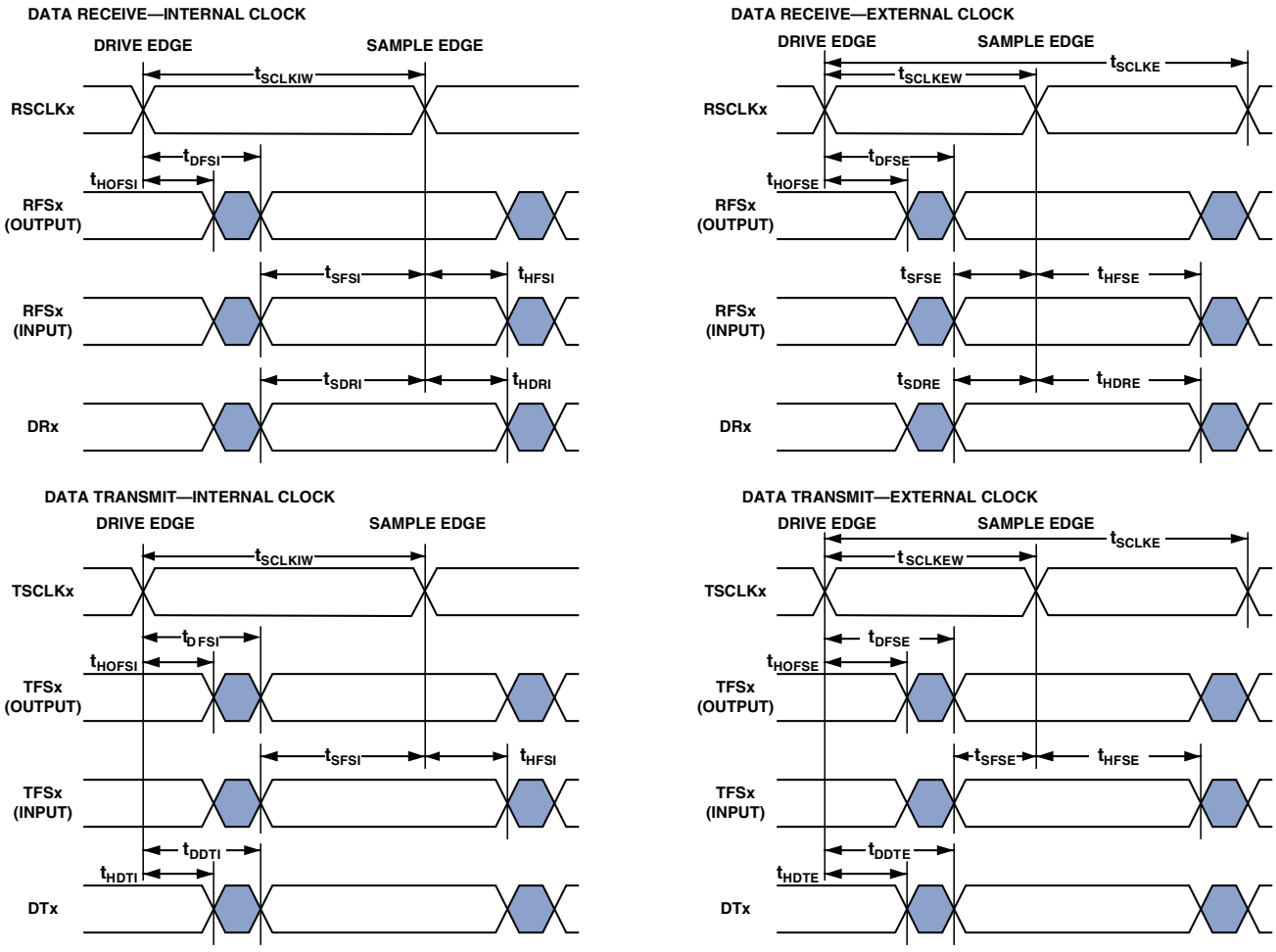


Figure 35. Serial Ports

Timer Cycle Timing

Table 48 and Figure 42 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of (f_{SCLK}/2) MHz.

Table 48. Timer Cycle Timing

Parameter		Min	Max	Unit
Timing Characteristics				
t_{WL}	Timer Pulse Width Input Low[1]	1× t_{SCLK}		ns
t_{WH}	Timer Pulse Width Input High[1]	1× t_{SCLK}		ns
t_{TIS}	Timer Input Setup Time Before CLKOUT Low[2]	6.5		ns
t_{TIH}	Timer Input Hold Time After CLKOUT Low[2]	–1		ns
Switching Characteristics				
t_{HTO}	Timer Pulse Width Output	1× t_{SCLK}	(2^{32} – 1) × t_{SCLK}	ns
t_{TOD}	Timer Output Delay After CLKOUT High		6	ns

[1] The minimum pulse widths apply for TMRx signals in width capture and external clock modes.
[2] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize timer flag inputs.

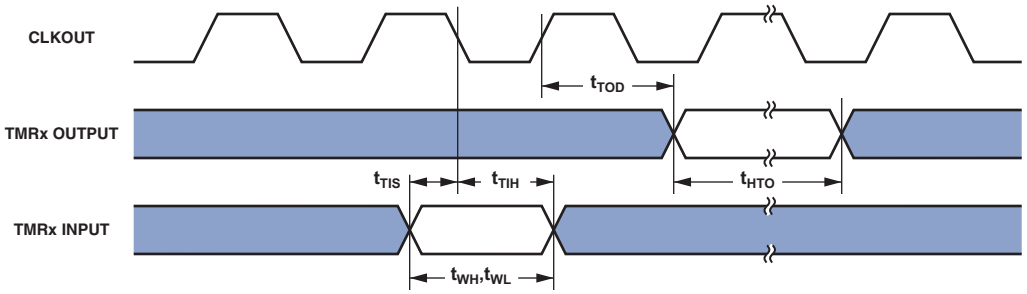


Figure 42. Timer Cycle Timing

MXVR Timing

Table 52 and Table 53 describe the MXVR timing requirements.
Figure 5 illustrates the MOST connection.

Table 52. MXVR Timing—MXI Center Frequency Requirements

Parameter		Fs = 38 kHz	Fs = 44.1 kHz	Fs = 48 kHz	Unit
f_{MXI_256}	MXI Center Frequency (256 Fs)	9.728	11.2896	12.288	MHz
f_{MXI_384}	MXI Center Frequency (384 Fs)	14.592	16.9344	18.432	MHz
f_{MXI_512}	MXI Center Frequency (512 Fs)	19.456	22.5792	24.576	MHz
f_{MXI_1024}	MXI Center Frequency (1024 Fs)	38.912	45.1584	49.152	MHz

Table 53. MXVR Timing— MXI Clock Requirements

Parameter		Min	Max	Unit
Timing Requirements				
FS_{MXI}	MXI Clock Frequency Stability	–50	+50	ppm
FT_{MXI}	MXI Frequency Tolerance Over Temperature	–300	+300	ppm
DC_{MXI}	MXI Clock Duty Cycle	+40	+60	%

ATAPI Ultra DMA Data-In Transfer Timing

Table 60 and Figure 53 through Figure 56 describe the ATAPI ultra DMA data-in data transfer timing. The material in these figures is adapted from ATAPI-6 (INCITS 361-2002[R2007] and is used with permission of the American National Standards Institute (ANSI) on behalf of the Information Technology Industry Council ("ITIC"). Copies of ATAPI-6 (INCITS 361-2002[R2007] can be purchased from ANSI.

Table 60. ATAPI Ultra DMA Data-In Transfer Timing

ATAPI Parameter		ATAPI_ULTRA_TIM_x Timing Register Setting[1]	Timing Equation
t_{DS}	Data setup time at host	N/A	$T_{SK3} + t_{SUDU}$
t_{DH}	Data hold time at host	N/A	$T_{SK3} + t_{HDU}$
t_{CVS}	CRC word valid setup time at host	TDVS	$TDVS \times t_{SCLK} - (t_{SK1} + t_{SK2})$
t_{CVH}	CRC word valid hold time at host	TACK	$TACK \times t_{SCLK} - (t_{SK1} + t_{SK2})$
t_{LI}	Limited interlock time	N/A	$2 \times t_{BD} + 2 \times t_{SCLK} + t_{OD}$
t_{MLI}	Interlock time with minimum	TZAH, TCVS	$(TZAH + TCVS) \times t_{SCLK} - (4 \times t_{BD} + 4 \times t_{SCLK} + 2 \times t_{OD})$
t_{AZ}	Maximum time allowed for output drivers to release	N/A	0
t_{ZAH}	Minimum delay time required for output	TZAH	$2 \times t_{SCLK} + TZAH \times t_{SCLK} + t_{SCLK}$
t_{ENV}[2]	$\overline{ATAPI\_DMACK}$ to $\overline{ATAPI\_DIOR}/\overline{DIOW}$	TENV	$(TENV \times t_{SCLK}) +/- (t_{SK1} + t_{SK2})$
t_{RP}	$\overline{ATAPI\_DMACK}$ to $\overline{ATAPI\_DIOR}/\overline{DIOW}$	TRP	$TRP \times t_{SCLK} - (t_{SK1} + t_{SK2} + t_{SK4})$
t_{ACK}	Setup and hold times for $\overline{ATAPI\_DMACK}$	TACK	$TACK \times t_{SCLK} - (t_{SK1} + t_{SK2})$

[1] ATAPI Timing Register Setting should be programmed with a value that guarantees parameter compliance with the ATA ANSI specification for ATA device mode of operation.
[2] This timing equation can be used to calculate both the minimum and maximum t_{ENV}.

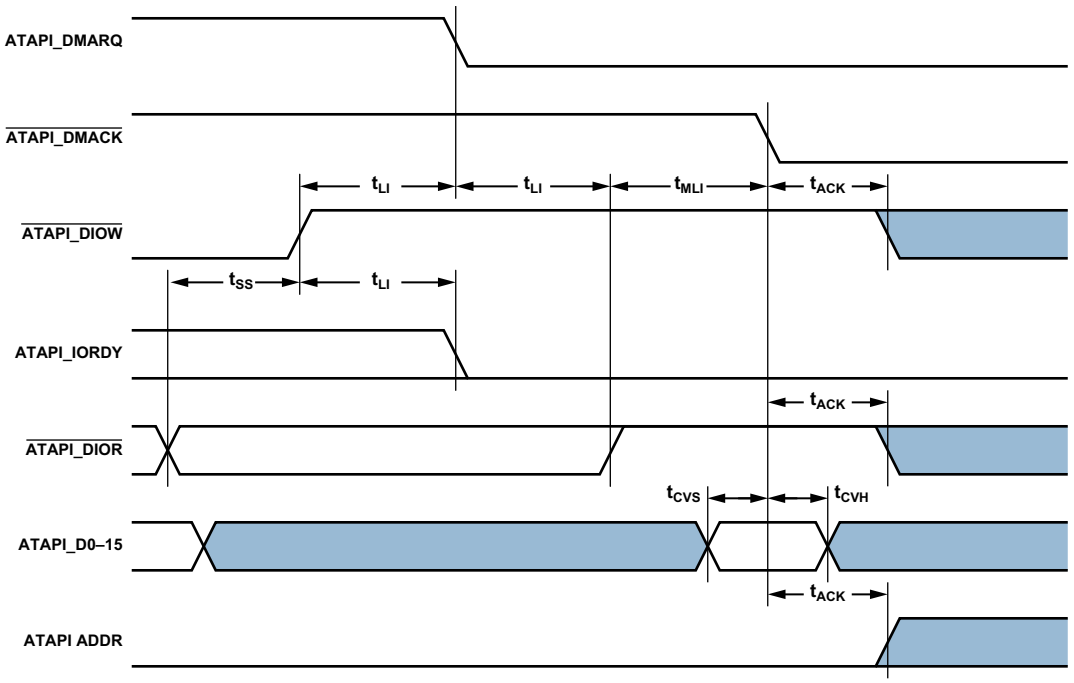


Figure 59. Host terminating an Ultra DMA Data-Out Burst

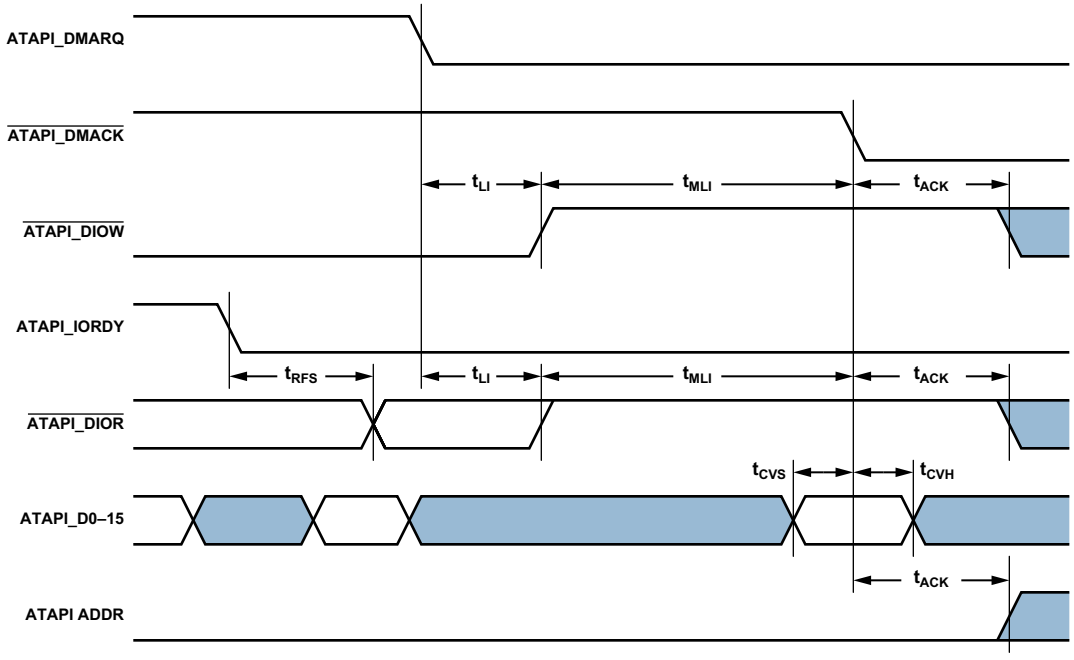


Figure 60. Device Terminating an Ultra DMA Data-Out Burst

Table 66. 400-Ball CSP_BGA Ball Assignment (Numerical by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
U1	PD8	V1	PD11	W1	BMODE0	Y1	GND
U2	PD9	V2	PD13	W2	BMODE1	Y2	PB1
U3	PD15	V3	TCK	W3	BMODE2	Y3	PB5
U4	PD14	V4	TDO	W4	BMODE3	Y4	PB4
U5	TMS	V5	TDI	W5	PB0	Y5	PB14
U6	PB3	V6	GND	W6	PB6	Y6	PB12
U7	PB10	V7	PB7	W7	PB11	Y7	PA14
U8	GND	V8	PB9	W8	PB8	Y8	PA12
U9	V_{DDINT}	V9	PB13	W9	PA15	Y9	PA10
U10	PA8	V10	PA11	W10	PA13	Y10	PA9
U11	PA7	V11	PA5	W11	PA4	Y11	PA6
U12	PA0	V12	PA1	W12	PA2	Y12	PA3
U13	PC10	V13	PC9	W13	PG15	Y13	PG14
U14	PH1	V14	PE3	W14	PC11	Y14	PC8
U15	PG11	V15	PG5	W15	PC13	Y15	PC12
U16	PE14	V16	PG8	W16	PG7	Y16	PE4
U17	PH4	V17	PH2	W17	PE15	Y17	PG6
U18	PE2	V18	PH3	W18	PH0	Y18	PG10
U19	PE9	V19	PE0	W19	PE6	Y19	PG9
U20	PJ5	V20	PE8	W20	PE5	Y20	GND

Figure 87 shows the top view of the BGA ball configuration.

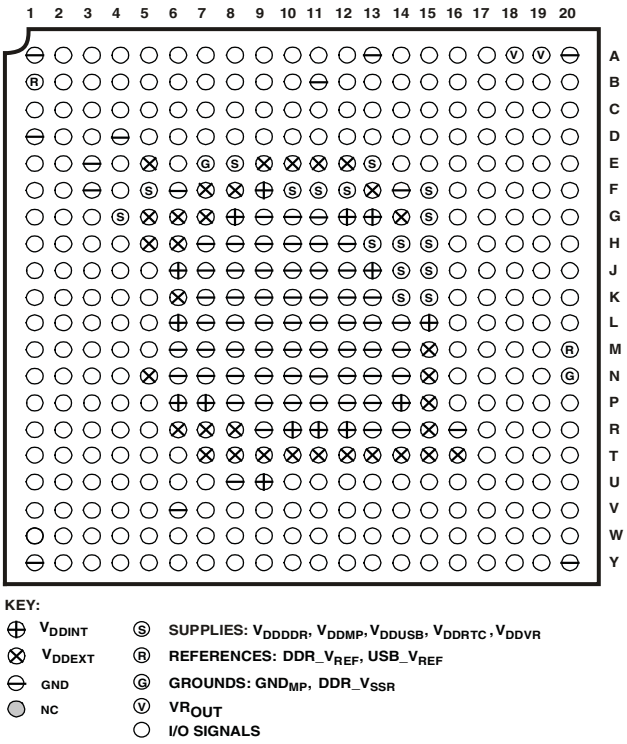


Figure 87. 400-Ball CSP_BGA Configuration (Top View)