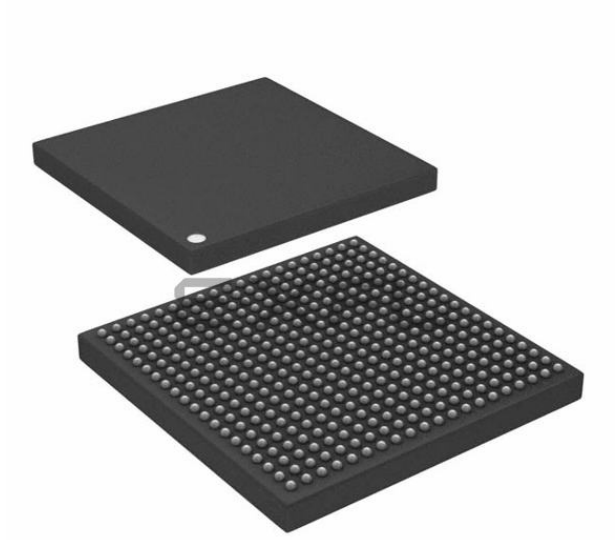

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	CAN, EBI/EMI, SD/SDIO, SPI, SPORT, TWI, UART/USART, USB OTG
Clock Rate	533MHz
Non-Volatile Memory	External
On-Chip RAM	260kB
Voltage - I/O	3.30V
Voltage - Core	1.19V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adbf549wbbcz5m03

The ADSP-BF54x Blackfin processors are completely code- and pin-compatible. They differ only with respect to their performance, on-chip memory, and selection of I/O peripherals. Specific performance, memory, and feature configurations are shown in Table 1.

By integrating a rich set of industry-leading system peripherals and memory, Blackfin processors are the platform of choice for next-generation applications that require RISC-like programmability, multimedia support, and leading-edge signal processing in one integrated package.

LOW POWER ARCHITECTURE

Blackfin processors provide world-class power management and performance. Blackfin processors are designed in a low power and low voltage design methodology and feature on-chip dynamic power management, the ability to vary both the voltage and frequency of operation to significantly lower overall power consumption. Reducing both voltage and frequency can result in a substantial reduction in power consumption as compared to reducing only the frequency of operation. This translates into longer battery life for portable appliances.

SYSTEM INTEGRATION

The ADSP-BF54x Blackfin processors are highly integrated system-on-a-chip solutions for the next generation of embedded network connected applications. By combining industry-standard interfaces with a high performance signal processing core, users can develop cost-effective solutions quickly without the need for costly external components. The system peripherals include a high speed USB OTG (On-the-Go) controller with integrated PHY, CAN 2.0B controllers, TWI controllers, UART ports, SPI ports, serial ports (SPORTs), ATAPI controller, SD/SDIO controller, a real-time clock, a watchdog timer, LCD controller, and multiple enhanced parallel peripheral interfaces.

BLACKFIN PROCESSOR PERIPHERALS

The ADSP-BF54x processors contain a rich set of peripherals connected to the core via several high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see Figure 1 on Page 1). The general-purpose peripherals include functions such as UARTs, SPI, TWI, timers with pulse width modulation (PWM) and pulse measurement capability, general-purpose I/O pins, a real-time clock, and a watchdog timer. This set of functions satisfies a wide variety of typical system support needs and is augmented by the system expansion capabilities of the part. The ADSP-BF54x processors contain dedicated network communication modules and high speed serial and parallel ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

All of the peripherals, except for general-purpose I/O, CAN, TWI, real-time clock, and timers, are supported by a flexible DMA structure. There are also separate memory DMA channels dedicated to data transfers between the processor's various memory spaces, including external DDR (either standard or mobile, depending on the device) and asynchronous memory. Multiple on-chip buses running at up to 133 MHz provide enough bandwidth to keep the processor core running along with activity on all of the on-chip and external peripherals.

The ADSP-BF54x Blackfin processors include an on-chip voltage regulator in support of the dynamic power management capability. The voltage regulator provides a range of core voltage levels when supplied from V_{DDEXT}. The voltage regulator can be bypassed at the user's discretion.

BLACKFIN PROCESSOR CORE

As shown in Figure 2 on Page 5, the Blackfin processor core contains two 16-bit multipliers, two 40-bit accumulators, two 40-bit ALUs, four video ALUs, and a 40-bit shifter. The computation units process 8-, 16-, or 32-bit data from the register file.

The compute register file contains eight 32-bit registers. When performing compute operations on 16-bit operand data, the register file operates as 16 independent 16-bit registers. All operands for compute operations come from the multiported register file and instruction constant fields.

Each MAC can perform a 16-bit by 16-bit multiply in each cycle, accumulating the results into the 40-bit accumulators. Signed and unsigned formats, rounding, and saturation are supported.

The ALUs perform a traditional set of arithmetic and logical operations on 16- or 32-bit data. In addition, many special instructions are included to accelerate various signal processing tasks. These include bit operations such as field extract and population count, modulo 2^{32} multiply, divide primitives, saturation and rounding, and sign/exponent detection. The set of video instructions include byte alignment and packing operations, 16-bit and 8-bit adds with clipping, 8-bit average operations, and 8-bit subtract/absolute value/accumulate (SAA) operations. Also provided are the compare/select and vector search instructions.

For certain instructions, two 16-bit ALU operations can be performed simultaneously on register pairs (a 16-bit high half and 16-bit low half of a compute register). By also using the second ALU, quad 16-bit operations are possible.

The 40-bit shifter can perform shifts and rotates and is used to support normalization, field extract, and field deposit instructions.

The program sequencer controls the flow of instruction execution, including instruction alignment and decoding. For program flow control, the sequencer supports PC relative and indirect conditional jumps (with static branch prediction), and subroutine calls. Hardware is provided to support zero-overhead looping. The architecture is fully interlocked, meaning that the programmer need not manage the pipeline when executing instructions with data dependencies.

The address arithmetic unit provides two addresses for simultaneous dual fetches from memory. It contains a multiported register file consisting of four sets of 32-bit index, modify,

The controller provides support for five different types of events:

- Emulation. An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- Reset. This event resets the processor.
- Non-maskable interrupt (NMI). The NMI event can be generated by the software watchdog timer or by the $\overline{\text{NMI}}$ input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shut-down of the system.
- Exceptions. Events that occur synchronously to program flow (that is, the exception is taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts. Events that occur asynchronously to program flow. They are caused by input pins, timers, and other peripherals, as well as by an explicit software instruction.

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The ADSP-BF54x Blackfin processor event controller consists of two stages, the core event controller (CEC) and the system interrupt controller (SIC). The core event controller works with the system interrupt controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC and are then routed directly into the general-purpose interrupts of the CEC.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest-priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the ADSP-BF54x Blackfin processors. Table 3 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the ADSP-BF54x Blackfin processors provide a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). The *ADSP-BF54x Hardware Reference Manual*, "System Interrupts" chapter describes the inputs into the SIC and the default mappings into the CEC.

Table 3. Core Event Controller (CEC)

Priority (0 is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	Reset	RST
2	Nonmaskable Interrupt	NMI
3	Exception	EVX
4	Reserved	—
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General Interrupt 7	IVG7
8	General Interrupt 8	IVG8
9	General Interrupt 9	IVG9
10	General Interrupt 10	IVG10
11	General Interrupt 11	IVG11
12	General Interrupt 12	IVG12
13	General Interrupt 13	IVG13
14	General Interrupt 14	IVG14
15	General Interrupt 15	IVG15

Event Control

The ADSP-BF54x Blackfin processors provide the user with a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 16 bits wide:

- CEC interrupt latch register (ILAT). The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it may be written only when its corresponding IMASK bit is cleared.
- CEC interrupt mask register (IMASK). The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and is processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register may be read or written while in supervisor mode. Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.
- CEC interrupt pending register (IPEND). The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates that the event is currently active or nested at some level. This register is updated automatically by the controller but may be read while in supervisor mode.

The SIC allows further control of event processing by providing three 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in the *ADSP-BF54x Hardware Reference Manual*, "System Interrupts" chapter.

The USB clock (USB_XI) is provided through a dedicated external crystal or crystal oscillator. See Table 62 for related timing requirements. If using a fundamental mode crystal to provide the USB clock, connect the crystal between USB_XI and USB_XO with a circuit similar to that shown in Figure 7. Use a parallel-resonant, fundamental mode, microprocessor-grade crystal. If a third-overtone crystal is used, follow the circuit guidelines outlined in Clock Signals on Page 17 for third-overtone crystals.

The USB On-the-Go dual-role device controller includes a Phase Locked Loop with programmable multipliers to generate the necessary internal clocking frequency for USB. The multiplier value should be programmed based on the USB_XI clock frequency to achieve the necessary 480 MHz internal clock for USB high speed operation. For example, for a USB_XI crystal frequency of 24 MHz, the USB_PLLOSC_CTRL register should be programmed with a multiplier value of 20 to generate a 480 MHz internal clock.

ATA/ATAPI-6 INTERFACE

The ATAPI interface connects to CD/DVD and HDD drives and is ATAPI-6 compliant. The controller implements the peripheral I/O mode, the multi-DMA mode, and the Ultra DMA mode. The DMA modes enable faster data transfer and reduced host management. The ATAPI controller supports PIO, multi-DMA, and ultra DMA ATAPI accesses. Key features include:

- Supports PIO modes 0, 1, 2, 3, 4
- Supports multiword DMA modes 0, 1, 2
- Supports ultra DMA modes 0, 1, 2, 3, 4, 5 (up to UDMA 100)
- Programmable timing for ATA interface unit
- Supports CompactFlash cards using true IDE mode

By default, the ATAPI_A0-2 address signals and the ATAPI_D0-15 data signals are shared on the asynchronous memory interface with the asynchronous memory and NAND flash controllers. The data and address signals can be remapped to GPIO ports F and G, respectively, by setting PORTF_MUX[1:0] to b#01.

KEYPAD INTERFACE

The keypad interface is a 16-pin interface module that is used to detect the key pressed in a 8 × 8 (maximum) keypad matrix. The size of the input keypad matrix is programmable. The interface is capable of filtering the bounce on the input pins, which is common in keypad applications. The width of the filtered bounce is programmable. The module is capable of generating an interrupt request to the core once it identifies that any key has been pressed.

The interface supports a press-release-press mode and infrastructure for a press-hold mode. The former mode identifies a press, release and press of a key as two consecutive presses of the same key, whereas the latter mode checks the input key's state in periodic intervals to determine the number of times the same key is meant to be pressed. It is possible to detect when multiple keys are pressed simultaneously and to provide limited key resolution capability when this happens.

SECURE DIGITAL (SD)/SDIO CONTROLLER

The SD/SDIO controller is a serial interface that stores data at a data rate of up to 10M bytes per second using a 4-bit data line.

The SD/SDIO controller supports the SD memory mode only. The interface supports all the power modes and performs error checking by CRC.

CODE SECURITY

An OTP/security system, consisting of a blend of hardware and software, provides customers with a flexible and rich set of code security features with Lockbox® secure technology. Key features include:

- OTP memory
- Unique chip ID
- Code authentication
- Secure mode of operation

The security scheme is based upon the concept of authentication of digital signatures using standards-based algorithms and provides a secure processing environment in which to execute code and protect assets. See Lockbox Secure Technology Disclaimer on Page 23.

MEDIA TRANSCEIVER MAC LAYER (MXVR)

The ADSP-BF549 Blackfin processors provide a media transceiver (MXVR) MAC layer, allowing the processor to be connected directly to a MOST® [1] network through an FOT. See Figure 5 on Page 15 for an example of a MXVR MOST connection.

The MXVR is fully compatible with industry-standard standalone MOST controller devices, supporting 22.579 Mbps or 24.576 Mbps data transfer. It offers faster lock times, greater jitter immunity, and a sophisticated DMA scheme for data transfers. The high speed internal interface to the core and L1 memory allows the full bandwidth of the network to be utilized. The MXVR can operate as either the network master or as a network slave.

The MXVR supports synchronous data, asynchronous packets, and control messages using dedicated DMA channels that operate autonomously from the processor core moving data to and from L1 and/or L2 memory. Synchronous data is transferred to or from the synchronous data physical channels on the MOST bus through eight programmable DMA channels. The synchronous data DMA channels can operate in various modes including modes that trigger DMA operation when data patterns are detected in the receive data stream. Furthermore, two DMA channels support asynchronous traffic, and two others support control message traffic.

[1] MOST is a registered trademark of Standard Microsystems, Corp.

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
DDR Memory Interface			
DA0–12	O	DDR Address Bus	D
DBA0–1	O	DDR Bank Active Strobe	D
DQ0–15	I/O	DDR Data Bus	D
DQS0–1	I/O	DDR Data Strobe	D
DQM0–1	O	DDR Data Mask for Reads and Writes	D
DCLK0–1	O	DDR Output Clock	D
$\overline{\text{DCLK0–1}}$	O	DDR Complementary Output Clock	D
$\overline{\text{DCS0–1}}$	O	DDR Chip Selects	D
DCLKE[9]	O	DDR Clock Enable (Requires a pull-down if hibernate with DDR self-refresh is used.)	D
$\overline{\text{DRAS}}$	O	DDR Row Address Strobe	D
$\overline{\text{DCAS}}$	O	DDR Column Address Strobe	D
$\overline{\text{DWE}}$	O	DDR Write Enable	D
DDR_VREF	I	DDR Voltage Reference	
DDR_VSSR	I	DDR Voltage Reference Shield (Must be connected to GND.)	
Asynchronous Memory Interface			
A1-3	O	Address Bus for Async and ATAPI Addresses	A
D0-15/ND_D0-15/ATAPI_D0-15	I/O	Data Bus for Async, NAND and ATAPI Accesses	A
$\overline{\text{AMS0–3}}$	O	Bank Selects (Pull high with a resistor when used as chip select. Require pull-ups if hibernate is used.)	A
$\overline{\text{ABE0}}$ / *ND_CLE*	O	Byte Enables: Data Masks for Asynchronous Access / *NAND Command Latch Enable*	A
$\overline{\text{ABE1}}$ / *ND_ALE*	O	Byte Enables: Data Masks for Asynchronous Access / *NAND Address Latch Enable*	A
$\overline{\text{AOE}}$ / *NR_ADV*	O	Output Enable / *NOR Address Data Valid*	A
$\overline{\text{ARE}}$	O	Read Enable / *NOR Output Enable*	A
$\overline{\text{AWE}}$	O	Write Enable	A
ATAPI Controller Pins			
$\overline{\text{ATAPI\_PDIAG}}$	I	Determines if an 80-pin cable is connected to the host. (Pull high or low when unused.)	
High Speed USB OTG Pins			
USB_DP	I/O	USB D+ Pin (Pull low when unused.)	
USB_DM	I/O	USB D– Pin (Pull low when unused.)	
USB_XI	C	Clock XTAL Input (Pull high or low when unused.)	
USB_XO	C	Clock XTAL Output (Leave unconnected when unused.)	
USB_ID[10]	I	USB OTG ID Pin (Pull high when unused.)	

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
Supplies			
V_{DDINT}	P	Internal Power Supply	
V_{DDEXT}[12]	P	External Power Supply	
V_{DDDDR}[12]	P	External DDR Power Supply	
V_{DDUSB}[12]	P	External USB Power Supply	
V_{DDRTC}[12]	P	RTC Clock Supply	
V_{DDVR}[13]	P	Internal Voltage Regulator Power Supply (Connect to V_{DDEXT} when unused.)	
GND	G	Ground	
V_{DDMP}[12]	P	MXVR PLL Power Supply. (Must be driven to same level as V_{DDINT}. Connect to V_{DDINT} when unused or when MXVR is not present.)	
GND_{MP}[12]	G	MXVR PLL Ground (Connect to GND when unused or when MXVR is not present.)	

[1] I = Input, O = Output, P =Power, G = Ground, C = Crystal, A = Analog.
[2] Refer to Table 62 on Page 88 through Table 71 on Page 89 for driver types.
[3] To use the SPI memory boot, SPI0SCK should have a pulldown, SPI0MISO should have a pullup, and $\overline{\text{SPI0SEL1}}$ is used as the $\overline{\text{CS}}$ with a pullup.
[4] $\overline{\text{HWAIT}}$/HWAITA should be pulled high or low to configure polarity. See Booting Modes on Page 18.
[5] $\overline{\text{GPW}}$ functionality is available when MXVR is not present or unused.
[6] This pin should not be used as GPIO if booting in mode 1.
[7] This pin should always be enabled as $\overline{\text{ND\_CE}}$ in software and pulled high with a resistor when using NAND flash.
[8] This pin should always be enabled as $\overline{\text{BR}}$ in software and pulled high to enable asynchronous access.
[9] This pin must be pulled low through a 10kOhm resistor if self-refresh mode is desired during hibernate state or deep-sleep mode.
[10] If the USB is used in device mode only, the USB_ID pin should be either pulled high or left unconnected.
[11] This pin is an output only during initialization of USB OTG session request pulses in peripheral mode. Therefore, host mode or OTG type A mode requires that an external voltage source of 5 V, at 8 mA or more per the OTG specification, be applied to this pin. Other OTG modes require that this external voltage be disabled.
[12] To ensure proper operation, the power pins should be driven to their specified level even if the associated peripheral is not used in the application.
[13] This pin must always be connected. If the internal voltage regulator is not being used, this pin may be connected to V_{DDEXT}. Otherwise it should be powered according to the VDDVR specification. For automotive grade models, the internal voltage regulator must not be used and this pin must be tied to V_{DDEXT}.

[10]Parameter value applies to USB_DP, USB_DM, and USB_VBUS pins. See Absolute Maximum Ratings on Page 40.
[11]Parameter value applies to all input and bidirectional pins, except PB1-0, PE15-14, PG15–11, and PH7-6.
[12]Parameter value applies to pins PG15–11 and PH7-6.
[13]Parameter value applies to pins PB1-0 and PE15-14. Consult the I^2C specification version 2.1 for the proper resistor value and other open drain pin electrical parameters.
[14]T_J must be in the range: 0°C < T_J < 55°C during OTP memory programming operations.

Table 12 and Table 15 describe the voltage/frequency requirements for the ADSP-BF54x Blackfin processors' clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock. Table 14 describes the phase-locked loop operating conditions.

Table 12. Core Clock (CCLK) Requirements—533 MHz and 600 MHz Speed Grade[1]

Parameter		Min V_{DDINT}	Internal Regulator Setting[2]	Max CCLK Frequency	Unit
f_{CCLK}	Core Clock Frequency	1.30 V	N/A[2]	600	MHz
		1.188 V	1.25 V	533	MHz
		1.14 V	1.20 V	500	MHz
		1.045 V	1.10 V	444	MHz
		0.95 V	1.00 V	400	MHz
		0.90 V	0.95 V	333	MHz

[1] See the Ordering Guide on Page 101.
[2] Use of an internal voltage regulator is not supported on automotive grade and 600 MHz speed grade models. Internal regulator setting should be used as recommended nominal V_{DDINT} for external regulator.

Table 13. Core Clock (CCLK) Requirements—400 MHz Speed Grade[1]

Parameter		Min V_{DDINT}	Internal Regulator Setting[2]	Max CCLK Frequency	Unit
f_{CCLK}	Core Clock Frequency	1.14 V	1.20 V	400	MHz
		1.045 V	1.10 V	364	MHz
		0.95 V	1.00 V	333	MHz
		0.90 V	0.95 V	300	MHz

[1] See Ordering Guide on Page 101.
[2] Use of an internal voltage regulator is not supported on automotive grade models. Internal regulator setting should be used as recommended nominal V_{DDINT} for external regulator.

Table 14. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	50	Maximum f_{CCLK}	MHz

Table 15. System Clock Requirements

Parameter	Condition	DDR SDRAM Models Max	Mobile DDR SDRAM Models Min	Mobile DDR SDRAM Models Max	Unit
f_{SCLK}	$V_{DDINT} \geq 1.14$ V[1], Non-extended temperature grades	133[2]	120[3]	133[2]	MHz
f_{SCLK}	$V_{DDINT} < 1.14$ V[1], Non-extended temperature grades	100	N/A[4]	N/A[4]	MHz
f_{SCLK}	$V_{DDINT} \geq 1.0$ V[1], Extended temperature grade	100	N/A	N/A	MHz

[1] f_{SCLK} must be less than or equal to f_{CCLK}.
[2] Rounded number. Actual test specification is SCLK period of 7.5 ns. See Table 25 on Page 43.
[3] Rounded number. Actual test specification is SCLK period of 8.33 ns.
[4] V_{DDINT} must be greater than or equal to 1.14 V for mobile DDR SDRAM models. See Operating Conditions on Page 34.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Nonautomotive 400 MHz[1] Min	Typ	Max	All Other Devices[2] Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage for 3.3 V I/O[3]	V_{DDEXT} = 2.7 V, I_{OH} = –0.5 mA	2.4			2.4			V
	High Level Output Voltage for 2.5 V I/O[3]	V_{DDEXT} = 2.25 V, I_{OH} = –0.5 mA	2.0			2.0			V
V_{OHDDR}	High Level Output Voltage for DDR SDRAM[4]	V_{DDDDR} = 2.5 V, I_{OH} = –8.1 mA	1.74			1.74			V
	High Level Output Voltage for Mobile DDR SDRAM[4]	V_{DDDDR} = 1.8 V, I_{OH} = –0.1 mA	1.62			1.62			V
V_{OL}	Low Level Output Voltage for 3.3 V I/O[3]	V_{DDEXT} = 2.7 V, I_{OL} = 2.0 mA			0.4			0.4	V
	Low Level Output Voltage for 2.5 V I/O[3]	V_{DDEXT} = 2.25 V, I_{OL} = 2.0 mA			0.4			0.4	V
V_{OLDDR}	Low Level Output Voltage for DDR SDRAM[4]	V_{DDDDR} = 2.5 V, I_{OL} = 8.1 mA			0.56			0.56	V
	Low Level Output Voltage for Mobile DDR SDRAM[4]	V_{DDDDR} = 1.8 V, I_{OL} = 0.1 mA			0.18			0.18	V
I_{IH}	High Level Input Current[5]	V_{DDEXT} = 3.6 V, V_{IN} = V_{IN} Max			10.0			10.0	µA
I_{IHP}	High Level Input Current[6]	V_{DDEXT} = 3.6 V, V_{IN} = V_{IN} Max			50.0			50.0	µA
I_{IHDDR_VREF}	High Level Input Current for DDR SDRAM[7]	V_{DDDDR} = 2.7 V, V_{IN} = 0.51 × V_{DDDDR}			30.0			30.0	µA
	High Level Input Current for Mobile DDR SDRAM[7]	V_{DDDDR} = 1.95 V, V_{IN} = 0.51 × V_{DDDDR}			30.0			30.0	µA
I_{IL}[8]	Low Level Input Current	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10.0			10.0	µA
I_{OZH}[9]	Three-State Leakage Current[10]	V_{DDEXT} = 3.6 V, V_{IN} = V_{IN} Max			10.0			10.0	µA
I_{OZL}[11]	Three-State Leakage Current[10]	V_{DDEXT} = 3.6 V, V_{IN} = 0 V			10.0			10.0	µA
C_{IN}	Input Capacitance[12]	f_{IN} = 1 MHz, $T_{AMBIENT}$ = 25°C, V_{IN} = 2.5 V		4[12]	8[12]		4[12]	8[12]	pF
$I_{DDDEEPSLEEP}$[13]	V_{DDINT} Current in Deep Sleep Mode	V_{DDINT} = 1.0 V, f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz, T_J = 25°C, ASF = 0.00		22			37		mA
$I_{DDSLEEP}$	V_{DDINT} Current in Sleep Mode	V_{DDINT} = 1.0 V, f_{SCLK} = 25 MHz, T_J = 25°C		35			50		mA
$I_{DD-IDLE}$	V_{DDINT} Current in Idle	V_{DDINT} = 1.0 V, f_{CCLK} = 50 MHz, T_J = 25°C, ASF = 0.47		44			59		mA

[13]See the *ADSP-BF54x Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[14]Includes current on V_{DDEXT}, V_{DDUSB}, V_{DDVR}, and V_{DDDR} supplies. Clock inputs are tied high or low.
[15]Guaranteed maximum specifications.
[16]Unit for V_{DDINT} is V (volts). Unit for f_{SCLK} is MHz. Example: 1.2 V, 133 MHz would be 0.77 × 1.2 × 133 = 122.9 mA added to $I_{DDDEEPSLEEP}$.
[17]See Table 18 for the list of I_{DDINT} power vectors covered.

Total power dissipation has two components:

- Static, including leakage current
- Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 36 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 16 and Table 17), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 19).

There are two parts to the dynamic component. The first part is due to transistor switching in the core clock (CCLK) domain. This part is subject to an activity scaling factor (ASF) which represents application code running on the processor core and L1/L2 memories (Table 18). The ASF is combined with the CCLK frequency and V_{DDINT} dependent data in Table 19 to calculate this part. The second part is due to transistor switching in the system clock (SCLK) domain, which is included in the I_{DDINT} specification equation.

Table 16. Static Current—Low Power Process (mA)[1]

	Voltage (V_{DDINT})[2]												
T_J (°C)[2]	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.38 V	1.40 V	1.43 V
–40	11.9	13.5	15.5	17.7	20.3	23.3	26.8	30.6	35.0	39.9	43.2	45.5	49.5
0	20.1	22.3	24.7	27.8	31.1	34.9	39.3	44.2	49.6	55.7	59.8	62.5	67.2
25	31.2	34.2	37.5	41.3	45.6	50.3	55.7	61.7	68.2	75.4	80.3	83.6	88.6
45	47.0	51.0	55.5	60.6	66.0	72.0	78.8	86.1	94.2	102.9	108.9	112.8	118.2
55	58.6	63.1	68.3	74.1	80.3	87.1	94.9	103.0	112.0	122.0	128.4	132.8	140.0
70	80.7	86.6	93.0	100.2	108.1	116.7	125.9	136.0	146.8	158.7	166.4	171.6	179.5
85	107.0	114.3	122.5	131.5	141.2	151.7	163.1	175.3	188.5	202.7	211.8	218.0	226.7
100	153.9	163.0	173.3	184.8	197.0	210.0	224.1	239.0	255.1	272.4	283.4	290.8	300.6
105	171.7	181.5	192.7	205.1	218.3	232.4	247.5	263.6	280.9	299.3	308.7	314.9	325.7
115	210.1	221.4	234.2	248.6	263.7	279.9	297.3	311.0	331.1	352.5	366.3	N/A	N/A
125	257.9	270.9	285.9	302.5	314.6	334.0	354.3	375.7	399.2	423.8	439.6	N/A	N/A

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ for 400 MHz speed-grade devices.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 34.

Table 17. Static Current—Automotive 400 MHz and All 533 MHz/600 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})[2]												
T_J (°C)[2]	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.38 V	1.40 V	1.43 V
–40	19.7	22.1	24.8	27.9	31.4	35.4	39.9	45.0	50.6	57.0	61.2	64.0	70.4
0	45.2	49.9	55.2	61.3	67.9	75.3	83.5	92.6	102.6	113.6	121.0	125.8	135.0
25	80.0	87.5	96.2	105.8	116.4	127.9	140.4	154.1	169.2	185.4	196.1	203.3	218.0
45	124.2	134.8	147.1	160.7	175.3	191.2	208.6	227.3	247.6	269.6	284.0	293.6	312.0
55	154.6	167.2	181.7	197.7	214.9	233.8	254.2	276.1	299.7	325.9	343.1	354.6	374.0
70	209.8	225.6	243.9	264.1	285.8	309.4	334.8	363.5	394.3	427.7	449.4	463.9	489.0
85	281.8	301.3	323.5	350.2	378.5	408.9	442.1	477.9	516.5	557.5	584.2	602.0	629.0
100	366.5	390.5	419.4	452.1	486.9	524.4	564.8	608.2	654.8	704.7	737.0	758.5	793.0
105	403.8	428.3	459.5	494.3	531.7	571.9	614.9	661.5	711.1	763.9	798.5	821.6	864.0

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ for automotive 400 MHz and all 533 MHz and 600 MHz speed grade devices.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 34.

Table 18. Activity Scaling Factors[1]

I_{DDINT} Power Vector	Activity Scaling Factor (ASF)
$I_{DD-PEAK}$	1.29
$I_{DD-HIGH}$	1.24
I_{DD-TYP}	1.00
I_{DD-APP}	0.87
I_{DD-NOP}	0.74
$I_{DD-IDLE}$	0.47

[1] See *Estimating Power for ADSP-BF534/BF536/BF537 Blackfin Processors (EE-297)*. The power vector information also applies to the ADSP-BF542/ADSP-BF544/ADSP-BF547/ADSP-BF548/ADSP-BF549 processors.

Table 19. Dynamic Current in CCLK Domain (mA, with ASF = 1.0)[1]

	Voltage (V_{DDINT})[2]												
f_{CCLK} (MHz)[2]	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.38 V	1.40 V	1.43 V
100	29.7	31.6	33.9	35.7	37.9	40.5	42.9	45.5	48.2	50.8	52.0	53.5	54.6
200	55.3	58.9	62.5	66.0	70.0	74.0	78.3	82.5	86.7	91.3	93.3	95.6	97.6
300	80.8	85.8	91.0	96.0	101.3	107.0	112.8	118.7	124.6	130.9	133.8	137.0	140.0
400	N/A	112.2	119.4	125.5	132.4	139.6	146.9	154.6	162.3	170.0	173.8	177.8	181.6
500	N/A	N/A	N/A	N/A	N/A	171.9	180.6	189.9	199.1	205.7	210.3	213.0	217.6
533	N/A	N/A	N/A	N/A	N/A	N/A	191.9	201.6	211.5	218.0	222.8	225.7	230.5
600	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	233.1	241.4	246.7	252.7	258.1

[1] The values are not guaranteed as stand-alone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 36.
[2] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 34.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 20 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Table 21 details the maximum duty cycle for input transient voltage.

Table 20. Absolute Maximum Ratings

Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.43 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +3.8 V
Input Voltage[1, 2, 3]	–0.5 V to +3.6 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
I_{OH}/I_{OL} Current per Single Pin[4]	40 mA (max)
I_{OH}/I_{OL} Current per Pin Group[4]	80 mA (max)
Storage Temperature Range	–65°C to +150°C
Junction Temperature Underbias	+125°C

[1] Applies to all bidirectional and input only pins except PB1-0, PE15-14, PG15–11, and PH7-6, where the absolute maximum input voltage range is –0.5 V to +5.5 V.

[2] Pins USB_DP, USB_DM, and USB_VBUS are 5 V-tolerant when VDDUSB is powered according to the operating conditions table. If VDDUSB supply voltage does not meet the specification in the operating conditions table, these pins could suffer long-term damage when driven to +5 V. If this condition is seen in the application, it can be corrected with additional circuitry to use the external host to power only the V_{DDUSB} pins. Contact factory for application detail and reliability information.

[3] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2 V.

[4] For more information, see description preceding Table 22.

Table 21. Maximum Duty Cycle for Input[1] Transient Voltage

V_{IN} Max (V)[2]	V_{IN} Min (V)	Maximum Duty Cycle
3.63	–0.33	100%
3.80	–0.50	48%
3.90	–0.60	30%
4.00	–0.70	20%
4.10	–0.80	10%
4.20	–0.90	8%
4.30	–1.00	5%

[1] Does not apply to CLKIN. Absolute maximum for pins PB1-0, PE15-14, PG15-11, and PH7-6 is +5.5V.

[2] Only one of the listed options can apply to a particular design.

The Absolute Maximum Ratings table specifies the maximum total source/sink (I_{OH}/I_{OL}) current for a group of pins. Permanent damage can occur if this value is exceeded. To understand this specification, if pins PA4, PA3, PA2, PA1 and PA0 from group 1 in the Total Current Pin Groups table were sourcing or sinking 2 mA each, the total current for those pins would be 10 mA. This would allow up to 70 mA total that could be sourced or sunk by the remaining pins in the group without damaging the device. For a list of all groups and their pins, see the Total Current Pin Groups table. Note that the V_{OL} and V_{OH} specifications have separate per-pin maximum current requirements, see the Electrical Characteristics table.

Table 22. Total Current Pin Groups

Group	Pins in Group
1	PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PA8, PA9, PA10, PA11
2	PA12, PA13, PA14, PA15, PB8, PB9, PB10, PB11, PB12, PB13, PB14
3	PB0, PB1, PB2, PB3, PB4, PB5, PB6, PB7, BMODE0, BMODE1, BMODE2, BMODE3
4	TCK, TDI, TDO, TMS, $\overline{\text{TRST}}$, PD14, $\overline{\text{EMU}}$
5	PD8, PD9, PD10, PD11, PD12, PD13, PD15
6	PD0, PD1, PD2, PD3, PD4, PD5, PD6, PD7
7	PE11, PE12, PE13, PF12, PF13, PF14, PF15, PG3, PG4
8	PF4, PF5, PF6, PF7, PF8, PF9, PF10, PF11
9	PF0, PF1, PF2, PF3, PG0, PG1, PG2
10	PC0, PC1, PC2, PC3, PC4, PC5, PC6, PC7
11	PH5, PH6, PH7
12	A1, A2, A3
13	PH8, PH9, PH10, PH11, PH12, PH13
14	PI0, PI1, PI2, PI3, PI4, PI5, PI6, PI7
15	PI8, PI9, PI10, PI11, PI12, PI13, PI14, PI15
16	$\overline{\text{AMS0}}$, $\overline{\text{AMS1}}$, $\overline{\text{AMS2}}$, $\overline{\text{AMS3}}$, $\overline{\text{AOE}}$, CLKBUF, $\overline{\text{NMI}}$
17	CLKIN, XTAL, $\overline{\text{RESET}}$, RTXI, RTXO, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$
18	D0, D1, D2, D3, D4, D5, D6, D7
19	D8, D9, D10, D11, D12
20	D13, D14, D15, $\overline{\text{ABE0}}$, $\overline{\text{ABE1}}$
21	EXT_WAKE, CLKOUT, PJ11, PJ12, PJ13
22	PJ0, PJ1, PJ2, PJ3, PJ4, PJ5, PJ6, PJ7, $\overline{\text{ATAPI\_PDIAG}}$
23	PJ8, PJ9, PJ10, PE7, PG12, PG13
24	PE0, PE1, PE2, PE4, PE5, PE6, PE8, PE9, PE10, PH3, PH4
25	PH0, PH2, PE14, PE15, PG5, PG6, PG7, PG8, PG9, PG10, PG11
26	PC8, PC9, PC10, PC11, PC12, PC13, PE3, PG14, PG15, PH1

DDR SDRAM/Mobile DDR SDRAM Write Cycle Timing

Table 33 and Figure 20 describe DDR SDRAM/mobile DDR SDRAM write cycle timing.

Table 33. DDR SDRAM/Mobile DDR SDRAM Write Cycle Timing

Parameter		DDR SDRAM Min	DDR SDRAM Max	Mobile DDR SDRAM Min	Mobile DDR SDRAM Max	Unit
Switching Characteristics						
t_{DQSS}	Write CMD to First DQS0-1	0.75	1.25	0.75	1.25	t_{CK}
t_{DS}	DQ0-15/DQM0-1 Setup to DQS0-1	0.90		0.90		ns
t_{DH}	DQ0-15/DQM0-1 Hold to DQS0-1	0.90		0.90		ns
t_{DSS}	DQS0-1 Falling to DCK0-1 Rising (DQS0-1 Setup)	0.20		0.20		t_{CK}
t_{DSH}	DQS0-1 Falling from DCK0-1 Rising (DQS0-1 Hold)	0.20		0.20		t_{CK}
t_{DQSH}	DQS0-1 High Pulse Width	0.35		0.40	0.60	t_{CK}
t_{DQSL}	DQS0-1 Low Pulse Width	0.35		0.40	0.60	t_{CK}
t_{WPRE}	DQS0-1 Write Preamble	0.25		0.25		t_{CK}
t_{WPST}	DQS0-1 Write Postamble	0.40	0.60	0.40	0.60	t_{CK}
t_{DOPW}	DQ0-15 and DQM0-1 Output Pulse Width (for Each)	1.75		1.75		ns

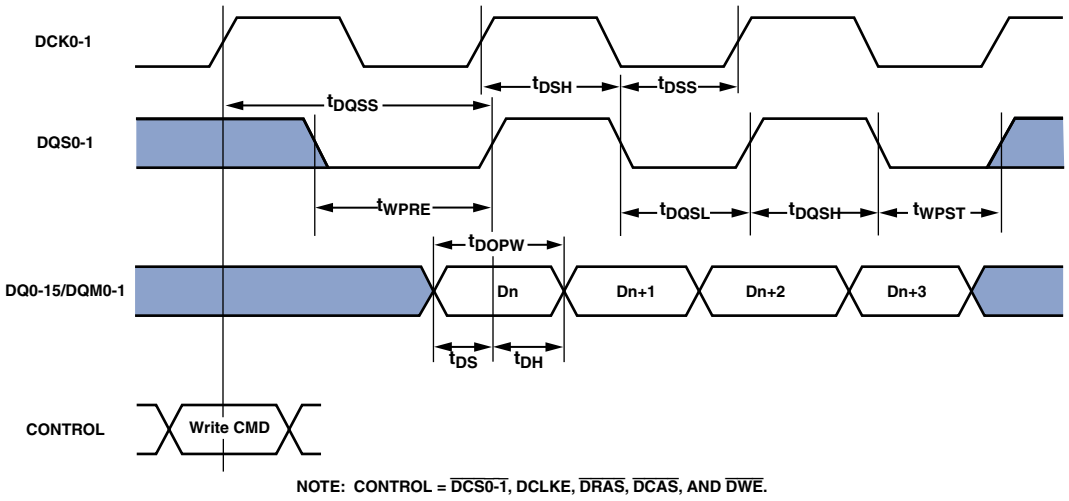


Figure 20. DDR SDRAM /Mobile DDR SDRAM Controller Write Cycle Timing

Timer Clock Timing

Table 47 and Figure 41 describe timer clock timing.

Table 47. Timer Clock Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TODP}	Timer Output Update Delay After PPI_CLK High		15	ns

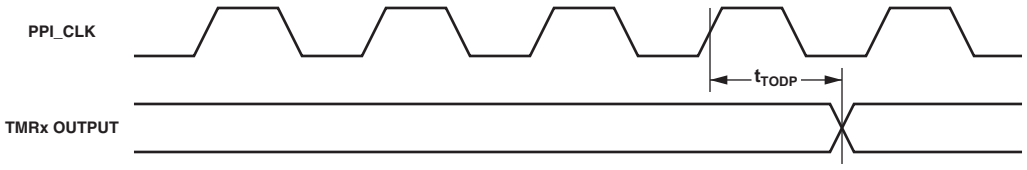


Figure 41. Timer Clock Timing

Timer Cycle Timing

Table 48 and Figure 42 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of (f_{SCLK}/2) MHz.

Table 48. Timer Cycle Timing

Parameter		Min	Max	Unit
Timing Characteristics				
t_{WL}	Timer Pulse Width Input Low[1]	1× t_{SCLK}		ns
t_{WH}	Timer Pulse Width Input High[1]	1× t_{SCLK}		ns
t_{TIS}	Timer Input Setup Time Before CLKOUT Low[2]	6.5		ns
t_{TIH}	Timer Input Hold Time After CLKOUT Low[2]	–1		ns
Switching Characteristics				
t_{HTO}	Timer Pulse Width Output	1× t_{SCLK}	(2^{32} – 1) × t_{SCLK}	ns
t_{TOD}	Timer Output Delay After CLKOUT High		6	ns

[1] The minimum pulse widths apply for TMRx signals in width capture and external clock modes.
[2] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize timer flag inputs.

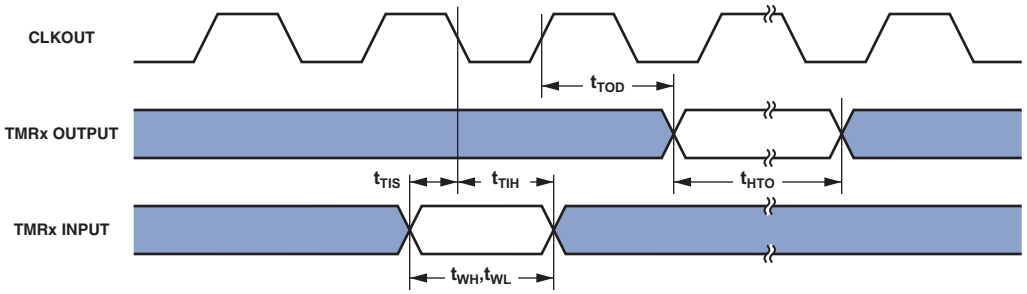


Figure 42. Timer Cycle Timing

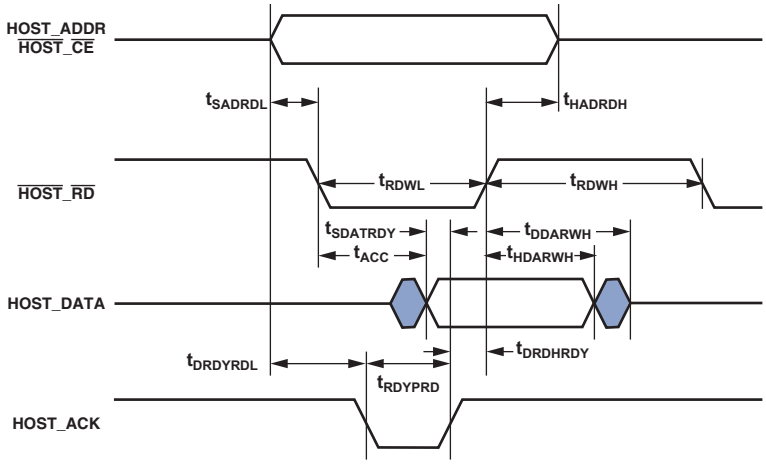
HOSTDP A/C Timing-Host Read Cycle

Table 54 and Figure 46 describe the HOSTDP A/C host read cycle timing requirements.

Table 54. Host Read Cycle Timing Requirements

Parameter		Min	Max	Unit
Timing Requirements				
t_{SADRDL}	HOST_ADDR and $\overline{\text{HOST\_CE}}$ Setup Before $\overline{\text{HOST\_RD}}$ Falling Edge	4		ns
t_{HADRDH}	HOST_ADDR and $\overline{\text{HOST\_CE}}$ Hold After $\overline{\text{HOST\_RD}}$ Rising Edge	2.5		ns
t_{RDWL}	$\overline{\text{HOST\_RD}}$ Pulse Width Low (ACK Mode)	$t_{DRDYRDL} + t_{RDYPRD} + t_{DRDHRDY}$		ns
	$\overline{\text{HOST\_RD}}$ Pulse Width Low (INT Mode)	$1.5 \times t_{SCLK} + 8.7$		ns
t_{RDWH}	$\overline{\text{HOST\_RD}}$ Pulse Width High or Time Between $\overline{\text{HOST\_RD}}$ Rising Edge and $\overline{\text{HOST\_WR}}$ Falling Edge	$2 \times t_{SCLK}$		ns
$t_{DRDHRDY}$	$\overline{\text{HOST\_RD}}$ Rising Edge Delay After HOST_ACK Rising Edge (ACK Mode)	0		ns
Switching Characteristics				
$t_{SDATRDY}$	HOST_D15–0 Valid Prior HOST_ACK Rising Edge (ACK Mode)	$t_{SCLK} - 4.0$		ns
$t_{DRDYRDL}$	HOST_ACK Falling Edge After $\overline{\text{HOST\_CE}}$ (ACK Mode)		11.25	ns
t_{RDYPRD}	HOST_ACK Low Pulse-Width for Read Access (ACK Mode)		NM[1]	ns
t_{DDARWH}	HOST_D15–0 Disable After $\overline{\text{HOST\_RD}}$		8.0	ns
t_{ACC}	HOST_D15–0 Valid After $\overline{\text{HOST\_RD}}$ Falling Edge (INT Mode)		$1.5 \times t_{SCLK}$	ns
t_{HDARWH}	HOST_D15–0 Hold After $\overline{\text{HOST\_RD}}$ Rising Edge	1.0		ns

[1] NM (Not Measured) — This parameter is based on t_{SCLK}. It is not measured because the number of SCLK cycles for which HOST_ACK remains low depends on the Host DMA FIFO status. This is system design dependent.



In Figure 46, HOST_DATA is HOST_D0–D15.

Figure 46. HOSTDP A/C—Host Read Cycle

Note that in Figure 49 an alternate ATAPI_D0–15 port bus is ATAPI_D0–15A.

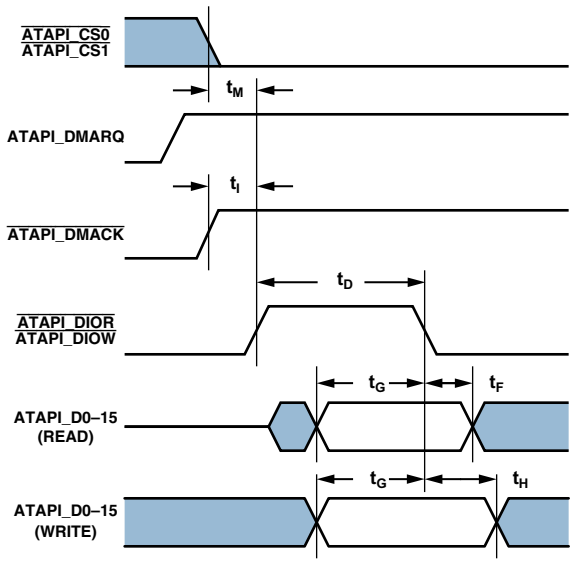


Figure 49. Initiating a Multiword DMA Data Burst

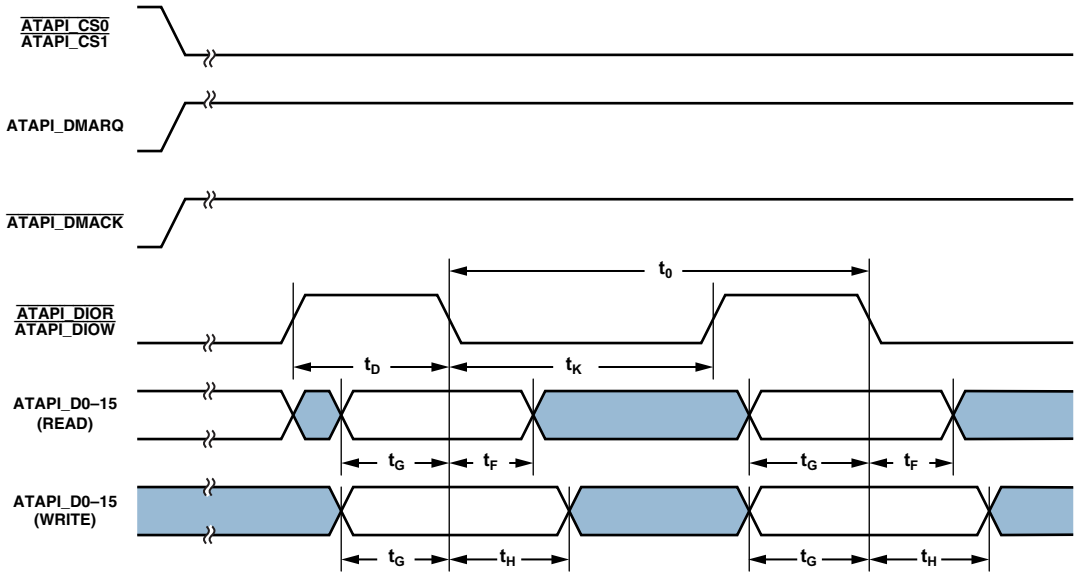


Figure 50. Sustained Multiword DMA Data Burst

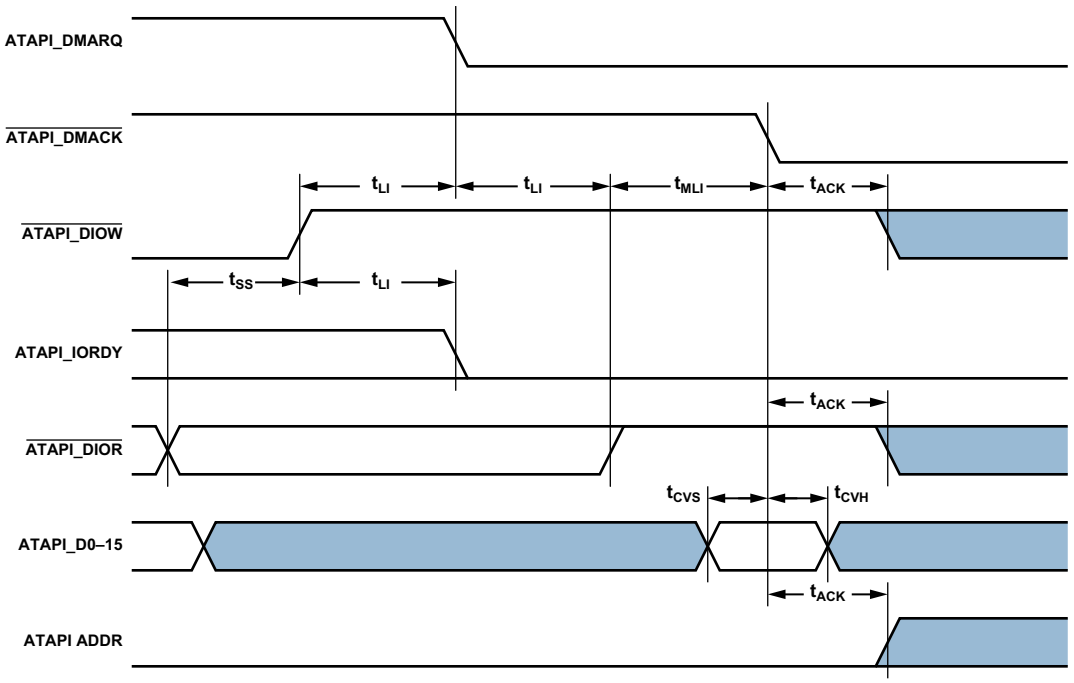


Figure 59. Host terminating an Ultra DMA Data-Out Burst

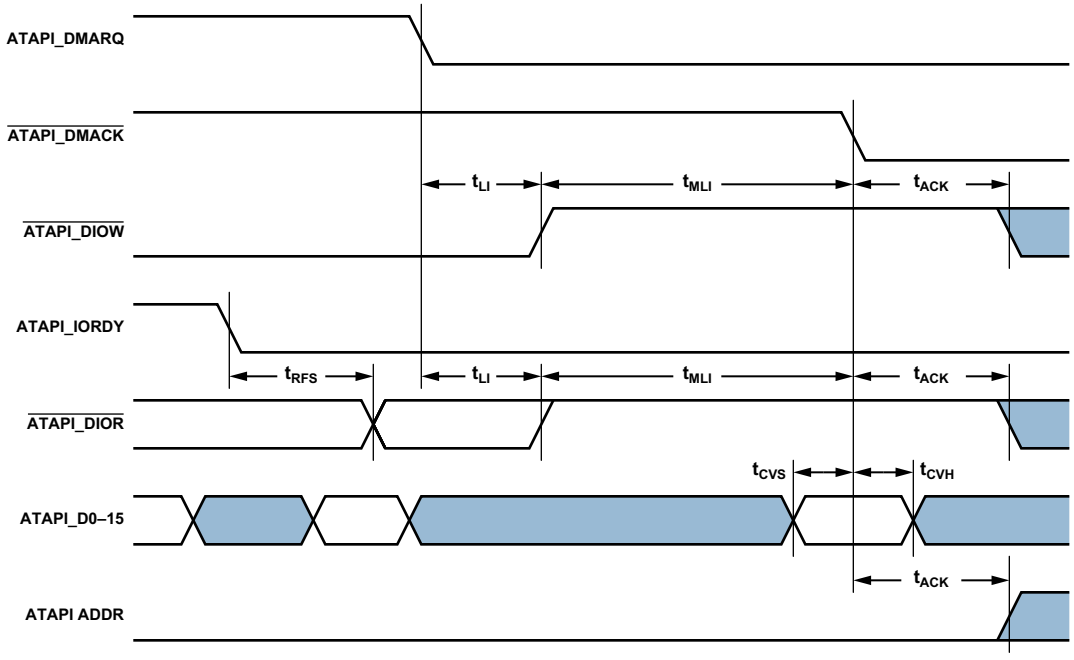


Figure 60. Device Terminating an Ultra DMA Data-Out Burst

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 72 shows the measurement point for AC measurements (except output enable/disable). The measurement point V_{MEAS} is $V_{DDEXT}/2$ or $V_{DDDDR}/2$, depending on the pin under test.

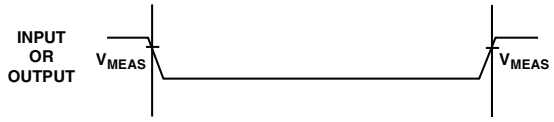


Figure 72. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to the point when they start driving. The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving as shown in the output enable/disable diagram (Figure 73). The time, $t_{ENA\_MEASURED}$, is the interval from the point when the reference signal switches to the point when the output voltage reaches either 1.75 V (output high) or 1.25 V (output low). Time t_{TRIP} is the interval from when the output starts driving to when the output reaches the 1.25 V or 1.75 V trip voltage. Time t_{ENA} is calculated as shown in the equation:

$$t_{ENA} = t_{ENA\_MEASURED} - t_{TRIP}$$

If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high-impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The output disable time t_{DIS} is the difference between $t_{DIS\_MEASURED}$ and t_{DECAY} as shown in Figure 73. The time $t_{DIS\_MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. The time t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.25 V.

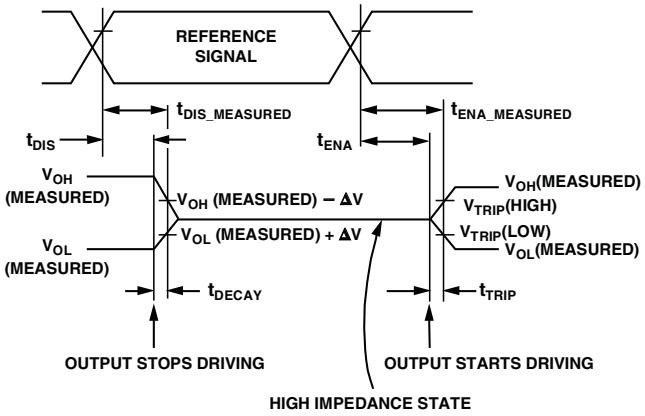


Figure 73. Output Enable/Disable

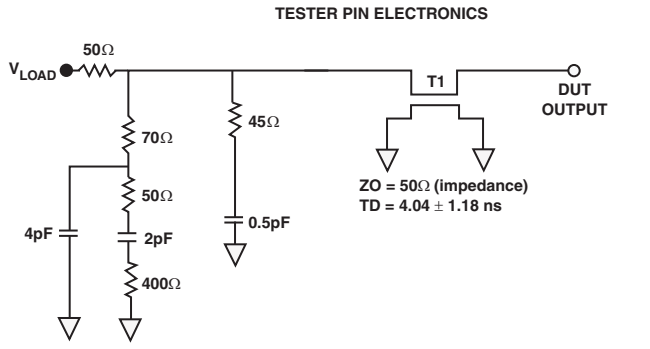
Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-BF54x Blackfin processors' output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (for example, t_{DDAT} for an asynchronous memory write cycle).

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all balls (see Figure 74).

V_{LOAD} is equal to $V_{DDEXT}/2$ or $V_{DDDDR}/2$, depending on the pin under test.



NOTES:
THE WORST-CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD), IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 74. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

TYPICAL RISE AND FALL TIMES

Figure 75 through Figure 86 on Page 93 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.

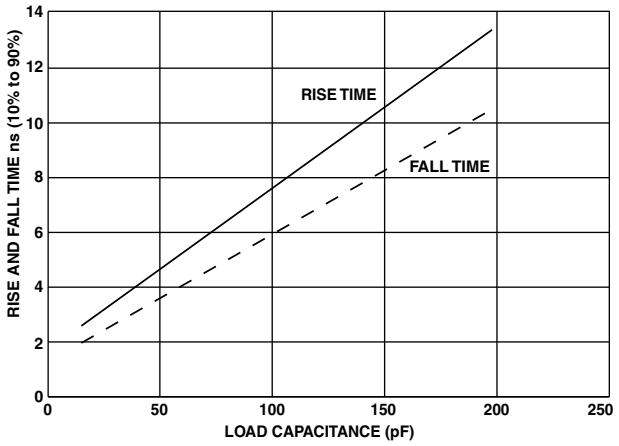


Figure 75. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 2.25 V

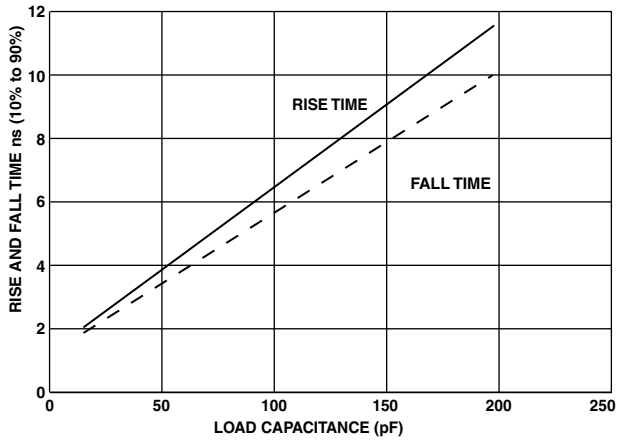


Figure 76. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 3.65 V

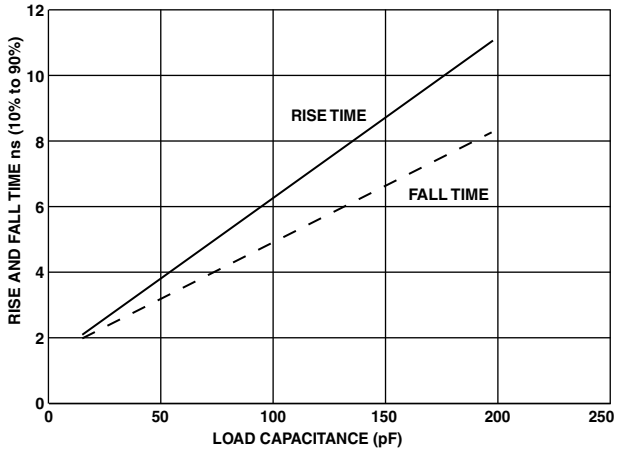


Figure 77. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 2.25 V

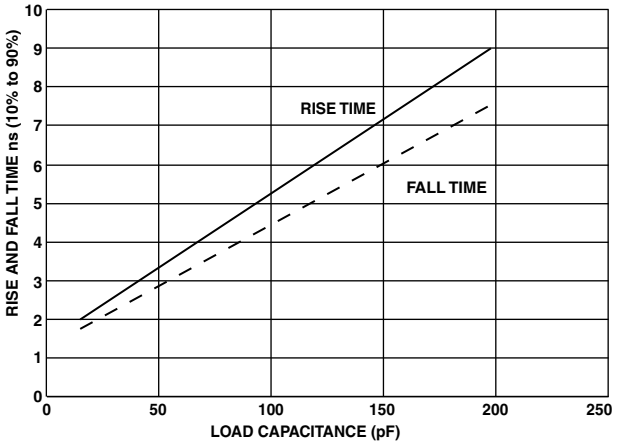


Figure 78. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 3.65 V

Table 65. 400-Ball CSP_BGA Ball Assignment (Alphabetical by Signal) (Continued)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
TCK	V3	V_{DDDDR}	J14	V_{DDEXT}	N5	V_{DDINT}	G13
TDI	V5	V_{DDDDR}	J15	V_{DDEXT}	N15	V_{DDINT}	J6
TDO	V4	V_{DDDDR}	K14	V_{DDEXT}	P15	V_{DDINT}	J13
TMS	U5	V_{DDDDR}	K15	V_{DDEXT}	R6	V_{DDINT}	L6
$\overline{TRST}$	T5	V_{DDEXT}	E5	V_{DDEXT}	R7	V_{DDINT}	L15
USB_DM	E2	V_{DDEXT}	E9	V_{DDEXT}	R8	V_{DDINT}	P6
USB_DP	E1	V_{DDEXT}	E10	V_{DDEXT}	R15	V_{DDINT}	P7
USB_ID	G3	V_{DDEXT}	E11	V_{DDEXT}	T7	V_{DDINT}	P14
USB_RSET	D3	V_{DDEXT}	E12	V_{DDEXT}	T8	V_{DDINT}	R10
USB_VBUS	D2	V_{DDEXT}	F7	V_{DDEXT}	T9	V_{DDINT}	R11
USB_VREF	B1	V_{DDEXT}	F8	V_{DDEXT}	T10	V_{DDINT}	R12
USB_XI	F1	V_{DDEXT}	F13	V_{DDEXT}	T11	V_{DDINT}	U9
USB_XO	F2	V_{DDEXT}	G5	V_{DDEXT}	T12	V_{DDMP}	E8
V_{DDDDR}	F10	V_{DDEXT}	G6	V_{DDEXT}	T13	V_{DDRTC}	E13
V_{DDDDR}	F11	V_{DDEXT}	G7	V_{DDEXT}	T14	V_{DDUSB}	F5
V_{DDDDR}	F12	V_{DDEXT}	G14	V_{DDEXT}	T15	V_{DDUSB}	G4
V_{DDDDR}	G15	V_{DDEXT}	H5	V_{DDEXT}	T16	V_{DDVR}	F15
V_{DDDDR}	H13	V_{DDEXT}	H6	V_{DDINT}	F9	VR_{OUT0}	A18
V_{DDDDR}	H14	V_{DDEXT}	K6	V_{DDINT}	G8	VR_{OUT1}	A19
V_{DDDDR}	H15	V_{DDEXT}	M15	V_{DDINT}	G12	XTAL	A12

OUTLINE DIMENSIONS

Dimensions for the 17 mm × 17 mm CSP_BGA package in Figure 88 are shown in millimeters.

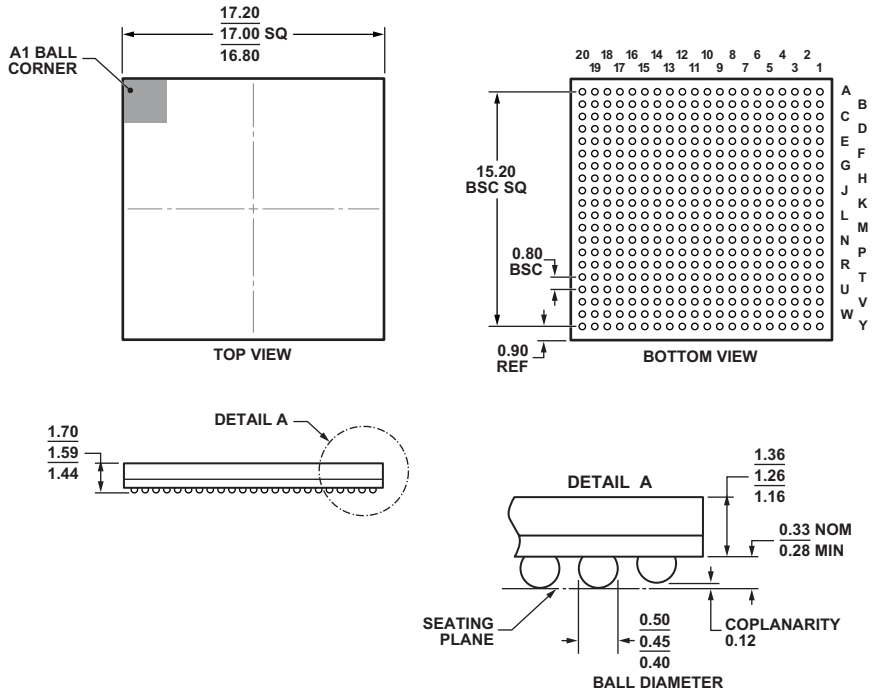


Figure 88. 400-Ball, 17 mm × 17 mm CSP_BGA (Chip Scale Package Ball Grid Array) (BC-400-1)

SURFACE-MOUNT DESIGN

Table 67 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Table 67. BGA Data for Use with Surface-Mount Design

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
400-Ball CSP_BGA (Chip Scale Package Ball Grid Array) BC-400-1	Solder Mask Defined	0.40 mm Diameter	0.50 mm Diameter