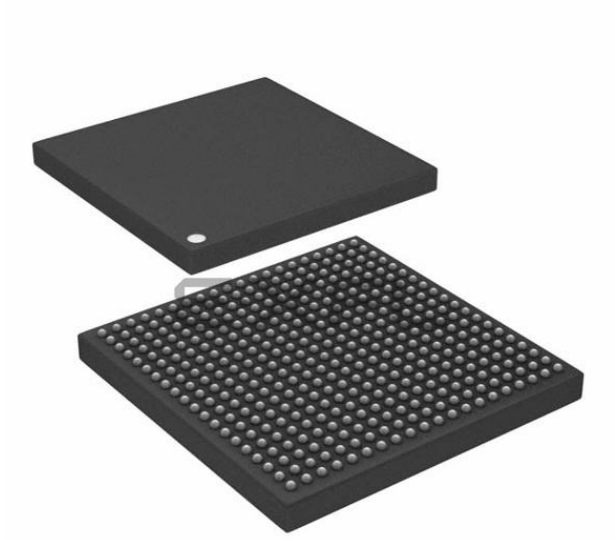

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART, USB
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	132kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf542bbcz-4a

The USB clock (USB_XI) is provided through a dedicated external crystal or crystal oscillator. See Table 62 for related timing requirements. If using a fundamental mode crystal to provide the USB clock, connect the crystal between USB_XI and USB_XO with a circuit similar to that shown in Figure 7. Use a parallel-resonant, fundamental mode, microprocessor-grade crystal. If a third-overtone crystal is used, follow the circuit guidelines outlined in Clock Signals on Page 17 for third-overtone crystals.

The USB On-the-Go dual-role device controller includes a Phase Locked Loop with programmable multipliers to generate the necessary internal clocking frequency for USB. The multiplier value should be programmed based on the USB_XI clock frequency to achieve the necessary 480 MHz internal clock for USB high speed operation. For example, for a USB_XI crystal frequency of 24 MHz, the USB_PLLOSC_CTRL register should be programmed with a multiplier value of 20 to generate a 480 MHz internal clock.

ATA/ATAPI-6 INTERFACE

The ATAPI interface connects to CD/DVD and HDD drives and is ATAPI-6 compliant. The controller implements the peripheral I/O mode, the multi-DMA mode, and the Ultra DMA mode. The DMA modes enable faster data transfer and reduced host management. The ATAPI controller supports PIO, multi-DMA, and ultra DMA ATAPI accesses. Key features include:

- Supports PIO modes 0, 1, 2, 3, 4
- Supports multiword DMA modes 0, 1, 2
- Supports ultra DMA modes 0, 1, 2, 3, 4, 5 (up to UDMA 100)
- Programmable timing for ATA interface unit
- Supports CompactFlash cards using true IDE mode

By default, the ATAPI_A0-2 address signals and the ATAPI_D0-15 data signals are shared on the asynchronous memory interface with the asynchronous memory and NAND flash controllers. The data and address signals can be remapped to GPIO ports F and G, respectively, by setting PORTF_MUX[1:0] to b#01.

KEYPAD INTERFACE

The keypad interface is a 16-pin interface module that is used to detect the key pressed in a 8 × 8 (maximum) keypad matrix. The size of the input keypad matrix is programmable. The interface is capable of filtering the bounce on the input pins, which is common in keypad applications. The width of the filtered bounce is programmable. The module is capable of generating an interrupt request to the core once it identifies that any key has been pressed.

The interface supports a press-release-press mode and infrastructure for a press-hold mode. The former mode identifies a press, release and press of a key as two consecutive presses of the same key, whereas the latter mode checks the input key's state in periodic intervals to determine the number of times the same key is meant to be pressed. It is possible to detect when multiple keys are pressed simultaneously and to provide limited key resolution capability when this happens.

SECURE DIGITAL (SD)/SDIO CONTROLLER

The SD/SDIO controller is a serial interface that stores data at a data rate of up to 10M bytes per second using a 4-bit data line.

The SD/SDIO controller supports the SD memory mode only. The interface supports all the power modes and performs error checking by CRC.

CODE SECURITY

An OTP/security system, consisting of a blend of hardware and software, provides customers with a flexible and rich set of code security features with Lockbox® secure technology. Key features include:

- OTP memory
- Unique chip ID
- Code authentication
- Secure mode of operation

The security scheme is based upon the concept of authentication of digital signatures using standards-based algorithms and provides a secure processing environment in which to execute code and protect assets. See Lockbox Secure Technology Disclaimer on Page 23.

MEDIA TRANSCEIVER MAC LAYER (MXVR)

The ADSP-BF549 Blackfin processors provide a media transceiver (MXVR) MAC layer, allowing the processor to be connected directly to a MOST® [1] network through an FOT. See Figure 5 on Page 15 for an example of a MXVR MOST connection.

The MXVR is fully compatible with industry-standard standalone MOST controller devices, supporting 22.579 Mbps or 24.576 Mbps data transfer. It offers faster lock times, greater jitter immunity, and a sophisticated DMA scheme for data transfers. The high speed internal interface to the core and L1 memory allows the full bandwidth of the network to be utilized. The MXVR can operate as either the network master or as a network slave.

The MXVR supports synchronous data, asynchronous packets, and control messages using dedicated DMA channels that operate autonomously from the processor core moving data to and from L1 and/or L2 memory. Synchronous data is transferred to or from the synchronous data physical channels on the MOST bus through eight programmable DMA channels. The synchronous data DMA channels can operate in various modes including modes that trigger DMA operation when data patterns are detected in the receive data stream. Furthermore, two DMA channels support asynchronous traffic, and two others support control message traffic.

[1] MOST is a registered trademark of Standard Microsystems, Corp.

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity will wake up the processor. In the sleep mode, assertion of a wakeup event enabled in the SIC_IWRx register causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor transitions to the full on mode. If BYPASS is enabled, the processor transitions to the active mode.

In the sleep mode, system DMA access to L1 memory is not supported.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such as the RTC, may still be running but will not be able to access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. In deep sleep mode, an asynchronous RTC interrupt causes the processor to transition to the active mode. Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full on mode.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and to all the synchronous peripherals (SCLK). The internal voltage regulator for the processor can be shut off by using the bfrom_SysControl() function in the on-chip ROM. This sets the internal power supply voltage (V_{DDINT}) to 0 V to provide the greatest power savings mode. Any critical information stored internally (memory contents, register contents, and so on) must be written to a non-volatile storage device prior to removing power if the processor state is to be preserved.

Since V_{DDEXT} is still supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to have power still applied without drawing unwanted current.

The internal supply regulator can be woken up by CAN, by the MXVR, by the keypad, by the up/down counter, by the USB, and by some GPIO pins. It can also be woken up by a real-time clock wakeup event or by asserting the $\overline{\text{RESET}}$ pin. Waking up from hibernate state initiates the hardware reset sequence.

With the exception of the VR_CTL and the RTC registers, all internal registers and memories lose their content in hibernate state. State variables may be held in external SRAM or DDR memory.

Power Domains

As shown in Table 5, the ADSP-BF54x Blackfin processors support different power domains. The use of multiple power domains maximizes flexibility while maintaining compliance with industry standards and conventions. By isolating the internal logic of the ADSP-BF54x Blackfin processors into its own power domain separate from the RTC and other I/O, the processors can take advantage of dynamic power management without affecting the RTC or other I/O devices. There are no sequencing requirements for the various power domains.

Table 5. Power Domains

Power Domain	VDD Range
All internal logic, except RTC, DDR, and USB	V_{DDINT}
RTC internal logic and crystal I/O	V_{DDRTC}
DDR external memory supply	V_{DDDDR}
USB internal logic and crystal I/O	V_{DDUSB}
Internal voltage regulator	V_{DDVR}
MXVR PLL and logic	V_{DDMP}
All other I/O	V_{DDEXT}

VOLTAGE REGULATION

The ADSP-BF54x Blackfin processors provide an on-chip voltage regulator that can generate processor core voltage levels from an external supply (see specifications in Operating Conditions on Page 34). Figure 6 on Page 17 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. This register can be accessed using the bfrom_SysControl() function in the on-chip ROM. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power supplied. While in hibernate state, V_{DDEXT}, V_{DDRTC}, V_{DDDDR}, V_{DDUSB}, and V_{DDVR} can still be applied, eliminating the need for external buffers. The voltage regulator can be activated from this power-down state by assertion of the $\overline{\text{RESET}}$ pin, which then initiates a boot sequence. The regulator can also be disabled and bypassed at the user's discretion. For all 600 MHz speed grade models and all automotive grade models, the internal voltage regulator must not be used and V_{DDVR} must be tied to V_{DDEXT}. For additional information regarding design of the voltage regulator circuit, see *Switching Regulator Design Considerations for the ADSP-BF533 Blackfin Processors (EE-228)*.

For large page NAND flash devices, the 4-byte electronic signature is read in order to configure the kernel for booting. This allows support for multiple large page devices. The fourth byte of the electronic signature must comply with the specifications in Table 9.

Any configuration from Table 9 that also complies with the command set listed below is directly supported by the boot kernel. There are no restrictions on the page size or block size as imposed by the small-page boot kernel.

Table 9. Byte 4 Electronic Signature Specification

Page Size (excluding spare area)	D1:D0	00	1K bytes
		01	2K bytes
		10	4K bytes
		11	8K bytes
Spare Area Size	D2	0	8 bytes/512 bytes
		1	16 bytes/512 bytes
Block Size (excluding spare area)	D5:4	00	64K bytes
		01	128K bytes
		10	256K bytes
		11	512K bytes
Bus Width	D6	0	x8
		1	x16
Not Used for Configuration	D3, D7		

Large page devices must support the following command set:

Reset: 0xFF
Read Electronic Signature: 0x90
Read: 0x00, 0x30 (confirm command)

Large page devices must not support or react to NAND flash command 0x50. This is a small page NAND flash command used for device auto detection.

By default, the boot kernel will always issue five address cycles; therefore, if a large page device requires only four cycles, the device must be capable of ignoring the additional address cycle.

16-bit NAND flash memory devices must only support the issuing of command and address cycles via the lower eight bits of the data bus. Devices that use the full 16-bit bus for command and address cycles are not supported.

- Boot from OTP memory (BMODE = 0xB)—This provides a standalone booting method. The boot stream is loaded from on-chip OTP memory. By default, the boot stream is expected to start from OTP page 0x40 and can occupy all public OTP memory up to page 0xDF (2560 bytes). Since the start page is programmable, the maximum size of the boot stream can be extended to 3072 bytes.
- Boot from 16-bit host DMA (BMODE = 0xE)—In this mode, the host DMA port is configured in 16-bit acknowledge mode with little endian data format. Unlike other modes, the host is responsible for interpreting the boot stream. It writes data blocks individually into the host DMA port. Before configuring the DMA settings for each block, the host may either poll the ALLOW_CONFIG bit in HOST_STATUS or wait to be interrupted by the HWAIT signal. When using HWAIT, the host must still check ALLOW_CONFIG at least once before beginning to configure the host DMA port. After completing the configuration, the host is required to poll the READY bit in HOST_STATUS before beginning to transfer data. When the host sends an HIRQ control command, the boot kernel issues a CALL instruction to address 0xFFA0 0000. It is the host's responsibility to ensure valid code has been placed at this address. The routine at address 0xFFA0 0000 can be a simple initialization routine to configure internal resources, such as the SDRAM controller, which then returns using an RTS instruction. The routine may also be the final application, which will never return to the boot kernel.
- Boot from 8-bit host DMA (BMODE = 0xF)—In this mode, the host DMA port is configured in 8-bit interrupt mode with little endian data format. Unlike other modes, the host is responsible for interpreting the boot stream. It writes data blocks individually to the host DMA port. Before configuring the DMA settings for each block, the host may either poll the ALLOW_CONFIG bit in HOST_STATUS or wait to be interrupted by the HWAIT signal. When using HWAIT, the host must still check ALLOW_CONFIG at least once before beginning to configure the host DMA port. The host will receive an interrupt from the HOST_ACK signal every time it is allowed to send the next FIFO depth's worth (sixteen 32-bit words) of information. When the host sends an HIRQ control command, the boot kernel issues a CALL instruction to address 0xFFA0 0000. It is the host's responsibility to ensure valid code has been placed at this address. The routine at address 0xFFA0 0000 can be a simple initialization routine to configure internal resources, such as the SDRAM controller, which then returns using an RTS instruction. The routine may also be the final application, which will never return to the boot kernel.

For each of the boot modes, a 16-byte header is first read from an external memory device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks may be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the address stored in the EVT1 register.

Prior to booting, the pre-boot routine interrogates the OTP memory. Individual boot modes can be customized or disabled based on OTP programming. External hardware, especially booting hosts, may monitor the HWAIT signal to determine

Fiber optic transceiver (FOT) connections:

- Keep the traces between the ADSP-BF549 processor and the FOT as short as possible.
- The receive data trace connecting the FOT receive data output pin to the ADSP-BF549 PH6/MRX input pin should have a 0 Ω series termination resistor placed close to the FOT receive data output pin. Typically, the edge rate of the FOT receive data signal driven by the FOT is very slow, and further degradation of the edge rate is not desirable.
- The transmit data trace connecting the ADSP-BF549 PH5/MTX output pin to the FOT transmit data input pin should have a 27 Ω series termination resistor placed close to the ADSP-BF549 PH5/MTX pin.
- The receive data trace and the transmit data trace between the ADSP-BF549 processor and the FOT should not be routed close to each other in parallel over long distances to avoid crosstalk.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF54x Blackfin processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on www.analog.com:

- *ADSP-BF54x Blackfin Processor Hardware Reference, Volume 1 and Volume 2*
- *Blackfin Processor Programming Reference*
- *ADSP-BF542/BF544/BF547/BF548/BF549 Blackfin Anomaly List*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

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Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
DDR Memory Interface			
DA0–12	O	DDR Address Bus	D
DBA0–1	O	DDR Bank Active Strobe	D
DQ0–15	I/O	DDR Data Bus	D
DQS0–1	I/O	DDR Data Strobe	D
DQM0–1	O	DDR Data Mask for Reads and Writes	D
DCLK0–1	O	DDR Output Clock	D
$\overline{\text{DCLK0–1}}$	O	DDR Complementary Output Clock	D
$\overline{\text{DCS0–1}}$	O	DDR Chip Selects	D
DCLKE[9]	O	DDR Clock Enable (Requires a pull-down if hibernate with DDR self-refresh is used.)	D
$\overline{\text{DRAS}}$	O	DDR Row Address Strobe	D
$\overline{\text{DCAS}}$	O	DDR Column Address Strobe	D
$\overline{\text{DWE}}$	O	DDR Write Enable	D
DDR_VREF	I	DDR Voltage Reference	
DDR_VSSR	I	DDR Voltage Reference Shield (Must be connected to GND.)	
Asynchronous Memory Interface			
A1-3	O	Address Bus for Async and ATAPI Addresses	A
D0-15/ND_D0-15/ATAPI_D0-15	I/O	Data Bus for Async, NAND and ATAPI Accesses	A
$\overline{\text{AMS0–3}}$	O	Bank Selects (Pull high with a resistor when used as chip select. Require pull-ups if hibernate is used.)	A
$\overline{\text{ABE0}}$ / *ND_CLE*	O	Byte Enables: Data Masks for Asynchronous Access / *NAND Command Latch Enable*	A
$\overline{\text{ABE1}}$ / *ND_ALE*	O	Byte Enables: Data Masks for Asynchronous Access / *NAND Address Latch Enable*	A
$\overline{\text{AOE}}$ / *NR_ADV*	O	Output Enable / *NOR Address Data Valid*	A
$\overline{\text{ARE}}$	O	Read Enable / *NOR Output Enable*	A
$\overline{\text{AWE}}$	O	Write Enable	A
ATAPI Controller Pins			
$\overline{\text{ATAPI\_PDIAG}}$	I	Determines if an 80-pin cable is connected to the host. (Pull high or low when unused.)	
High Speed USB OTG Pins			
USB_DP	I/O	USB D+ Pin (Pull low when unused.)	
USB_DM	I/O	USB D– Pin (Pull low when unused.)	
USB_XI	C	Clock XTAL Input (Pull high or low when unused.)	
USB_XO	C	Clock XTAL Output (Leave unconnected when unused.)	
USB_ID[10]	I	USB OTG ID Pin (Pull high when unused.)	

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
USB_VBUS[11]	I/O	USB VBUS Pin (Pull high or low when unused.)	
USB_VREF	A	USB Voltage Reference (Connect to GND through a 0.1 µF capacitor or leave unconnected when not used.)	
USB_RSET	A	USB Resistance Set (Connect to GND through an unpopulated resistor pad.)	
MXVR (MOST) Interface			
MFS	O	MXVR Frame Sync (Leave unconnected when unused.)	C
MLF_P	A	MXVR Loop Filter Plus (Leave unconnected when unused.)	
MLF_M	A	MXVR Loop Filter Minus (Leave unconnected when unused.)	
MXI	C	MXVR Crystal Input (Pull high or low when unused.)	
MXO	C	MXVR Crystal Output (Pull high or low when unused.)	
Mode Control Pins			
BMODE0–3	I	Boot Mode Strap 0–3	
JTAG Port Pins			
TDI	I	JTAG Serial Data In	
TDO	O	JTAG Serial Data Out	C
$\overline{\text{TRST}}$	I	JTAG Reset (Pull low when unused.)	
TMS	I	JTAG Mode Select	
TCK	I	JTAG Clock	
$\overline{\text{EMU}}$	O	Emulation Output	C
Voltage Regulator			
$VR_{OUT}0$, $VR_{OUT}1$	O	External FET/BJT Drivers (Always connect together to reduce signal impedance.)	
Real Time Clock			
RTXO	C	RTC Crystal Output (Leave unconnected when unused. Does not three-state during hibernate.)	
RTXI	C	RTC Crystal Input (Pull high or low when unused.)	
Clock (PLL) Pins			
CLKIN	C	Clock/Crystal Input	
CLKOUT	O	Clock Output	B
XTAL	C	Crystal Output (If CLKBUF is enabled, does not three-state during hibernate.)	
CLKBUF	O	Buffered Oscillator Output (If enabled, does not three-state during hibernate.)	C
EXT_WAKE	O	External Wakeup from Hibernate Output (Does not three-state during hibernate.)	A
$\overline{\text{RESET}}$	I	Reset	
$\overline{\text{NMI}}$	I	Non-maskable Interrupt (Pull high when unused.)	

Table 18. Activity Scaling Factors[1]

I_{DDINT} Power Vector	Activity Scaling Factor (ASF)
$I_{DD-PEAK}$	1.29
$I_{DD-HIGH}$	1.24
I_{DD-TYP}	1.00
I_{DD-APP}	0.87
I_{DD-NOP}	0.74
$I_{DD-IDLE}$	0.47

[1] See *Estimating Power for ADSP-BF534/BF536/BF537 Blackfin Processors (EE-297)*. The power vector information also applies to the ADSP-BF542/ADSP-BF544/ADSP-BF547/ADSP-BF548/ADSP-BF549 processors.

Table 19. Dynamic Current in CCLK Domain (mA, with ASF = 1.0)[1]

	Voltage (V_{DDINT})[2]												
f_{CCLK} (MHz)[2]	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.38 V	1.40 V	1.43 V
100	29.7	31.6	33.9	35.7	37.9	40.5	42.9	45.5	48.2	50.8	52.0	53.5	54.6
200	55.3	58.9	62.5	66.0	70.0	74.0	78.3	82.5	86.7	91.3	93.3	95.6	97.6
300	80.8	85.8	91.0	96.0	101.3	107.0	112.8	118.7	124.6	130.9	133.8	137.0	140.0
400	N/A	112.2	119.4	125.5	132.4	139.6	146.9	154.6	162.3	170.0	173.8	177.8	181.6
500	N/A	N/A	N/A	N/A	N/A	171.9	180.6	189.9	199.1	205.7	210.3	213.0	217.6
533	N/A	N/A	N/A	N/A	N/A	N/A	191.9	201.6	211.5	218.0	222.8	225.7	230.5
600	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	233.1	241.4	246.7	252.7	258.1

[1] The values are not guaranteed as stand-alone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 36.
[2] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 34.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 9 and Table 23 provides information related to specific product features. For a complete listing of product offerings, see the Ordering Guide on Page 101.

Figure 9. Product Information on Package

Table 23. Package Information

Brand Key	Description
BF54x	x = 2, 4, 7, 8 or 9
(M)	Mobile DDR Indicator (Optional)
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part (Optional)
cc	See Ordering Guide
vvvvvv.x-q	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

Asynchronous Memory Read Cycle Timing

Table 27 and Table 28 on Page 45 and Figure 13 and Figure 14 on Page 45 describe asynchronous memory read cycle operations for synchronous and for asynchronous ARDY.

Table 27. Asynchronous Memory Read Cycle Timing with Synchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA15–0 Setup Before CLKOUT	5.0		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
t_{SARDY}	ARDY Setup Before the Falling Edge of CLKOUT	5.0		ns
t_{HARDY}	ARDY Hold After the Falling Edge of CLKOUT	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT[1]	0.3		ns

[1] Output pins include $\overline{AMS3–0}$, $\overline{ABE1–0}$, ADDR19–1, $\overline{AOE}$, and $\overline{ARE}$.

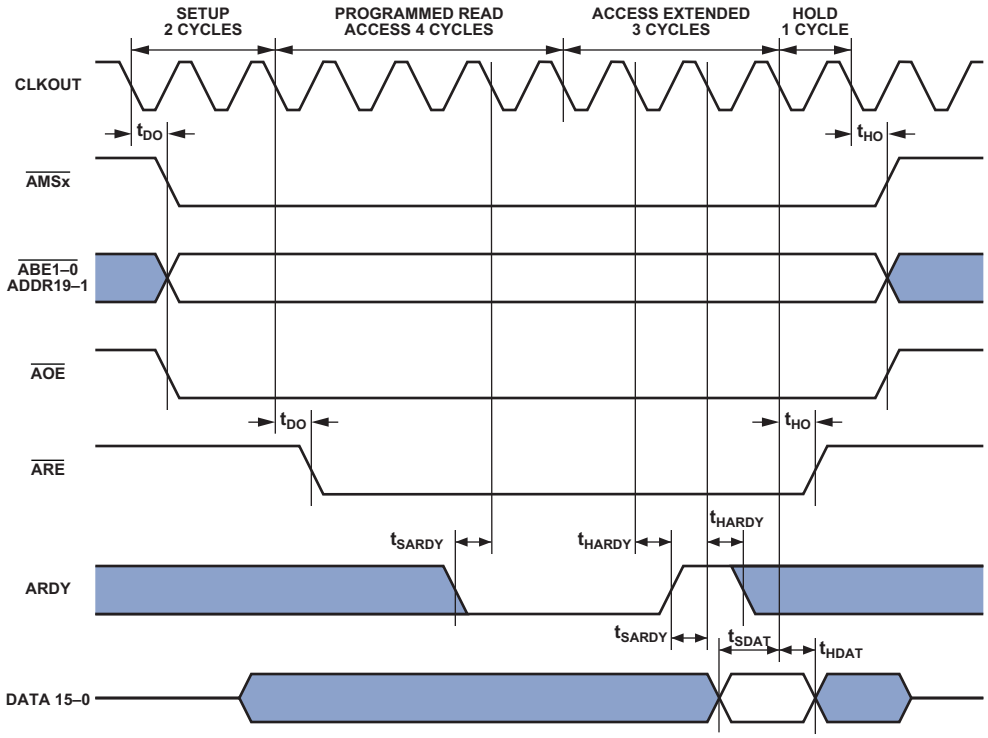

Figure 13. Asynchronous Memory Read Cycle Timing with Synchronous ARDY

Table 35. External Port Bus Request and Grant Cycle Timing with Asynchronous $\overline{BR}$

Parameter		Min	Max	Unit
Timing Requirement				
t_{WBR}	$\overline{BR}$ Pulsewidth	$2 \times t_{SCLK}$		ns
Switching Characteristics				
t_{SD}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}/\overline{AWE}$ Disable		5.0	ns
t_{SE}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}/\overline{AWE}$ Enable		5.0	ns
t_{DBG}	CLKOUT Low to $\overline{BG}$ Asserted Output Delay		4.0	ns
t_{EBG}	CLKOUT Low to $\overline{BG}$ Deasserted Output Hold		4.0	ns
t_{DBH}	CLKOUT Low to $\overline{BGH}$ Asserted Output Delay		3.6	ns
t_{EBH}	CLKOUT Low to $\overline{BGH}$ Deasserted Output Hold		3.6	ns

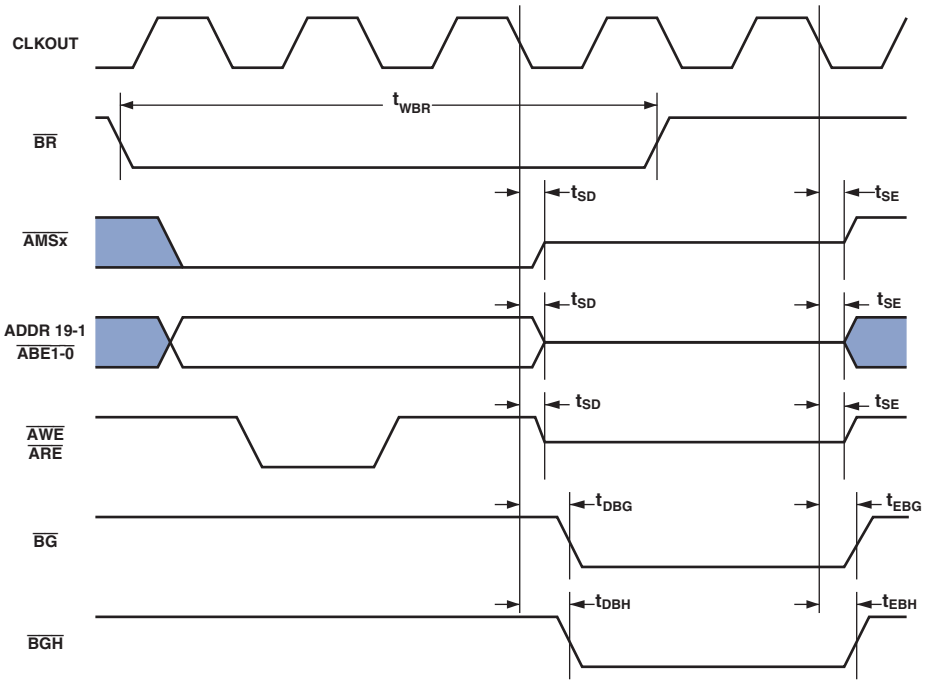

Figure 22. External Port Bus Request and Grant Cycle Timing with Asynchronous $\overline{BR}$

NAND Flash Controller Interface Timing

Table 36 and Figure 23 on Page 54 through Figure 27 on Page 56 describe NAND flash controller interface operations. In the figures, ND_DATA is ND_D0–D15.

Table 36. NAND Flash Controller Interface Timing

Parameter		Min	Max	Unit
Write Cycle				
Switching Characteristics				
t_{CWL}	$\overline{ND\_CE}$ Setup Time to $\overline{AWE}$ Low	$1.0 \times t_{SCLK} - 4$		ns
t_{CH}	$\overline{ND\_CE}$ Hold Time from $\overline{AWE}$ High	$3.0 \times t_{SCLK} - 4$		ns
t_{CLEWL}	ND_CLE Setup Time High to $\overline{AWE}$ Low	0.0		ns
t_{CLH}	ND_CLE Hold Time from $\overline{AWE}$ High	$2.5 \times t_{SCLK} - 4$		ns
t_{ALEWL}	ND_ALE Setup Time Low to $\overline{AWE}$ Low	0.0		ns
t_{ALH}	ND_ALE Hold Time from $\overline{AWE}$ High	$2.5 \times t_{SCLK} - 4$		ns
t_{WP}[1]	$\overline{AWE}$ Low to $\overline{AWE}$ High	$(WR\_DLY + 1.0) \times t_{SCLK} - 4$		ns
t_{WHWL}	$\overline{AWE}$ High to $\overline{AWE}$ Low	$4.0 \times t_{SCLK} - 4$		ns
t_{WC}[1]	$\overline{AWE}$ Low to $\overline{AWE}$ Low	$(WR\_DLY + 5.0) \times t_{SCLK} - 4$		ns
t_{DWS}[1]	Data Setup Time for a Write Access	$(WR\_DLY + 1.5) \times t_{SCLK} - 4$		ns
t_{DWH}	Data Hold Time for a Write Access	$2.5 \times t_{SCLK} - 4$		ns
Read Cycle				
Switching Characteristics				
t_{CRL}	$\overline{ND\_CE}$ Setup Time to $\overline{ARE}$ Low	$1.0 \times t_{SCLK} - 4$		ns
t_{CRH}	$\overline{ND\_CE}$ Hold Time from $\overline{ARE}$ High	$3.0 \times t_{SCLK} - 4$		ns
t_{RP}[1]	$\overline{ARE}$ Low to $\overline{ARE}$ High	$(RD\_DLY + 1.0) \times t_{SCLK} - 4$		ns
t_{RHRL}	$\overline{ARE}$ High to $\overline{ARE}$ Low	$4.0 \times t_{SCLK} - 4$		ns
t_{RC}[1]	$\overline{ARE}$ Low to $\overline{ARE}$ Low	$(RD\_DLY + 5.0) \times t_{SCLK} - 4$		ns
Timing Requirements				
t_{DRS}	Data Setup Time for a Read Transaction	8.0		ns
t_{DRH}	Data Hold Time for a Read Transaction	0.0		ns
Write Followed by Read				
Switching Characteristic				
t_{WHRL}	$\overline{AWE}$ High to $\overline{ARE}$ Low	$5.0 \times t_{SCLK} - 4$		ns

[1] WR_DLY and RD_DLY are defined in the NFC_CTL register.

Timer Clock Timing

Table 47 and Figure 41 describe timer clock timing.

Table 47. Timer Clock Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TODP}	Timer Output Update Delay After PPI_CLK High		15	ns

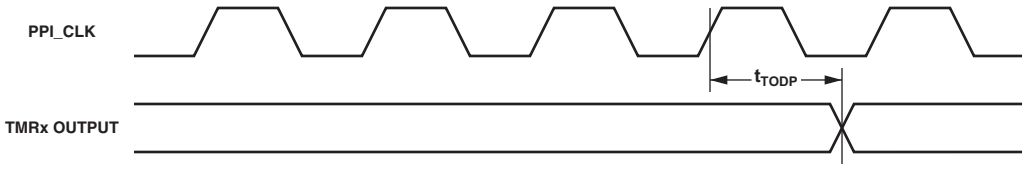

Figure 41. Timer Clock Timing

Timer Cycle Timing

Table 48 and Figure 42 describe timer expired operations. The input signal is asynchronous in "width capture mode" and "external clock mode" and has an absolute maximum input frequency of (f_{SCLK}/2) MHz.

Table 48. Timer Cycle Timing

Parameter		Min	Max	Unit
Timing Characteristics				
t_{WL}	Timer Pulse Width Input Low[1]	1× t_{SCLK}		ns
t_{WH}	Timer Pulse Width Input High[1]	1× t_{SCLK}		ns
t_{TIS}	Timer Input Setup Time Before CLKOUT Low[2]	6.5		ns
t_{TIH}	Timer Input Hold Time After CLKOUT Low[2]	–1		ns
Switching Characteristics				
t_{HTO}	Timer Pulse Width Output	1× t_{SCLK}	(2^{32} – 1) × t_{SCLK}	ns
t_{TOD}	Timer Output Delay After CLKOUT High		6	ns

[1] The minimum pulse widths apply for TMRx signals in width capture and external clock modes.
[2] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize timer flag inputs.

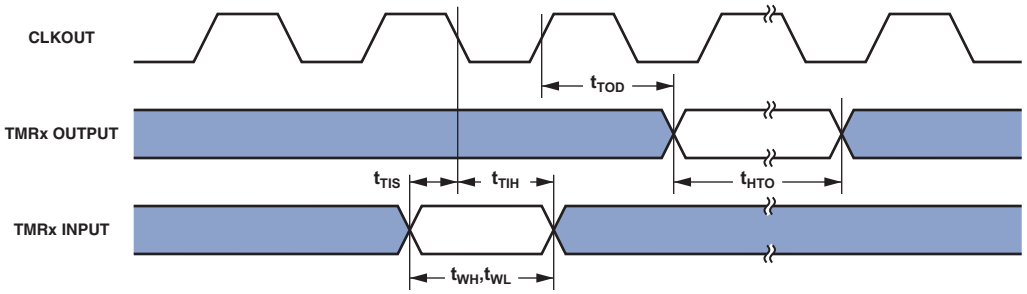

Figure 42. Timer Cycle Timing

MXVR Timing

Table 52 and Table 53 describe the MXVR timing requirements.
Figure 5 illustrates the MOST connection.

Table 52. MXVR Timing—MXI Center Frequency Requirements

Parameter		Fs = 38 kHz	Fs = 44.1 kHz	Fs = 48 kHz	Unit
f_{MXI_256}	MXI Center Frequency (256 Fs)	9.728	11.2896	12.288	MHz
f_{MXI_384}	MXI Center Frequency (384 Fs)	14.592	16.9344	18.432	MHz
f_{MXI_512}	MXI Center Frequency (512 Fs)	19.456	22.5792	24.576	MHz
f_{MXI_1024}	MXI Center Frequency (1024 Fs)	38.912	45.1584	49.152	MHz

Table 53. MXVR Timing— MXI Clock Requirements

Parameter		Min	Max	Unit
Timing Requirements				
FS_{MXI}	MXI Clock Frequency Stability	–50	+50	ppm
FT_{MXI}	MXI Frequency Tolerance Over Temperature	–300	+300	ppm
DC_{MXI}	MXI Clock Duty Cycle	+40	+60	%

ATA/ATAPI-6 Interface Timing

The following tables and figures specify ATAPI timing parameters. For detailed parameter descriptions, refer to the ATAPI specification (ANSI INCITS 361-2002). Table 58 to Table 61 include ATAPI timing parameter equations. System designers should use these equations along with the parameters provided in Table 56 and Table 57. ATAPI timing control registers should be programmed such that ANSI INCITS 361-2002 specifications are met for the desired transfer type and mode.

Table 56. ATA/ATAPI-6 Timing Parameters

Parameter		Min	Max	Unit
t_{SK1}	Difference in output delay after CLKOUT for ATAPI output pins[1]		6	ns
t_{OD}	Output delay after CLKOUT for outputs[1]		12	ns
t_{SUD}	ATAPI_D0-15 or ATAPI_D0-15A Setup Before CLKOUT	6		ns
t_{SUI}	$\overline{\text{ATAPI\_IORDY}}$ Setup Before CLKOUT	6		ns
t_{SUDU}	ATAPI_D0-15 or ATAPI_D0-15A Setup Before $\overline{\text{ATAPI\_IORDY}}$ (UDMA-in only)	2		ns
t_{HDU}	ATAPI_D0-15 or ATAPI_D0-15A Hold After $\overline{\text{ATAPI\_IORDY}}$ (UDMA-in only)	2.6		ns

[1] ATAPI output pins include $\overline{\text{ATAPI\_CS0}}$, $\overline{\text{ATAPI\_CS1}}$, A1-3, $\overline{\text{ATAPI\_DIOR}}$, $\overline{\text{ATAPI\_DIOW}}$, $\overline{\text{ATAPI\_DMACK}}$, ATAPI_D0-15, ATAPI_A0-2A, and ATAPI_D0-15A.

Table 57. ATA/ATAPI-6 System Timing Parameters

Parameter		Source
t_{SK2}	Maximum difference in board propagation delay between any 2 ATAPI output pins[1]	System Design
t_{BD}	Maximum board propagation delay.	System Design
t_{SK3}	Maximum difference in board propagation delay during a read between $\overline{\text{ATAPI\_IORDY}}$ and ATAPI_D0-15/ATAPI_D0-15A.	System Design
t_{SK4}	Maximum difference in ATAPI cable propagation delay between output pin group A and output pin group B[2]	ATAPI Cable Specification
t_{CDD}	ATAPI cable propagation delay for ATAPI_D0-15 and ATAPI_D0-15A signals.	ATAPI Cable Specification
t_{CDC}	ATAPI cable propagation delay for $\overline{\text{ATAPI\_DIOR}}$, $\overline{\text{ATAPI\_DIOW}}$, $\overline{\text{ATAPI\_IORDY}}$, and $\overline{\text{ATAPI\_DMACK}}$ signals.	ATAPI Cable Specification

[1] ATAPI output pins include $\overline{\text{ATAPI\_CS0}}$, $\overline{\text{ATAPI\_CS1}}$, A1-3, $\overline{\text{ATAPI\_DIOR}}$, $\overline{\text{ATAPI\_DIOW}}$, $\overline{\text{ATAPI\_DMACK}}$, ATAPI_D0-15, ATAPI_A0-2A, and ATAPI_D0-15A.
[2] Output pin group A includes $\overline{\text{ATAPI\_DIOR}}$, $\overline{\text{ATAPI\_DIOW}}$, and $\overline{\text{ATAPI\_DMACK}}$. Output pin group B includes $\overline{\text{ATAPI\_CS0}}$, $\overline{\text{ATAPI\_CS1}}$, A1-3, ATAPI_D0-15, ATAPI_A0-2A, and ATAPI_D0-15A.

In Figure 57 and Figure 58 an alternate ATAPI_D0–15 port bus is ATAPI_D0–15A.

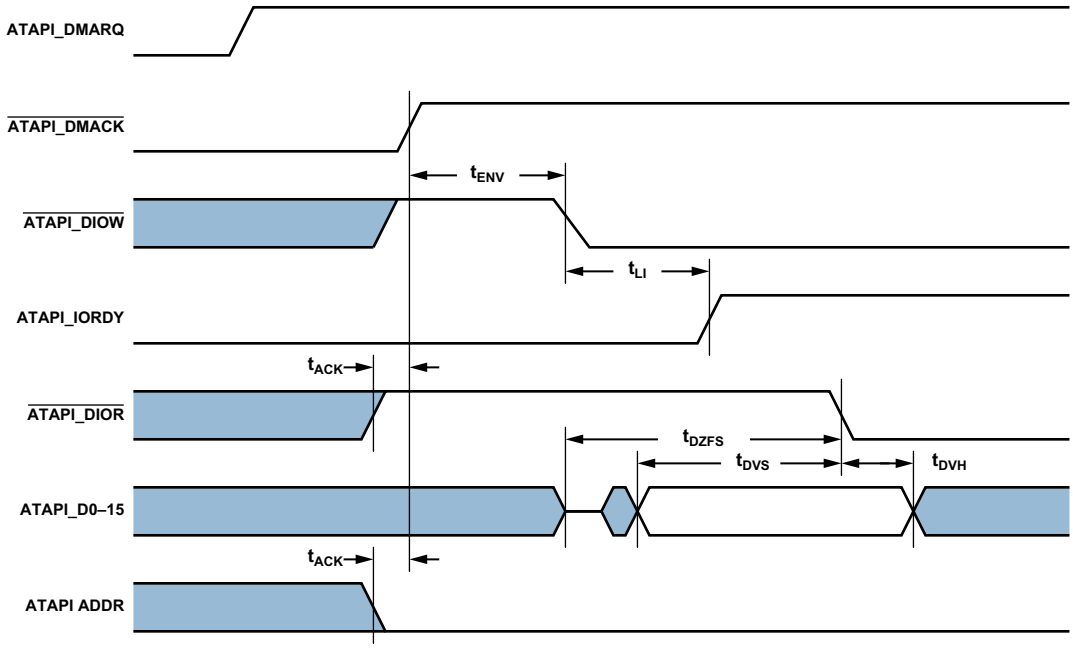

Figure 57. Initiating an Ultra DMA Data-Out Burst

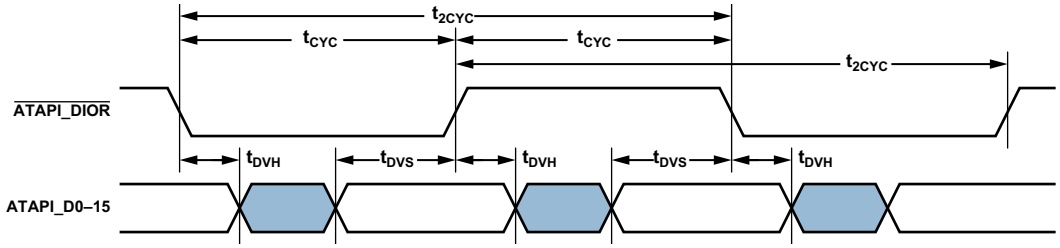

Figure 58. Sustained Ultra DMA Data-Out Burst

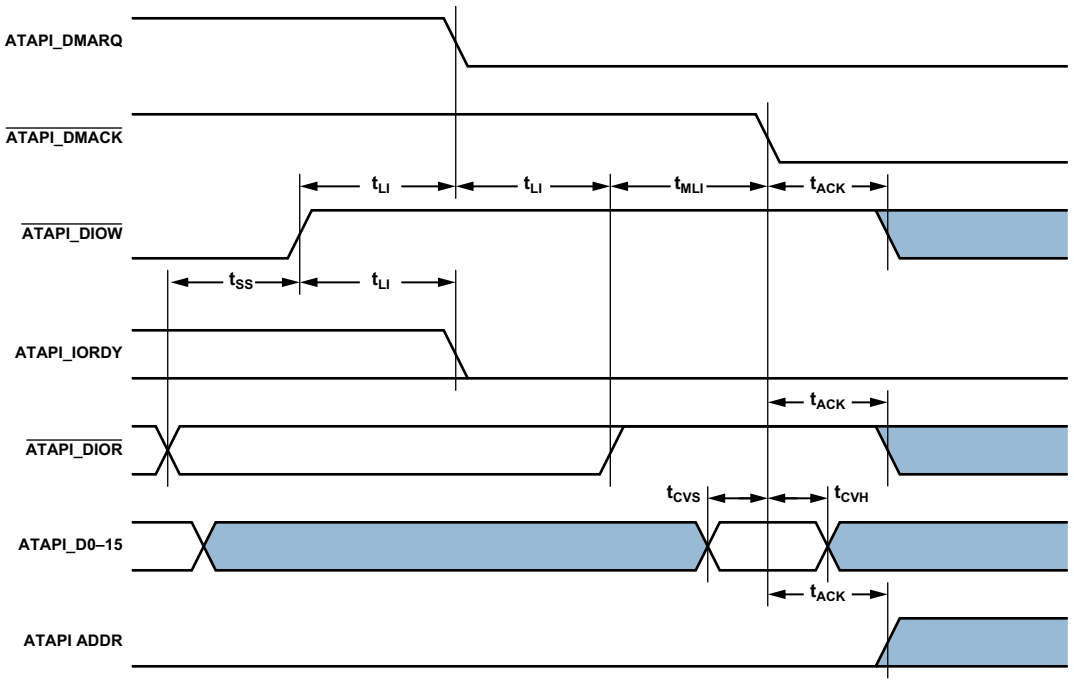

Figure 59. Host terminating an Ultra DMA Data-Out Burst

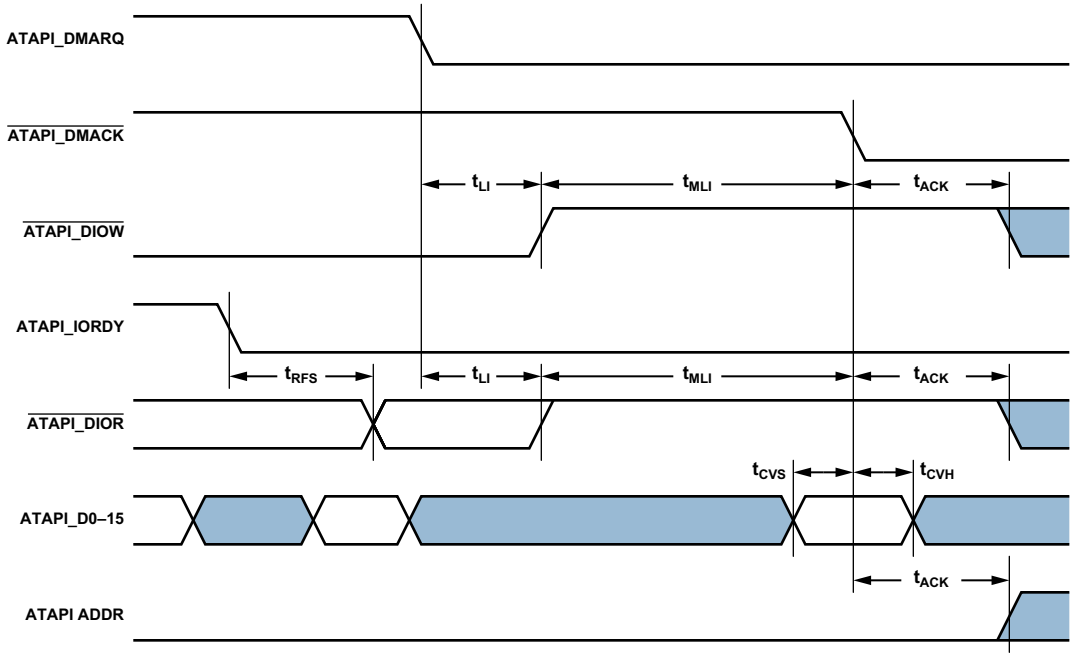

Figure 60. Device Terminating an Ultra DMA Data-Out Burst

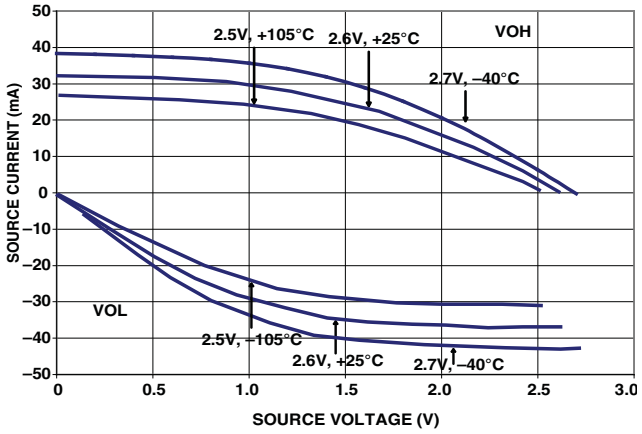

Figure 68. Drive Current D (DDR SDRAM)

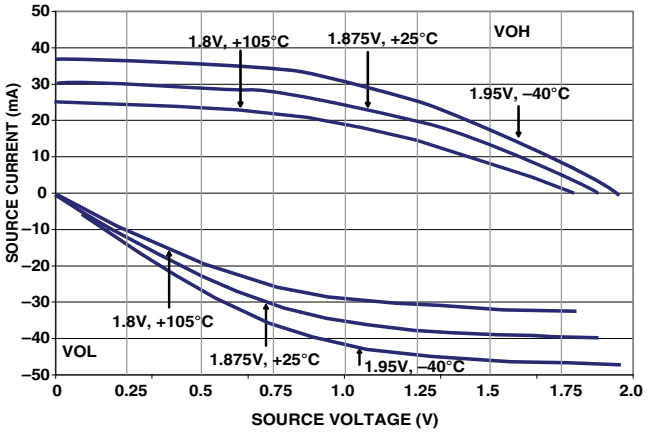

Figure 69. Drive Current D (Mobile DDR SDRAM)

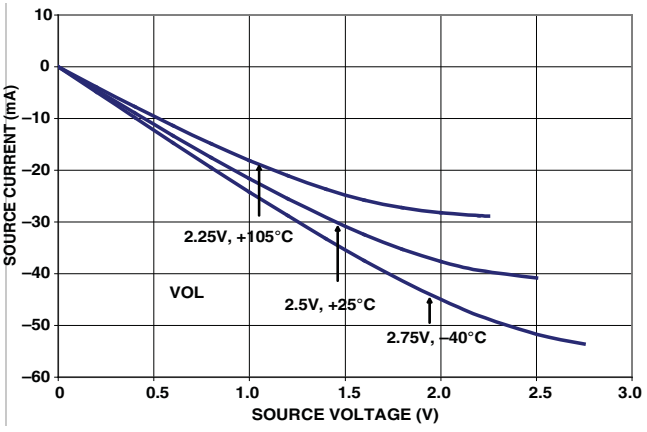

Figure 70. Drive Current E (Low V_{DDEXT})

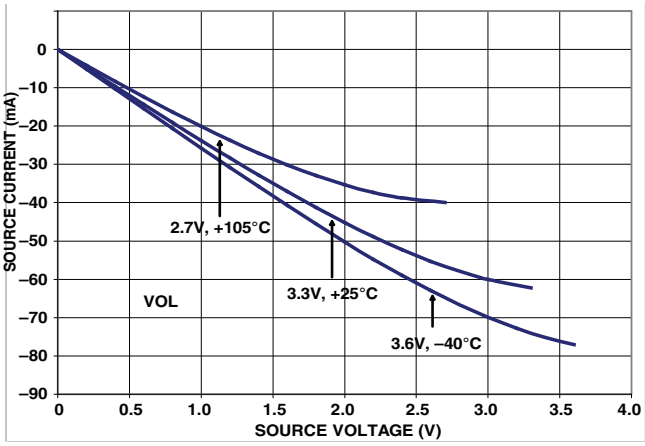

Figure 71. Drive Current E (High V_{DDEXT})

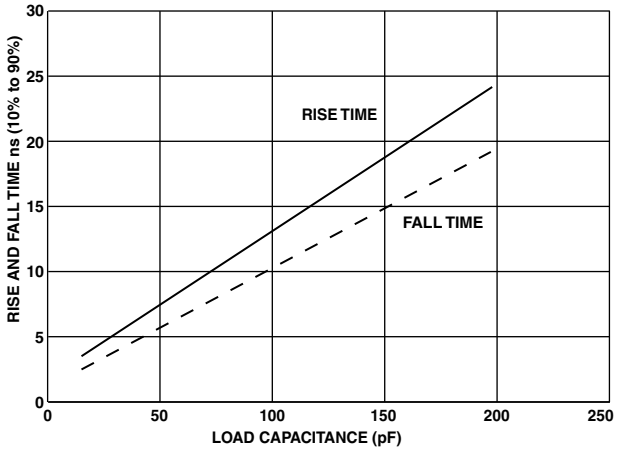

Figure 79. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 2.25 V

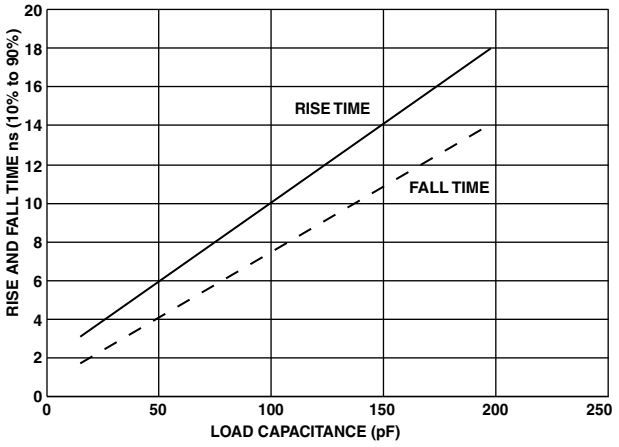

Figure 80. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 3.65 V

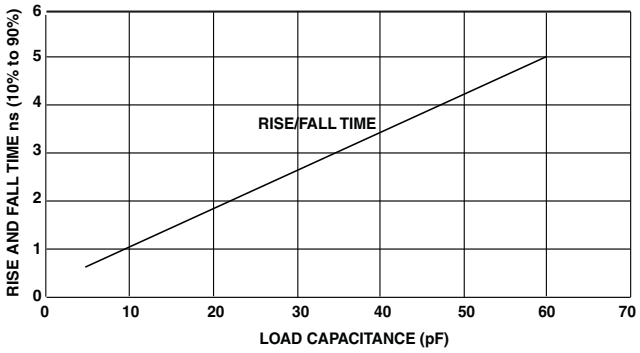

Figure 81. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D DDR SDRAM at V_{DDDDR} = 2.5 V

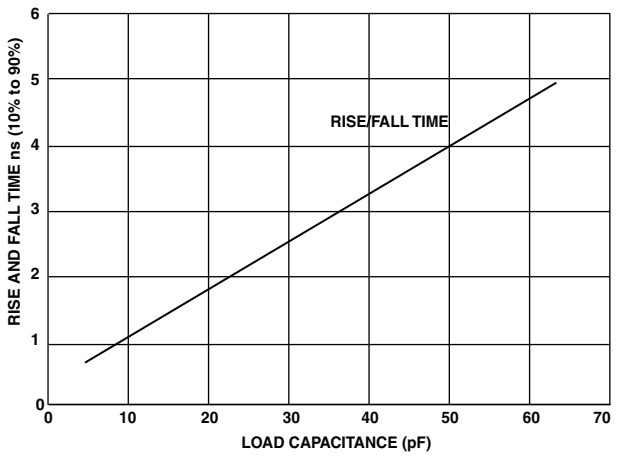

Figure 82. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D DDR SDRAM at V_{DDDDR} = 2.7 V

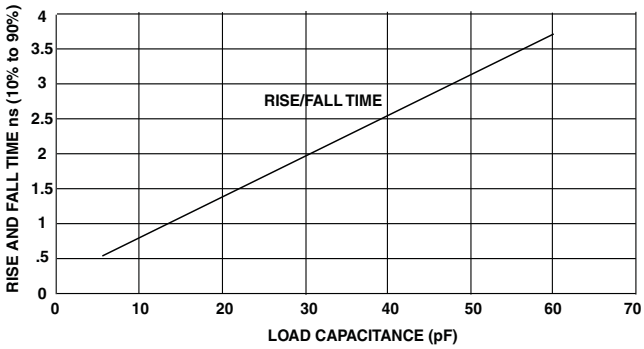

Figure 83. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D Mobile DDR SDRAM at V_{DDDDR} = 1.8 V

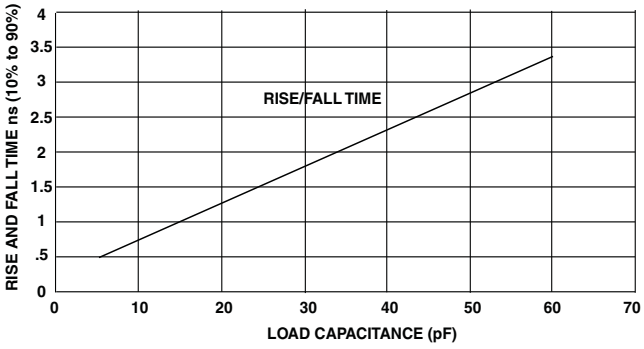

Figure 84. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D Mobile DDR SDRAM at V_{DDDDR} = 1.95 V

OUTLINE DIMENSIONS

Dimensions for the 17 mm × 17 mm CSP_BGA package in Figure 88 are shown in millimeters.

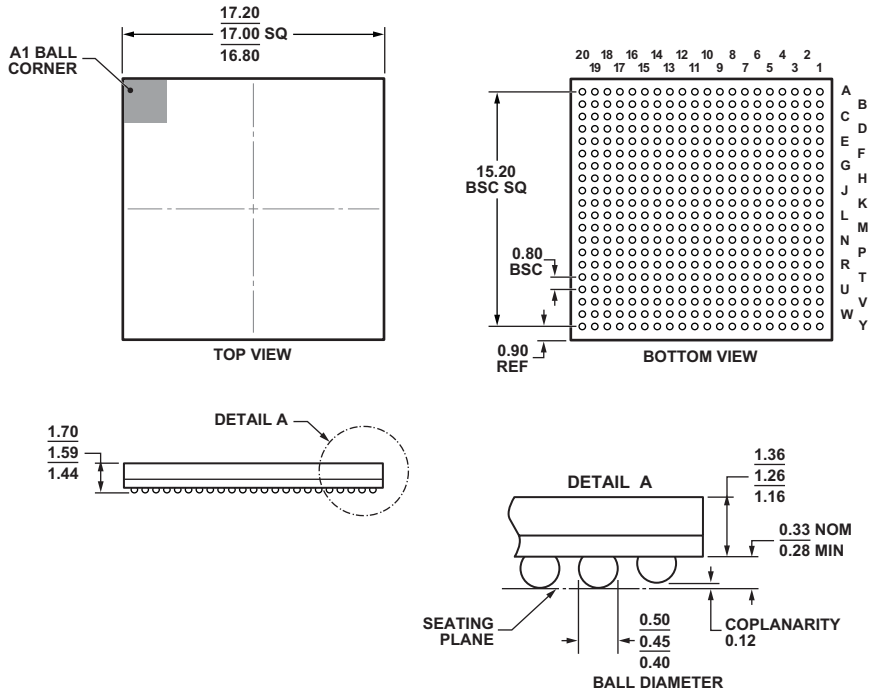

Figure 88. 400-Ball, 17 mm × 17 mm CSP_BGA (Chip Scale Package Ball Grid Array) (BC-400-1)

SURFACE-MOUNT DESIGN

Table 67 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Table 67. BGA Data for Use with Surface-Mount Design

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
400-Ball CSP_BGA (Chip Scale Package Ball Grid Array) BC-400-1	Solder Mask Defined	0.40 mm Diameter	0.50 mm Diameter