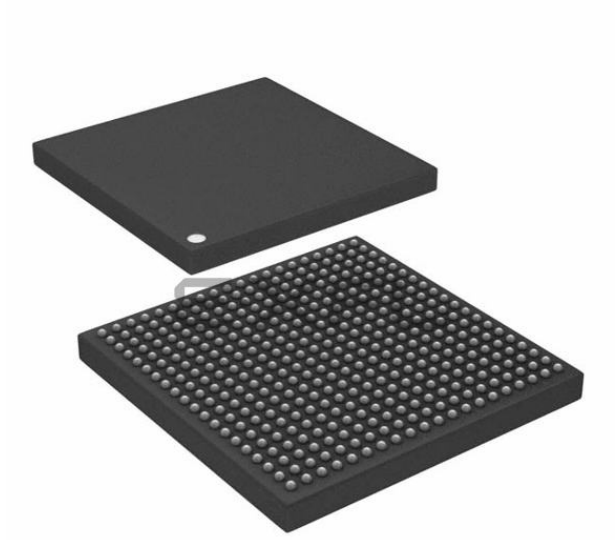

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART, USB
Clock Rate	533MHz
Non-Volatile Memory	External
On-Chip RAM	132kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf542bbcz-5a

For large page NAND flash devices, the 4-byte electronic signature is read in order to configure the kernel for booting. This allows support for multiple large page devices. The fourth byte of the electronic signature must comply with the specifications in Table 9.

Any configuration from Table 9 that also complies with the command set listed below is directly supported by the boot kernel. There are no restrictions on the page size or block size as imposed by the small-page boot kernel.

Table 9. Byte 4 Electronic Signature Specification

Page Size (excluding spare area)	D1:D0	00	1K bytes
		01	2K bytes
		10	4K bytes
		11	8K bytes
Spare Area Size	D2	0	8 bytes/512 bytes
		1	16 bytes/512 bytes
Block Size (excluding spare area)	D5:4	00	64K bytes
		01	128K bytes
		10	256K bytes
		11	512K bytes
Bus Width	D6	0	x8
		1	x16
Not Used for Configuration	D3, D7		

Large page devices must support the following command set:

Reset: 0xFF
Read Electronic Signature: 0x90
Read: 0x00, 0x30 (confirm command)

Large page devices must not support or react to NAND flash command 0x50. This is a small page NAND flash command used for device auto detection.

By default, the boot kernel will always issue five address cycles; therefore, if a large page device requires only four cycles, the device must be capable of ignoring the additional address cycle.

16-bit NAND flash memory devices must only support the issuing of command and address cycles via the lower eight bits of the data bus. Devices that use the full 16-bit bus for command and address cycles are not supported.

- Boot from OTP memory (BMODE = 0xB)—This provides a standalone booting method. The boot stream is loaded from on-chip OTP memory. By default, the boot stream is expected to start from OTP page 0x40 and can occupy all public OTP memory up to page 0xDF (2560 bytes). Since the start page is programmable, the maximum size of the boot stream can be extended to 3072 bytes.
- Boot from 16-bit host DMA (BMODE = 0xE)—In this mode, the host DMA port is configured in 16-bit acknowledge mode with little endian data format. Unlike other modes, the host is responsible for interpreting the boot stream. It writes data blocks individually into the host DMA port. Before configuring the DMA settings for each block, the host may either poll the ALLOW_CONFIG bit in HOST_STATUS or wait to be interrupted by the HWAIT signal. When using HWAIT, the host must still check ALLOW_CONFIG at least once before beginning to configure the host DMA port. After completing the configuration, the host is required to poll the READY bit in HOST_STATUS before beginning to transfer data. When the host sends an HIRQ control command, the boot kernel issues a CALL instruction to address 0xFFA0 0000. It is the host's responsibility to ensure valid code has been placed at this address. The routine at address 0xFFA0 0000 can be a simple initialization routine to configure internal resources, such as the SDRAM controller, which then returns using an RTS instruction. The routine may also be the final application, which will never return to the boot kernel.
- Boot from 8-bit host DMA (BMODE = 0xF)—In this mode, the host DMA port is configured in 8-bit interrupt mode with little endian data format. Unlike other modes, the host is responsible for interpreting the boot stream. It writes data blocks individually to the host DMA port. Before configuring the DMA settings for each block, the host may either poll the ALLOW_CONFIG bit in HOST_STATUS or wait to be interrupted by the HWAIT signal. When using HWAIT, the host must still check ALLOW_CONFIG at least once before beginning to configure the host DMA port. The host will receive an interrupt from the HOST_ACK signal every time it is allowed to send the next FIFO depth's worth (sixteen 32-bit words) of information. When the host sends an HIRQ control command, the boot kernel issues a CALL instruction to address 0xFFA0 0000. It is the host's responsibility to ensure valid code has been placed at this address. The routine at address 0xFFA0 0000 can be a simple initialization routine to configure internal resources, such as the SDRAM controller, which then returns using an RTS instruction. The routine may also be the final application, which will never return to the boot kernel.

For each of the boot modes, a 16-byte header is first read from an external memory device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks may be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the address stored in the EVT1 register.

Prior to booting, the pre-boot routine interrogates the OTP memory. Individual boot modes can be customized or disabled based on OTP programming. External hardware, especially booting hosts, may monitor the HWAIT signal to determine

PIN DESCRIPTIONS

The ADSP-BF54x processor pin multiplexing scheme is shown in Table 10.

Table 10. Pin Multiplexing

Primary Pin Function (Number of Pins)[1, 2]	First Peripheral Function	Second Peripheral Function	Third Peripheral Function	Fourth Peripheral Function	Interrupt Capability
Port A					
GPIO (16 pins)	SPORT2 (8 pins)	TMR4 (1 pin)	TACI7 (1 pin) TACLK7–0 (8 pins)		Interrupts (16 pins)
		TMR5 (1 pin)			
	SPORT3 (8 pins)	TMR6 (1 pin)			
		TMR7 (1 pin)			
Port B					
GPIO (15 pins)	TWI1 (2 pins) UART2 or 3 CTL (2 pins) UART2 (2 pins) UART3 (2 pins)		TACI2-3 (2 pins)		Interrupts (15 pins)
	$\overline{\text{SPI2 SEL1-3}}$ (3 pins)	TMR0–2 (3 pins)			
	SPI2 (4 pins)	TMR3 (1 pin)	HWAIT (1 pin)		
Port C					
GPIO (16 pins)	SPORT0 (8 pins)	MXVR MMCLK, MBCLK (2 pins)			Interrupts (8 pins)[3]
	SDH (6 pins)				Interrupts (8 pins)
Port D					
GPIO (16 pins)	PPI1 D0–15 (16 pins)	Host D0–15 (16 pins)	SPORT1 (8 pins)	PPI0 D18– 23 (6 pins)	Interrupts (8 pins)
			PPI2 D0–7 (8 pins)	Keypad Row 0–3 Col 0–3 (8 pins)	Interrupts (8 pins)
Port E					
GPIO (16 pins)	SPI0 (7 pins)	Keypad Row 4–6 Col 4–7 (7 pins)	TACI0 (1 pin)		Interrupts (8 pins)
	UART0 TX (1 pin)	Keypad R7 (1 pin)			
	UART0 RX (1 pin) UART0 or 1 CTL (2 pins) PPI1 CLK,FS (3 pins) TWI0 (2 pins)				Interrupts (8 pins)
Port F					
GPIO (16 pins)	PPI0 D0–15 (16 pins)	ATAPI D0-15A			Interrupts (8 pins) Interrupts (8 pins)
Port G					
GPIO (16 pins)	PPI0 CLK,FS (3 pins) DATA 16–17 (2 pins)	TMRCLK (1 pin)			Interrupts (8 pins)
		ATAPI A0-2A			
	$\overline{\text{SPI1 SEL1–3}}$ (3 pins)	Host CTL (3 pins)	PPI2 CLK,FS (3 pins)	CZM (1 pin)	
	SPI1 (4 pins)	MXVR $\overline{\text{MTXON}}$ (1 pin)	TACI4-5 (2 pins)		Interrupts (8 pins)
	CAN0 (2 pins)				
	CAN1 (2 pins)				

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
DDR Memory Interface			
DA0–12	O	DDR Address Bus	D
DBA0–1	O	DDR Bank Active Strobe	D
DQ0–15	I/O	DDR Data Bus	D
DQS0–1	I/O	DDR Data Strobe	D
DQM0–1	O	DDR Data Mask for Reads and Writes	D
DCLK0–1	O	DDR Output Clock	D
$\overline{\text{DCLK0–1}}$	O	DDR Complementary Output Clock	D
$\overline{\text{DCS0–1}}$	O	DDR Chip Selects	D
DCLKE[9]	O	DDR Clock Enable (Requires a pull-down if hibernate with DDR self-refresh is used.)	D
$\overline{\text{DRAS}}$	O	DDR Row Address Strobe	D
$\overline{\text{DCAS}}$	O	DDR Column Address Strobe	D
$\overline{\text{DWE}}$	O	DDR Write Enable	D
DDR_VREF	I	DDR Voltage Reference	
DDR_VSSR	I	DDR Voltage Reference Shield (Must be connected to GND.)	
Asynchronous Memory Interface			
A1-3	O	Address Bus for Async and ATAPI Addresses	A
D0-15/ND_D0-15/ATAPI_D0-15	I/O	Data Bus for Async, NAND and ATAPI Accesses	A
$\overline{\text{AMS0–3}}$	O	Bank Selects (Pull high with a resistor when used as chip select. Require pull-ups if hibernate is used.)	A
$\overline{\text{ABE0}}$ / *ND_CLE*	O	Byte Enables: Data Masks for Asynchronous Access / *NAND Command Latch Enable*	A
$\overline{\text{ABE1}}$ / *ND_ALE*	O	Byte Enables: Data Masks for Asynchronous Access / *NAND Address Latch Enable*	A
$\overline{\text{AOE}}$ / *NR_ADV*	O	Output Enable / *NOR Address Data Valid*	A
$\overline{\text{ARE}}$	O	Read Enable / *NOR Output Enable*	A
$\overline{\text{AWE}}$	O	Write Enable	A
ATAPI Controller Pins			
$\overline{\text{ATAPI\_PDIAG}}$	I	Determines if an 80-pin cable is connected to the host. (Pull high or low when unused.)	
High Speed USB OTG Pins			
USB_DP	I/O	USB D+ Pin (Pull low when unused.)	
USB_DM	I/O	USB D– Pin (Pull low when unused.)	
USB_XI	C	Clock XTAL Input (Pull high or low when unused.)	
USB_XO	C	Clock XTAL Output (Leave unconnected when unused.)	
USB_ID[10]	I	USB OTG ID Pin (Pull high when unused.)	

[10]Parameter value applies to USB_DP, USB_DM, and USB_VBUS pins. See Absolute Maximum Ratings on Page 40.
[11]Parameter value applies to all input and bidirectional pins, except PB1-0, PE15-14, PG15–11, and PH7-6.
[12]Parameter value applies to pins PG15–11 and PH7-6.
[13]Parameter value applies to pins PB1-0 and PE15-14. Consult the I^2C specification version 2.1 for the proper resistor value and other open drain pin electrical parameters.
[14]T_J must be in the range: 0°C < T_J < 55°C during OTP memory programming operations.

Table 12 and Table 15 describe the voltage/frequency requirements for the ADSP-BF54x Blackfin processors' clocks. Take care in selecting MSEL, SSEL, and CSEL ratios so as not to exceed the maximum core clock and system clock. Table 14 describes the phase-locked loop operating conditions.

Table 12. Core Clock (CCLK) Requirements—533 MHz and 600 MHz Speed Grade[1]

Parameter		Min V_{DDINT}	Internal Regulator Setting[2]	Max CCLK Frequency	Unit
f_{CCLK}	Core Clock Frequency	1.30 V	N/A[2]	600	MHz
		1.188 V	1.25 V	533	MHz
		1.14 V	1.20 V	500	MHz
		1.045 V	1.10 V	444	MHz
		0.95 V	1.00 V	400	MHz
		0.90 V	0.95 V	333	MHz

[1] See the Ordering Guide on Page 101.
[2] Use of an internal voltage regulator is not supported on automotive grade and 600 MHz speed grade models. Internal regulator setting should be used as recommended nominal V_{DDINT} for external regulator.

Table 13. Core Clock (CCLK) Requirements—400 MHz Speed Grade[1]

Parameter		Min V_{DDINT}	Internal Regulator Setting[2]	Max CCLK Frequency	Unit
f_{CCLK}	Core Clock Frequency	1.14 V	1.20 V	400	MHz
		1.045 V	1.10 V	364	MHz
		0.95 V	1.00 V	333	MHz
		0.90 V	0.95 V	300	MHz

[1] See Ordering Guide on Page 101.
[2] Use of an internal voltage regulator is not supported on automotive grade models. Internal regulator setting should be used as recommended nominal V_{DDINT} for external regulator.

Table 14. Phase-Locked Loop Operating Conditions

Parameter		Min	Max	Unit
f_{VCO}	Voltage Controlled Oscillator (VCO) Frequency	50	Maximum f_{CCLK}	MHz

Table 15. System Clock Requirements

Parameter	Condition	DDR SDRAM Models Max	Mobile DDR SDRAM Models Min	Mobile DDR SDRAM Models Max	Unit
f_{SCLK}	$V_{DDINT} \geq 1.14$ V[1], Non-extended temperature grades	133[2]	120[3]	133[2]	MHz
f_{SCLK}	$V_{DDINT} < 1.14$ V[1], Non-extended temperature grades	100	N/A[4]	N/A[4]	MHz
f_{SCLK}	$V_{DDINT} \geq 1.0$ V[1], Extended temperature grade	100	N/A	N/A	MHz

[1] f_{SCLK} must be less than or equal to f_{CCLK}.
[2] Rounded number. Actual test specification is SCLK period of 7.5 ns. See Table 25 on Page 43.
[3] Rounded number. Actual test specification is SCLK period of 8.33 ns.
[4] V_{DDINT} must be greater than or equal to 1.14 V for mobile DDR SDRAM models. See Operating Conditions on Page 34.

Table 18. Activity Scaling Factors[1]

I_{DDINT} Power Vector	Activity Scaling Factor (ASF)
$I_{DD-PEAK}$	1.29
$I_{DD-HIGH}$	1.24
I_{DD-TYP}	1.00
I_{DD-APP}	0.87
I_{DD-NOP}	0.74
$I_{DD-IDLE}$	0.47

[1] See *Estimating Power for ADSP-BF534/BF536/BF537 Blackfin Processors (EE-297)*. The power vector information also applies to the ADSP-BF542/ADSP-BF544/ADSP-BF547/ADSP-BF548/ADSP-BF549 processors.

Table 19. Dynamic Current in CCLK Domain (mA, with ASF = 1.0)[1]

	Voltage (V_{DDINT})[2]												
f_{CCLK} (MHz)[2]	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.38 V	1.40 V	1.43 V
100	29.7	31.6	33.9	35.7	37.9	40.5	42.9	45.5	48.2	50.8	52.0	53.5	54.6
200	55.3	58.9	62.5	66.0	70.0	74.0	78.3	82.5	86.7	91.3	93.3	95.6	97.6
300	80.8	85.8	91.0	96.0	101.3	107.0	112.8	118.7	124.6	130.9	133.8	137.0	140.0
400	N/A	112.2	119.4	125.5	132.4	139.6	146.9	154.6	162.3	170.0	173.8	177.8	181.6
500	N/A	N/A	N/A	N/A	N/A	171.9	180.6	189.9	199.1	205.7	210.3	213.0	217.6
533	N/A	N/A	N/A	N/A	N/A	N/A	191.9	201.6	211.5	218.0	222.8	225.7	230.5
600	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	233.1	241.4	246.7	252.7	258.1

[1] The values are not guaranteed as stand-alone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 36.
[2] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 34.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 9 and Table 23 provides information related to specific product features. For a complete listing of product offerings, see the Ordering Guide on Page 101.

Figure 9. Product Information on Package

Table 23. Package Information

Brand Key	Description
BF54x	x = 2, 4, 7, 8 or 9
(M)	Mobile DDR Indicator (Optional)
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part (Optional)
cc	See Ordering Guide
vvvvvv.x-q	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

Asynchronous Memory Read Cycle Timing

Table 27 and Table 28 on Page 45 and Figure 13 and Figure 14 on Page 45 describe asynchronous memory read cycle operations for synchronous and for asynchronous ARDY.

Table 27. Asynchronous Memory Read Cycle Timing with Synchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA15–0 Setup Before CLKOUT	5.0		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
t_{SARDY}	ARDY Setup Before the Falling Edge of CLKOUT	5.0		ns
t_{HARDY}	ARDY Hold After the Falling Edge of CLKOUT	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT[1]	0.3		ns

[1] Output pins include $\overline{AMS3–0}$, $\overline{ABE1–0}$, ADDR19–1, $\overline{AOE}$, and $\overline{ARE}$.

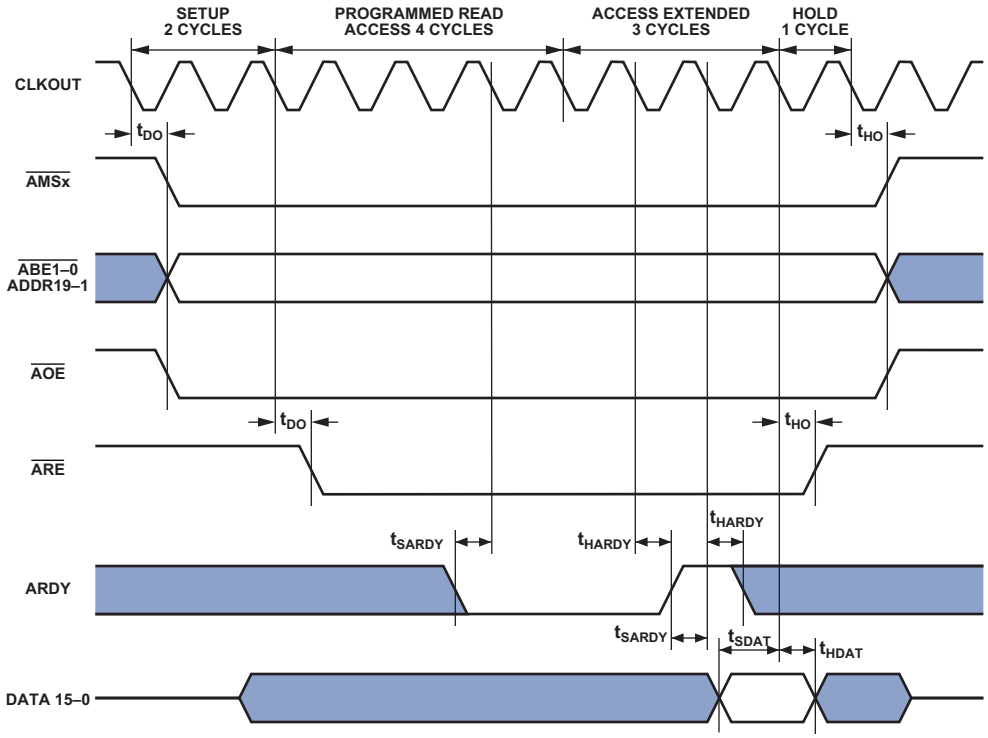


Figure 13. Asynchronous Memory Read Cycle Timing with Synchronous ARDY

Table 35. External Port Bus Request and Grant Cycle Timing with Asynchronous $\overline{BR}$

Parameter		Min	Max	Unit
Timing Requirement				
t_{WBR}	$\overline{BR}$ Pulsewidth	$2 \times t_{SCLK}$		ns
Switching Characteristics				
t_{SD}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}/\overline{AWE}$ Disable		5.0	ns
t_{SE}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}/\overline{AWE}$ Enable		5.0	ns
t_{DBG}	CLKOUT Low to $\overline{BG}$ Asserted Output Delay		4.0	ns
t_{EBG}	CLKOUT Low to $\overline{BG}$ Deasserted Output Hold		4.0	ns
t_{DBH}	CLKOUT Low to $\overline{BGH}$ Asserted Output Delay		3.6	ns
t_{EBH}	CLKOUT Low to $\overline{BGH}$ Deasserted Output Hold		3.6	ns

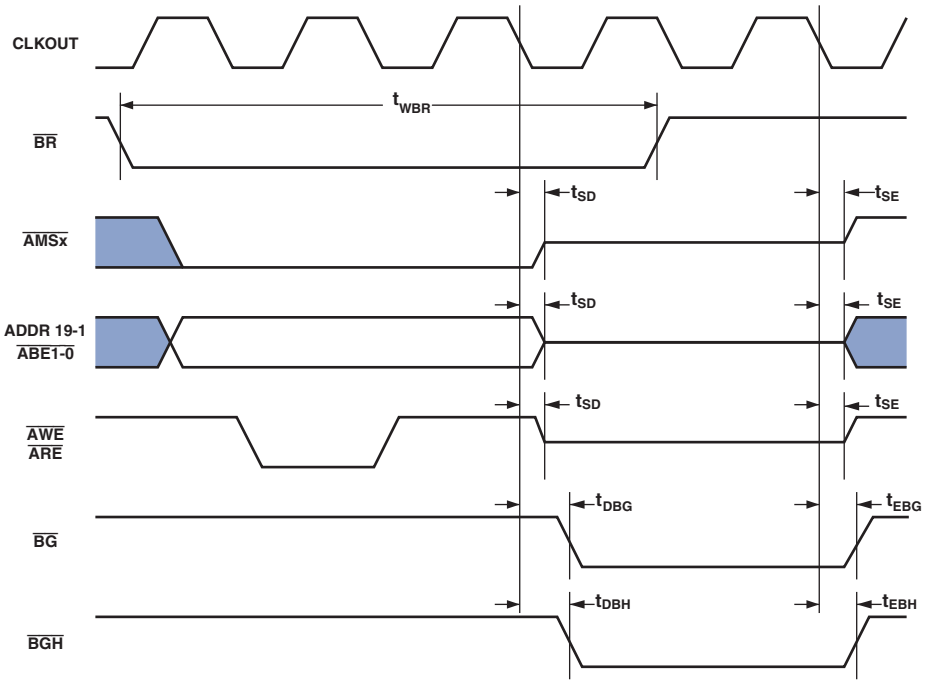


Figure 22. External Port Bus Request and Grant Cycle Timing with Asynchronous $\overline{BR}$

NAND Flash Controller Interface Timing

Table 36 and Figure 23 on Page 54 through Figure 27 on Page 56 describe NAND flash controller interface operations. In the figures, ND_DATA is ND_D0–D15.

Table 36. NAND Flash Controller Interface Timing

Parameter		Min	Max	Unit
Write Cycle				
Switching Characteristics				
t_{CWL}	$\overline{ND\_CE}$ Setup Time to $\overline{AWE}$ Low	$1.0 \times t_{SCLK} - 4$		ns
t_{CH}	$\overline{ND\_CE}$ Hold Time from $\overline{AWE}$ High	$3.0 \times t_{SCLK} - 4$		ns
t_{CLEWL}	ND_CLE Setup Time High to $\overline{AWE}$ Low	0.0		ns
t_{CLH}	ND_CLE Hold Time from $\overline{AWE}$ High	$2.5 \times t_{SCLK} - 4$		ns
t_{ALEWL}	ND_ALE Setup Time Low to $\overline{AWE}$ Low	0.0		ns
t_{ALH}	ND_ALE Hold Time from $\overline{AWE}$ High	$2.5 \times t_{SCLK} - 4$		ns
t_{WP}[1]	$\overline{AWE}$ Low to $\overline{AWE}$ High	$(WR\_DLY + 1.0) \times t_{SCLK} - 4$		ns
t_{WHWL}	$\overline{AWE}$ High to $\overline{AWE}$ Low	$4.0 \times t_{SCLK} - 4$		ns
t_{WC}[1]	$\overline{AWE}$ Low to $\overline{AWE}$ Low	$(WR\_DLY + 5.0) \times t_{SCLK} - 4$		ns
t_{DWS}[1]	Data Setup Time for a Write Access	$(WR\_DLY + 1.5) \times t_{SCLK} - 4$		ns
t_{DWH}	Data Hold Time for a Write Access	$2.5 \times t_{SCLK} - 4$		ns
Read Cycle				
Switching Characteristics				
t_{CRL}	$\overline{ND\_CE}$ Setup Time to $\overline{ARE}$ Low	$1.0 \times t_{SCLK} - 4$		ns
t_{CRH}	$\overline{ND\_CE}$ Hold Time from $\overline{ARE}$ High	$3.0 \times t_{SCLK} - 4$		ns
t_{RP}[1]	$\overline{ARE}$ Low to $\overline{ARE}$ High	$(RD\_DLY + 1.0) \times t_{SCLK} - 4$		ns
t_{RHRL}	$\overline{ARE}$ High to $\overline{ARE}$ Low	$4.0 \times t_{SCLK} - 4$		ns
t_{RC}[1]	$\overline{ARE}$ Low to $\overline{ARE}$ Low	$(RD\_DLY + 5.0) \times t_{SCLK} - 4$		ns
Timing Requirements				
t_{DRS}	Data Setup Time for a Read Transaction	8.0		ns
t_{DRH}	Data Hold Time for a Read Transaction	0.0		ns
Write Followed by Read				
Switching Characteristic				
t_{WHRL}	$\overline{AWE}$ High to $\overline{ARE}$ Low	$5.0 \times t_{SCLK} - 4$		ns

[1] WR_DLY and RD_DLY are defined in the NFC_CTL register.

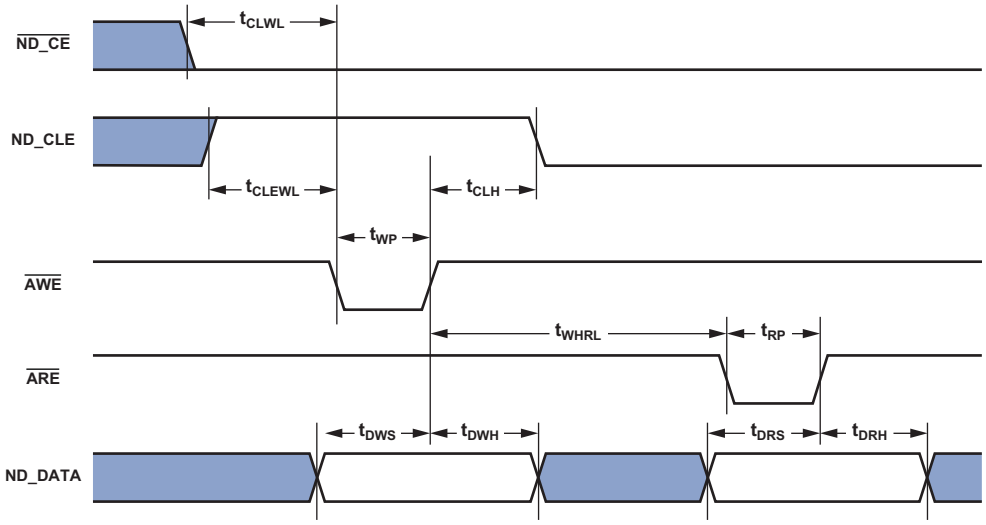


Figure 27. NAND Flash Controller Interface Timing—Write Followed by Read Operation

External DMA Request Timing

Table 38 and Figure 29 describe the external DMA request timing operations.

Table 38. External DMA Request Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{DS}	DMARx Asserted to CLKOUT High Setup	6.0		ns
t_{DH}	CLKOUT High to DMARx Deasserted Hold Time	0.0		ns
$t_{DMARACT}$	DMARx Active Pulse Width	$1.0 \times t_{SCLK}$		ns
$t_{DMARINACT}$	DMARx Inactive Pulse Width	$1.75 \times t_{SCLK}$		ns

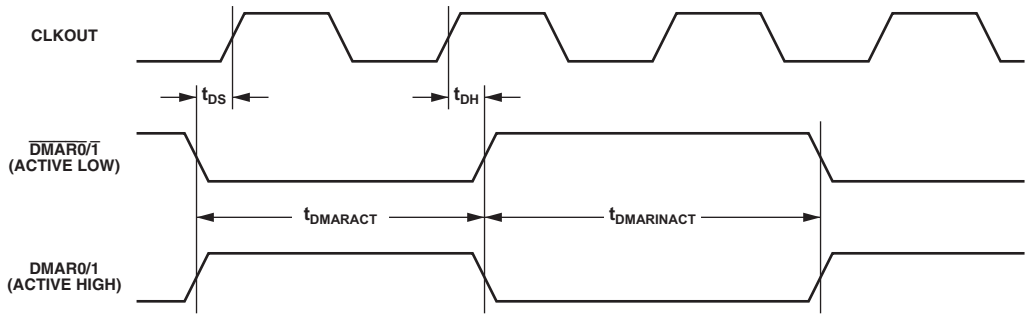


Figure 29. External DMA Request Timing

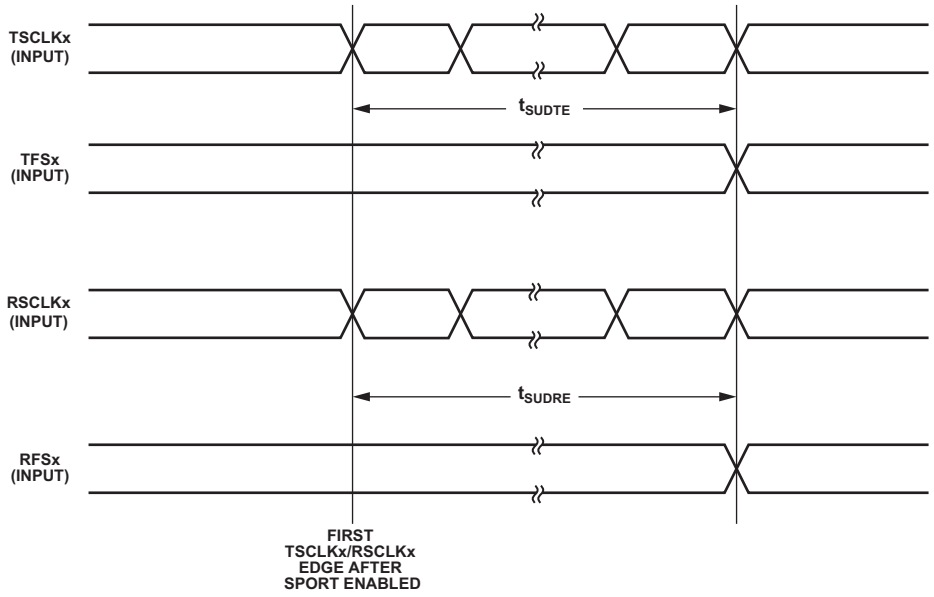


Figure 34. Serial Port Start-Up with External Clock and Frame Sync

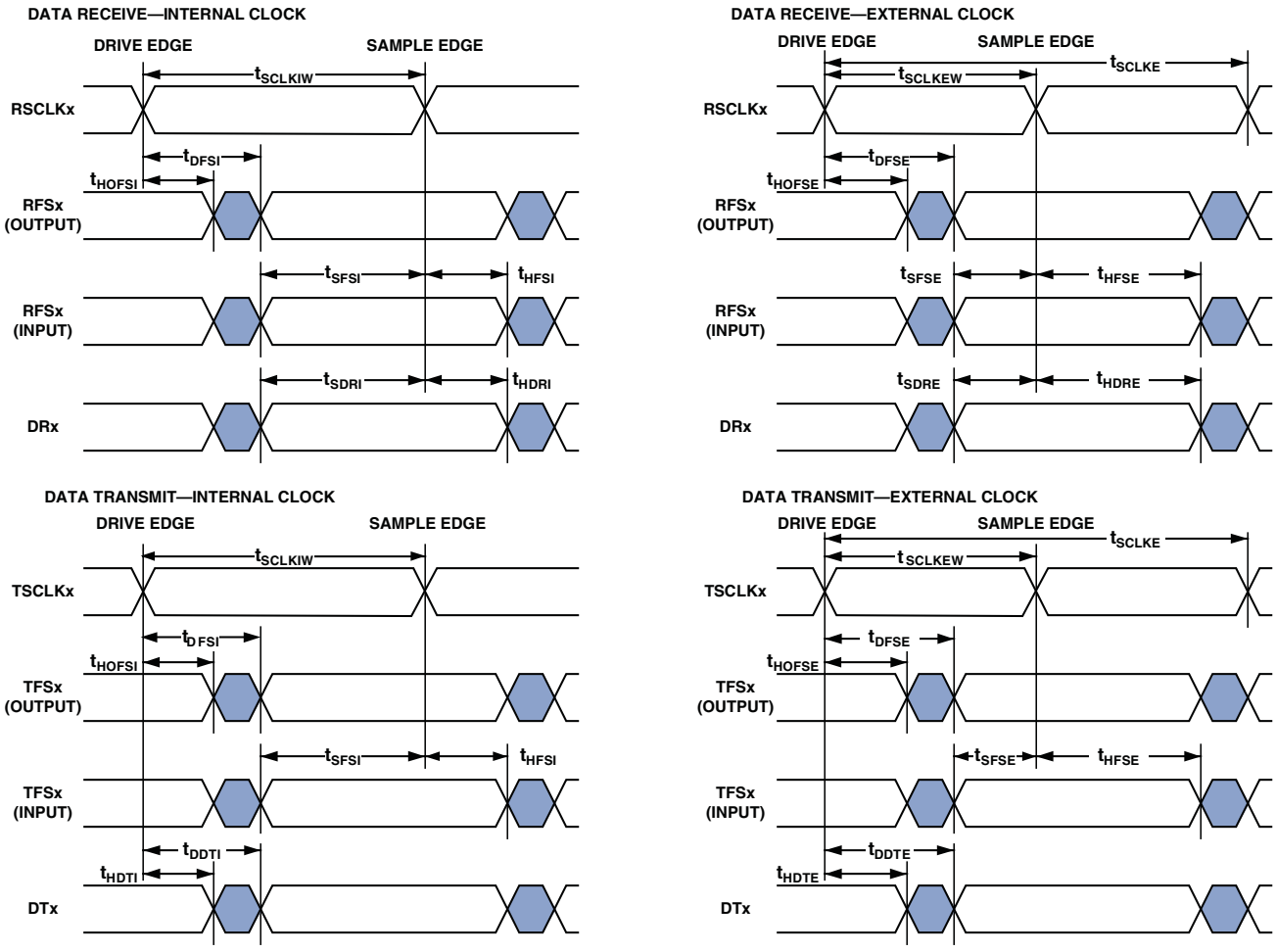


Figure 35. Serial Ports

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 45 and Figure 39 describe SPI port slave operations.

Table 45. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	SPIxSCK High Period	$2t_{SCLK}-1.5$		ns
t_{SPICLS}	SPIxSCK Low Period	$2t_{SCLK}-1.5$		ns
t_{SPICLK}	SPIxSCK Period	$4t_{SCLK}$		ns
t_{HDS}	Last SPIxSCK Edge to $\overline{\text{SPIxSS}}$ Not Asserted	$2t_{SCLK}-1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2t_{SCLK}-1.5$		ns
t_{SDSCI}	$\overline{\text{SPIxSS}}$ Assertion to First SPIxSCK Edge	$2t_{SCLK}-1.5$		ns
t_{SSPID}	Data Input Valid to SPIxSCK Edge (Data Input Setup)	1.6		ns
t_{HSPID}	SPIxSCK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{\text{SPIxSS}}$ Assertion to Data Out Active	0	8	ns
t_{DSDHI}	$\overline{\text{SPIxSS}}$ Deassertion to Data High Impedance	0	8	ns
t_{DDSPID}	SPIxSCK Edge to Data Out Valid (Data Out Delay)		10	ns
t_{HDSPID}	SPIxSCK Edge to Data Out Invalid (Data Out Hold)	0		ns

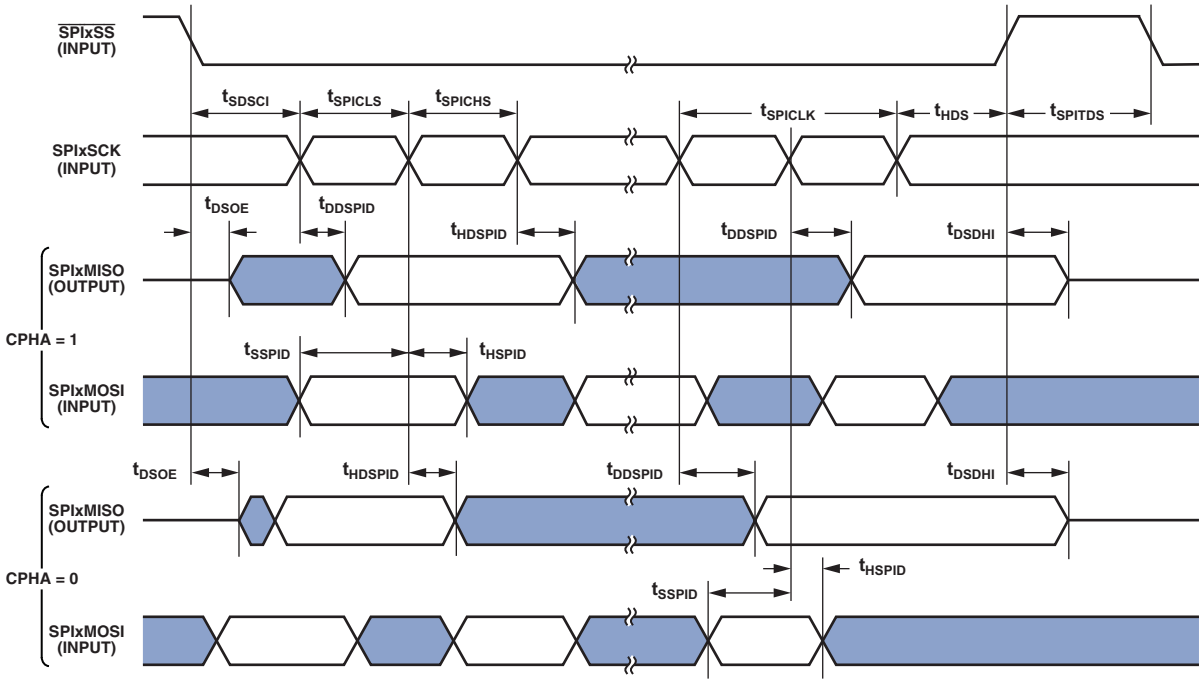


Figure 39. Serial Peripheral Interface (SPI) Port—Slave Timing

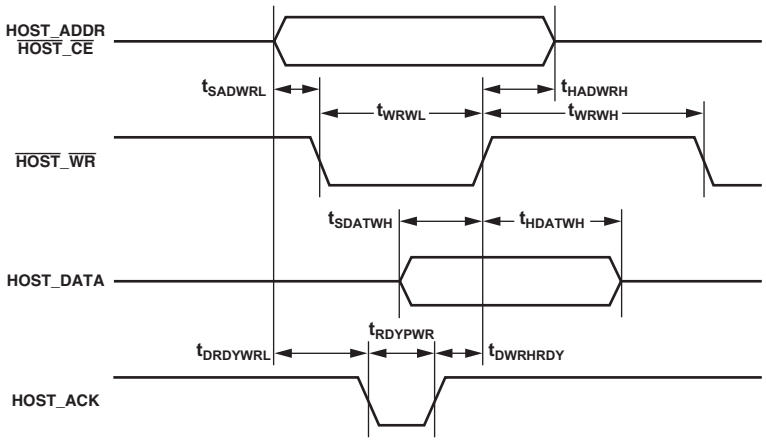
HOSTDP A/C Timing-Host Write Cycle

Table 55 and Figure 47 describe the HOSTDP A/C host write cycle timing requirements.

Table 55. Host Write Cycle Timing Requirements

Parameter		Min	Max	Unit
Timing Requirements				
t_{SADWRL}	HOST_ADDR/$\overline{\text{HOST\_CE}}$ Setup Before $\overline{\text{HOST\_WR}}$ Falling Edge	4		ns
t_{HADWRH}	HOST_ADDR/$\overline{\text{HOST\_CE}}$ Hold After $\overline{\text{HOST\_WR}}$ Rising Edge	2.5		ns
t_{WRWL}	$\overline{\text{HOST\_WR}}$ Pulse Width Low (ACK Mode)	$t_{DRDYWRL} + t_{RDYPRD} + t_{DWRHRDY}$		ns
	$\overline{\text{HOST\_WR}}$ Pulse Width Low (INT Mode)	$1.5 \times t_{SCLK} + 8.7$		ns
t_{WRWH}	$\overline{\text{HOST\_WR}}$ Pulse Width High or Time Between $\overline{\text{HOST\_WR}}$ Rising Edge and $\overline{\text{HOST\_RD}}$ Falling Edge	$2 \times t_{SCLK}$		ns
$t_{DWRHRDY}$	$\overline{\text{HOST\_WR}}$ Rising Edge Delay After HOST_ACK Rising Edge (ACK Mode)	0		ns
t_{HDATWH}	HOST_D15–0 Hold After $\overline{\text{HOST\_WR}}$ Rising Edge	2.5		ns
t_{SDATWH}	HOST_D15–0 Setup Before $\overline{\text{HOST\_WR}}$ Rising Edge	3.5		ns
Switching Characteristics				
$t_{DRDYWRL}$	HOST_ACK Falling Edge After $\overline{\text{HOST\_CE}}$ Asserted (ACK Mode)		11.25	ns
t_{RDYPWR}	HOST_ACK Low Pulse-Width for Write Access (ACK Mode)		NM[1]	ns

[1] NM (not measured)—This parameter is based on t_{SCLK}. It is not measured because the number of SCLK cycles for which HOST_ACK remains low depends on the Host DMA FIFO status. This is system design dependent.



In Figure 47, HOST_DATA is HOST_D0–D15.

Figure 47. HOSTDP A/C- Host Write Cycle

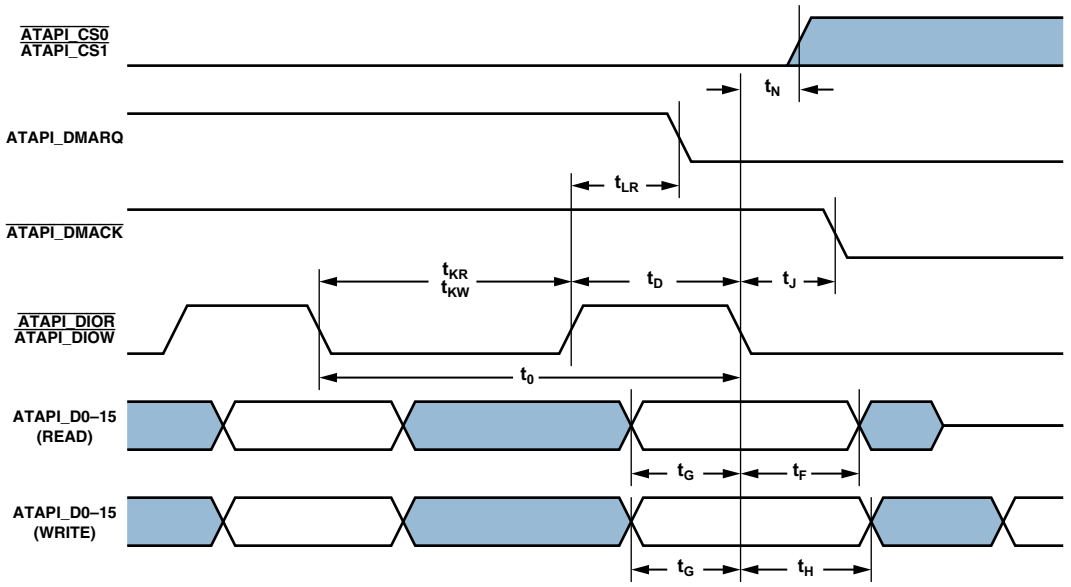


Figure 51. Device Terminating a Multiword DMA Data Burst

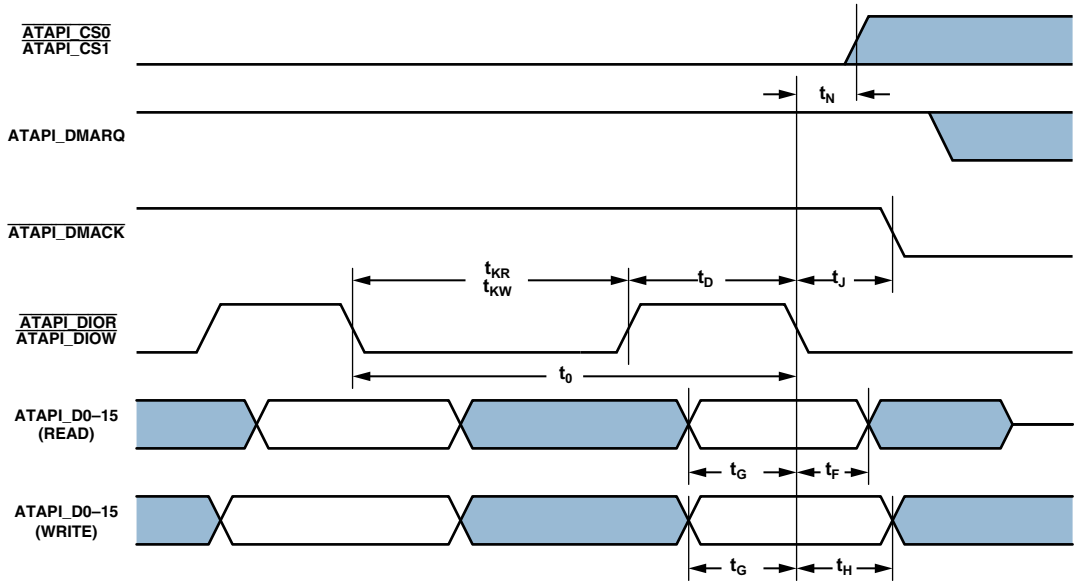


Figure 52. Host Terminating a Multiword DMA Data Burst

ATAPI Ultra DMA Data-Out Transfer Timing

Table 61 and Figure 57 through Figure 60 describes the ATAPI ultra DMA data-out transfer timing. The material in these figures is adapted from ATAPI-6 (INCITS 361-2002[R2007] and is used with permission of the American National Standards Institute (ANSI) on behalf of the Information Technology Industry Council ("ITIC"). Copies of ATAPI-6 (INCITS 361-2002 [R2007] can be purchased from ANSI.

Table 61. ATAPI Ultra DMA Data-Out Transfer Timing

ATAPI Parameter		ATAPI_ULTRA_TIM_x Timing Register Setting[1]	Timing Equation
t_{CYC}[2]	Cycle time	TDVS, TCYC_TDVS	$(TDVS + TCYC\_TDVS) \times t_{SCLK}$
t_{2CYC}	Two cycle time	TDVS, TCYC_TDVS	$2 \times (TDVS + TCYC\_TDVS) \times t_{SCLK}$
t_{DVS}	Data valid setup time at sender	TDVS	$TDVS \times t_{SCLK} - (t_{SK1} + t_{SK2})$
t_{DVH}	Data valid hold time at sender	TCYC_TDVS	$TCYC\_TDVS \times t_{SCLK} - (t_{SK1} + t_{SK2})$
t_{CVS}	CRC word valid setup time at host	TDVS	$TDVS \times t_{SCLK} - (t_{SK1} + t_{SK2})$
t_{CVH}	CRC word valid hold time at host	TACK	$TACK \times t_{SCLK} - (t_{SK1} + t_{SK2})$
t_{DZFS}	Time from data output released-to-driving to first strobe timing	TDVS	$TDVS \times t_{SCLK} - (t_{SK1} + t_{SK2})$
t_{LI}	Limited interlock time	N/A	$2 \times t_{BD} + 2 \times t_{SCLK} + t_{OD}$
t_{MLI}	Interlock time with minimum	TMLI	$TMLI \times t_{SCLK} - (t_{SK1} + t_{SK2})$
t_{ENV}[3]	$\overline{\text{ATAPI\_DMACK}}$ to $\overline{\text{ATAPI\_DIOR}}$/$\overline{\text{DIOW}}$	TENV	$(TENV \times t_{SCLK}) +/- (t_{SK1} + t_{SK2})$
t_{RFS}	Ready to final strobe time	N/A	$2 \times t_{BD} + 2 \times t_{SCLK} + t_{OD}$
t_{ACK}	Setup and Hold time for $\overline{\text{ATAPI\_DMACK}}$	TACK	$TACK \times t_{SCLK} - (t_{SK1} + t_{SK2})$
t_{SS}	Time from STROBE edge to assertion of $\overline{\text{ATAPI\_DIOW}}$	TSS	$TSS \times t_{SCLK} - (t_{SK1} + t_{SK2})$

[1] ATAPI Timing Register Setting should be programmed with a value that guarantees parameter compliance with the ATA ANSI specification for ATA device mode of operation.
[2] ATA/ATAPI-6 compliant functionality with limited speed.
[3] This timing equation can be used to calculate both the minimum and maximum t_{ENV}.

USB On-The-Go-Dual-Role Device Controller Timing

Table 62 describes the USB On-The-Go Dual-Role Device Controller timing requirements.

Table 62. USB On-The-Go Dual-Role Device Controller Timing Requirements

Parameter		Min	Max	Unit
Timing Requirements				
f_{USB}	USB_XI frequency	9	33.3	MHz
FS_{USB}	USB_XI Clock Frequency Stability	–50	+50	ppm

JTAG Test And Emulation Port Timing

Table 63 and Figure 61 describe JTAG port operations.

Table 63. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	11		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse-Width[2] (measured in TCK cycles)	4		t_{TCK}
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	16.5	ns

[1] System inputs = PA15–0, PB14–0, PC13–0, PD15–0, PE15–0, PF15–0, PG15–0, PH13–0, PI15–0, PJ13–0, DQ15–0, DQS1–0, D15–0, $\overline{\text{ATAPI\_PDIAG}}$, $\overline{\text{RESET}}$, $\overline{\text{NMI}}$, and BMODE3–0.

[2] 50 MHz Maximum.

[3] System outputs = PA15–0, PB14–0, PC13–0, PD15–0, PE15–0, PF15–0, PG15–0, PH13–0, PI15–0, PJ13–0, DQ15–0, DQS1–0, D15–0, DA12–0, DBA1–0, DQM1–0, DCLK0-1, $\overline{\text{DCLK0–1}}$, $\overline{\text{DCS1–0}}$, DCLKE, $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, $\overline{\text{DWE}}$, $\overline{\text{AMS3–0}}$, $\overline{\text{ABE1–0}}$, $\overline{\text{AOE}}$, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$, CLKOUT, A3–1, and MFS.

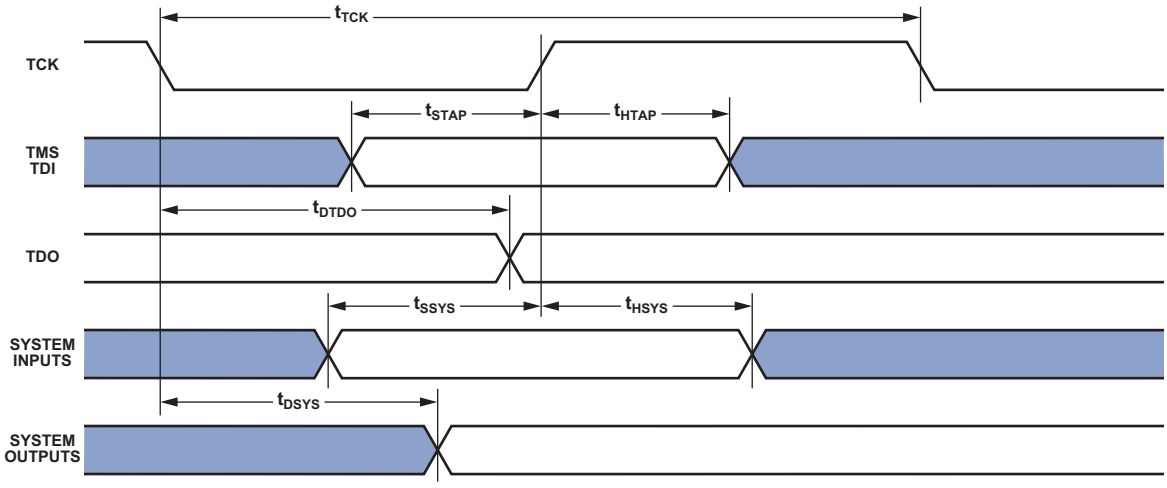


Figure 61. JTAG Port Timing

400-BALL CSP_BGA PACKAGE

Table 65 lists the CSP_BGA package by signal for the ADSP-BF549. Table 66 on Page 97 lists the CSP_BGA package by ball number.

Table 65. 400-Ball CSP_BGA Ball Assignment (Alphabetical by Signal)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
A1	B2	DA4	G16	DQS1	H18	GND	L10
A2	A2	DA5	F19	$\overline{\text{DRAS}}$	E17	GND	L11
A3	B3	DA6	D20	$\overline{\text{DWE}}$	E18	GND	L12
$\overline{\text{ABE0}}$	C17	DA7	C20	$\overline{\text{EMU}}$	R5	GND	L13
$\overline{\text{ABE1}}$	C16	DA8	F18	EXT_WAKE	M18	GND	L14
$\overline{\text{AMS0}}$	A10	DA9	E19	GND	A1	GND	M6
$\overline{\text{AMS1}}$	D9	DA10	B20	GND	A13	GND	M7
$\overline{\text{AMS2}}$	B10	DA11	F17	GND	A20	GND	M8
$\overline{\text{AMS3}}$	D10	DA12	D19	GND	B11	GND	M9
$\overline{\text{AOE}}$	C10	DBA0	H17	GND	D1	GND	M10
$\overline{\text{ARE}}$	B12	DBA1	H16	GND	D4	GND	M11
$\overline{\text{ATAPI\_PDIAG}}$	P19	$\overline{\text{DCAS}}$	F16	GND	E3	GND	M12
$\overline{\text{AWE}}$	D12	$\overline{\text{DCLK0}}$	E16	GND	F3	GND	M13
BMODE0	W1	DCLK0	D16	GND	F6	GND	M14
BMODE1	W2	DCLK1	C18	GND	F14	GND	N6
BMODE2	W3	$\overline{\text{DCLK1}}$	D18	GND	G9	GND	N7
BMODE3	W4	DCLKE	B18	GND	G10	GND	N8
CLKBUF	D11	$\overline{\text{DCS0}}$	C19	GND	G11	GND	N9
CLKIN	A11	$\overline{\text{DCS1}}$	B19	GND	H7	GND	N10
CLKOUT	L16	DDR_VREF	M20	GND	H8	GND	N11
D0	D13	DDR_VSSR	N20	GND	H9	GND	N12
D1	C13	DQ0	L18	GND	H10	GND	N13
D2	B13	DQ1	M19	GND	H11	GND	N14
D3	B15	DQ2	L19	GND	H12	GND	P8
D4	A15	DQ3	L20	GND	J7	GND	P9
D5	B16	DQ4	L17	GND	J8	GND	P10
D6	A16	DQ5	K16	GND	J9	GND	P11
D7	B17	DQ6	K20	GND	J10	GND	P12
D8	C14	DQ7	K17	GND	J11	GND	P13
D9	C15	DQ8	K19	GND	J12	GND	R9
D10	A17	DQ9	J20	GND	K7	GND	R13
D11	D14	DQ10	K18	GND	K8	GND	R14
D12	D15	DQ11	H20	GND	K9	GND	R16
D13	E15	DQ12	J19	GND	K10	GND	U8
D14	E14	DQ13	J18	GND	K11	GND	V6
D15	D17	DQ14	J17	GND	K12	GND	Y1
DA0	G19	DQ15	J16	GND	K13	GND	Y20
DA1	G17	DQM0	G20	GND	L7	GND_{MP}	E7
DA2	E20	DQM1	H19	GND	L8	MFS	E6
DA3	G18	DQS0	F20	GND	L9	MLF_M	F4

Table 66 lists the CSP_BGA package by ball number for the ADSP-BF549. Table 65 on Page 94 lists the CSP_BGA package by signal.

Table 66. 400-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	GND	C1	MXO	E1	USB_DP	G1	PC5
A2	A2	C2	MXI	E2	USB_DM	G2	PC4
A3	PI0	C3	PH5	E3	GND	G3	USB_ID
A4	PI2	C4	PH9	E4	MLF_P	G4	V_{DDUSB}
A5	PI4	C5	PH11	E5	V_{DDEXT}	G5	V_{DDEXT}
A6	PI6	C6	PH13	E6	MFS	G6	V_{DDEXT}
A7	PI8	C7	PH10	E7	GND_{MP}	G7	V_{DDEXT}
A8	PI11	C8	PI9	E8	V_{DDMP}	G8	V_{DDINT}
A9	PI12	C9	PI13	E9	V_{DDEXT}	G9	GND
A10	$\overline{AMS0}$	C10	$\overline{AOE}$	E10	V_{DDEXT}	G10	GND
A11	CLKIN	C11	$\overline{NMI}$	E11	V_{DDEXT}	G11	GND
A12	XTAL	C12	$\overline{RESET}$	E12	V_{DDEXT}	G12	V_{DDINT}
A13	GND	C13	D1	E13	V_{DDRTC}	G13	V_{DDINT}
A14	RTXI	C14	D8	E14	D14	G14	V_{DDEXT}
A15	D4	C15	D9	E15	D13	G15	V_{DDDDR}
A16	D6	C16	$\overline{ABE1}$	E16	$\overline{DCLK0}$	G16	DA4
A17	D10	C17	$\overline{ABE0}$	E17	$\overline{DRAS}$	G17	DA1
A18	$VROUT_0$	C18	DCLK1	E18	$\overline{DWE}$	G18	DA3
A19	$VROUT_1$	C19	$\overline{DCS0}$	E19	DA9	G19	DA0
A20	GND	C20	DA7	E20	DA2	G20	DQM0
B1	USB_VREF	D1	GND	F1	USB_XI	H1	PC3
B2	A1	D2	USB_VBUS	F2	USB_XO	H2	PC0
B3	A3	D3	USB_RSET	F3	GND	H3	PC7
B4	PI1	D4	GND	F4	MLF_M	H4	PH7
B5	PI3	D5	PH8	F5	V_{DDUSB}	H5	V_{DDEXT}
B6	PI5	D6	PH6	F6	GND	H6	V_{DDEXT}
B7	PI7	D7	PH12	F7	V_{DDEXT}	H7	GND
B8	PI10	D8	PI14	F8	V_{DDEXT}	H8	GND
B9	PI15	D9	$\overline{AMS1}$	F9	V_{DDINT}	H9	GND
B10	$\overline{AMS2}$	D10	$\overline{AMS3}$	F10	V_{DDDDR}	H10	GND
B11	GND	D11	CLKBUF	F11	V_{DDDDR}	H11	GND
B12	$\overline{ARE}$	D12	$\overline{AWE}$	F12	V_{DDDDR}	H12	GND
B13	D2	D13	D0	F13	V_{DDEXT}	H13	V_{DDDDR}
B14	RTXO	D14	D11	F14	GND	H14	V_{DDDDR}
B15	D3	D15	D12	F15	V_{DDVR}	H15	V_{DDDDR}
B16	D5	D16	DCLK0	F16	$\overline{DCAS}$	H16	DBA1
B17	D7	D17	D15	F17	DA11	H17	DBA0
B18	DCLKE	D18	$\overline{DCLK1}$	F18	DA8	H18	DQS1
B19	$\overline{DCS1}$	D19	DA12	F19	DA5	H19	DQM1
B20	DA10	D20	DA6	F20	DQS0	H20	DQ11

Table 66. 400-Ball CSP_BGA Ball Assignment (Numerical by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
J1	PF1	L1	PF5	N1	PF14	R1	PD2
J2	PC2	L2	PF4	N2	PF15	R2	PD3
J3	PC1	L3	PF8	N3	PG3	R3	PD5
J4	PG0	L4	PF6	N4	PF13	R4	PD7
J5	PC6	L5	PG2	N5	V_{DDEXT}	R5	$\overline{EMU}$
J6	V_{DDINT}	L6	V_{DDINT}	N6	GND	R6	V_{DDEXT}
J7	GND	L7	GND	N7	GND	R7	V_{DDEXT}
J8	GND	L8	GND	N8	GND	R8	V_{DDEXT}
J9	GND	L9	GND	N9	GND	R9	GND
J10	GND	L10	GND	N10	GND	R10	V_{DDINT}
J11	GND	L11	GND	N11	GND	R11	V_{DDINT}
J12	GND	L12	GND	N12	GND	R12	V_{DDINT}
J13	V_{DDINT}	L13	GND	N13	GND	R13	GND
J14	V_{DDDDR}	L14	GND	N14	GND	R14	GND
J15	V_{DDDDR}	L15	V_{DDINT}	N15	V_{DDEXT}	R15	V_{DDEXT}
J16	DQ15	L16	CLKOUT	N16	PJ7	R16	GND
J17	DQ14	L17	DQ4	N17	PJ4	R17	PE7
J18	DQ13	L18	DQ0	N18	PJ1	R18	PG13
J19	DQ12	L19	DQ2	N19	PJ13	R19	PJ8
J20	DQ9	L20	DQ3	N20	DDR_VSSR	R20	PJ0
K1	PF3	M1	PF9	P1	PG4	T1	PD4
K2	PF2	M2	PF10	P2	PE11	T2	PD6
K3	PF0	M3	PF11	P3	PD0	T3	PD10
K4	PF7	M4	PF12	P4	PD1	T4	PD12
K5	PG1	M5	PE12	P5	PE13	T5	$\overline{TRST}$
K6	V_{DDEXT}	M6	GND	P6	V_{DDINT}	T6	PB2
K7	GND	M7	GND	P7	V_{DDINT}	T7	V_{DDEXT}
K8	GND	M8	GND	P8	GND	T8	V_{DDEXT}
K9	GND	M9	GND	P9	GND	T9	V_{DDEXT}
K10	GND	M10	GND	P10	GND	T10	V_{DDEXT}
K11	GND	M11	GND	P11	GND	T11	V_{DDEXT}
K12	GND	M12	GND	P12	GND	T12	V_{DDEXT}
K13	GND	M13	GND	P13	GND	T13	V_{DDEXT}
K14	V_{DDDDR}	M14	GND	P14	V_{DDINT}	T14	V_{DDEXT}
K15	V_{DDDDR}	M15	V_{DDEXT}	P15	V_{DDEXT}	T15	V_{DDEXT}
K16	DQ5	M16	PJ2	P16	PG12	T16	V_{DDEXT}
K17	DQ7	M17	PJ11	P17	PJ9	T17	PE1
K18	DQ10	M18	EXT_WAKE	P18	PJ6	T18	PE10
K19	DQ8	M19	DQ1	P19	$\overline{ATAPI\_PDIAG}$	T19	PJ10
K20	DQ6	M20	DDR_VREF	P20	PJ12	T20	PJ3