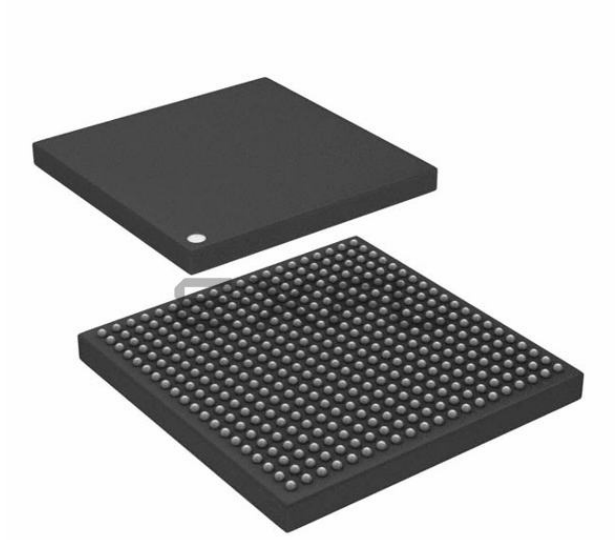

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART, USB
Clock Rate	533MHz
Non-Volatile Memory	External
On-Chip RAM	132kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf542mbbcz-5m

Host DMA Port Interface

The host DMA port (HOSTDP) facilitates a host device external to the ADSP-BF54x Blackfin processors to be a DMA master and transfer data back and forth. The host device always masters the transactions, and the processor is always a DMA slave device.

The HOSTDP is enabled through the peripheral access bus. Once the port has been enabled, the transactions are controlled by the external host. The external host programs standard DMA configuration words in order to send/receive data to any valid internal or external memory location. The host DMA port controller includes the following features:

- Allows an external master to configure DMA read/write data transfers and read port status
- Uses a flexible asynchronous memory protocol for its external interface
- Allows an 8- or 16-bit external data interface to the host device
- Supports half-duplex operation
- Supports little/big endian data transfers
- Acknowledge mode allows flow control on host transactions
- Interrupt mode guarantees a burst of FIFO depth host transactions

REAL-TIME CLOCK

The ADSP-BF54x Blackfin processors' real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the ADSP-BF54x Blackfin processors. The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low-power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and a 32,768-day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms. The first alarm is for a time of day. The second alarm is for a day and time of that day.

The stopwatch function counts down from a programmed value with one-second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like the other peripherals, the RTC can wake up the ADSP-BF54x processor from sleep mode upon generation of any RTC wakeup event. Additionally, an RTC wakeup event can wake up the ADSP-BF54x processors from deep sleep mode, and it can wake up the on-chip internal voltage regulator from the hibernate state.

Connect RTC pins RTXI and RTXO with external components as shown in Figure 4.

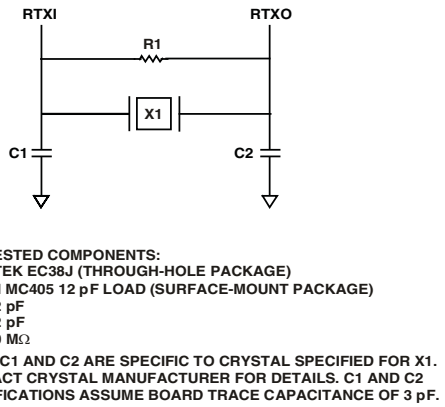

Figure 4. External Components for RTC

WATCHDOG TIMER

The ADSP-BF54x processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system reliability by forcing the processor to a known state through generation of a hardware reset, non-maskable interrupt (NMI), or general-purpose interrupt if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, and then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the ADSP-BF54x processors' peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK) at a maximum frequency of f_{SCLK}.

TIMERS

There are up to two timer units in the ADSP-BF54x Blackfin processors. One unit provides eight general-purpose programmable timers, and the other unit provides three. Each timer has an external pin that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input on the TMRx pins, an external clock TMRCLK input pin, or to the internal SCLK.

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity will wake up the processor. In the sleep mode, assertion of a wakeup event enabled in the SIC_IWRx register causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor transitions to the full on mode. If BYPASS is enabled, the processor transitions to the active mode.

In the sleep mode, system DMA access to L1 memory is not supported.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such as the RTC, may still be running but will not be able to access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. In deep sleep mode, an asynchronous RTC interrupt causes the processor to transition to the active mode. Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full on mode.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and to all the synchronous peripherals (SCLK). The internal voltage regulator for the processor can be shut off by using the bfrom_SysControl() function in the on-chip ROM. This sets the internal power supply voltage (V_{DDINT}) to 0 V to provide the greatest power savings mode. Any critical information stored internally (memory contents, register contents, and so on) must be written to a non-volatile storage device prior to removing power if the processor state is to be preserved.

Since V_{DDEXT} is still supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to have power still applied without drawing unwanted current.

The internal supply regulator can be woken up by CAN, by the MXVR, by the keypad, by the up/down counter, by the USB, and by some GPIO pins. It can also be woken up by a real-time clock wakeup event or by asserting the $\overline{\text{RESET}}$ pin. Waking up from hibernate state initiates the hardware reset sequence.

With the exception of the VR_CTL and the RTC registers, all internal registers and memories lose their content in hibernate state. State variables may be held in external SRAM or DDR memory.

Power Domains

As shown in Table 5, the ADSP-BF54x Blackfin processors support different power domains. The use of multiple power domains maximizes flexibility while maintaining compliance with industry standards and conventions. By isolating the internal logic of the ADSP-BF54x Blackfin processors into its own power domain separate from the RTC and other I/O, the processors can take advantage of dynamic power management without affecting the RTC or other I/O devices. There are no sequencing requirements for the various power domains.

Table 5. Power Domains

Power Domain	VDD Range
All internal logic, except RTC, DDR, and USB	V_{DDINT}
RTC internal logic and crystal I/O	V_{DDRTC}
DDR external memory supply	V_{DDDDR}
USB internal logic and crystal I/O	V_{DDUSB}
Internal voltage regulator	V_{DDVR}
MXVR PLL and logic	V_{DDMP}
All other I/O	V_{DDEXT}

VOLTAGE REGULATION

The ADSP-BF54x Blackfin processors provide an on-chip voltage regulator that can generate processor core voltage levels from an external supply (see specifications in Operating Conditions on Page 34). Figure 6 on Page 17 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. This register can be accessed using the bfrom_SysControl() function in the on-chip ROM. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power supplied. While in hibernate state, V_{DDEXT}, V_{DDRTC}, V_{DDDDR}, V_{DDUSB}, and V_{DDVR} can still be applied, eliminating the need for external buffers. The voltage regulator can be activated from this power-down state by assertion of the $\overline{\text{RESET}}$ pin, which then initiates a boot sequence. The regulator can also be disabled and bypassed at the user's discretion. For all 600 MHz speed grade models and all automotive grade models, the internal voltage regulator must not be used and V_{DDVR} must be tied to V_{DDEXT}. For additional information regarding design of the voltage regulator circuit, see *Switching Regulator Design Considerations for the ADSP-BF533 Blackfin Processors (EE-228)*.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *“Analog Devices JTAG Emulation Technical Reference”* (EE-68) on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

MXVR BOARD LAYOUT GUIDELINES

The MXVR Loop Filter RC network is connected between the MLF_P and MLF_M pins in the following manner:

Capacitors:

- C1: 0.047 µF (PPS type, 2% tolerance recommended)
- C2: 330 pF (PPS type, 2% tolerance recommended)

Resistor:

- R1: 330 Ω (1% tolerance)

The RC network should be located physically close to the MLF_P and MLF_M pins on the board.

The RC network should be shielded using GND_{MP} traces.

Avoid routing other switching signals near the RC network to avoid crosstalk.

MXI driven with external clock oscillator IC:

- MXI should be driven with the clock output of a clock oscillator IC running at a frequency of 49.152 MHz or 45.1584 MHz.
- MXO should be left unconnected.
- Avoid routing other switching signals near the oscillator and clock output trace to avoid crosstalk. When not possible, shield traces with ground.

MXI/MXO with external crystal:

- The crystal must be a fundamental mode crystal running at a frequency of 49.152 MHz or 45.1584 MHz.
- The crystal and load capacitors should be placed physically close to the MXI and MXO pins on the board.
- Board trace capacitance on each lead should not be more than 3 pF.
- Trace capacitance plus load capacitance should equal the load capacitance specification for the crystal.
- Avoid routing other switching signals near the crystal and components to avoid crosstalk. When not possible, shield traces and components with ground.

V_{DDMP}/GND_{MP}—MXVR PLL power domain:

- Route V_{DDMP} and GND_{MP} with wide traces or as isolated power planes.
- Drive V_{DDMP} to same level as V_{DDINT}.
- Place a ferrite bead between the V_{DDINT} power plane and the V_{DDMP} pin for noise isolation.
- Locally bypass V_{DDMP} with 0.1 µF and 0.01 µF decoupling capacitors to GND_{MP}.
- Avoid routing switching signals near to V_{DDMP} and GND_{MP} traces to avoid crosstalk.

Fiber optic transceiver (FOT) connections:

- Keep the traces between the ADSP-BF549 processor and the FOT as short as possible.
- The receive data trace connecting the FOT receive data output pin to the ADSP-BF549 PH6/MRX input pin should have a 0 Ω series termination resistor placed close to the FOT receive data output pin. Typically, the edge rate of the FOT receive data signal driven by the FOT is very slow, and further degradation of the edge rate is not desirable.
- The transmit data trace connecting the ADSP-BF549 PH5/MTX output pin to the FOT transmit data input pin should have a 27 Ω series termination resistor placed close to the ADSP-BF549 PH5/MTX pin.
- The receive data trace and the transmit data trace between the ADSP-BF549 processor and the FOT should not be routed close to each other in parallel over long distances to avoid crosstalk.

ADDITIONAL INFORMATION

The following publications that describe the ADSP-BF54x Blackfin processors (and related processors) can be ordered from any Analog Devices sales office or accessed electronically on www.analog.com:

- *ADSP-BF54x Blackfin Processor Hardware Reference, Volume 1 and Volume 2*
- *Blackfin Processor Programming Reference*
- *ADSP-BF542/BF544/BF547/BF548/BF549 Blackfin Anomaly List*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

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Table 10. Pin Multiplexing (Continued)

Primary Pin Function (Number of Pins)[1, 2]	First Peripheral Function	Second Peripheral Function	Third Peripheral Function	Fourth Peripheral Function	Interrupt Capability
Port H					
GPIO (14 pins)	UART1 (2 pins)	PPI0-1_FS3 (2 pins)	TACI1 (1 pin)		Interrupts (8 pins)
	$\overline{\text{ATAPI\_RESET}}$ (1 pin)	TMR8 (1 pin)	PPI2_FS3 (1 pin)		
	HOST_ADDR (1 pin)	TMR9 (1 pin)	Counter Down/Gate (1 pin)		
	HOST_ACK (1 pin)	TMR10 (1 pin)	Counter Up/Dir (1 pin)		
	MXVR MRX, MTX, $\overline{\text{MRXON}}$/$\overline{\text{GPW}}$ (3 pins)[4]		DMAR 0–1 (2 pins)	TACI8–10 (3 pins) TACLK8–10 (3 pins) HWAITA	
		AMC Addr 4-9 (6 pins)			Interrupts (6 pins)
Port I					
GPIO (16 pins)	Async Addr10–25 (16 pins)				Interrupts (8 pins)
					Interrupts (8 pins)
Port J					
GPIO (14 pins)	Async CTL and MISC				Interrupts (8 pins)
					Interrupts (6 pins)

[1] Port connections may be inputs or outputs after power up depending on the model and boot mode chosen.
[2] All port connections always power up as inputs for some period of time and require resistive termination to a safe condition if used as outputs in the system.
[3] A total of 32 interrupts at once are available from ports C through J, configurable in byte-wide blocks.
[4] $\overline{\text{GPW}}$ functionality available when MXVR is not present or unused.

Pin definitions for the ADSP-BF54x processors are listed in Table 11. In order to maintain maximum function and reduce package size and ball count, some balls have dual, multiplexed functions. In cases where ball function is reconfigurable, the default state is shown in plain text, while the alternate function is shown in italics.

All pins are three-stated during and immediately after reset, with the exception of the external memory interface, asynchronous and synchronous memory control, and the buffered XTAL output pin (CLKBUF). On the external memory interface, the control and address lines are driven high, with the exception of CLKOUT, which toggles at the system clock rate. During hibernate, all outputs are three-stated unless otherwise noted in Table 11.

All I/O pins have their input buffers disabled with the exception of the pins that need pull-ups or pull-downs, as noted in Table 11.

It is strongly advised to use the available IBIS models to ensure that a given board design meets overshoot/undershoot and signal integrity requirements.

Additionally, adding a parallel termination to CLKOUT may prove useful in further enhancing signal integrity. Be sure to verify overshoot/undershoot and signal integrity specifications on actual hardware.

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
Port C: GPIO/*SPORT0/SD Controller/MXVR (MOST)*			
PC0/*TFS0*	I/O	GPIO/*SPORT0 Transmit Frame Sync*	C
PC1/*DT0SEC/MMCLK*	I/O	GPIO/*SPORT0 Transmit Data Secondary/MXVR Master Clock*	C
PC2/*DT0PRI*	I/O	GPIO/*SPORT0 Transmit Data Primary*	C
PC3/*TSCLK0*	I/O	GPIO/*SPORT0 Transmit Serial Clock*	A
PC4/*RFS0*	I/O	GPIO/*SPORT0 Receive Frame Sync*	C
PC5/*DR0SEC/MBCLK*	I/O	GPIO/*SPORT0 Receive Data Secondary/MXVR Bit Clock*	C
PC6/*DR0PRI*	I/O	GPIO/*SPORT0 Receive Data Primary*	C
PC7/*RSCLK0*	I/O	GPIO/*SPORT0 Receive Serial Clock*	C
PC8/*SD_D0*	I/O	GPIO/*SD Data Bus*	A
PC9/*SD_D1*	I/O	GPIO/*SD Data Bus*	A
PC10/*SD_D2*	I/O	GPIO/*SD Data Bus*	A
PC11/*SD_D3*	I/O	GPIO/*SD Data Bus*	A
PC12/*SD_CLK*	I/O	GPIO/*SD Clock Output*	A
PC13/*SD_CMD*	I/O	GPIO/*SD Command*	A
Port D: GPIO/*PPI0–2/SPORT 1/Keypad/Host DMA*			
PD0/*PPI1_D0/HOST_D8/ TFS1/PPI0_D18*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Transmit Frame Sync/PPI0 Data*	C
PD1/*PPI1_D1/HOST_D9/ DT1SEC/PPI0_D19*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Transmit Data Secondary/PPI0 Data*	C
PD2/*PPI1_D2/HOST_D10/ DT1PRI/PPI0_D20*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Transmit Data Primary/PPI0 Data*	C
PD3/*PPI1_D3/HOST_D11/ TSCLK1/PPI0_D21*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Transmit Serial Clock/PPI0 Data*	A
PD4/*PPI1_D4/HOST_D12/RFS1/PPI0_D22*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Receive Frame Sync/PPI0 Data*	C
PD5/*PPI1_D5/HOST_D13/DR1SEC/PPI0_D23*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Receive Data Secondary/PPI0 Data*	C
PD6/*PPI1_D6/HOST_D14/DR1PRI*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Receive Data Primary*	C
PD7/*PPI1_D7/HOST_D15/RSCLK1*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Receive Serial Clock*	A
PD8/*PPI1_D8/HOST_D0/ PPI2_D0/KEY_ROW0*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Row Input*	A
PD9/*PPI1_D9/HOST_D1/PPI2_D1/KEY_ROW1*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Row Input*	A
PD10/*PPI1_D10/HOST_D2/PPI2_D2/KEY_ROW2*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Row Input*	A
PD11/*PPI1_D11/HOST_D3/PPI2_D3/KEY_ROW3*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Row Input*	A
PD12/*PPI1_D12/HOST_D4/PPI2_D4/KEY_COL0*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Column Output*	A
PD13/*PPI1_D13/HOST_D5/PPI2_D5/KEY_COL1*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Column Output*	A
PD14/*PPI1_D14/HOST_D6/PPI2_D6/KEY_COL2*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Column Output*	A
PD15/*PPI1_D15/HOST_D7/PPI2_D7/KEY_COL3*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Column Output*	A

SPECIFICATIONS

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}[1, 2]	Internal Supply Voltage	Nonautomotive grade models	0.9		1.43	V
	Internal Supply Voltage	Automotive and extended temp grade models	1.0		1.38	V
	Internal Supply Voltage	Mobile DDR SDRAM models	1.14		1.31	V
V_{DDEXT}[3]	External Supply Voltage	Nonautomotive 3.3 V I/O	2.7	3.3	3.6	V
	External Supply Voltage	Nonautomotive 2.5 V I/O	2.25	2.5	2.75	V
	External Supply Voltage	Automotive and extended temp grade models	2.7	3.3	3.6	V
V_{DDUSB}	USB External Supply Voltage		3.0	3.3	3.6	V
V_{DDMP}	MXVR PLL Supply Voltage	Nonautomotive grade models	0.9		1.43	V
	MXVR PLL Supply Voltage	Automotive and extended temp grade models	1.0		1.38	V
V_{DDRTC}	Real Time Clock Supply Voltage	Nonautomotive grade models	2.25		3.6	V
	Real Time Clock Supply Voltage	Automotive and extended temp grade models	2.7	3.3	3.6	V
V_{DDDDR}	DDR Memory Supply Voltage	DDR SDRAM models	2.5	2.6	2.7	V
	DDR Memory Supply Voltage	Mobile DDR SDRAM models	1.8	1.875	1.95	V
V_{DDVR}[4]	Internal Voltage Regulator Supply Voltage		2.7	3.3	3.6	V
V_{IH}	High Level Input Voltage[5, 6]	V_{DDEXT} = maximum	2.0		3.6	V
V_{IHDDR}	High Level Input Voltage[7]	DDR SDRAM models	V_{DDR_VREF} + 0.15		V_{DDDDR} + 0.3	V
	High Level Input Voltage[7]	Mobile DDR SDRAM models	V_{DDR_VREF} + 0.125		V_{DDDDR} + 0.3	V
V_{IH5V}[12]	High Level Input Voltage[8]	V_{DDEXT} = maximum	2.0		5.5	V
V_{IHTWI}	High Level Input Voltage[9, 13]	V_{DDEXT} = maximum	0.7 × V_{DDEXT}		5.5	V
V_{IHUSB}	High Level Input Voltage[10]				5.25	V
V_{IL}	Low Level Input Voltage[5, 11]	V_{DDEXT} = minimum	–0.3		0.6	V
V_{IL5V}	Low Level Input Voltage[12]	3.3 V I/O, V_{DDEXT} = minimum	–0.3		0.8	V
	Low Level Input Voltage[12]	2.5 V I/O, V_{DDEXT} = minimum	–0.3		0.6	V
V_{ILDDR}	Low Level Input Voltage[7]	DDR SDRAM models	–0.3		V_{DDR_VREF} – 0.15	V
	Low Level Input Voltage[7]	Mobile DDR SDRAM models	–0.3		V_{DDR_VREF} – 0.125	V
V_{ILTWI}	Low Level Input Voltage[9, 13]		–0.3		0.3 × V_{DDEXT}	V
V_{DDR_VREF}	DDR_VREF Pin Input Voltage		0.49 × V_{DDDDR}	0.50 × V_{DDDDR}	0.51 × V_{DDDDR}	V
T_J[14]	Junction Temperature (400/533 MHz)	400-Ball CSP_BGA @$T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
	Junction Temperature (600 MHz)	400-Ball CSP_BGA @$T_{AMBIENT}$ = 0°C to +70°C	0		+90	°C
	Junction Temperature (400 MHz)	400-Ball CSP_BGA @$T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C

[1] See Table 12 on Page 35 for frequency/voltage specifications.
[2] V_{DDINT} maximum is 1.10 V during one-time-programmable (OTP) memory programming operations.
[3] V_{DDEXT} minimum is 3.0 V and maximum is 3.6 V during OTP memory programming operations.
[4] Use of the internal voltage regulator is not supported on 600 MHz speed grade models or on automotive grade models. An external voltage regulator must be used.
[5] Bidirectional pins (D15–0, PA15–0, PB14–0, PC15–0, PD15–0, PE15–0, PF15–0, PG15–0, PH13–0, PI15–0, PJ14–0) and input pins ($\overline{ATAPI\_PDIAG}$, USB_ID, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE3–0) of the ADSP-BF54x Blackfin processors are 3.3 V-tolerant (always accept up to 3.6 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage. The regulator can generate V_{DDINT} at levels of 0.90 V to 1.30 V with -5% to +5% tolerance.
[6] Parameter value applies to all input and bidirectional pins except PB1-0, PE15-14, PG15–11, PH7-6, DQ0-15, and DQS0-1.
[7] Parameter value applies to pins DQ0–15 and DQS0–1.
[8] PB1-0, PE15-14, PG15-11, and PH7-6 are 5.0 V-tolerant (always accept up to 5.5 V maximum V_{IH} when power is applied to V_{DDEXT} pins). Voltage compliance (on output V_{OH}) is limited by V_{DDEXT} supply voltage.
[9] SDA and SCL are 5.0 V tolerant (always accept up to 5.5 V maximum V_{IH}). Voltage compliance on outputs (V_{OH}) is limited by the $_{VDDEXT}$ supply voltage.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 20 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Table 21 details the maximum duty cycle for input transient voltage.

Table 20. Absolute Maximum Ratings

Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.43 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +3.8 V
Input Voltage[1, 2, 3]	–0.5 V to +3.6 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
I_{OH}/I_{OL} Current per Single Pin[4]	40 mA (max)
I_{OH}/I_{OL} Current per Pin Group[4]	80 mA (max)
Storage Temperature Range	–65°C to +150°C
Junction Temperature Underbias	+125°C

[1] Applies to all bidirectional and input only pins except PB1-0, PE15-14, PG15–11, and PH7-6, where the absolute maximum input voltage range is –0.5 V to +5.5 V.

[2] Pins USB_DP, USB_DM, and USB_VBUS are 5 V-tolerant when VDDUSB is powered according to the operating conditions table. If VDDUSB supply voltage does not meet the specification in the operating conditions table, these pins could suffer long-term damage when driven to +5 V. If this condition is seen in the application, it can be corrected with additional circuitry to use the external host to power only the V_{DDUSB} pins. Contact factory for application detail and reliability information.

[3] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2 V.

[4] For more information, see description preceding Table 22.

Table 21. Maximum Duty Cycle for Input[1] Transient Voltage

V_{IN} Max (V)[2]	V_{IN} Min (V)	Maximum Duty Cycle
3.63	–0.33	100%
3.80	–0.50	48%
3.90	–0.60	30%
4.00	–0.70	20%
4.10	–0.80	10%
4.20	–0.90	8%
4.30	–1.00	5%

[1] Does not apply to CLKIN. Absolute maximum for pins PB1-0, PE15-14, PG15-11, and PH7-6 is +5.5V.

[2] Only one of the listed options can apply to a particular design.

The Absolute Maximum Ratings table specifies the maximum total source/sink (I_{OH}/I_{OL}) current for a group of pins. Permanent damage can occur if this value is exceeded. To understand this specification, if pins PA4, PA3, PA2, PA1 and PA0 from group 1 in the Total Current Pin Groups table were sourcing or sinking 2 mA each, the total current for those pins would be 10 mA. This would allow up to 70 mA total that could be sourced or sunk by the remaining pins in the group without damaging the device. For a list of all groups and their pins, see the Total Current Pin Groups table. Note that the V_{OL} and V_{OH} specifications have separate per-pin maximum current requirements, see the Electrical Characteristics table.

Table 22. Total Current Pin Groups

Group	Pins in Group
1	PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PA8, PA9, PA10, PA11
2	PA12, PA13, PA14, PA15, PB8, PB9, PB10, PB11, PB12, PB13, PB14
3	PB0, PB1, PB2, PB3, PB4, PB5, PB6, PB7, BMODE0, BMODE1, BMODE2, BMODE3
4	TCK, TDI, TDO, TMS, $\overline{\text{TRST}}$, PD14, $\overline{\text{EMU}}$
5	PD8, PD9, PD10, PD11, PD12, PD13, PD15
6	PD0, PD1, PD2, PD3, PD4, PD5, PD6, PD7
7	PE11, PE12, PE13, PF12, PF13, PF14, PF15, PG3, PG4
8	PF4, PF5, PF6, PF7, PF8, PF9, PF10, PF11
9	PF0, PF1, PF2, PF3, PG0, PG1, PG2
10	PC0, PC1, PC2, PC3, PC4, PC5, PC6, PC7
11	PH5, PH6, PH7
12	A1, A2, A3
13	PH8, PH9, PH10, PH11, PH12, PH13
14	PI0, PI1, PI2, PI3, PI4, PI5, PI6, PI7
15	PI8, PI9, PI10, PI11, PI12, PI13, PI14, PI15
16	$\overline{\text{AMS0}}$, $\overline{\text{AMS1}}$, $\overline{\text{AMS2}}$, $\overline{\text{AMS3}}$, $\overline{\text{AOE}}$, CLKBUF, $\overline{\text{NMI}}$
17	CLKIN, XTAL, $\overline{\text{RESET}}$, RTXI, RTXO, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$
18	D0, D1, D2, D3, D4, D5, D6, D7
19	D8, D9, D10, D11, D12
20	D13, D14, D15, $\overline{\text{ABE0}}$, $\overline{\text{ABE1}}$
21	EXT_WAKE, CLKOUT, PJ11, PJ12, PJ13
22	PJ0, PJ1, PJ2, PJ3, PJ4, PJ5, PJ6, PJ7, $\overline{\text{ATAPI\_PDIAG}}$
23	PJ8, PJ9, PJ10, PE7, PG12, PG13
24	PE0, PE1, PE2, PE4, PE5, PE6, PE8, PE9, PE10, PH3, PH4
25	PH0, PH2, PE14, PE15, PG5, PG6, PG7, PG8, PG9, PG10, PG11
26	PC8, PC9, PC10, PC11, PC12, PC13, PE3, PG14, PG15, PH1

TIMING SPECIFICATIONS

Timing specifications are detailed in this section.

Clock and Reset Timing

Table 24 and Figure 10 describe Clock Input and Reset Timing.
Table 25 and Figure 11 describe Clock Out Timing.

Table 24. Clock Input and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN Period[1, 2, 3, 4]	20.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse[2]	8.0		ns
t_{CKINH}	CLKIN High Pulse[2]	8.0		ns
$t_{BUFDLAY}$	CLKIN to CLKBUF Delay		10	ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulsewidth Low[5]	11 t_{CKIN}		ns
t_{RHWFT}	RESET High to First HWAIT/HWAITA Transition (Boot Host Wait Mode)[6, 7, 8, 9]	6100 t_{CKIN} + 7900 t_{SCLK}		ns
	RESET High to First HWAIT/HWAITA Transition (Reset Output Mode)[7, 10, 11]	6100 t_{CKIN}	7000 t_{CKIN}	ns

[1] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 15 and Table 12 on Page 35.
[2] Applies to PLL bypass mode and PLL non-bypass mode.
[3] CLKIN frequency and duty cycle must not change on the fly.
[4] If the DF bit in the PLL_CTL register is set, then the maximum t_{CKIN} period is 50 ns.
[5] Applies after power-up sequence is complete. See Table 26 and Figure 12 for more information about power-up reset timing.
[6] Maximum value not specified due to variation resulting from boot mode selection and OTP memory programming.
[7] Values specified assume no invalidation preboot settings in OTP page PBS00L. Invalidating a PBS set will increase the value by 1875 t_{CKIN} (typically).
[8] Applies only to boot modes BMODE=1, 2, 4, 6, 7, 10, 11, 14, 15.
[9] Use default t_{SCLK} value unless PLL is reprogrammed during preboot. In case of PLL reprogramming use the new t_{SCLK} value and add PLL_LOCKCNT settle time.
[10] When enabled by OTP_RESETOUT_HWAIT bit. If regular HWAIT is not required in an application, the OTP_RESETOUT_HWAIT bit in the same page instructs the HWAIT or HWAITA to simulate reset output functionality. Then an external resistor is expected to pull the signal to the reset level, as the pin itself is in high performance mode during reset.
[11] Variances are mainly dominated by PLL programming instructions in PBS00L page and boot code differences between silicon revisions. The earlier is bypassed in boot mode BMODE = 0. Maximum value assumes PLL programming instructions do not cause the SCLK frequency to decrease.

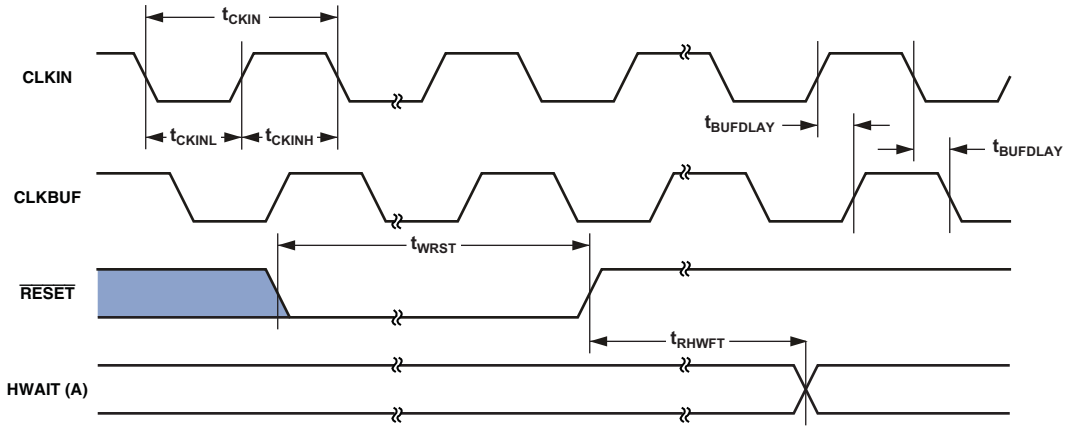


Figure 10. Clock and Reset Timing

DDR SDRAM/Mobile DDR SDRAM Write Cycle Timing

Table 33 and Figure 20 describe DDR SDRAM/mobile DDR SDRAM write cycle timing.

Table 33. DDR SDRAM/Mobile DDR SDRAM Write Cycle Timing

Parameter		DDR SDRAM Min	DDR SDRAM Max	Mobile DDR SDRAM Min	Mobile DDR SDRAM Max	Unit
Switching Characteristics						
t_{DQSS}	Write CMD to First DQS0-1	0.75	1.25	0.75	1.25	t_{CK}
t_{DS}	DQ0-15/DQM0-1 Setup to DQS0-1	0.90		0.90		ns
t_{DH}	DQ0-15/DQM0-1 Hold to DQS0-1	0.90		0.90		ns
t_{DSS}	DQS0-1 Falling to DCK0-1 Rising (DQS0-1 Setup)	0.20		0.20		t_{CK}
t_{DSH}	DQS0-1 Falling from DCK0-1 Rising (DQS0-1 Hold)	0.20		0.20		t_{CK}
t_{DQSH}	DQS0-1 High Pulse Width	0.35		0.40	0.60	t_{CK}
t_{DQSL}	DQS0-1 Low Pulse Width	0.35		0.40	0.60	t_{CK}
t_{WPRE}	DQS0-1 Write Preamble	0.25		0.25		t_{CK}
t_{WPST}	DQS0-1 Write Postamble	0.40	0.60	0.40	0.60	t_{CK}
t_{DOPW}	DQ0-15 and DQM0-1 Output Pulse Width (for Each)	1.75		1.75		ns

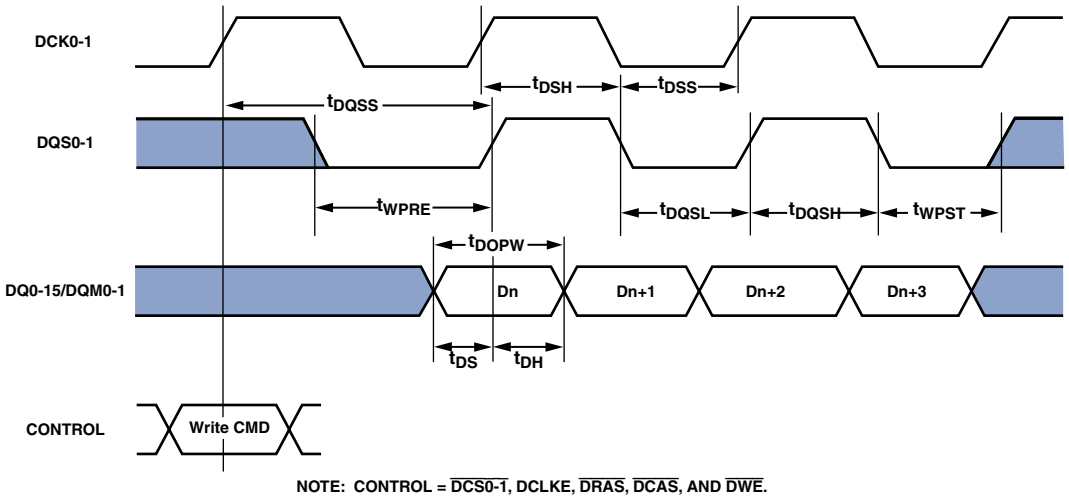


Figure 20. DDR SDRAM /Mobile DDR SDRAM Controller Write Cycle Timing

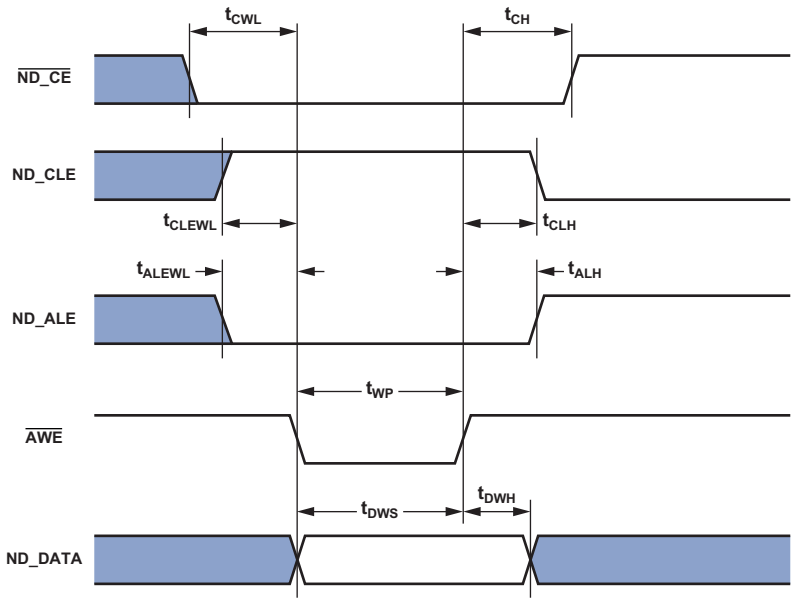


Figure 23. NAND Flash Controller Interface Timing—Command Write Cycle

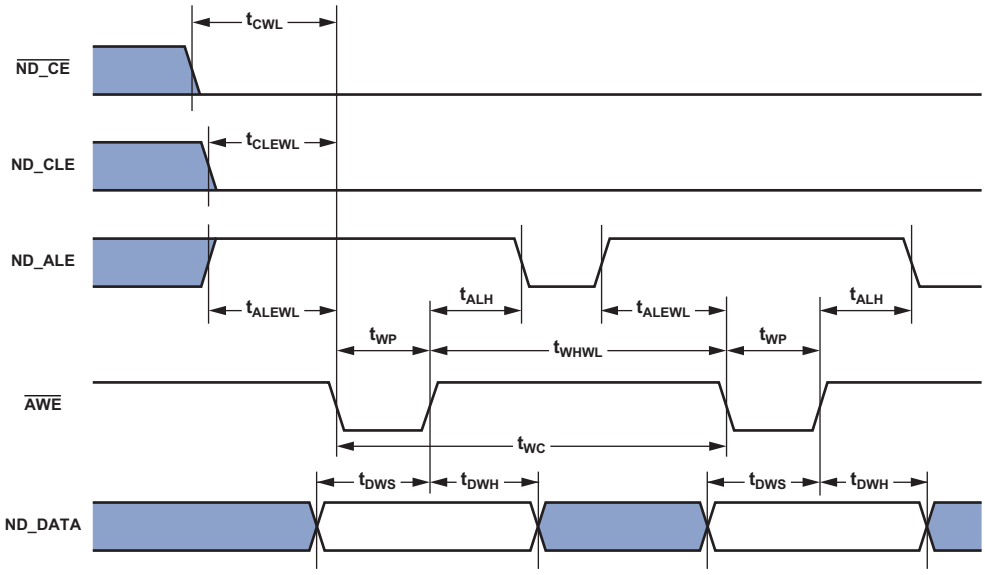


Figure 24. NAND Flash Controller Interface Timing—Address Write Cycle

Serial Ports Timing

Table 40 through Table 43 on Page 63 and Figure 34 on Page 62 through Figure 37 on Page 64 describe serial port operations.

Table 40. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}	TFSx/RFSx Setup Before TSCLKx/RSCLKx (Externally Generated TFSx/RFSx)[1]	3.0		ns
t_{HFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Externally Generated TFSx/RFSx)[1]	3.0		ns
t_{SDRE}	Receive Data Setup Before RSCLKx[1]	3.0		ns
t_{HDRE}	Receive Data Hold After RSCLKx[1]	3.0		ns
t_{SCLKEW}	TSCLKx/RSCLKx Width	4.5		ns
t_{SCLKE}	TSCLKx/RSCLKx Period	15.0[2]		ns
t_{SUDTE}	Start-Up Delay From SPORT Enable To First External TFSx	$4 \times t_{SCLKE}$		ns
t_{SUDRE}	Start-Up Delay From SPORT Enable To First External RFSx	$4 \times t_{RCLKE}$		ns
Switching Characteristics				
t_{DFSE}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[3]		10.0	ns
t_{HOFSE}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[3]	0.0		ns
t_{DDTE}	Transmit Data Delay After TSCLKx[3]		10.0	ns
t_{HDTE}	Transmit Data Hold After TSCLKx[3]	0.0		ns

[1] Referenced to sample edge.
[2] For receive mode with external RSCLKx and external RFSx only, the maximum specification is 11.11 ns (90 MHz).
[3] Referenced to drive edge.

Table 41. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}	TFSx/RFSx Setup Before TSCLKx/RSCLKx (Externally Generated TFSx/RFSx)[1]	10.0		ns
t_{HFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Externally Generated TFSx/RFSx)[1]	–1.5		ns
t_{SDRI}	Receive Data Setup Before RSCLKx[1]	10.0		ns
t_{HDRI}	Receive Data Hold After RSCLKx[1]	–1.5		ns
Switching Characteristics				
t_{DFSI}	TFSx/RFSx Delay After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]		3.0	ns
t_{HOFSI}	TFSx/RFSx Hold After TSCLKx/RSCLKx (Internally Generated TFSx/RFSx)[2]	–1.0		ns
t_{DDTI}	Transmit Data Delay After TSCLKx[2]		3.0	ns
t_{HDTI}	Transmit Data Hold After TSCLKx[2]	–2.0		ns
t_{SCLKIW}	TSCLKx/RSCLKx Width	4.5		ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 42. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1, 2, 3]		10	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	–2		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1, 2, 3]		3	ns

[1] Referenced to drive edge.
[2] Applicable to multichannel mode only.
[3] TSCLKx is tied to RSCLKx.

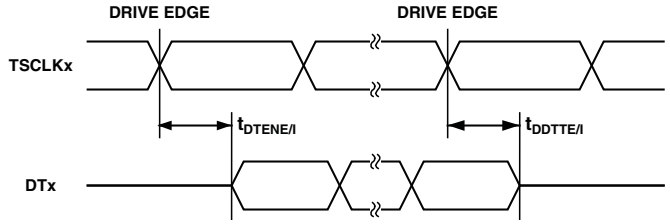


Figure 36. Serial Ports—Enable and Three-State

Table 43. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFSx or External RFSx in multi-channel mode with MFD = 01[1, 2]		10.0	ns
$t_{DTENLFSE}$	Data Enable from External RFSx in multi-channel mode with MFD = 0[1, 2]	0		ns

[1] In multichannel mode, TFSx enable and TFSx valid follow $t_{DTENLFS}$ and $t_{DDTLFSE}$.
[2] If external RFS/TFS setup to RSCLK/TSCLK > $t_{SCLKE}/2$, then $t_{DDTE/I}$ and $t_{DTENE/I}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

Timer Clock Timing

Table 47 and Figure 41 describe timer clock timing.

Table 47. Timer Clock Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{TODP}	Timer Output Update Delay After PPI_CLK High		15	ns

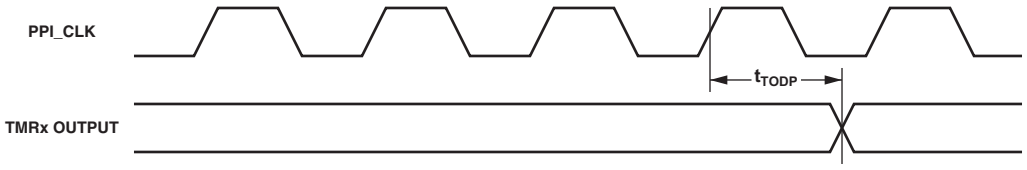


Figure 41. Timer Clock Timing

Up/Down Counter/Rotary Encoder Timing

Table 49 and Figure 43 describe up/down counter/rotary encoder timing.

Table 49. Up/Down Counter/Rotary Encoder Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{WCOUNT}	CUD/CDG/CZM Input Pulse Width	t_{SCLK} + 1		ns
t_{CIS}	CUD/CDG/CZM Input Setup Time Before CLKOUT High[1]	7.2		ns
t_{CIH}	CUD/CDG/CZM Input Hold Time After CLKOUT High[1]	0.0		ns

[1] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize counter inputs.

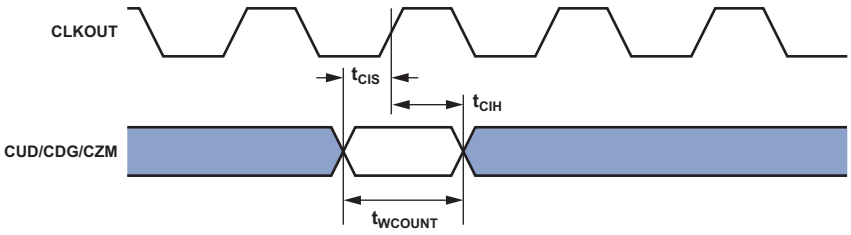


Figure 43. Up/Down Counter/Rotary Encoder Timing

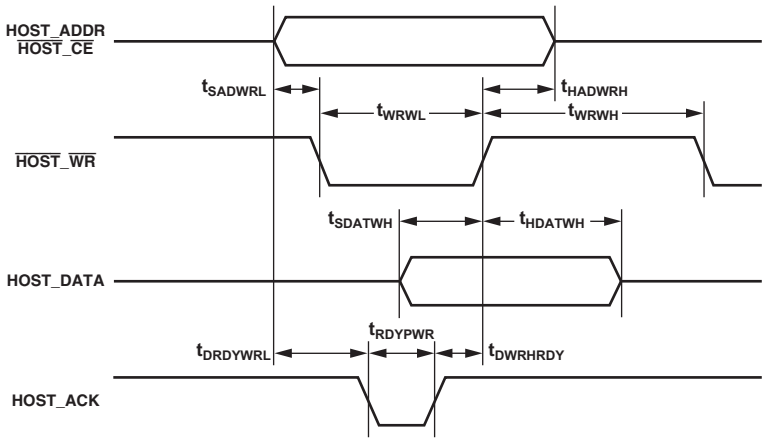
HOSTDP A/C Timing-Host Write Cycle

Table 55 and Figure 47 describe the HOSTDP A/C host write cycle timing requirements.

Table 55. Host Write Cycle Timing Requirements

Parameter		Min	Max	Unit
Timing Requirements				
t_{SADWRL}	HOST_ADDR/$\overline{\text{HOST\_CE}}$ Setup Before $\overline{\text{HOST\_WR}}$ Falling Edge	4		ns
t_{HADWRH}	HOST_ADDR/$\overline{\text{HOST\_CE}}$ Hold After $\overline{\text{HOST\_WR}}$ Rising Edge	2.5		ns
t_{WRWL}	$\overline{\text{HOST\_WR}}$ Pulse Width Low (ACK Mode)	$t_{DRDYWRL} + t_{RDYPRD} + t_{DWRHRDY}$		ns
	$\overline{\text{HOST\_WR}}$ Pulse Width Low (INT Mode)	$1.5 \times t_{SCLK} + 8.7$		ns
t_{WRWH}	$\overline{\text{HOST\_WR}}$ Pulse Width High or Time Between $\overline{\text{HOST\_WR}}$ Rising Edge and $\overline{\text{HOST\_RD}}$ Falling Edge	$2 \times t_{SCLK}$		ns
$t_{DWRHRDY}$	$\overline{\text{HOST\_WR}}$ Rising Edge Delay After HOST_ACK Rising Edge (ACK Mode)	0		ns
t_{HDATWH}	HOST_D15–0 Hold After $\overline{\text{HOST\_WR}}$ Rising Edge	2.5		ns
t_{SDATWH}	HOST_D15–0 Setup Before $\overline{\text{HOST\_WR}}$ Rising Edge	3.5		ns
Switching Characteristics				
$t_{DRDYWRL}$	HOST_ACK Falling Edge After $\overline{\text{HOST\_CE}}$ Asserted (ACK Mode)		11.25	ns
t_{RDYPWR}	HOST_ACK Low Pulse-Width for Write Access (ACK Mode)		NM[1]	ns

[1] NM (not measured)—This parameter is based on t_{SCLK}. It is not measured because the number of SCLK cycles for which HOST_ACK remains low depends on the Host DMA FIFO status. This is system design dependent.



In Figure 47, HOST_DATA is HOST_D0–D15.

Figure 47. HOSTDP A/C- Host Write Cycle

ATAPI Ultra DMA Data-In Transfer Timing

Table 60 and Figure 53 through Figure 56 describe the ATAPI ultra DMA data-in data transfer timing. The material in these figures is adapted from ATAPI-6 (INCITS 361-2002[R2007] and is used with permission of the American National Standards Institute (ANSI) on behalf of the Information Technology Industry Council ("ITIC"). Copies of ATAPI-6 (INCITS 361-2002[R2007] can be purchased from ANSI.

Table 60. ATAPI Ultra DMA Data-In Transfer Timing

ATAPI Parameter		ATAPI_ULTRA_TIM_x Timing Register Setting[1]	Timing Equation
t_{DS}	Data setup time at host	N/A	$T_{SK3} + t_{SUDU}$
t_{DH}	Data hold time at host	N/A	$T_{SK3} + t_{HDU}$
t_{CVS}	CRC word valid setup time at host	TDVS	$TDVS \times t_{SCLK} - (t_{SK1} + t_{SK2})$
t_{CVH}	CRC word valid hold time at host	TACK	$TACK \times t_{SCLK} - (t_{SK1} + t_{SK2})$
t_{LI}	Limited interlock time	N/A	$2 \times t_{BD} + 2 \times t_{SCLK} + t_{OD}$
t_{MLI}	Interlock time with minimum	TZAH, TCVS	$(TZAH + TCVS) \times t_{SCLK} - (4 \times t_{BD} + 4 \times t_{SCLK} + 2 \times t_{OD})$
t_{AZ}	Maximum time allowed for output drivers to release	N/A	0
t_{ZAH}	Minimum delay time required for output	TZAH	$2 \times t_{SCLK} + TZAH \times t_{SCLK} + t_{SCLK}$
t_{ENV}[2]	$\overline{ATAPI\_DMACK}$ to $\overline{ATAPI\_DIOR}/\overline{DIOW}$	TENV	$(TENV \times t_{SCLK}) +/- (t_{SK1} + t_{SK2})$
t_{RP}	$\overline{ATAPI\_DMACK}$ to $\overline{ATAPI\_DIOR}/\overline{DIOW}$	TRP	$TRP \times t_{SCLK} - (t_{SK1} + t_{SK2} + t_{SK4})$
t_{ACK}	Setup and hold times for $\overline{ATAPI\_DMACK}$	TACK	$TACK \times t_{SCLK} - (t_{SK1} + t_{SK2})$

[1] ATAPI Timing Register Setting should be programmed with a value that guarantees parameter compliance with the ATA ANSI specification for ATA device mode of operation.
[2] This timing equation can be used to calculate both the minimum and maximum t_{ENV}.

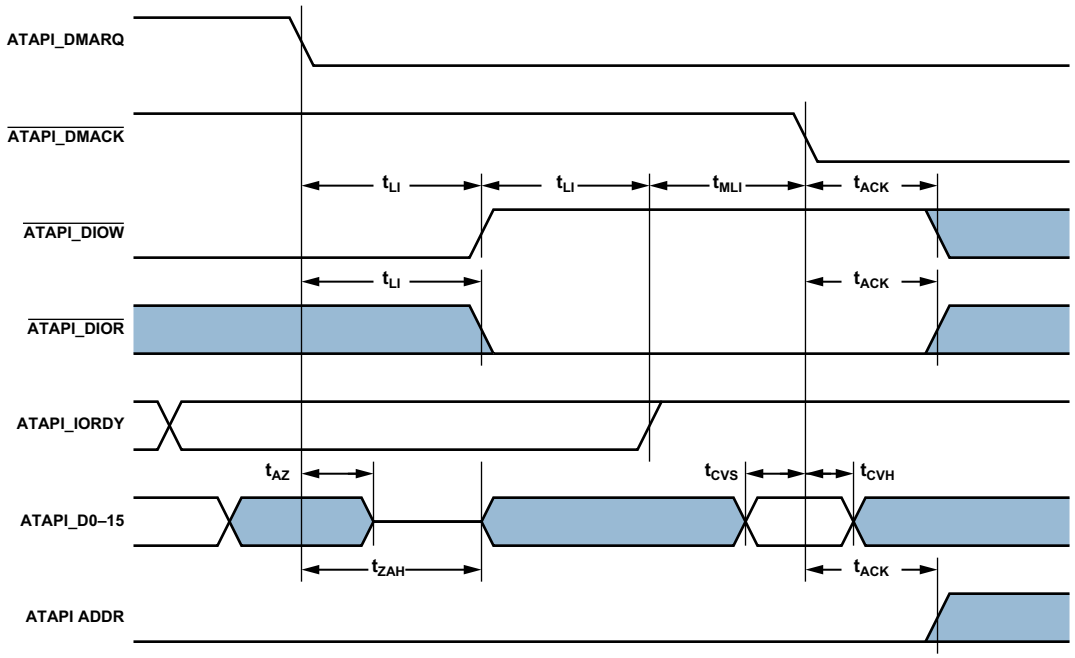


Figure 55. Device Terminating an Ultra DMA Data-In Burst

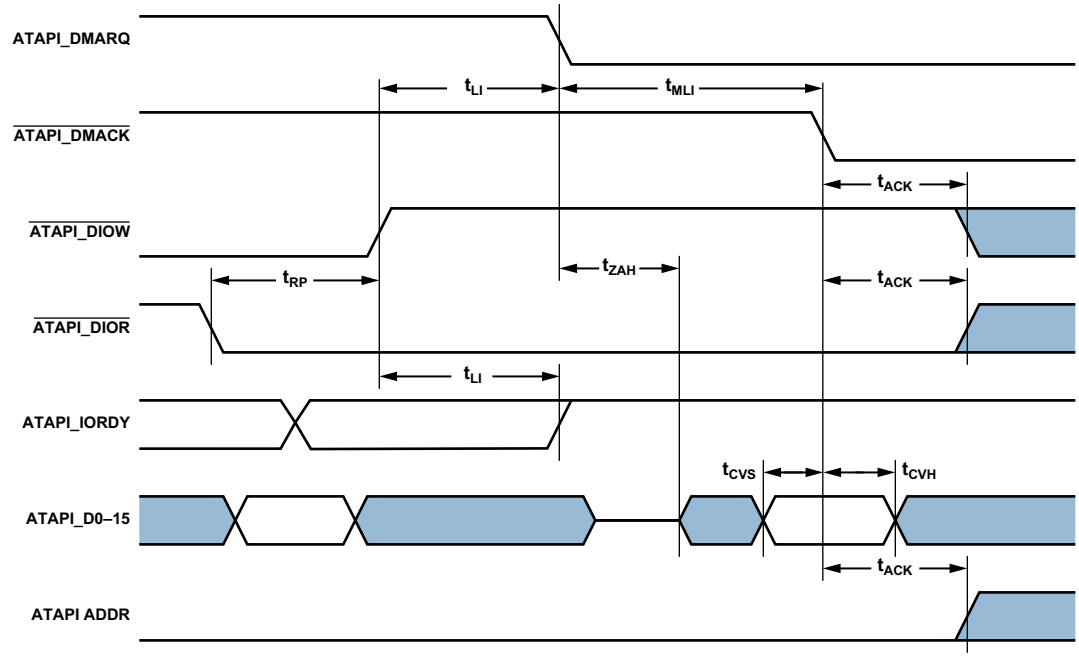


Figure 56. Host Terminating an Ultra DMA Data-In Burst

OUTPUT DRIVE CURRENTS

Figure 62 through Figure 71 show typical current-voltage characteristics for the output drivers of the ADSP-BF54x Blackfin processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

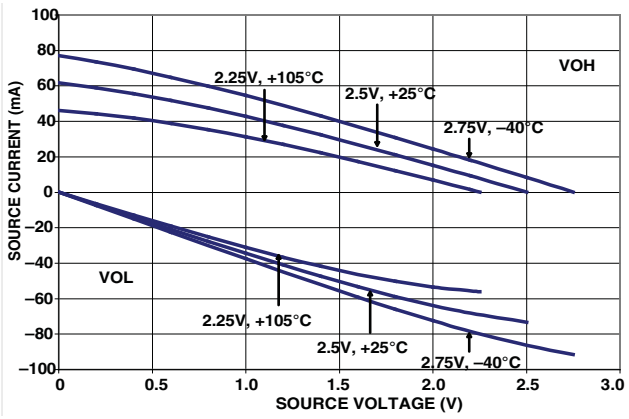


Figure 62. Drive Current A (Low V_{DDEXT})

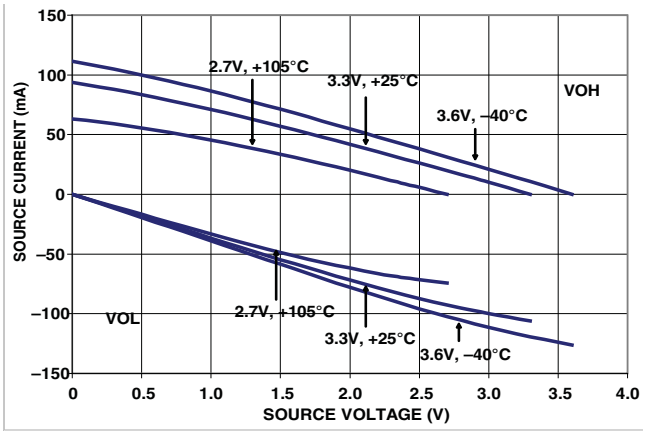


Figure 63. Drive Current A (High V_{DDEXT})

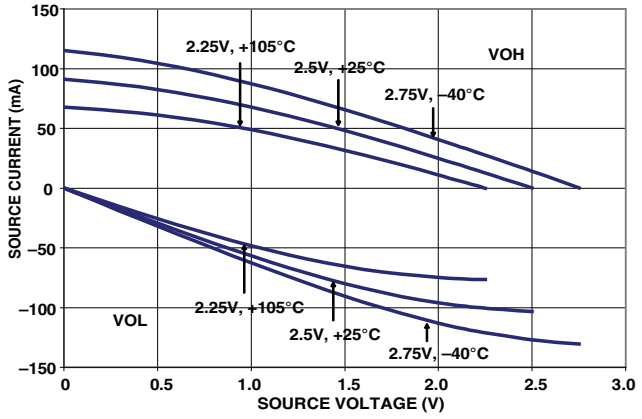


Figure 64. Drive Current B (Low V_{DDEXT})

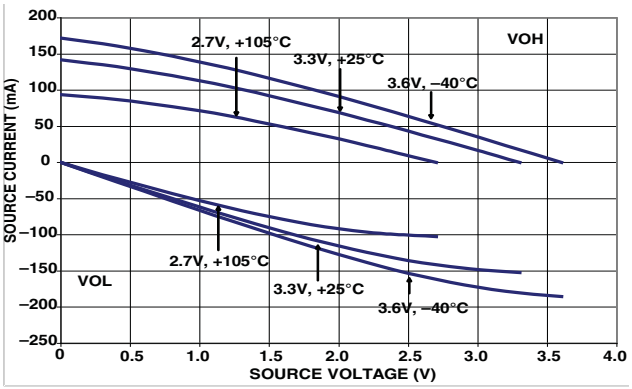


Figure 65. Drive Current B (High V_{DDEXT})

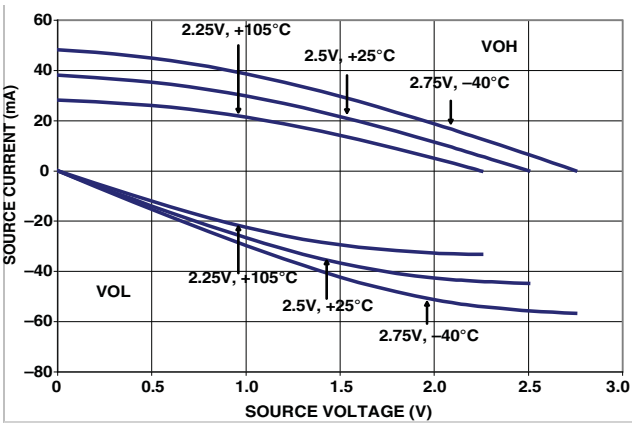


Figure 66. Drive Current C (Low V_{DDEXT})

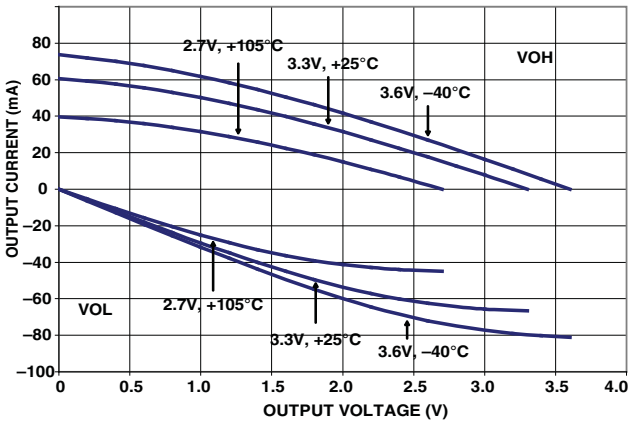


Figure 67. Drive Current C (High V_{DDEXT})

Table 66 lists the CSP_BGA package by ball number for the ADSP-BF549. Table 65 on Page 94 lists the CSP_BGA package by signal.

Table 66. 400-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	GND	C1	MXO	E1	USB_DP	G1	PC5
A2	A2	C2	MXI	E2	USB_DM	G2	PC4
A3	PI0	C3	PH5	E3	GND	G3	USB_ID
A4	PI2	C4	PH9	E4	MLF_P	G4	V_{DDUSB}
A5	PI4	C5	PH11	E5	V_{DDEXT}	G5	V_{DDEXT}
A6	PI6	C6	PH13	E6	MFS	G6	V_{DDEXT}
A7	PI8	C7	PH10	E7	GND_{MP}	G7	V_{DDEXT}
A8	PI11	C8	PI9	E8	V_{DDMP}	G8	V_{DDINT}
A9	PI12	C9	PI13	E9	V_{DDEXT}	G9	GND
A10	$\overline{AMS0}$	C10	$\overline{AOE}$	E10	V_{DDEXT}	G10	GND
A11	CLKIN	C11	$\overline{NMI}$	E11	V_{DDEXT}	G11	GND
A12	XTAL	C12	$\overline{RESET}$	E12	V_{DDEXT}	G12	V_{DDINT}
A13	GND	C13	D1	E13	V_{DDRTC}	G13	V_{DDINT}
A14	RTXI	C14	D8	E14	D14	G14	V_{DDEXT}
A15	D4	C15	D9	E15	D13	G15	V_{DDDDR}
A16	D6	C16	$\overline{ABE1}$	E16	$\overline{DCLK0}$	G16	DA4
A17	D10	C17	$\overline{ABE0}$	E17	$\overline{DRAS}$	G17	DA1
A18	$VROUT_0$	C18	DCLK1	E18	$\overline{DWE}$	G18	DA3
A19	$VROUT_1$	C19	$\overline{DCS0}$	E19	DA9	G19	DA0
A20	GND	C20	DA7	E20	DA2	G20	DQM0
B1	USB_VREF	D1	GND	F1	USB_XI	H1	PC3
B2	A1	D2	USB_VBUS	F2	USB_XO	H2	PC0
B3	A3	D3	USB_RSET	F3	GND	H3	PC7
B4	PI1	D4	GND	F4	MLF_M	H4	PH7
B5	PI3	D5	PH8	F5	V_{DDUSB}	H5	V_{DDEXT}
B6	PI5	D6	PH6	F6	GND	H6	V_{DDEXT}
B7	PI7	D7	PH12	F7	V_{DDEXT}	H7	GND
B8	PI10	D8	PI14	F8	V_{DDEXT}	H8	GND
B9	PI15	D9	$\overline{AMS1}$	F9	V_{DDINT}	H9	GND
B10	$\overline{AMS2}$	D10	$\overline{AMS3}$	F10	V_{DDDDR}	H10	GND
B11	GND	D11	CLKBUF	F11	V_{DDDDR}	H11	GND
B12	$\overline{ARE}$	D12	$\overline{AWE}$	F12	V_{DDDDR}	H12	GND
B13	D2	D13	D0	F13	V_{DDEXT}	H13	V_{DDDDR}
B14	RTXO	D14	D11	F14	GND	H14	V_{DDDDR}
B15	D3	D15	D12	F15	V_{DDVR}	H15	V_{DDDDR}
B16	D5	D16	DCLK0	F16	$\overline{DCAS}$	H16	DBA1
B17	D7	D17	D15	F17	DA11	H17	DBA0
B18	DCLKE	D18	$\overline{DCLK1}$	F18	DA8	H18	DQS1
B19	$\overline{DCS1}$	D19	DA12	F19	DA5	H19	DQM1
B20	DA10	D20	DA6	F20	DQS0	H20	DQ11