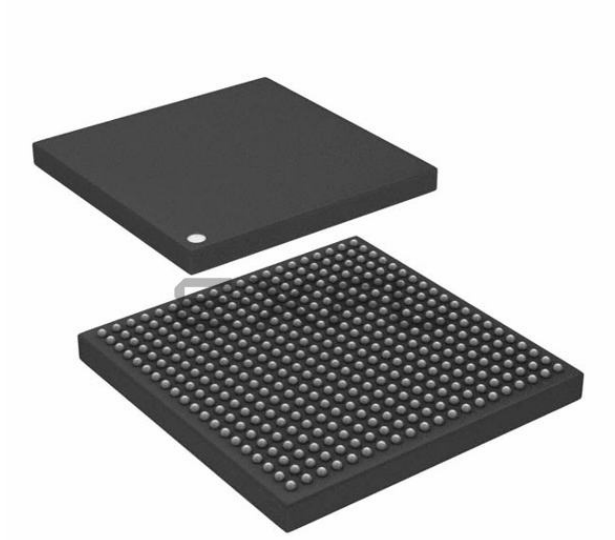


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	196kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf544bbcz-4a

- SIC interrupt mask registers (SIC_IMASKx). These registers control the masking and unmasking of each peripheral interrupt event. When a bit is set in a register, that peripheral event is unmasked and is processed by the system when asserted. A cleared bit in the register masks the peripheral event, preventing the processor from servicing the event.
- SIC interrupt status registers (SIC_ISRx). As multiple peripherals can be mapped to a single event, these registers allow the software to determine which peripheral event source triggered the interrupt. A set bit indicates the peripheral is asserting the interrupt, and a cleared bit indicates the peripheral is not asserting the event.
- SIC interrupt wakeup enable registers (SIC_IWRx). By enabling the corresponding bit in this register, a peripheral can be configured to wake up the processor, should the core be idled or in Sleep mode when the event is generated. (For more information, see Dynamic Power Management on Page 15.)

Because multiple interrupt sources can map to a single general-purpose interrupt, multiple pulse assertions can occur simultaneously, before or during interrupt processing for an interrupt event already detected on this interrupt input. The IPEND register contents are monitored by the SIC as the interrupt acknowledgement.

The appropriate ILAT register bit is set when an interrupt rising edge is detected. (Detection requires two core clock cycles.) The bit is cleared when the respective IPEND register bit is set. The IPEND bit indicates that the event has entered into the processor pipeline. At this point the CEC recognizes and queues the next rising edge event on the corresponding event input. The minimum latency from the rising edge transition of the general-purpose interrupt to the IPEND output asserted is three core clock cycles; however, the latency can be much higher, depending on the activity within and the state of the processor.

DMA CONTROLLERS

ADSP-BF54x Blackfin processors have multiple, independent DMA channels that support automated data transfers with minimal overhead for the processor core. DMA transfers can occur between the ADSP-BF54x processors' internal memories and any of the DMA-capable peripherals. Additionally, DMA transfers can be accomplished between any of the DMA-capable peripherals and external devices connected to the external memory interfaces, including DDR and asynchronous memory controllers.

While the USB controller and MXVR have their own dedicated DMA controllers, the other on-chip peripherals are managed by two centralized DMA controllers, called DMAC1 (32-bit) and DMAC0 (16-bit). Both operate in the SCLK domain. Each DMA controller manages 12 independent peripheral DMA channels, as well as two independent memory DMA streams. The DMAC1 controller masters high-bandwidth peripherals over a dedicated 32-bit DMA access bus (DAB32). Similarly, the DMAC0 controller masters most serial interfaces over the 16-bit DAB16 bus. Individual DMA channels have fixed access priority on the DAB buses. DMA priority of peripherals is managed by a flexible peripheral-to-DMA channel assignment scheme.

All four DMA controllers use the same 32-bit DCB bus to exchange data with L1 memory. This includes L1 ROM, but excludes scratchpad memory. Fine granulation of L1 memory and special DMA buffers minimize potential memory conflicts when the L1 memory is accessed simultaneously by the core. Similarly, there are dedicated DMA buses between the external bus interface unit (EBIU) and the three DMA controllers (DMAC1, DMAC0, and USB) that arbitrate DMA accesses to external memories and the boot ROM.

The ADSP-BF54x Blackfin processors' DMA controllers support both 1-dimensional (1D) and 2-dimensional (2D) DMA transfers. DMA transfer initialization can be implemented from registers or from sets of parameters called descriptor blocks.

The 2D DMA capability supports arbitrary row and column sizes up to 64K elements by 64K elements, and arbitrary row and column step sizes up to ±32K elements. Furthermore, the column step size can be less than the row step size, allowing implementation of interleaved data streams. This feature is especially useful in video applications where data can be de-interleaved on the fly.

Examples of DMA types supported by the ADSP-BF54x Blackfin processors' DMA controllers include:

- A single, linear buffer that stops upon completion
- A circular, auto-refreshing buffer that interrupts on each full or fractionally full buffer
- 1D or 2D DMA using a linked list of descriptors
- 2D DMA using an array of descriptors, specifying only the base DMA address within a common page

In addition to the dedicated peripheral DMA channels, the DMAC1 and DMAC0 controllers each feature two memory DMA channel pairs for transfers between the various memories of the ADSP-BF54x Blackfin processors. This enables transfers of blocks of data between any of the memories—including external DDR, ROM, SRAM, and flash memory—with minimal processor intervention. Like peripheral DMAs, memory DMA transfers can be controlled by a very flexible descriptor-based methodology or by a standard register-based autobuffer mechanism.

The memory DMA channels of the DMAC1 controller (MDMA2 and MDMA3) can be controlled optionally by the external DMA request input pins. When used in conjunction with the External Bus Interface Unit (EBIU), this handshaked memory DMA (HMDMA) scheme can be used to efficiently exchange data with block-buffered or FIFO-style devices connected externally. Users can select whether the DMA request pins control the source or the destination side of the memory DMA. It allows control of the number of data transfers for memory DMA. The number of transfers per edge is programmable. This feature can be programmed to allow memory DMA to have an increased priority on the external bus relative to the core.

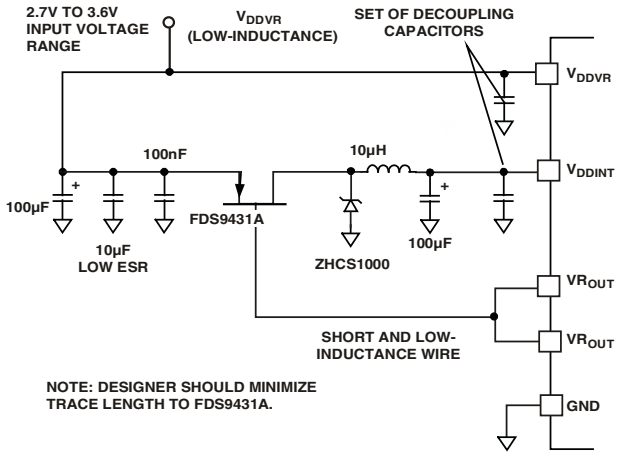


Figure 6. Voltage Regulator Circuit

CLOCK SIGNALS

The ADSP-BF54x Blackfin processors can be clocked by an external crystal, a sine wave input, or a buffered, shaped clock derived from an external clock oscillator.

If an external clock is used, it should be a TTL-compatible signal and must not be halted, changed, or operated below the specified frequency during normal operation. This signal is connected to the processor's CLKIN pin. When an external clock is used, the XTAL pin must be left unconnected.

Alternatively, because the ADSP-BF54x Blackfin processors include an on-chip oscillator circuit, an external crystal may be used. For fundamental frequency operation, use the circuit shown in Figure 7. A parallel-resonant, fundamental frequency, microprocessor-grade crystal is connected across the CLKIN and XTAL pins. The on-chip resistance between CLKIN and the XTAL pin is in the 500 kΩ range. Typically, further parallel resistors are not recommended. The two capacitors and the series resistor shown in Figure 7 fine-tune phase and amplitude of the sine frequency. The 1MOhm pull-up resistor on the XTAL pin guarantees that the clock circuit is properly held inactive when the processor is in the hibernate state.

The capacitor and resistor values shown in Figure 7 are typical values only. The capacitor values are dependent upon the crystal manufacturers' load capacitance recommendations and the PCB physical layout. The resistor value depends on the drive level specified by the crystal manufacturer. System designs should verify the customized values based on careful investigations on multiple devices over temperature range.

A third-overtone crystal can be used at frequencies above 25 MHz. The circuit is then modified to ensure crystal operation only at the third overtone by adding a tuned inductor circuit as shown in Figure 7. A design procedure for third-overtone operation is discussed in detail in an Application Note, *Using Third Overtone Crystals (EE-168)*.

The Blackfin core runs at a different clock rate than the on-chip peripherals. As shown in Figure 8 on Page 17, the core clock (CCLK) and system peripheral clock (SCLK) are derived from

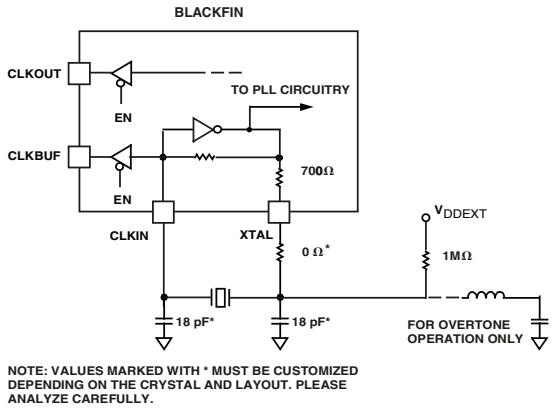
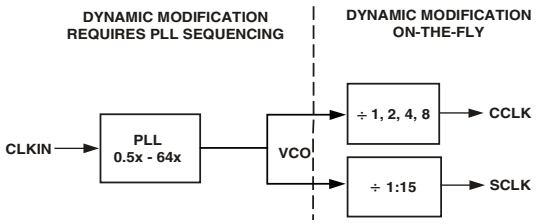


Figure 7. External Crystal Connections

the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a programmable 0.5× to 64× multiplication factor (bounded by specified minimum and maximum VCO frequencies). The default multiplier is 8×, but it can be modified by a software instruction sequence. This sequence is managed by the bfrom_SysControl() function in the on-chip ROM.

On-the-fly CCLK and SCLK frequency changes can be applied by using the bfrom_SysControl() function in the on-chip ROM. Whereas the maximum allowed CCLK and SCLK rates depend on the applied voltages V_{DDINT} and V_{DDEXT}, the VCO is always permitted to run up to the frequency specified by the part's speed grade.

The CLKOUT pin reflects the SCLK frequency to the off-chip world. It functions as a reference for many timing specifications. While inactive by default, it can be enabled using the EBIU_AMGCTL register.



Note: For CCLK and SCLK specifications, see Table 15.

Figure 8. Frequency Modification Methods

All on-chip peripherals are clocked by the system clock (SCLK). The system clock frequency is programmable by means of the SSEL3–0 bits of the PLL_DIV register. The values programmed into the SSEL fields define a divide ratio between the PLL output (VCO) and the system clock. SCLK divider values are 1 through 15. Table 6 illustrates typical system clock ratios. The default ratio is 4.

- Boot from 16-bit asynchronous FIFO (BMODE = 0x2)—In this mode, the boot kernel starts booting from address 0x2030 0000. Every 16-bit word that the boot kernel has to read from the FIFO must be requested by a low pulse on the DMAR1 pin.
- Boot from serial SPI memory, EEPROM or flash (BMODE = 0x3)—8-, 16-, 24- or 32-bit addressable devices are supported. The processor uses the PE4 GPIO pin to select a single SPI EEPROM or flash device and uses SPI0 to submit a read command and successive address bytes (0x00) until a valid 8-, 16-, 24-, or 32-bit addressable device is detected. Pull-up resistors are required on the $\overline{\text{SPI0SEL1}}$ and SPI0MISO pins. By default, a value of 0x85 is written to the SPI0_BAUD register.
- Boot from SPI host device (BMODE = 0x4)—The processor operates in SPI slave mode (using SPI0) and is configured to receive the bytes of the .LDR file from an SPI host (master) agent. The HWAIT signal must be interrogated by the host before every transmitted byte. A pull-up resistor is required on the $\overline{\text{SPI0SS}}$ input. A pull-down resistor on the serial clock (SPI0SCK) may improve signal quality and booting robustness.
- Boot from serial TWI memory, EEPROM or flash (BMODE = 0x5)—The processor operates in master mode (using TWI0) and selects the TWI slave with the unique ID 0xA0. The processor submits successive read commands to the memory device starting at two-byte internal address 0x0000 and begins clocking data into the processor. The TWI memory device should comply with Philips I^2C Bus Specification version 2.1 and have the capability to autoincrement its internal address counter such that the contents of the memory device can be read sequentially. By default, a prescale value of 0xA and CLKDIV value of 0x0811 is used. Unless altered by OTP settings, an I^2C memory that takes two address bytes is assumed. Development tools ensure that data that is booted to memories that cannot be accessed by the Blackfin core is written to an intermediate storage place and then copied to the final destination via memory DMA.
- Boot from TWI host (BMODE = 0x6)—The TWI host agent selects the slave with the unique ID 0x5F. The processor (using TWI0) replies with an acknowledgement, and the host can then download the boot stream. The TWI host agent should comply with Philips I^2C Bus Specification version 2.1. An I^2C multiplexer can be used to select one processor at a time when booting multiple processors from a single TWI.
- Boot from UART host (BMODE = 0x7)—In this mode, the processor uses UART1 as the booting source. Using an autobaud handshake sequence, a boot-stream-formatted program is downloaded by the host. The host agent selects a bit rate within the UART's clocking capabilities.

  When performing the autobaud, the UART expects an "@" (0x40) character (eight data bits, one start bit, one stop bit, no parity bit) on the UART1RX pin to determine the bit rate. It then replies with an acknowledgement, which is composed of four bytes (0xBF, the value of UART1_DLL, the value of UART1_DLH, and finally 0x00). The host can then download the boot stream. The processor deasserts the $\overline{\text{UART1RTS}}$ output to hold off the host; $\overline{\text{UART1CTS}}$ functionality is not enabled at boot time.
- Boot from (DDR) SDRAM (BMODE = 0xA)—In this mode, the boot kernel starts booting from address 0x0000 0010. This is a warm boot scenario only. The SDRAM is expected to contain a valid boot stream and the SDRAM controller must have been configured by the OTP settings.
- Boot from 8-bit and 16-bit external NAND flash memory (BMODE = 0xD)—In this mode, auto detection of the NAND flash device is performed. The processor configures PORTJ GPIO pins PJ1 and PJ2 to enable the $\overline{\text{ND\_CE}}$ and $\overline{\text{ND\_RB}}$ signals, respectively. For correct device operation, pull-up resistors are required on both $\overline{\text{ND\_CE}}$ (PJ1) and $\overline{\text{ND\_RB}}$ (PJ2) signals. By default, a value of 0x0033 is written to the NFC_CTL register. The booting procedure always starts by booting from byte 0 of block 0 of the NAND flash device. In this boot mode, the HWAIT signal does not toggle. The respective GPIO pin remains in the high-impedance state.

  NAND flash boot supports the following features:

  - Device auto detection
  - Error detection and correction for maximum reliability
  - No boot stream size limitation
  - Peripheral DMA via channel 22, providing efficient transfer of all data (excluding the ECC parity data)
  - Software-configurable boot mode for booting from boot streams expanding multiple blocks, including bad blocks
  - Software-configurable boot mode for booting from multiple copies of the boot stream allowing for handling of bad blocks and uncorrectable errors
  - Configurable timing via OTP memory

  Small page NAND flash devices must have a 512-byte page size, 32 pages per block, a 16-byte spare area size and a bus configuration of eight bits. By default, all read requests from the NAND flash are followed by four address cycles. If the NAND flash device requires only three address cycles, then the device must be capable of ignoring the additional address cycle.

  The small page NAND flash device must comply with the following command set:

Reset: 0xFF
Read lower half of page: 0x00
Read upper half of page: 0x01
Read spare area: 0x50

Table 11. Pin Descriptions

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
Port A: GPIO/*SPORT2–3/TMR4–7*			
PA0/*TFS2*	I/O	GPIO/*SPORT2 Transmit Frame Sync*	C
PA1/*DT2SEC/TMR4*	I/O	GPIO/*SPORT2 Transmit Data Secondary/Timer 4*	C
PA2/*DT2PRI*	I/O	GPIO/*SPORT2 Transmit Data Primary*	C
PA3/*TSCLK2*	I/O	GPIO/*SPORT2 Transmit Serial Clock*	A
PA4/*RFS2*	I/O	GPIO/*SPORT2 Receive Frame Sync*	C
PA5/*DR2SEC/TMR5*	I/O	GPIO/*SPORT2 Receive Data Secondary/Timer 5*	C
PA6/*DR2PRI*	I/O	GPIO/*SPORT2 Receive Data Primary*	C
PA7/*RSCLK2/TACLK0*	I/O	GPIO/*SPORT2 Receive Serial Clock/Alternate Input Clock 0*	A
PA8/*TFS3/TACLK1*	I/O	GPIO/*SPORT3 Transmit Frame Sync/Alternate Input Clock 1*	C
PA9/*DT3SEC/TMR6*	I/O	GPIO/*SPORT3 Transmit Data Secondary/Timer 6*	C
PA10/*DT3PRI/TACLK2*	I/O	GPIO/*SPORT3 Transmit Data Primary/Alternate Input Clock 2*	C
PA11/*TSCLK3/TACLK3*	I/O	GPIO/*SPORT3 Transmit Serial Clock/Alternate Input Clock 3*	A
PA12/*RFS3/TACLK4*	I/O	GPIO/*SPORT3 Receive Frame Sync/Alternate Input Clock 4*	C
PA13/*DR3SEC/TMR7/TACLK5*	I/O	GPIO/*SPORT3 Receive Data Secondary/Timer 7/Alternate Input Clock 5*	C
PA14/*DR3PRI/TACLK6*	I/O	GPIO/*SPORT3 Receive Data Primary/Alternate Input Clock 6*	C
PA15/*RSCLK3/TACLK7 and TACI7*	I/O	GPIO/*SPORT3 Receive Serial Clock/Alt Input Clock 7 and Alt Capture Input 7*	A
Port B: GPIO/*TWI1/UART2–3/SPI2/TMR0–3*			
PB0/*SCL1*	I/O	GPIO/*TWI1 Serial Clock* (Open-drain output: requires a pull-up resistor.)	E
PB1/*SDA1*	I/O	GPIO/*TWI1 Serial Data* (Open-drain output: requires a pull-up resistor.)	E
PB2/$\overline{\textit{UART3RTS}}$	I/O	GPIO/*UART3 Request to Send*	C
PB3/$\overline{\textit{UART3CTS}}$	I/O	GPIO/*UART3 Clear to Send*	A
PB4/*UART2TX*	I/O	GPIO/*UART2 Transmit*	A
PB5/*UART2RX/TACI2*	I/O	GPIO/*UART2 Receive/Alternate Capture Input 2*	A
PB6/*UART3TX*	I/O	GPIO/*UART3 Transmit*	A
PB7/*UART3RX/TACI3*	I/O	GPIO/*UART3 Receive/Alternate Capture Input 3*	A
PB8/$\overline{\textit{SPI2SS}}$/*TMR0*	I/O	GPIO/*SPI2 Slave Select Input/Timer 0*	A
PB9/$\overline{\textit{SPI2SEL1}}$/*TMR1*	I/O	GPIO/*SPI2 Slave Select Enable 1/Timer 1*	A
PB10 $\overline{\textit{SPI2SEL2}}$/*TMR2*	I/O	GPIO/*SPI2 Slave Select Enable 2/Timer 2*	A
PB11/$\overline{\textit{SPI2SEL3}}$/*TMR3/HWAIT*	I/O	GPIO/*SPI2 Slave Select Enable 3/Timer 3/Boot Host Wait*	A
PB12/*SPI2SCK*	I/O	GPIO/*SPI2 Clock*	A
PB13/*SPI2MOSI*	I/O	GPIO/*SPI2 Master Out Slave In*	C
PB14/*SPI2MISO*	I/O	GPIO/*SPI2 Master In Slave Out*	C

Parameter		Test Conditions	Nonautomotive 400 MHz[1] Min	Typ	Max	All Other Devices[2] Min	Typ	Max	Unit
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.10 V, f_{CCLK} = 300 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00		145			178		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.20 V, f_{CCLK} = 400 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00		199			239		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.25 V, f_{CCLK} = 533 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00					301		mA
I_{DD-TYP}	V_{DDINT} Current	V_{DDINT} = 1.35 V, f_{CCLK} = 600 MHz, f_{SCLK} = 25 MHz, T_J = 25°C, ASF = 1.00					360		mA
$I_{DDHIBERNATE}$[13, 14]	Hibernate State Current	V_{DDEXT} = V_{DDVR} = V_{DDUSB} = 3.30 V, V_{DDDDR} = 2.5 V, T_J = 25°C, CLKIN= 0 MHz with voltage regulator off (V_{DDINT} = 0 V)		60			60		µA
I_{DDRTC}	V_{DDRTC} Current	V_{DDRTC} = 3.3 V, T_J = 25°C		20			20		µA
$I_{DDUSB-FS}$	V_{DDUSB} Current in Full/Low Speed Mode	V_{DDUSB} = 3.3 V, T_J = 25°C, Full Speed USB Transmit		9			9		mA
$I_{DDUSB-HS}$	V_{DDUSB} Current in High Speed Mode	V_{DDUSB} = 3.3 V, T_J = 25°C, High Speed USB Transmit		25			25		mA
$I_{DDDEEPSLEEP}$[13, 15]	V_{DDINT} Current in Deep Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} = 0 MHz			Table 16			Table 17	mA
$I_{DDSLEEP}$[13, 15]	V_{DDINIT} Current in Sleep Mode	f_{CCLK} = 0 MHz, f_{SCLK} > 0 MHz			$I_{DDDEEPSLEEP}$ + (0.77 × V_{DDINT} × f_{SCLK})[16]			$I_{DDDEEPSLEEP}$ + (0.77 × V_{DDINT} × f_{SCLK})[16]	mA[16]
I_{DDINT}[15, 17]	V_{DDINT} Current	f_{CCLK} > 0 MHz, f_{SCLK} > 0 MHz			$I_{DDSLEEP}$ + (Table 19 × ASF)			$I_{DDSLEEP}$ + (Table 19 × ASF)	mA

[1] Applies to all nonautomotive 400 MHz speed grade models and all extended temperature grade models. See Ordering Guide.
[2] Applies to all 533 MHz and 600 MHz speed grade models and automotive 400 MHz speed grade models. See Ordering Guide.
[3] Applies to output and bidirectional pins, except USB_VBUS and the pins listed in table note 4.
[4] Applies to pins DA0–12, DBA0–1, DQ0–15, DQS0–1, DQM0–1, DCLK1–2, $\overline{\text{DCLK1–2}}$, $\overline{\text{DCS0–1}}$, DCLKE, $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, and $\overline{\text{DWE}}$.
[5] Applies to all input pins except JTAG inputs.
[6] Applies to JTAG input pins (TCK, TDI, TMS, $\overline{\text{TRST}}$).
[7] Applies to DDR_VREF pin.
[8] Absolute value.
[9] For DDR pins (DQ0-15, DQS0-1), test conditions are V_{DDDDR} = Maximum, V_{IN} = V_{DDDDR} Maximum.
[10] Applies to three-statable pins.
[11] For DDR pins (DQ0-15, DQS0-1), test conditions are V_{DDDDR} = Maximum, V_{IN} = 0 V.
[12] Guaranteed, but not tested.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Figure 9 and Table 23 provides information related to specific product features. For a complete listing of product offerings, see the Ordering Guide on Page 101.

Figure 9. Product Information on Package

Table 23. Package Information

Brand Key	Description
BF54x	x = 2, 4, 7, 8 or 9
(M)	Mobile DDR Indicator (Optional)
t	Temperature Range
pp	Package Type
Z	RoHS Compliant Part (Optional)
cc	See Ordering Guide
vvvvvv.x-q	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliant Designation
yyww	Date Code

TIMING SPECIFICATIONS

Timing specifications are detailed in this section.

Clock and Reset Timing

Table 24 and Figure 10 describe Clock Input and Reset Timing.
Table 25 and Figure 11 describe Clock Out Timing.

Table 24. Clock Input and Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{CKIN}	CLKIN Period[1, 2, 3, 4]	20.0	100.0	ns
t_{CKINL}	CLKIN Low Pulse[2]	8.0		ns
t_{CKINH}	CLKIN High Pulse[2]	8.0		ns
$t_{BUFDLAY}$	CLKIN to CLKBUF Delay		10	ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulsewidth Low[5]	11 t_{CKIN}		ns
t_{RHWFT}	RESET High to First HWAIT/HWAITA Transition (Boot Host Wait Mode)[6, 7, 8, 9]	6100 t_{CKIN} + 7900 t_{SCLK}		ns
	RESET High to First HWAIT/HWAITA Transition (Reset Output Mode)[7, 10, 11]	6100 t_{CKIN}	7000 t_{CKIN}	ns

[1] Combinations of the CLKIN frequency and the PLL clock multiplier must not exceed the allowed f_{VCO}, f_{CCLK}, and f_{SCLK} settings discussed in Table 15 and Table 12 on Page 35.
[2] Applies to PLL bypass mode and PLL non-bypass mode.
[3] CLKIN frequency and duty cycle must not change on the fly.
[4] If the DF bit in the PLL_CTL register is set, then the maximum t_{CKIN} period is 50 ns.
[5] Applies after power-up sequence is complete. See Table 26 and Figure 12 for more information about power-up reset timing.
[6] Maximum value not specified due to variation resulting from boot mode selection and OTP memory programming.
[7] Values specified assume no invalidation preboot settings in OTP page PBS00L. Invalidating a PBS set will increase the value by 1875 t_{CKIN} (typically).
[8] Applies only to boot modes BMODE=1, 2, 4, 6, 7, 10, 11, 14, 15.
[9] Use default t_{SCLK} value unless PLL is reprogrammed during preboot. In case of PLL reprogramming use the new t_{SCLK} value and add PLL_LOCKCNT settle time.
[10] When enabled by OTP_RESETOUT_HWAIT bit. If regular HWAIT is not required in an application, the OTP_RESETOUT_HWAIT bit in the same page instructs the HWAIT or HWAITA to simulate reset output functionality. Then an external resistor is expected to pull the signal to the reset level, as the pin itself is in high performance mode during reset.
[11] Variances are mainly dominated by PLL programming instructions in PBS00L page and boot code differences between silicon revisions. The earlier is bypassed in boot mode BMODE = 0. Maximum value assumes PLL programming instructions do not cause the SCLK frequency to decrease.

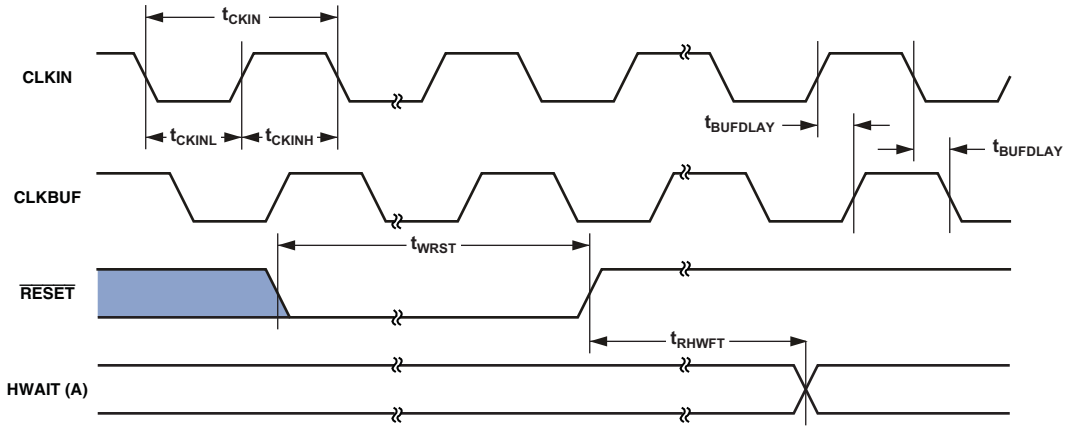


Figure 10. Clock and Reset Timing

Table 28. Asynchronous Memory Read Cycle Timing with Asynchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA15–0 Setup Before CLKOUT	5.0		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
t_{DANR}	ARDY Negated Delay from $\overline{AMSx}$ Asserted[1]		$(S + RA - 2) \times t_{SCLK}$	ns
t_{HAA}	ARDY Asserted Hold After $\overline{ARE}$ Negated	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[2]		6.0	ns
t_{HO}	Output Hold After CLKOUT[2]	0.3		ns

[1] S = number of programmed setup cycles, RA = number of programmed read access cycles.
[2] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, $\overline{AOE}$, and $\overline{ARE}$.

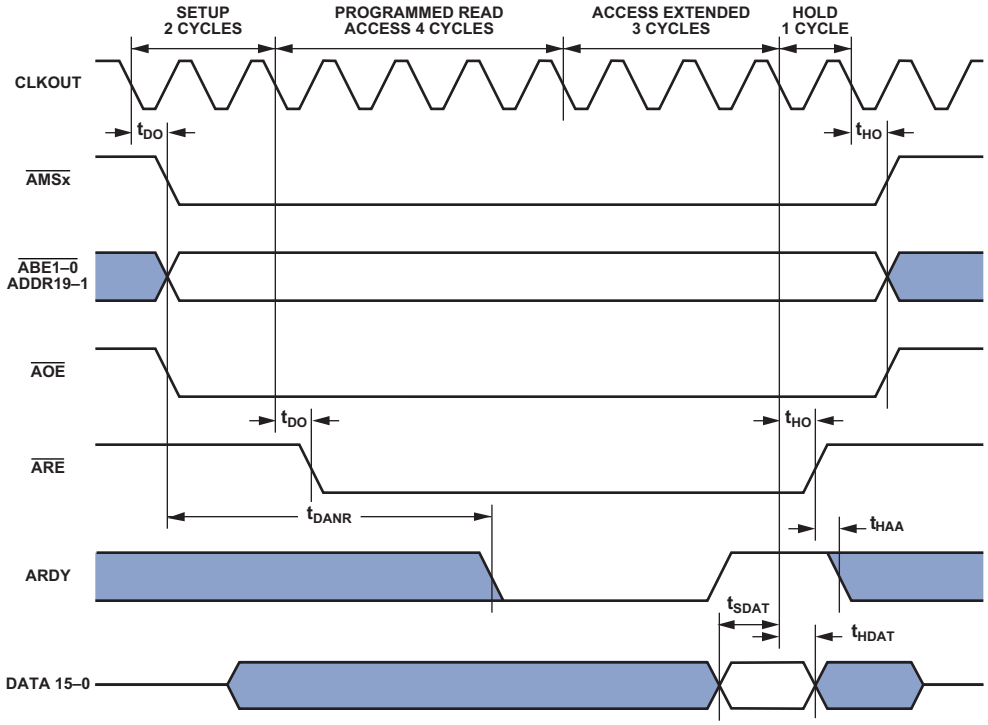


Figure 14. Asynchronous Memory Read Cycle Timing with Asynchronous ARDY

DDR SDRAM/Mobile DDR SDRAM Write Cycle Timing

Table 33 and Figure 20 describe DDR SDRAM/mobile DDR SDRAM write cycle timing.

Table 33. DDR SDRAM/Mobile DDR SDRAM Write Cycle Timing

Parameter		DDR SDRAM Min	DDR SDRAM Max	Mobile DDR SDRAM Min	Mobile DDR SDRAM Max	Unit
Switching Characteristics						
t_{DQSS}	Write CMD to First DQS0-1	0.75	1.25	0.75	1.25	t_{CK}
t_{DS}	DQ0-15/DQM0-1 Setup to DQS0-1	0.90		0.90		ns
t_{DH}	DQ0-15/DQM0-1 Hold to DQS0-1	0.90		0.90		ns
t_{DSS}	DQS0-1 Falling to DCK0-1 Rising (DQS0-1 Setup)	0.20		0.20		t_{CK}
t_{DSH}	DQS0-1 Falling from DCK0-1 Rising (DQS0-1 Hold)	0.20		0.20		t_{CK}
t_{DQSH}	DQS0-1 High Pulse Width	0.35		0.40	0.60	t_{CK}
t_{DQSL}	DQS0-1 Low Pulse Width	0.35		0.40	0.60	t_{CK}
t_{WPRE}	DQS0-1 Write Preamble	0.25		0.25		t_{CK}
t_{WPST}	DQS0-1 Write Postamble	0.40	0.60	0.40	0.60	t_{CK}
t_{DOPW}	DQ0-15 and DQM0-1 Output Pulse Width (for Each)	1.75		1.75		ns

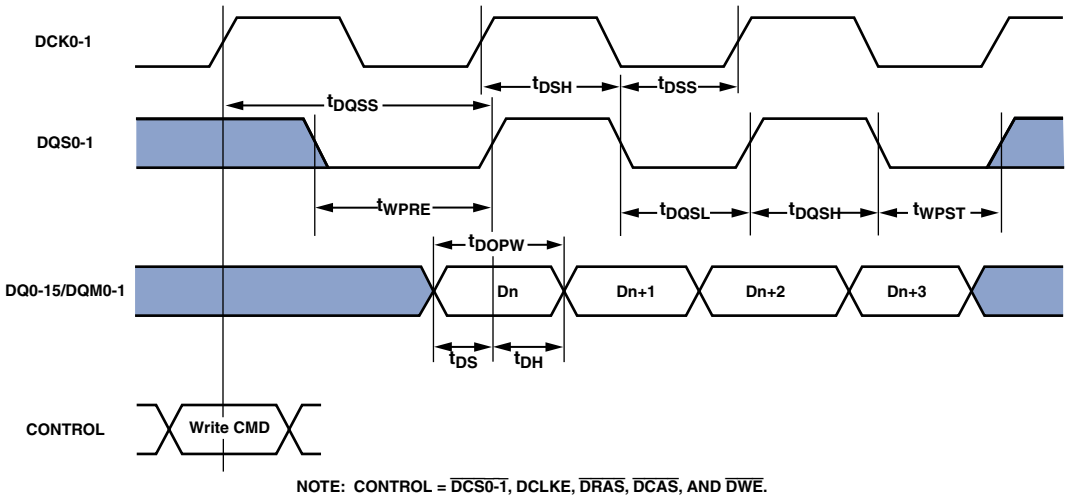


Figure 20. DDR SDRAM /Mobile DDR SDRAM Controller Write Cycle Timing

Table 35. External Port Bus Request and Grant Cycle Timing with Asynchronous $\overline{BR}$

Parameter		Min	Max	Unit
Timing Requirement				
t_{WBR}	$\overline{BR}$ Pulsewidth	$2 \times t_{SCLK}$		ns
Switching Characteristics				
t_{SD}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}/\overline{AWE}$ Disable		5.0	ns
t_{SE}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}/\overline{AWE}$ Enable		5.0	ns
t_{DBG}	CLKOUT Low to $\overline{BG}$ Asserted Output Delay		4.0	ns
t_{EBG}	CLKOUT Low to $\overline{BG}$ Deasserted Output Hold		4.0	ns
t_{DBH}	CLKOUT Low to $\overline{BGH}$ Asserted Output Delay		3.6	ns
t_{EBH}	CLKOUT Low to $\overline{BGH}$ Deasserted Output Hold		3.6	ns

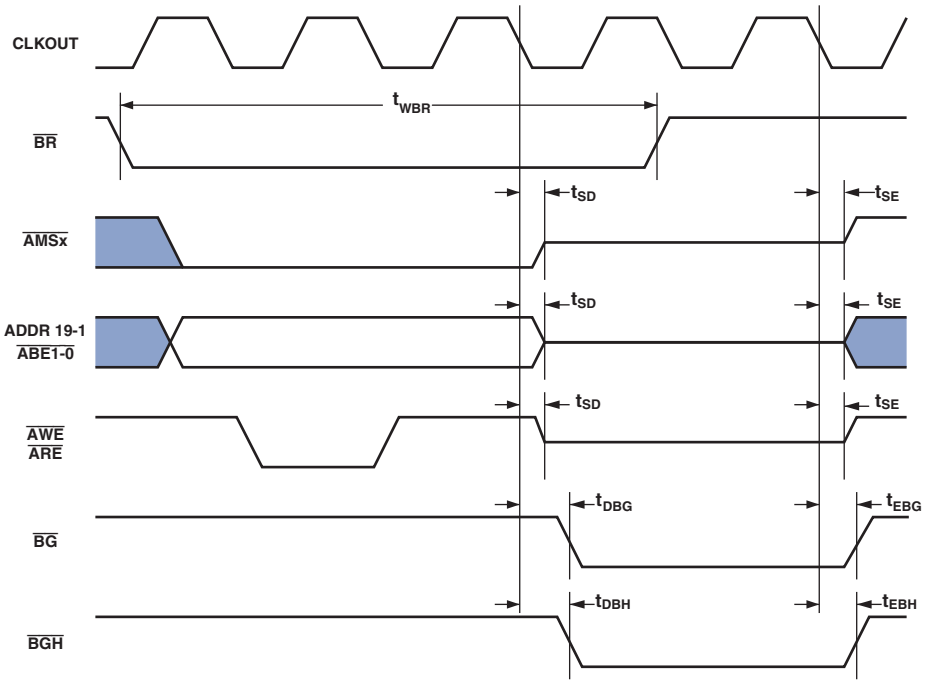


Figure 22. External Port Bus Request and Grant Cycle Timing with Asynchronous $\overline{BR}$

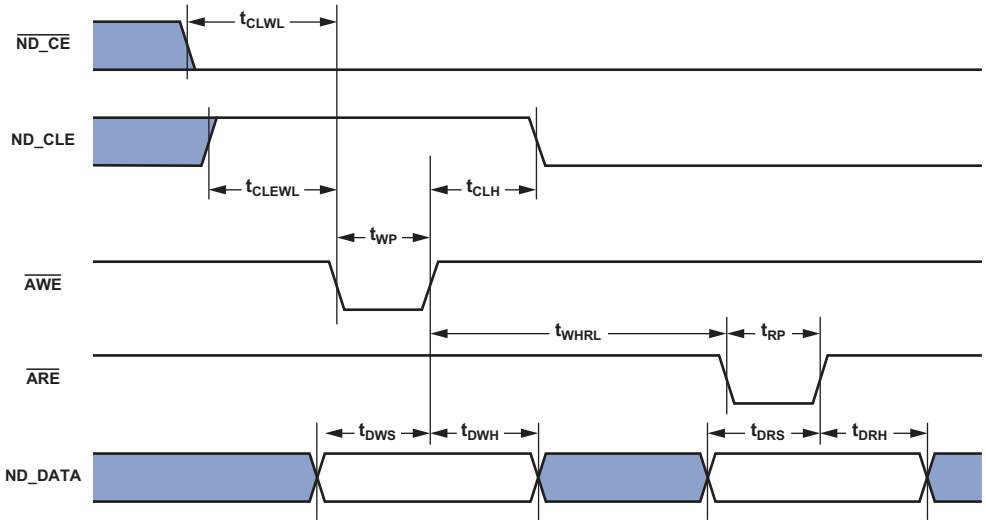


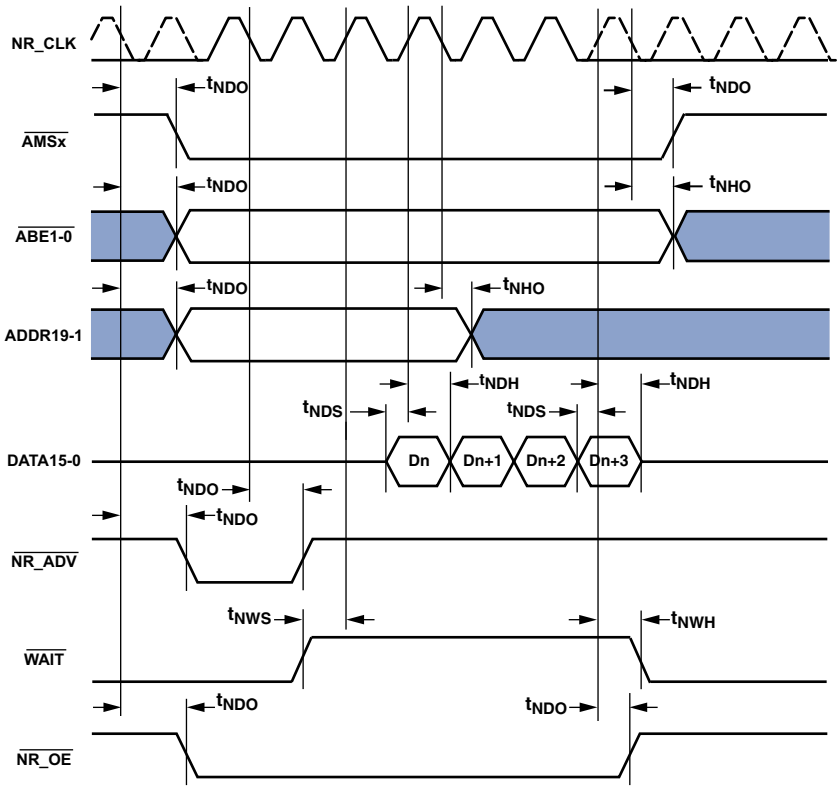
Figure 27. NAND Flash Controller Interface Timing—Write Followed by Read Operation

Synchronous Burst AC Timing

Table 37 and Figure 28 on Page 57 describe Synchronous Burst AC operations.

Table 37. Synchronous Burst AC Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{NDS}	DATA15-0 Setup Before NR_CLK	4.0		ns
t_{NDH}	DATA15-0 Hold After NR_CLK	2.0		ns
t_{NWS}	WAIT Setup Before NR_CLK	8.0		ns
t_{NWH}	WAIT Hold After NR_CLK	0.0		ns
Switching Characteristics				
t_{NDO}	$\overline{AMSx}$, $\overline{ABE1-0}$, ADDR19-1, $\overline{NR\_ADV}$, $\overline{NR\_OE}$ Output Delay After NR_CLK	6.0		ns
t_{NHO}	$\overline{ABE1-0}$, ADDR19-1 Output Hold After NR_CLK	–3.0		ns



NOTE: NR_CLK dotted line represents a free running version of NR_CLK that is not visible on the NR_CLK pin.

Figure 28. Synchronous Burst AC Interface Timing

Serial Peripheral Interface (SPI) Port—Master Timing

Table 44 and Figure 38 describe SPI port master operations.

Table 44. Serial Peripheral Interface (SPI) Port—Master Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SPIxSCK Edge (Data Input Setup)	9.0		ns
t_{HSPIDM}	SPIxSCK Sampling Edge to Data Input Invalid	–1.5		ns
Switching Characteristics				
t_{SDSCIM}	$\overline{\text{SPIxSELy}}$ Low to First SPIxSCK Edge	$2t_{SCLK}$–1.5		ns
t_{SPICHM}	SPIxSCK High Period	$2t_{SCLK}$–1.5		ns
t_{SPICLM}	SPIxSCK Low Period	$2t_{SCLK}$–1.5		ns
t_{SPICLK}	SPIxSCK Period	$4t_{SCLK}$–1.5		ns
t_{HDSM}	Last SPIxSCK Edge to $\overline{\text{SPIxSELy}}$ High	$2t_{SCLK}$–1.5		ns
t_{SPITDM}	Sequential Transfer Delay	$2t_{SCLK}$–1.5		ns
$t_{DDSPIDM}$	SPIxSCK Edge to Data Out Valid (Data Out Delay)		6	ns
$t_{HDSPIDM}$	SPIxSCK Edge to Data Out Invalid (Data Out Hold)	–1.0		ns

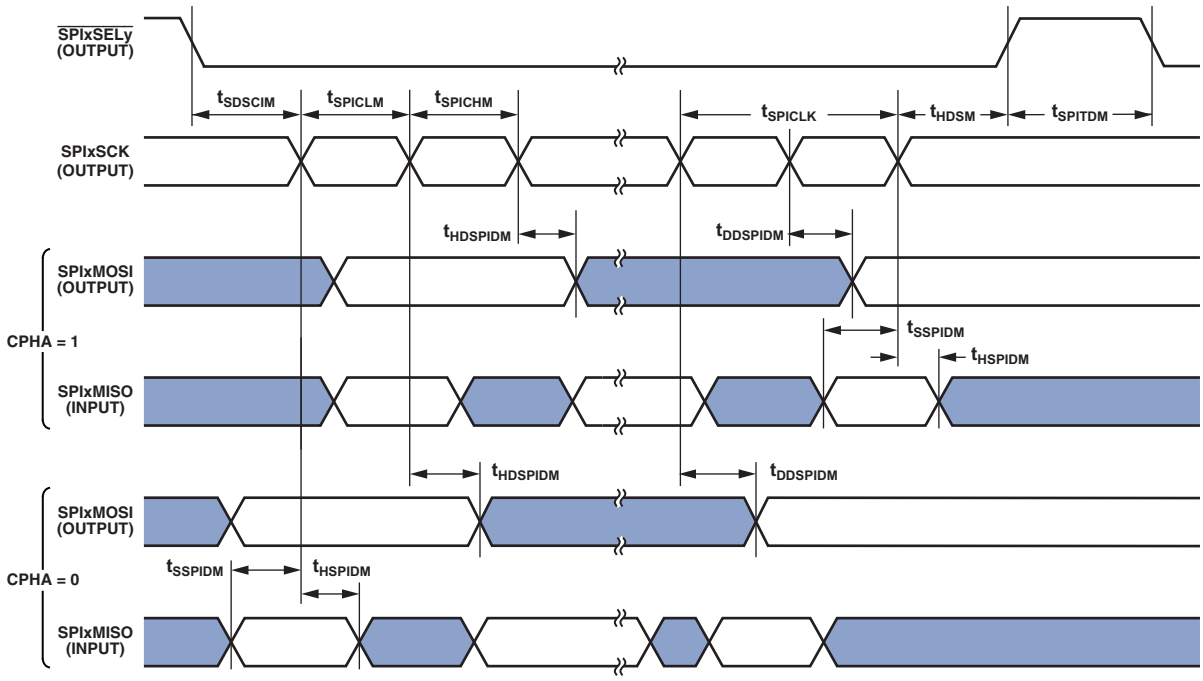


Figure 38. Serial Peripheral Interface (SPI) Port—Master Timing

SD/SDIO Controller Timing

Table 50 and Figure 44 describe SD/SDIO controller timing.
Table 51 and Figure 45 describe SD/SDIO controller (high-speed mode) timing.

Table 50. SD/SDIO Controller Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	SD_Dx and SD_CMD Input Setup Time	7.2		ns
t_{IH}	SD_Dx and SD_CMD Input Hold Time	2		ns
Switching Characteristics				
f_{PP}	SD_CLK Frequency During Data Transfer Mode[1]	0	20	MHz
f_{PP}	SD_CLK Frequency During Identification Mode[1]	100[2]	400	kHz
t_{WL}	SD_CLK Low Time	15		ns
t_{WH}	SD_CLK High Time	15		ns
t_{TLH}	SD_CLK Rise Time		10	ns
t_{THL}	SD_CLK Fall Time		10	ns
t_{ODLY}	SD_Dx and SD_CMD Output Delay Time During Data Transfer Mode	–1	+14	ns
	SD_Dx and SD_CMD Output Delay Time During Identification Mode	–1	+50	ns

[1] $t_{PP}=1/f_{PP}$.
[2] Spec can be 0 kHz, meaning to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

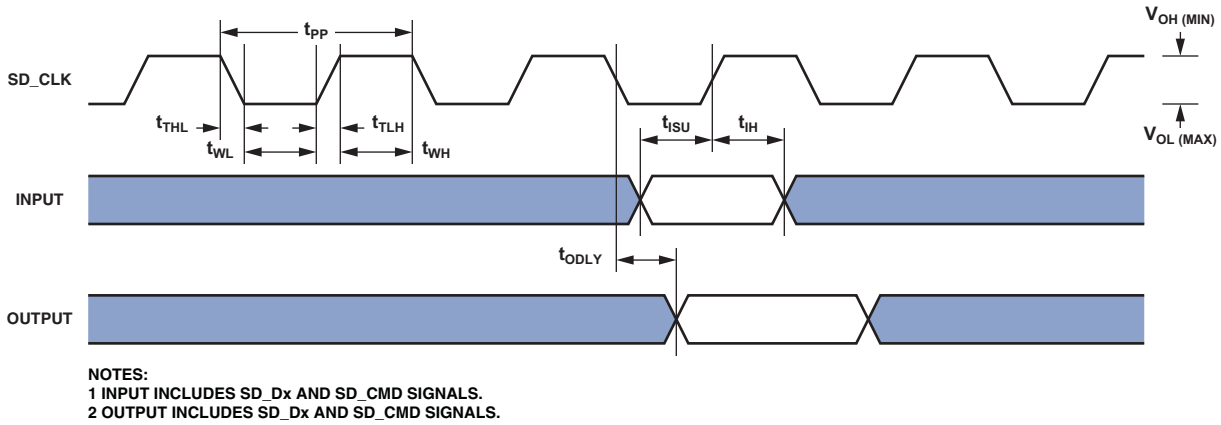


Figure 44. SD/SDIO Controller Timing

ATAPI Ultra DMA Data-In Transfer Timing

Table 60 and Figure 53 through Figure 56 describe the ATAPI ultra DMA data-in data transfer timing. The material in these figures is adapted from ATAPI-6 (INCITS 361-2002[R2007] and is used with permission of the American National Standards Institute (ANSI) on behalf of the Information Technology Industry Council ("ITIC"). Copies of ATAPI-6 (INCITS 361-2002[R2007] can be purchased from ANSI.

Table 60. ATAPI Ultra DMA Data-In Transfer Timing

ATAPI Parameter		ATAPI_ULTRA_TIM_x Timing Register Setting[1]	Timing Equation
t_{DS}	Data setup time at host	N/A	$T_{SK3} + t_{SUDU}$
t_{DH}	Data hold time at host	N/A	$T_{SK3} + t_{HDU}$
t_{CVS}	CRC word valid setup time at host	TDVS	$TDVS \times t_{SCLK} - (t_{SK1} + t_{SK2})$
t_{CVH}	CRC word valid hold time at host	TACK	$TACK \times t_{SCLK} - (t_{SK1} + t_{SK2})$
t_{LI}	Limited interlock time	N/A	$2 \times t_{BD} + 2 \times t_{SCLK} + t_{OD}$
t_{MLI}	Interlock time with minimum	TZAH, TCVS	$(TZAH + TCVS) \times t_{SCLK} - (4 \times t_{BD} + 4 \times t_{SCLK} + 2 \times t_{OD})$
t_{AZ}	Maximum time allowed for output drivers to release	N/A	0
t_{ZAH}	Minimum delay time required for output	TZAH	$2 \times t_{SCLK} + TZAH \times t_{SCLK} + t_{SCLK}$
t_{ENV}[2]	$\overline{ATAPI\_DMACK}$ to $\overline{ATAPI\_DIOR}/\overline{DIOW}$	TENV	$(TENV \times t_{SCLK}) +/- (t_{SK1} + t_{SK2})$
t_{RP}	$\overline{ATAPI\_DMACK}$ to $\overline{ATAPI\_DIOR}/\overline{DIOW}$	TRP	$TRP \times t_{SCLK} - (t_{SK1} + t_{SK2} + t_{SK4})$
t_{ACK}	Setup and hold times for $\overline{ATAPI\_DMACK}$	TACK	$TACK \times t_{SCLK} - (t_{SK1} + t_{SK2})$

[1] ATAPI Timing Register Setting should be programmed with a value that guarantees parameter compliance with the ATA ANSI specification for ATA device mode of operation.
[2] This timing equation can be used to calculate both the minimum and maximum t_{ENV}.

In Figure 53 and Figure 54 an alternate ATAPI_D0–15 port bus is ATAPI_D0–15A.

Also note that ATAPI_ADDR pins include A1-3, $\overline{\text{ATAPI\_CS0}}$, and $\overline{\text{ATAPI\_CS1}}$. Alternate ATAPI port ATAPI _ADDR pins include ATAPI_A0A, ATAPI_A1A, ATAPI_A2A, $\overline{\text{ATAPI\_CS0}}$, and $\overline{\text{ATAPI\_CS1}}$.

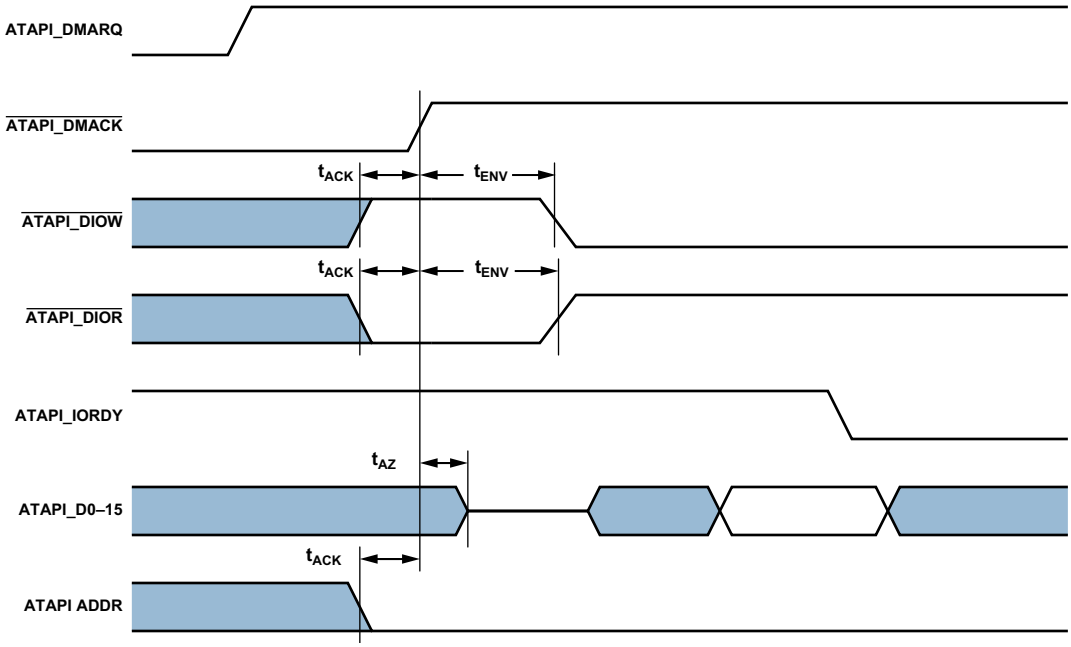


Figure 53. Initiating an Ultra DMA Data-In Burst

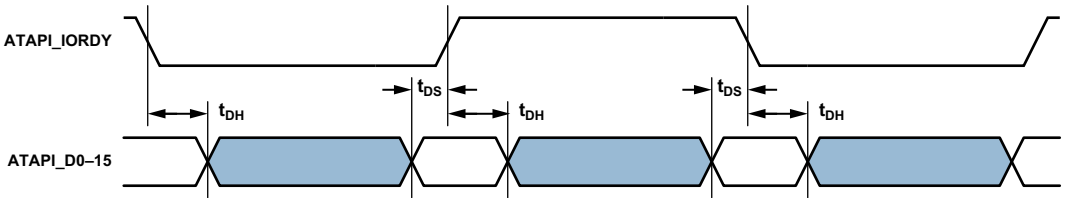


Figure 54. Sustained Ultra DMA Data-In Burst

OUTPUT DRIVE CURRENTS

Figure 62 through Figure 71 show typical current-voltage characteristics for the output drivers of the ADSP-BF54x Blackfin processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

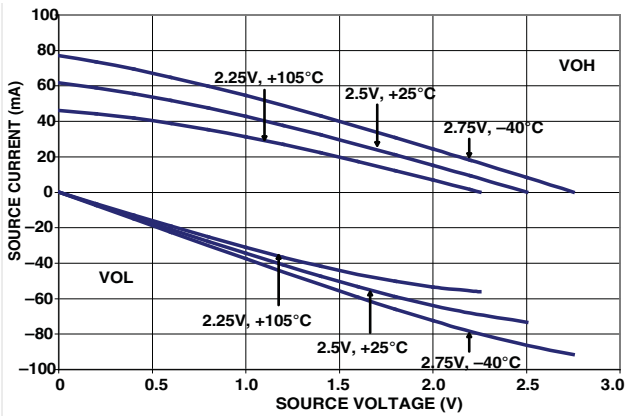


Figure 62. Drive Current A (Low V_{DDEXT})

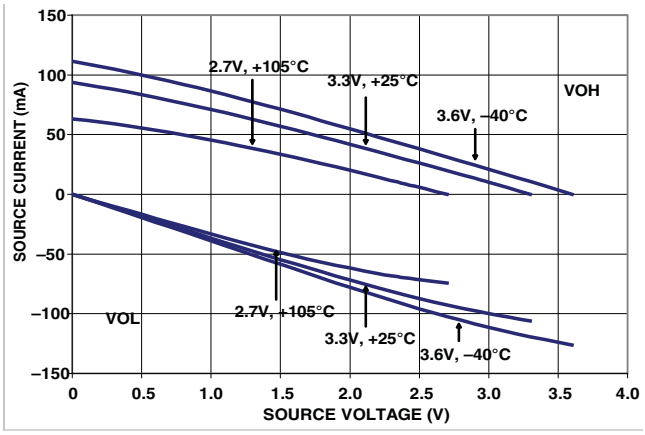


Figure 63. Drive Current A (High V_{DDEXT})

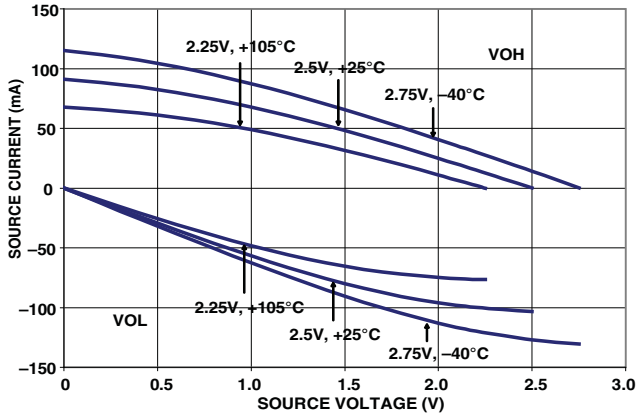


Figure 64. Drive Current B (Low V_{DDEXT})

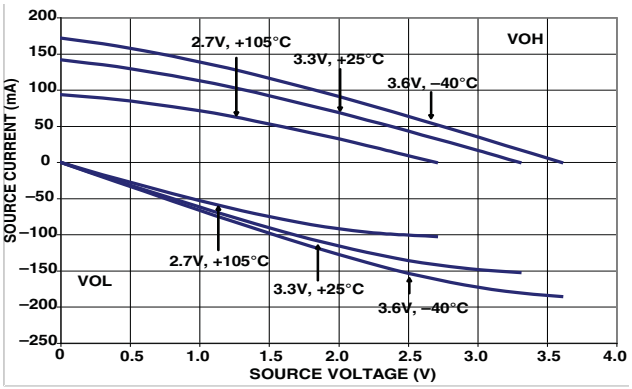


Figure 65. Drive Current B (High V_{DDEXT})

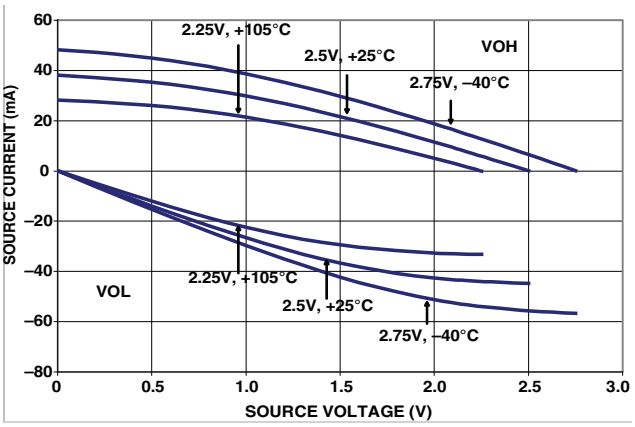


Figure 66. Drive Current C (Low V_{DDEXT})

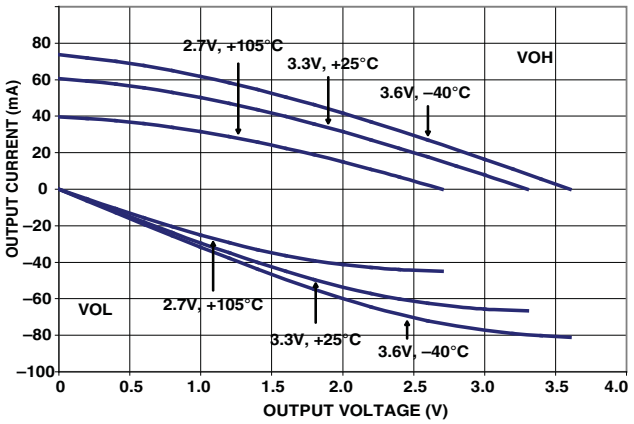


Figure 67. Drive Current C (High V_{DDEXT})

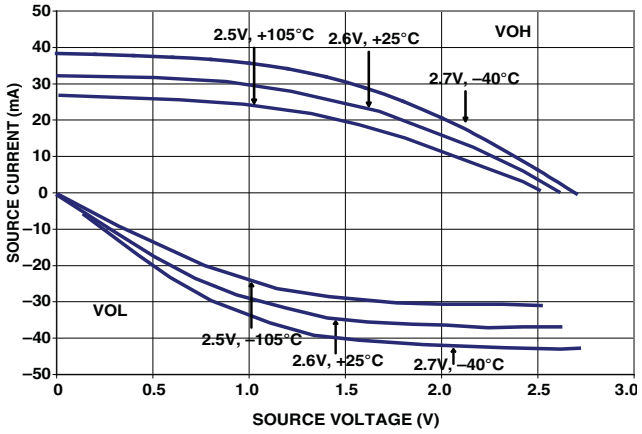


Figure 68. Drive Current D (DDR SDRAM)

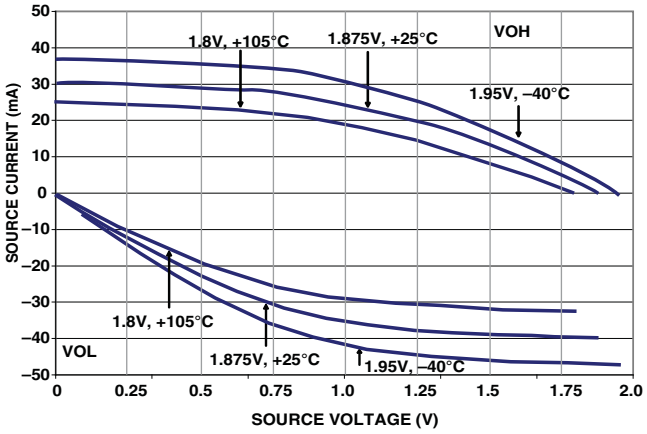


Figure 69. Drive Current D (Mobile DDR SDRAM)

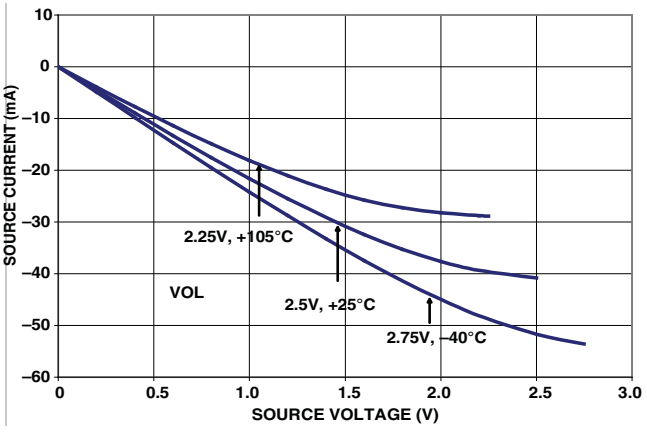


Figure 70. Drive Current E (Low V_{DDEXT})

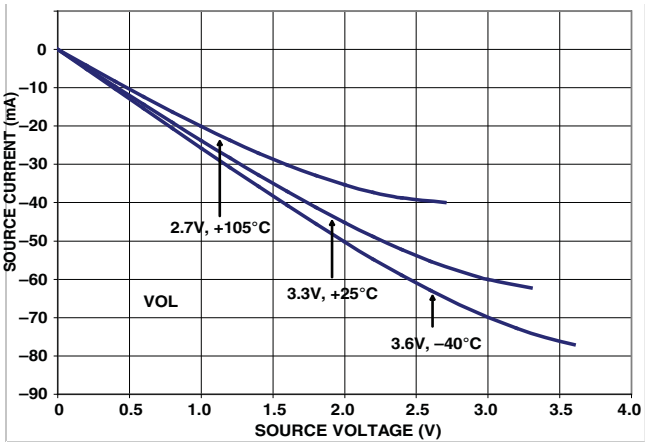


Figure 71. Drive Current E (High V_{DDEXT})

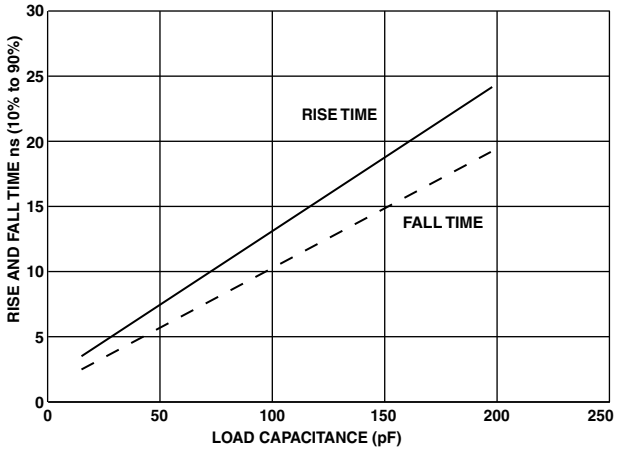


Figure 79. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 2.25 V

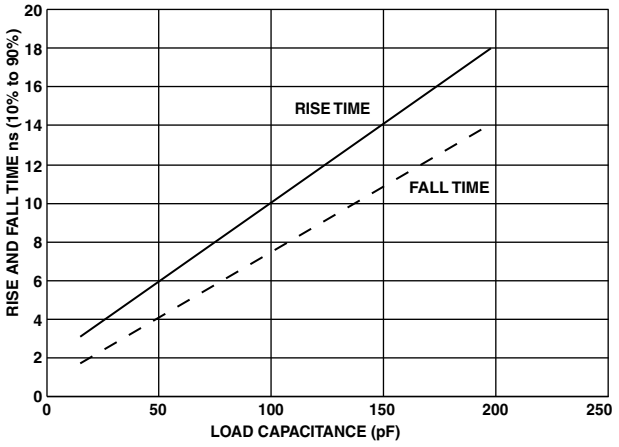


Figure 80. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 3.65 V

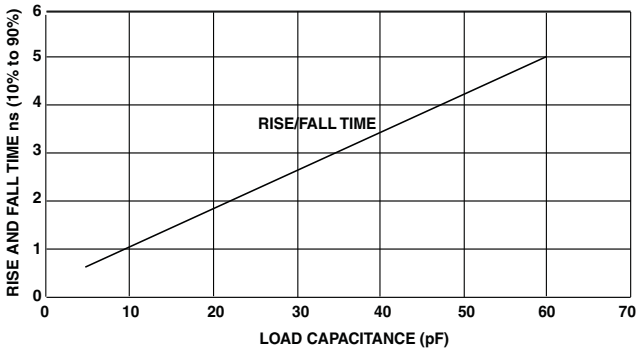


Figure 81. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D DDR SDRAM at V_{DDDDR} = 2.5 V

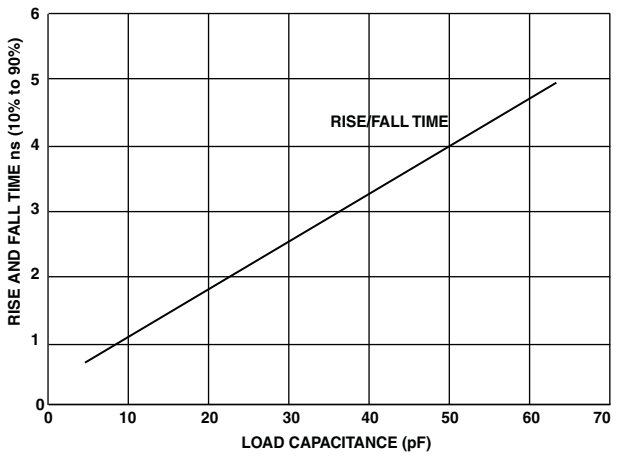


Figure 82. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D DDR SDRAM at V_{DDDDR} = 2.7 V

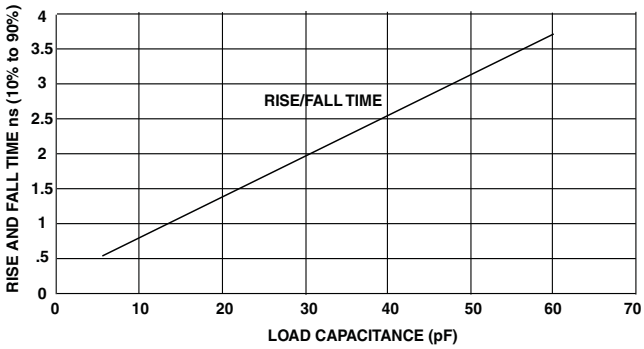


Figure 83. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D Mobile DDR SDRAM at V_{DDDDR} = 1.8 V

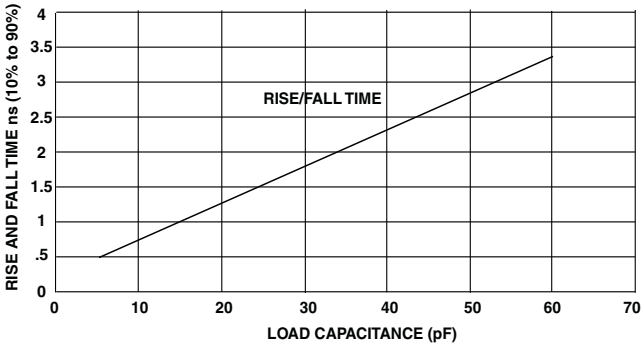


Figure 84. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D Mobile DDR SDRAM at V_{DDDDR} = 1.95 V

Table 66 lists the CSP_BGA package by ball number for the ADSP-BF549. Table 65 on Page 94 lists the CSP_BGA package by signal.

Table 66. 400-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	GND	C1	MXO	E1	USB_DP	G1	PC5
A2	A2	C2	MXI	E2	USB_DM	G2	PC4
A3	PI0	C3	PH5	E3	GND	G3	USB_ID
A4	PI2	C4	PH9	E4	MLF_P	G4	V_{DDUSB}
A5	PI4	C5	PH11	E5	V_{DDEXT}	G5	V_{DDEXT}
A6	PI6	C6	PH13	E6	MFS	G6	V_{DDEXT}
A7	PI8	C7	PH10	E7	GND_{MP}	G7	V_{DDEXT}
A8	PI11	C8	PI9	E8	V_{DDMP}	G8	V_{DDINT}
A9	PI12	C9	PI13	E9	V_{DDEXT}	G9	GND
A10	$\overline{AMS0}$	C10	$\overline{AOE}$	E10	V_{DDEXT}	G10	GND
A11	CLKIN	C11	$\overline{NMI}$	E11	V_{DDEXT}	G11	GND
A12	XTAL	C12	$\overline{RESET}$	E12	V_{DDEXT}	G12	V_{DDINT}
A13	GND	C13	D1	E13	V_{DDRTC}	G13	V_{DDINT}
A14	RTXI	C14	D8	E14	D14	G14	V_{DDEXT}
A15	D4	C15	D9	E15	D13	G15	V_{DDDDR}
A16	D6	C16	$\overline{ABE1}$	E16	$\overline{DCLK0}$	G16	DA4
A17	D10	C17	$\overline{ABE0}$	E17	$\overline{DRAS}$	G17	DA1
A18	$VROUT_0$	C18	DCLK1	E18	$\overline{DWE}$	G18	DA3
A19	$VROUT_1$	C19	$\overline{DCS0}$	E19	DA9	G19	DA0
A20	GND	C20	DA7	E20	DA2	G20	DQM0
B1	USB_VREF	D1	GND	F1	USB_XI	H1	PC3
B2	A1	D2	USB_VBUS	F2	USB_XO	H2	PC0
B3	A3	D3	USB_RSET	F3	GND	H3	PC7
B4	PI1	D4	GND	F4	MLF_M	H4	PH7
B5	PI3	D5	PH8	F5	V_{DDUSB}	H5	V_{DDEXT}
B6	PI5	D6	PH6	F6	GND	H6	V_{DDEXT}
B7	PI7	D7	PH12	F7	V_{DDEXT}	H7	GND
B8	PI10	D8	PI14	F8	V_{DDEXT}	H8	GND
B9	PI15	D9	$\overline{AMS1}$	F9	V_{DDINT}	H9	GND
B10	$\overline{AMS2}$	D10	$\overline{AMS3}$	F10	V_{DDDDR}	H10	GND
B11	GND	D11	CLKBUF	F11	V_{DDDDR}	H11	GND
B12	$\overline{ARE}$	D12	$\overline{AWE}$	F12	V_{DDDDR}	H12	GND
B13	D2	D13	D0	F13	V_{DDEXT}	H13	V_{DDDDR}
B14	RTXO	D14	D11	F14	GND	H14	V_{DDDDR}
B15	D3	D15	D12	F15	V_{DDVR}	H15	V_{DDDDR}
B16	D5	D16	DCLK0	F16	$\overline{DCAS}$	H16	DBA1
B17	D7	D17	D15	F17	DA11	H17	DBA0
B18	DCLKE	D18	$\overline{DCLK1}$	F18	DA8	H18	DQS1
B19	$\overline{DCS1}$	D19	DA12	F19	DA5	H19	DQM1
B20	DA10	D20	DA6	F20	DQS0	H20	DQ11