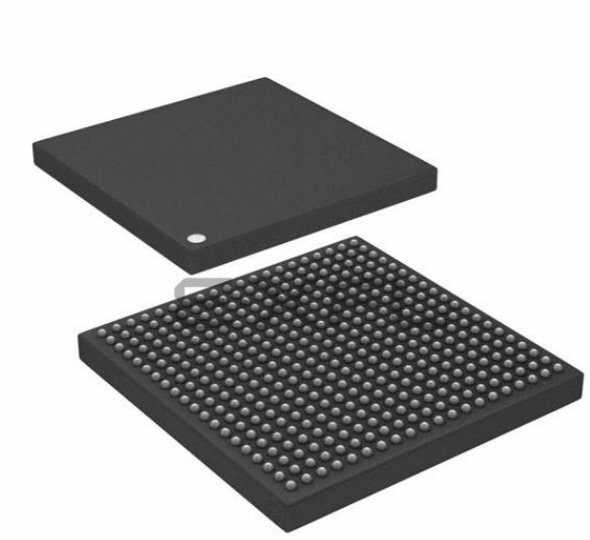

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	533MHz
Non-Volatile Memory	External
On-Chip RAM	196kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf544bbcz-5a

The DDR memory controller can gluelessly manage up to two banks of double-rate synchronous dynamic memory (DDR and mobile DDR SDRAM). The 16-bit interface operates at the SCLK frequency, enabling a maximum throughput of 532M bytes/s. The DDR and mobile DDR controller is augmented with a queuing mechanism that performs efficient bursts into the DDR and mobile DDR. The controller is an industry standard DDR and mobile DDR SDRAM controller with each bank supporting from 64M bit to 512M bit device sizes and 4-, 8-, or 16-bit widths. The controller supports up to 256M bytes per external bank. With 2 external banks, the controller supports up to 512M bytes total. Each bank is independently programmable and is contiguous with adjacent banks regardless of the sizes of the different banks or their placement.

Traditional 16-bit asynchronous memories, such as SRAM, EPROM, and flash devices, can be connected to one of the four 64M byte asynchronous memory banks, represented by four memory select strobes. Alternatively, these strobes can function as bank-specific read or write strobes preventing further glue logic when connecting to asynchronous FIFO devices. See the Ordering Guide on Page 101 for a list of specific products that provide support for DDR memory.

In addition, the external bus can connect to advanced flash device technologies, such as:

- Page-mode NOR flash devices
- Synchronous burst-mode NOR flash devices
- NAND flash devices

Customers should consult the Ordering Guide when selecting a specific ADSP-BF54x component for the intended application. Products that provide support for mobile DDR memory are noted in the ordering guide footnotes.

NAND Flash Controller (NFC)

The ADSP-BF54x Blackfin processors provide a NAND Flash Controller (NFC) as part of the external bus interface. NAND flash devices provide high-density, low-cost memory. However, NAND flash devices also have long random access times, invalid blocks, and lower reliability over device lifetimes. Because of this, NAND flash is often used for read-only code storage. In this case, all DSP code can be stored in NAND flash and then transferred to a faster memory (such as DDR or SRAM) before execution. Another common use of NAND flash is for storage of multimedia files or other large data segments. In this case, a software file system may be used to manage reading and writing of the NAND flash device. The file system selects memory segments for storage with the goal of avoiding bad blocks and equally distributing memory accesses across all address locations. Hardware features of the NFC include:

- Support for page program, page read, and block erase of NAND flash devices, with accesses aligned to page boundaries.
- Error checking and correction (ECC) hardware that facilitates error detection and correction.
- A single 8-bit or 16-bit external bus interface for commands, addresses, and data.
- Support for SLC (single level cell) NAND flash devices unlimited in size, with page sizes of 256 bytes and 512 bytes. Larger page sizes can be supported in software.
- The ability to release external bus interface pins during long accesses.
- Support for internal bus requests of 16 bits or 32 bits.
- A DMA engine to transfer data between internal memory and a NAND flash device.

One-Time-Programmable Memory

The ADSP-BF54x Blackfin processors have 64K bits of one-time-programmable (OTP) non-volatile memory that can be programmed by the developer only one time. It includes the array and logic to support read access and programming. Additionally, its pages can be write protected.

OTP enables developers to store both public and private data on-chip. In addition to storing public and private key data for applications requiring security, it also allows developers to store completely user-definable data such as a customer ID, product ID, or a MAC address. By using this feature, generic parts can be shipped, which are then programmed and protected by the developer within this non-volatile memory. The OTP memory can be accessed through an API provided by the on-chip ROM.

I/O Memory Space

The ADSP-BF54x Blackfin processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one containing the control MMRs for all core functions and the other containing the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The ADSP-BF54x Blackfin processors contain a small on-chip boot kernel, which configures the appropriate peripheral for booting. If the ADSP-BF54x Blackfin processors are configured to boot from boot ROM memory space, the processor starts executing from the on-chip boot ROM. For more information, see Booting Modes on Page 18.

Event Handling

The event controller on the ADSP-BF54x Blackfin processors handles all asynchronous and synchronous events to the processors. The ADSP-BF54x Blackfin processors provide event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher-priority event takes precedence over servicing of a lower-priority event.

Host DMA Port Interface

The host DMA port (HOSTDP) facilitates a host device external to the ADSP-BF54x Blackfin processors to be a DMA master and transfer data back and forth. The host device always masters the transactions, and the processor is always a DMA slave device.

The HOSTDP is enabled through the peripheral access bus. Once the port has been enabled, the transactions are controlled by the external host. The external host programs standard DMA configuration words in order to send/receive data to any valid internal or external memory location. The host DMA port controller includes the following features:

- Allows an external master to configure DMA read/write data transfers and read port status
- Uses a flexible asynchronous memory protocol for its external interface
- Allows an 8- or 16-bit external data interface to the host device
- Supports half-duplex operation
- Supports little/big endian data transfers
- Acknowledge mode allows flow control on host transactions
- Interrupt mode guarantees a burst of FIFO depth host transactions

REAL-TIME CLOCK

The ADSP-BF54x Blackfin processors' real-time clock (RTC) provides a robust set of digital watch features, including current time, stopwatch, and alarm. The RTC is clocked by a 32.768 kHz crystal external to the ADSP-BF54x Blackfin processors. The RTC peripheral has dedicated power supply pins so that it can remain powered up and clocked even when the rest of the processor is in a low-power state. The RTC provides several programmable interrupt options, including interrupt per second, minute, hour, or day clock ticks, interrupt on programmable stopwatch countdown, or interrupt at a programmed alarm time.

The 32.768 kHz input clock frequency is divided down to a 1 Hz signal by a prescaler. The counter function of the timer consists of four counters: a 60-second counter, a 60-minute counter, a 24-hour counter, and a 32,768-day counter.

When enabled, the alarm function generates an interrupt when the output of the timer matches the programmed value in the alarm control register. There are two alarms. The first alarm is for a time of day. The second alarm is for a day and time of that day.

The stopwatch function counts down from a programmed value with one-second resolution. When the stopwatch is enabled and the counter underflows, an interrupt is generated.

Like the other peripherals, the RTC can wake up the ADSP-BF54x processor from sleep mode upon generation of any RTC wakeup event. Additionally, an RTC wakeup event can wake up the ADSP-BF54x processors from deep sleep mode, and it can wake up the on-chip internal voltage regulator from the hibernate state.

Connect RTC pins RTXI and RTXO with external components as shown in Figure 4.

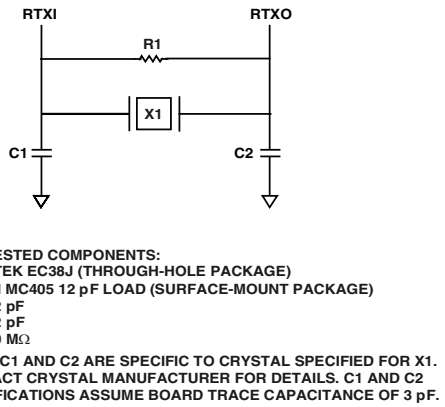


Figure 4. External Components for RTC

WATCHDOG TIMER

The ADSP-BF54x processors include a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system reliability by forcing the processor to a known state through generation of a hardware reset, non-maskable interrupt (NMI), or general-purpose interrupt if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, and then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

If configured to generate a hardware reset, the watchdog timer resets both the core and the ADSP-BF54x processors' peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

The timer is clocked by the system clock (SCLK) at a maximum frequency of f_{SCLK}.

TIMERS

There are up to two timer units in the ADSP-BF54x Blackfin processors. One unit provides eight general-purpose programmable timers, and the other unit provides three. Each timer has an external pin that can be configured either as a pulse width modulator (PWM) or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input on the TMRx pins, an external clock TMRCLK input pin, or to the internal SCLK.

- Boot from 16-bit asynchronous FIFO (BMODE = 0x2)—In this mode, the boot kernel starts booting from address 0x2030 0000. Every 16-bit word that the boot kernel has to read from the FIFO must be requested by a low pulse on the DMAR1 pin.
- Boot from serial SPI memory, EEPROM or flash (BMODE = 0x3)—8-, 16-, 24- or 32-bit addressable devices are supported. The processor uses the PE4 GPIO pin to select a single SPI EEPROM or flash device and uses SPI0 to submit a read command and successive address bytes (0x00) until a valid 8-, 16-, 24-, or 32-bit addressable device is detected. Pull-up resistors are required on the $\overline{\text{SPI0SEL1}}$ and SPI0MISO pins. By default, a value of 0x85 is written to the SPI0_BAUD register.
- Boot from SPI host device (BMODE = 0x4)—The processor operates in SPI slave mode (using SPI0) and is configured to receive the bytes of the .LDR file from an SPI host (master) agent. The HWAIT signal must be interrogated by the host before every transmitted byte. A pull-up resistor is required on the $\overline{\text{SPI0SS}}$ input. A pull-down resistor on the serial clock (SPI0SCK) may improve signal quality and booting robustness.
- Boot from serial TWI memory, EEPROM or flash (BMODE = 0x5)—The processor operates in master mode (using TWI0) and selects the TWI slave with the unique ID 0xA0. The processor submits successive read commands to the memory device starting at two-byte internal address 0x0000 and begins clocking data into the processor. The TWI memory device should comply with Philips I^2C Bus Specification version 2.1 and have the capability to autoincrement its internal address counter such that the contents of the memory device can be read sequentially. By default, a prescale value of 0xA and CLKDIV value of 0x0811 is used. Unless altered by OTP settings, an I^2C memory that takes two address bytes is assumed. Development tools ensure that data that is booted to memories that cannot be accessed by the Blackfin core is written to an intermediate storage place and then copied to the final destination via memory DMA.
- Boot from TWI host (BMODE = 0x6)—The TWI host agent selects the slave with the unique ID 0x5F. The processor (using TWI0) replies with an acknowledgement, and the host can then download the boot stream. The TWI host agent should comply with Philips I^2C Bus Specification version 2.1. An I^2C multiplexer can be used to select one processor at a time when booting multiple processors from a single TWI.
- Boot from UART host (BMODE = 0x7)—In this mode, the processor uses UART1 as the booting source. Using an autobaud handshake sequence, a boot-stream-formatted program is downloaded by the host. The host agent selects a bit rate within the UART's clocking capabilities.

  When performing the autobaud, the UART expects an "@" (0x40) character (eight data bits, one start bit, one stop bit, no parity bit) on the UART1RX pin to determine the bit rate. It then replies with an acknowledgement, which is composed of four bytes (0xBF, the value of UART1_DLL, the value of UART1_DLH, and finally 0x00). The host can then download the boot stream. The processor deasserts the $\overline{\text{UART1RTS}}$ output to hold off the host; $\overline{\text{UART1CTS}}$ functionality is not enabled at boot time.
- Boot from (DDR) SDRAM (BMODE = 0xA)—In this mode, the boot kernel starts booting from address 0x0000 0010. This is a warm boot scenario only. The SDRAM is expected to contain a valid boot stream and the SDRAM controller must have been configured by the OTP settings.
- Boot from 8-bit and 16-bit external NAND flash memory (BMODE = 0xD)—In this mode, auto detection of the NAND flash device is performed. The processor configures PORTJ GPIO pins PJ1 and PJ2 to enable the $\overline{\text{ND\_CE}}$ and $\overline{\text{ND\_RB}}$ signals, respectively. For correct device operation, pull-up resistors are required on both $\overline{\text{ND\_CE}}$ (PJ1) and $\overline{\text{ND\_RB}}$ (PJ2) signals. By default, a value of 0x0033 is written to the NFC_CTL register. The booting procedure always starts by booting from byte 0 of block 0 of the NAND flash device. In this boot mode, the HWAIT signal does not toggle. The respective GPIO pin remains in the high-impedance state.

  NAND flash boot supports the following features:

  - Device auto detection
  - Error detection and correction for maximum reliability
  - No boot stream size limitation
  - Peripheral DMA via channel 22, providing efficient transfer of all data (excluding the ECC parity data)
  - Software-configurable boot mode for booting from boot streams expanding multiple blocks, including bad blocks
  - Software-configurable boot mode for booting from multiple copies of the boot stream allowing for handling of bad blocks and uncorrectable errors
  - Configurable timing via OTP memory

  Small page NAND flash devices must have a 512-byte page size, 32 pages per block, a 16-byte spare area size and a bus configuration of eight bits. By default, all read requests from the NAND flash are followed by four address cycles. If the NAND flash device requires only three address cycles, then the device must be capable of ignoring the additional address cycle.

  The small page NAND flash device must comply with the following command set:

Reset: 0xFF
Read lower half of page: 0x00
Read upper half of page: 0x01
Read spare area: 0x50

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
Port C: GPIO/*SPORT0/SD Controller/MXVR (MOST)*			
PC0/*TFS0*	I/O	GPIO/*SPORT0 Transmit Frame Sync*	C
PC1/*DT0SEC/MMCLK*	I/O	GPIO/*SPORT0 Transmit Data Secondary/MXVR Master Clock*	C
PC2/*DT0PRI*	I/O	GPIO/*SPORT0 Transmit Data Primary*	C
PC3/*TSCLK0*	I/O	GPIO/*SPORT0 Transmit Serial Clock*	A
PC4/*RFS0*	I/O	GPIO/*SPORT0 Receive Frame Sync*	C
PC5/*DR0SEC/MBCLK*	I/O	GPIO/*SPORT0 Receive Data Secondary/MXVR Bit Clock*	C
PC6/*DR0PRI*	I/O	GPIO/*SPORT0 Receive Data Primary*	C
PC7/*RSCLK0*	I/O	GPIO/*SPORT0 Receive Serial Clock*	C
PC8/*SD_D0*	I/O	GPIO/*SD Data Bus*	A
PC9/*SD_D1*	I/O	GPIO/*SD Data Bus*	A
PC10/*SD_D2*	I/O	GPIO/*SD Data Bus*	A
PC11/*SD_D3*	I/O	GPIO/*SD Data Bus*	A
PC12/*SD_CLK*	I/O	GPIO/*SD Clock Output*	A
PC13/*SD_CMD*	I/O	GPIO/*SD Command*	A
Port D: GPIO/*PPI0–2/SPORT 1/Keypad/Host DMA*			
PD0/*PPI1_D0/HOST_D8/ TFS1/PPI0_D18*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Transmit Frame Sync/PPI0 Data*	C
PD1/*PPI1_D1/HOST_D9/ DT1SEC/PPI0_D19*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Transmit Data Secondary/PPI0 Data*	C
PD2/*PPI1_D2/HOST_D10/ DT1PRI/PPI0_D20*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Transmit Data Primary/PPI0 Data*	C
PD3/*PPI1_D3/HOST_D11/ TSCLK1/PPI0_D21*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Transmit Serial Clock/PPI0 Data*	A
PD4/*PPI1_D4/HOST_D12/RFS1/PPI0_D22*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Receive Frame Sync/PPI0 Data*	C
PD5/*PPI1_D5/HOST_D13/DR1SEC/PPI0_D23*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Receive Data Secondary/PPI0 Data*	C
PD6/*PPI1_D6/HOST_D14/DR1PRI*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Receive Data Primary*	C
PD7/*PPI1_D7/HOST_D15/RSCLK1*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Receive Serial Clock*	A
PD8/*PPI1_D8/HOST_D0/ PPI2_D0/KEY_ROW0*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Row Input*	A
PD9/*PPI1_D9/HOST_D1/PPI2_D1/KEY_ROW1*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Row Input*	A
PD10/*PPI1_D10/HOST_D2/PPI2_D2/KEY_ROW2*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Row Input*	A
PD11/*PPI1_D11/HOST_D3/PPI2_D3/KEY_ROW3*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Row Input*	A
PD12/*PPI1_D12/HOST_D4/PPI2_D4/KEY_COL0*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Column Output*	A
PD13/*PPI1_D13/HOST_D5/PPI2_D5/KEY_COL1*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Column Output*	A
PD14/*PPI1_D14/HOST_D6/PPI2_D6/KEY_COL2*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Column Output*	A
PD15/*PPI1_D15/HOST_D7/PPI2_D7/KEY_COL3*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Column Output*	A

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
Port I: GPIO/*AMC*			
PI0/*A10*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI1/*A11*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI2/*A12*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI3/*A13*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI4/*A14*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI5/*A15*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI6/*A16*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI7/*A17*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI8/*A18*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI9/*A19*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI10/*A20*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI11/*A21*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI12/*A22*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI13/*A23*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI14/*A24*[6]	I/O	GPIO/*Address Bus for Async Access*	A
PI15/*A25/NR_CLK*[6]	I/O	GPIO/*Address Bus for Async Access/ NOR clock*	A
Port J: GPIO/*AMC/ATAPI*			
PJ0/*ARDY*/$\overline{WAIT}$	I/O	GPIO/ *Async Ready/NOR Wait*	A
PJ1/$\overline{ND\_CE}$[7]	I/O	GPIO/*NAND Chip Enable*	A
PJ2/$\overline{ND\_RB}$	I/O	GPIO/*NAND Ready Busy*	A
PJ3/$\overline{ATAPI\_DIOR}$	I/O	GPIO/*ATAPI Read*	A
PJ4/$\overline{ATAPI\_DIOW}$	I/O	GPIO/*ATAPI Write*	A
PJ5/$\overline{ATAPI\_CS0}$	I/O	GPIO/*ATAPI Chip Select/Command Block*	A
PJ6/$\overline{ATAPI\_CS1}$	I/O	GPIO/*ATAPI Chip Select*	A
PJ7/$\overline{ATAPI\_DMACK}$	I/O	GPIO/*ATAPI DMA Acknowledge*	A
PJ8/$\overline{ATAPI\_DMARQ}$	I/O	GPIO/*ATAPI DMA Request*	A
PJ9/*ATAPI_INTRQ*	I/O	GPIO/*Interrupt Request from the Device*	A
PJ10/$\overline{ATAPI\_IORDY}$	I/O	GPIO/*ATAPI Ready Handshake*	A
PJ11/$\overline{BR}$[8]	I/O	GPIO/*Bus Request*	A
PJ12/$\overline{BG}$[6]	I/O	GPIO/*Bus Grant*	A
PJ13/$\overline{BGH}$[6]	I/O	GPIO/*Bus Grant Hang*	A

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
USB_VBUS[11]	I/O	USB VBUS Pin (Pull high or low when unused.)	
USB_VREF	A	USB Voltage Reference (Connect to GND through a 0.1 µF capacitor or leave unconnected when not used.)	
USB_RSET	A	USB Resistance Set (Connect to GND through an unpopulated resistor pad.)	
MXVR (MOST) Interface			
MFS	O	MXVR Frame Sync (Leave unconnected when unused.)	C
MLF_P	A	MXVR Loop Filter Plus (Leave unconnected when unused.)	
MLF_M	A	MXVR Loop Filter Minus (Leave unconnected when unused.)	
MXI	C	MXVR Crystal Input (Pull high or low when unused.)	
MXO	C	MXVR Crystal Output (Pull high or low when unused.)	
Mode Control Pins			
BMODE0–3	I	Boot Mode Strap 0–3	
JTAG Port Pins			
TDI	I	JTAG Serial Data In	
TDO	O	JTAG Serial Data Out	C
$\overline{\text{TRST}}$	I	JTAG Reset (Pull low when unused.)	
TMS	I	JTAG Mode Select	
TCK	I	JTAG Clock	
$\overline{\text{EMU}}$	O	Emulation Output	C
Voltage Regulator			
$VR_{OUT}0$, $VR_{OUT}1$	O	External FET/BJT Drivers (Always connect together to reduce signal impedance.)	
Real Time Clock			
RTXO	C	RTC Crystal Output (Leave unconnected when unused. Does not three-state during hibernate.)	
RTXI	C	RTC Crystal Input (Pull high or low when unused.)	
Clock (PLL) Pins			
CLKIN	C	Clock/Crystal Input	
CLKOUT	O	Clock Output	B
XTAL	C	Crystal Output (If CLKBUF is enabled, does not three-state during hibernate.)	
CLKBUF	O	Buffered Oscillator Output (If enabled, does not three-state during hibernate.)	C
EXT_WAKE	O	External Wakeup from Hibernate Output (Does not three-state during hibernate.)	A
$\overline{\text{RESET}}$	I	Reset	
$\overline{\text{NMI}}$	I	Non-maskable Interrupt (Pull high when unused.)	

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
Supplies			
V_{DDINT}	P	Internal Power Supply	
V_{DDEXT}[12]	P	External Power Supply	
V_{DDDDR}[12]	P	External DDR Power Supply	
V_{DDUSB}[12]	P	External USB Power Supply	
V_{DDRTC}[12]	P	RTC Clock Supply	
V_{DDVR}[13]	P	Internal Voltage Regulator Power Supply (Connect to V_{DDEXT} when unused.)	
GND	G	Ground	
V_{DDMP}[12]	P	MXVR PLL Power Supply. (Must be driven to same level as V_{DDINT}. Connect to V_{DDINT} when unused or when MXVR is not present.)	
GND_{MP}[12]	G	MXVR PLL Ground (Connect to GND when unused or when MXVR is not present.)	

[1] I = Input, O = Output, P =Power, G = Ground, C = Crystal, A = Analog.
[2] Refer to Table 62 on Page 88 through Table 71 on Page 89 for driver types.
[3] To use the SPI memory boot, SPI0SCK should have a pulldown, SPI0MISO should have a pullup, and $\overline{\text{SPI0SEL1}}$ is used as the $\overline{\text{CS}}$ with a pullup.
[4] $\overline{\text{HWAIT}}$/HWAITA should be pulled high or low to configure polarity. See Booting Modes on Page 18.
[5] $\overline{\text{GPW}}$ functionality is available when MXVR is not present or unused.
[6] This pin should not be used as GPIO if booting in mode 1.
[7] This pin should always be enabled as $\overline{\text{ND\_CE}}$ in software and pulled high with a resistor when using NAND flash.
[8] This pin should always be enabled as $\overline{\text{BR}}$ in software and pulled high to enable asynchronous access.
[9] This pin must be pulled low through a 10kOhm resistor if self-refresh mode is desired during hibernate state or deep-sleep mode.
[10] If the USB is used in device mode only, the USB_ID pin should be either pulled high or left unconnected.
[11] This pin is an output only during initialization of USB OTG session request pulses in peripheral mode. Therefore, host mode or OTG type A mode requires that an external voltage source of 5 V, at 8 mA or more per the OTG specification, be applied to this pin. Other OTG modes require that this external voltage be disabled.
[12] To ensure proper operation, the power pins should be driven to their specified level even if the associated peripheral is not used in the application.
[13] This pin must always be connected. If the internal voltage regulator is not being used, this pin may be connected to V_{DDEXT}. Otherwise it should be powered according to the VDDVR specification. For automotive grade models, the internal voltage regulator must not be used and this pin must be tied to V_{DDEXT}.

SPECIFICATIONS

OPERATING CONDITIONS

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DDINT}[1, 2]	Internal Supply Voltage	Nonautomotive grade models	0.9		1.43	V
	Internal Supply Voltage	Automotive and extended temp grade models	1.0		1.38	V
	Internal Supply Voltage	Mobile DDR SDRAM models	1.14		1.31	V
V_{DDEXT}[3]	External Supply Voltage	Nonautomotive 3.3 V I/O	2.7	3.3	3.6	V
	External Supply Voltage	Nonautomotive 2.5 V I/O	2.25	2.5	2.75	V
	External Supply Voltage	Automotive and extended temp grade models	2.7	3.3	3.6	V
V_{DDUSB}	USB External Supply Voltage		3.0	3.3	3.6	V
V_{DDMP}	MXVR PLL Supply Voltage	Nonautomotive grade models	0.9		1.43	V
	MXVR PLL Supply Voltage	Automotive and extended temp grade models	1.0		1.38	V
V_{DDRTC}	Real Time Clock Supply Voltage	Nonautomotive grade models	2.25		3.6	V
	Real Time Clock Supply Voltage	Automotive and extended temp grade models	2.7	3.3	3.6	V
V_{DDDDR}	DDR Memory Supply Voltage	DDR SDRAM models	2.5	2.6	2.7	V
	DDR Memory Supply Voltage	Mobile DDR SDRAM models	1.8	1.875	1.95	V
V_{DDVR}[4]	Internal Voltage Regulator Supply Voltage		2.7	3.3	3.6	V
V_{IH}	High Level Input Voltage[5, 6]	V_{DDEXT} = maximum	2.0		3.6	V
V_{IHDDR}	High Level Input Voltage[7]	DDR SDRAM models	V_{DDR_VREF} + 0.15		V_{DDDDR} + 0.3	V
	High Level Input Voltage[7]	Mobile DDR SDRAM models	V_{DDR_VREF} + 0.125		V_{DDDDR} + 0.3	V
V_{IH5V}[12]	High Level Input Voltage[8]	V_{DDEXT} = maximum	2.0		5.5	V
V_{IHTWI}	High Level Input Voltage[9, 13]	V_{DDEXT} = maximum	0.7 × V_{DDEXT}		5.5	V
V_{IHUSB}	High Level Input Voltage[10]				5.25	V
V_{IL}	Low Level Input Voltage[5, 11]	V_{DDEXT} = minimum	–0.3		0.6	V
V_{IL5V}	Low Level Input Voltage[12]	3.3 V I/O, V_{DDEXT} = minimum	–0.3		0.8	V
	Low Level Input Voltage[12]	2.5 V I/O, V_{DDEXT} = minimum	–0.3		0.6	V
V_{ILDDR}	Low Level Input Voltage[7]	DDR SDRAM models	–0.3		V_{DDR_VREF} – 0.15	V
	Low Level Input Voltage[7]	Mobile DDR SDRAM models	–0.3		V_{DDR_VREF} – 0.125	V
V_{ILTWI}	Low Level Input Voltage[9, 13]		–0.3		0.3 × V_{DDEXT}	V
V_{DDR_VREF}	DDR_VREF Pin Input Voltage		0.49 × V_{DDDDR}	0.50 × V_{DDDDR}	0.51 × V_{DDDDR}	V
T_J[14]	Junction Temperature (400/533 MHz)	400-Ball CSP_BGA @$T_{AMBIENT}$ = –40°C to +85°C	–40		+105	°C
	Junction Temperature (600 MHz)	400-Ball CSP_BGA @$T_{AMBIENT}$ = 0°C to +70°C	0		+90	°C
	Junction Temperature (400 MHz)	400-Ball CSP_BGA @$T_{AMBIENT}$ = –40°C to +105°C	–40		+125	°C

[1] See Table 12 on Page 35 for frequency/voltage specifications.
[2] V_{DDINT} maximum is 1.10 V during one-time-programmable (OTP) memory programming operations.
[3] V_{DDEXT} minimum is 3.0 V and maximum is 3.6 V during OTP memory programming operations.
[4] Use of the internal voltage regulator is not supported on 600 MHz speed grade models or on automotive grade models. An external voltage regulator must be used.
[5] Bidirectional pins (D15–0, PA15–0, PB14–0, PC15–0, PD15–0, PE15–0, PF15–0, PG15–0, PH13–0, PI15–0, PJ14–0) and input pins ($\overline{ATAPI\_PDIAG}$, USB_ID, TCK, TDI, TMS, $\overline{TRST}$, CLKIN, $\overline{RESET}$, $\overline{NMI}$, and BMODE3–0) of the ADSP-BF54x Blackfin processors are 3.3 V-tolerant (always accept up to 3.6 V maximum V_{IH}). Voltage compliance (on outputs, V_{OH}) is limited by the V_{DDEXT} supply voltage. The regulator can generate V_{DDINT} at levels of 0.90 V to 1.30 V with -5% to +5% tolerance.
[6] Parameter value applies to all input and bidirectional pins except PB1-0, PE15-14, PG15–11, PH7-6, DQ0-15, and DQS0-1.
[7] Parameter value applies to pins DQ0–15 and DQS0–1.
[8] PB1-0, PE15-14, PG15-11, and PH7-6 are 5.0 V-tolerant (always accept up to 5.5 V maximum V_{IH} when power is applied to V_{DDEXT} pins). Voltage compliance (on output V_{OH}) is limited by V_{DDEXT} supply voltage.
[9] SDA and SCL are 5.0 V tolerant (always accept up to 5.5 V maximum V_{IH}). Voltage compliance on outputs (V_{OH}) is limited by the $_{VDDEXT}$ supply voltage.

[13]See the *ADSP-BF54x Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[14]Includes current on V_{DDEXT}, V_{DDUSB}, V_{DDVR}, and V_{DDDR} supplies. Clock inputs are tied high or low.
[15]Guaranteed maximum specifications.
[16]Unit for V_{DDINT} is V (volts). Unit for f_{SCLK} is MHz. Example: 1.2 V, 133 MHz would be 0.77 × 1.2 × 133 = 122.9 mA added to $I_{DDDEEPSLEEP}$.
[17]See Table 18 for the list of I_{DDINT} power vectors covered.

Total power dissipation has two components:

- Static, including leakage current
- Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 36 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 16 and Table 17), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 19).

There are two parts to the dynamic component. The first part is due to transistor switching in the core clock (CCLK) domain. This part is subject to an activity scaling factor (ASF) which represents application code running on the processor core and L1/L2 memories (Table 18). The ASF is combined with the CCLK frequency and V_{DDINT} dependent data in Table 19 to calculate this part. The second part is due to transistor switching in the system clock (SCLK) domain, which is included in the I_{DDINT} specification equation.

Table 16. Static Current—Low Power Process (mA)[1]

	Voltage (V_{DDINT})[2]												
T_J (°C)[2]	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.38 V	1.40 V	1.43 V
–40	11.9	13.5	15.5	17.7	20.3	23.3	26.8	30.6	35.0	39.9	43.2	45.5	49.5
0	20.1	22.3	24.7	27.8	31.1	34.9	39.3	44.2	49.6	55.7	59.8	62.5	67.2
25	31.2	34.2	37.5	41.3	45.6	50.3	55.7	61.7	68.2	75.4	80.3	83.6	88.6
45	47.0	51.0	55.5	60.6	66.0	72.0	78.8	86.1	94.2	102.9	108.9	112.8	118.2
55	58.6	63.1	68.3	74.1	80.3	87.1	94.9	103.0	112.0	122.0	128.4	132.8	140.0
70	80.7	86.6	93.0	100.2	108.1	116.7	125.9	136.0	146.8	158.7	166.4	171.6	179.5
85	107.0	114.3	122.5	131.5	141.2	151.7	163.1	175.3	188.5	202.7	211.8	218.0	226.7
100	153.9	163.0	173.3	184.8	197.0	210.0	224.1	239.0	255.1	272.4	283.4	290.8	300.6
105	171.7	181.5	192.7	205.1	218.3	232.4	247.5	263.6	280.9	299.3	308.7	314.9	325.7
115	210.1	221.4	234.2	248.6	263.7	279.9	297.3	311.0	331.1	352.5	366.3	N/A	N/A
125	257.9	270.9	285.9	302.5	314.6	334.0	354.3	375.7	399.2	423.8	439.6	N/A	N/A

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ for 400 MHz speed-grade devices.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 34.

Table 17. Static Current—Automotive 400 MHz and All 533 MHz/600 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})[2]												
T_J (°C)[2]	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.38 V	1.40 V	1.43 V
–40	19.7	22.1	24.8	27.9	31.4	35.4	39.9	45.0	50.6	57.0	61.2	64.0	70.4
0	45.2	49.9	55.2	61.3	67.9	75.3	83.5	92.6	102.6	113.6	121.0	125.8	135.0
25	80.0	87.5	96.2	105.8	116.4	127.9	140.4	154.1	169.2	185.4	196.1	203.3	218.0
45	124.2	134.8	147.1	160.7	175.3	191.2	208.6	227.3	247.6	269.6	284.0	293.6	312.0
55	154.6	167.2	181.7	197.7	214.9	233.8	254.2	276.1	299.7	325.9	343.1	354.6	374.0
70	209.8	225.6	243.9	264.1	285.8	309.4	334.8	363.5	394.3	427.7	449.4	463.9	489.0
85	281.8	301.3	323.5	350.2	378.5	408.9	442.1	477.9	516.5	557.5	584.2	602.0	629.0
100	366.5	390.5	419.4	452.1	486.9	524.4	564.8	608.2	654.8	704.7	737.0	758.5	793.0
105	403.8	428.3	459.5	494.3	531.7	571.9	614.9	661.5	711.1	763.9	798.5	821.6	864.0

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ for automotive 400 MHz and all 533 MHz and 600 MHz speed grade devices.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 34.

Table 28. Asynchronous Memory Read Cycle Timing with Asynchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDAT}	DATA15–0 Setup Before CLKOUT	5.0		ns
t_{HDAT}	DATA15–0 Hold After CLKOUT	0.8		ns
t_{DANR}	ARDY Negated Delay from $\overline{AMSx}$ Asserted[1]		$(S + RA - 2) \times t_{SCLK}$	ns
t_{HAA}	ARDY Asserted Hold After $\overline{ARE}$ Negated	0.0		ns
Switching Characteristics				
t_{DO}	Output Delay After CLKOUT[2]		6.0	ns
t_{HO}	Output Hold After CLKOUT[2]	0.3		ns

[1] S = number of programmed setup cycles, RA = number of programmed read access cycles.
[2] Output pins include $\overline{AMS3-0}$, $\overline{ABE1-0}$, ADDR19–1, $\overline{AOE}$, and $\overline{ARE}$.

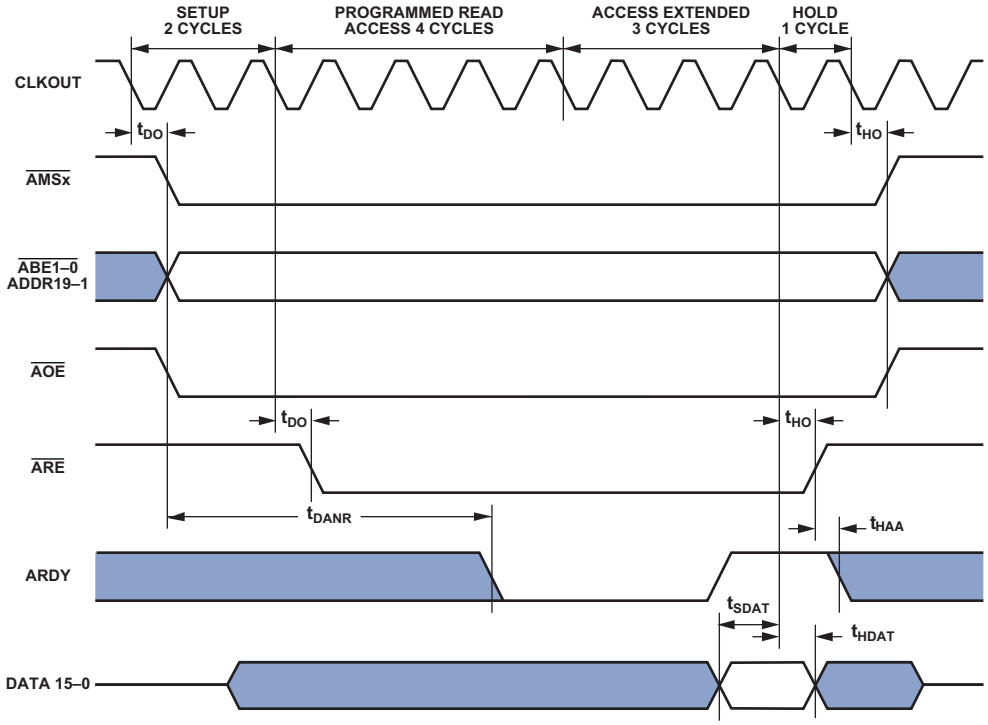


Figure 14. Asynchronous Memory Read Cycle Timing with Asynchronous ARDY

Asynchronous Memory Write Cycle Timing

Table 29 and Table 30 on Page 47 and Figure 15 and Figure 16 on Page 47 describe asynchronous memory write cycle operations for synchronous and for asynchronous ARDY.

Table 29. Asynchronous Memory Write Cycle Timing with Synchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{SARDY}	ARDY Setup Before the Falling Edge of CLKOUT	5.0		ns
t_{HARDY}	ARDY Hold After the Falling Edge of CLKOUT	0.0		ns
Switching Characteristics				
t_{DDAT}	DATA15–0 Disable After CLKOUT		6.0	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT	0.0		ns
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT[1]	0.3		ns

[1] Output pins include $\overline{AMS3–0}$, $\overline{ABE1–0}$, ADDR19–1, and $\overline{AWE}$.

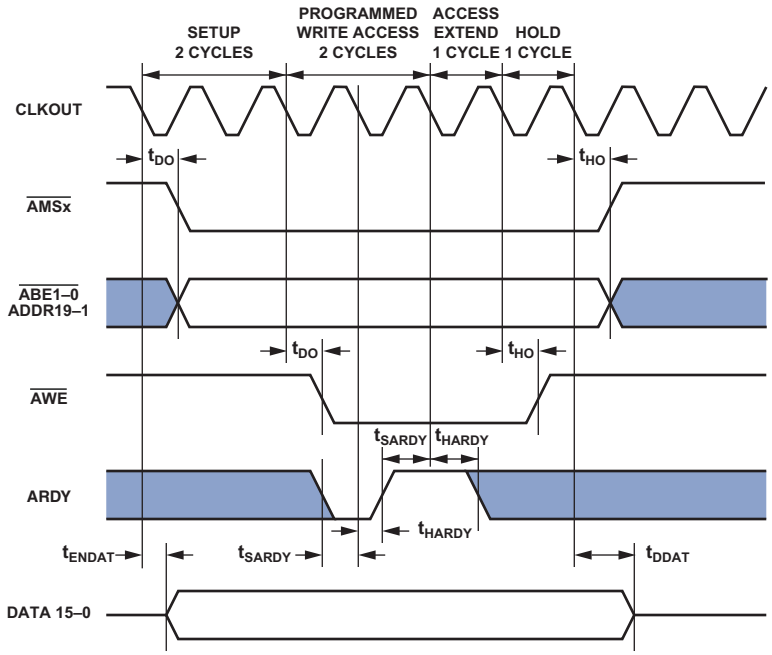


Figure 15. Asynchronous Memory Write Cycle Timing with Synchronous ARDY

DDR SDRAM/Mobile DDR SDRAM Clock and Control Cycle Timing

Table 31 and Figure 17 describe DDR SDRAM/mobile DDR SDRAM clock and control cycle timing.

Table 31. DDR SDRAM/Mobile DDR SDRAM Clock and Control Cycle Timing

Parameter		DDR SDRAM Min	DDR SDRAM Max	Mobile DDR SDRAM Min	Mobile DDR SDRAM Max	Unit
Switching Characteristics						
t_{CK}[1]	DCK0-1 Period, Non-Extended Temperature Grade Models	7.50		7.50	8.33	ns
	DCK0-1 Period, Extended Temperature Grade Models	10.00		N/A	N/A	ns
t_{CH}	DCK0-1 High Pulse Width	0.45	0.55	0.45	0.55	t_{CK}
t_{CL}	DCK0-1 Low Pulse Width	0.45	0.55	0.45	0.55	t_{CK}
t_{AS}[2, 3]	Address and Control Output SETUP Time Relative to CK	1.00		1.00		ns
t_{AH}[2, 3]	Address and Control Output HOLD Time Relative to CK	1.00		1.00		ns
t_{OPW}[2, 3]	Address and Control Output Pulse Width	2.20		2.30		ns

[1] The t_{CK} specification does not account for the effects of jitter.
[2] Address pins include DA0-12 and DBA0-1.
[3] Control pins include $\overline{\text{DCS0-1}}$, DCLKE, $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, and $\overline{\text{DWE}}$.

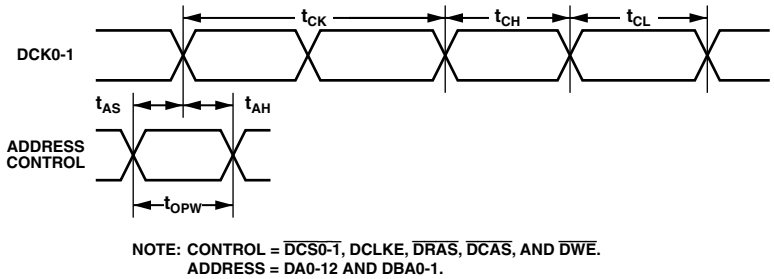


Figure 17. DDR SDRAM /Mobile DDR SDRAM Clock and Control Cycle Timing

External Port Bus Request and Grant Cycle Timing

Table 34 and Table 35 on Page 52 and Figure 21 and Figure 22 on Page 52 describe external port bus request and grant cycle operations for synchronous and for asynchronous $\overline{BR}$.

Table 34. External Port Bus Request and Grant Cycle Timing with Synchronous $\overline{BR}$

Parameter		Min	Max	Unit
Timing Requirements				
t_{BS}	$\overline{BR}$ Asserted to CLKOUT Low Setup	5.0		ns
t_{BH}	CLKOUT Low to $\overline{BR}$ Deasserted Hold Time	0.0		ns
Switching Characteristics				
t_{SD}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Disable		5.0	ns
t_{SE}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}$/$\overline{AWE}$ Enable		5.0	ns
t_{DBG}	CLKOUT Low to $\overline{BG}$ Asserted Output Delay		4.0	ns
t_{EBG}	CLKOUT Low to $\overline{BG}$ Deasserted Output Hold		4.0	ns
t_{DBH}	CLKOUT Low to $\overline{BGH}$ Asserted Output Delay		3.6	ns
t_{EBH}	CLKOUT Low to $\overline{BGH}$ Deasserted Output Hold		3.6	ns

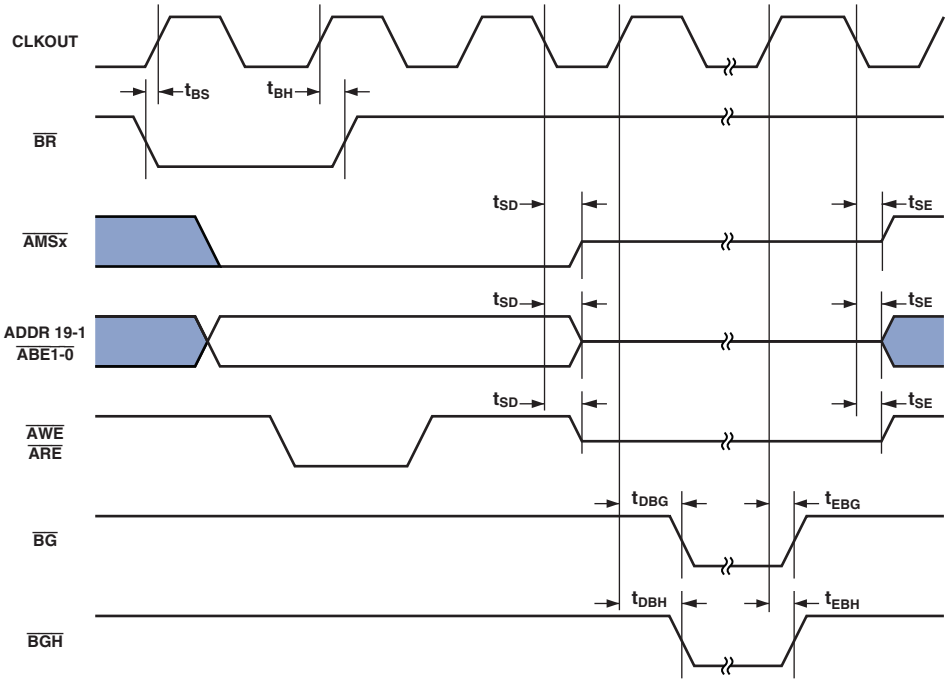


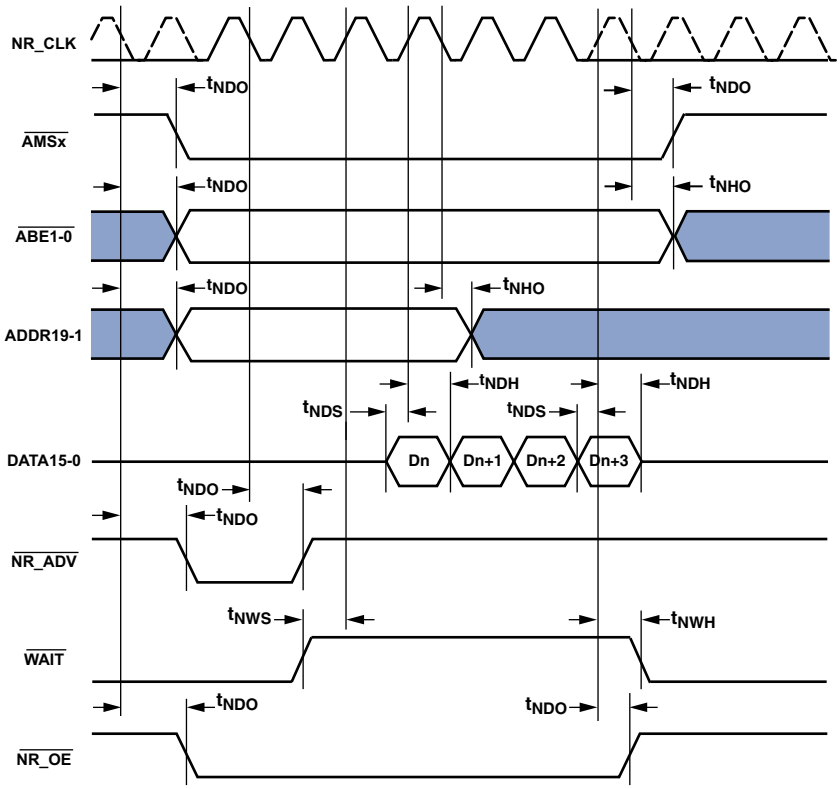
Figure 21. External Port Bus Request and Grant Cycle Timing with Synchronous $\overline{BR}$

Synchronous Burst AC Timing

Table 37 and Figure 28 on Page 57 describe Synchronous Burst AC operations.

Table 37. Synchronous Burst AC Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{NDS}	DATA15-0 Setup Before NR_CLK	4.0		ns
t_{NDH}	DATA15-0 Hold After NR_CLK	2.0		ns
t_{NWS}	WAIT Setup Before NR_CLK	8.0		ns
t_{NWH}	WAIT Hold After NR_CLK	0.0		ns
Switching Characteristics				
t_{NDO}	$\overline{AMSx}$, $\overline{ABE1-0}$, ADDR19-1, $\overline{NR\_ADV}$, $\overline{NR\_OE}$ Output Delay After NR_CLK	6.0		ns
t_{NHO}	$\overline{ABE1-0}$, ADDR19-1 Output Hold After NR_CLK	–3.0		ns



NOTE: NR_CLK dotted line represents a free running version of NR_CLK that is not visible on the NR_CLK pin.

Figure 28. Synchronous Burst AC Interface Timing

Table 42. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DTENE}	Data Enable Delay from External TSCLKx[1]	0		ns
t_{DDTTE}	Data Disable Delay from External TSCLKx[1, 2, 3]		10	ns
t_{DTENI}	Data Enable Delay from Internal TSCLKx[1]	–2		ns
t_{DDTTI}	Data Disable Delay from Internal TSCLKx[1, 2, 3]		3	ns

[1] Referenced to drive edge.
[2] Applicable to multichannel mode only.
[3] TSCLKx is tied to RSCLKx.

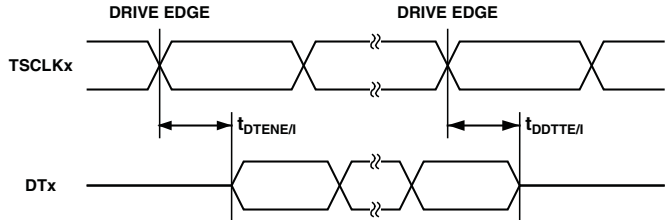


Figure 36. Serial Ports—Enable and Three-State

Table 43. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFSx or External RFSx in multi-channel mode with MFD = 01[1, 2]		10.0	ns
$t_{DTENLFSE}$	Data Enable from External RFSx in multi-channel mode with MFD = 0[1, 2]	0		ns

[1] In multichannel mode, TFSx enable and TFSx valid follow $t_{DTENLFS}$ and $t_{DDTLFSE}$.
[2] If external RFS/TFS setup to RSCLK/TSCLK > $t_{SCLKE}/2$, then $t_{DDTE/I}$ and $t_{DTENE/I}$ apply; otherwise $t_{DDTLFSE}$ and $t_{DTENLFS}$ apply.

Register and PIO

Table 58 and Figure 48 describe the ATAPI register and the PIO data transfer timing. The material in this figure is adapted from ATAPI-6 (INCITS 361-2002[R2007] and is used with permission of the American National Standards Institute (ANSI) on behalf of the Information Technology Industry Council ("ITIC"). Copies of ATAPI-6 (INCITS 361-2002 [R2007] can be purchased from ANSI.

Table 58. ATAPI Register and PIO Data Transfer Timing

ATAPI Parameter/Description		ATAPI_REG/PIO_TIM_x Timing Register Setting[1]	Timing Equation
t_0	Cycle time	T2_PIO, TEOC_PIO	$(T2\_PIO + TEOC\_PIO) \times t_{SCLK}$
t_1	ATAPI_ADDR valid to ATAPI_DIOR/ATAPI_DIOW setup	T1	$T1 \times t_{SCLK} - (t_{SK1} + t_{SK2} + t_{SK4})$
t_2	ATAPI_DIOR/ATAPI_DIOW pulse width	T2_PIO	$T2\_PIO \times t_{SCLK}$
t_{2i}	ATAPI_DIOR/ATAPI_DIOW recovery time	TEOC_PIO	$TEOC\_PIO \times t_{SCLK}$
t_3	ATAPI_DIOW data setup	T2_PIO	$T2\_PIO \times t_{SCLK} - (t_{SK1} + t_{SK2} + t_{SK4})$
t_4	ATAPI_DIOW data hold	T4	$T4 \times t_{SCLK} - (t_{SK1} + t_{SK2} + t_{SK4})$
t_5	ATAPI_DIOR data setup	N/A	$t_{OD} + t_{SUD} + 2 \times t_{BD} + t_{CDD} + t_{CDC}$
t_6	ATAPI_DIOR data hold	N/A	0
t_9	ATAPI_DIOR/ATAPI_DIOW to ATAPI_ADDR valid hold	TEOC_PIO	$TEOC\_PIO \times t_{SCLK} - (t_{SK1} + t_{SK2} + t_{SK4})$
t_A	ATAPI_IORDY setup time	T2_PIO	$T2\_PIO \times t_{SCLK} - (t_{OD} + t_{SUI} + 2 \times t_{CDC} + 2 \times t_{BD})$

[1] ATAPI timing register setting should be programmed with a value that guarantees parameter compliance with the ATA ANSI specification for the ATA device mode of operation.

Note that in Figure 48 ATAPI_ADDR pins include A1-3, ATAPI_CS0, and ATAPI_CS1. Alternate ATAPI port ATAPI_ADDR pins include ATAPI_A0A, ATAPI_A1A, ATAPI_A2A, ATAPI_CS0, and ATAPI_CS1. Note that an alternate ATAPI_D0-15 port bus is ATAPI_D0-15A.

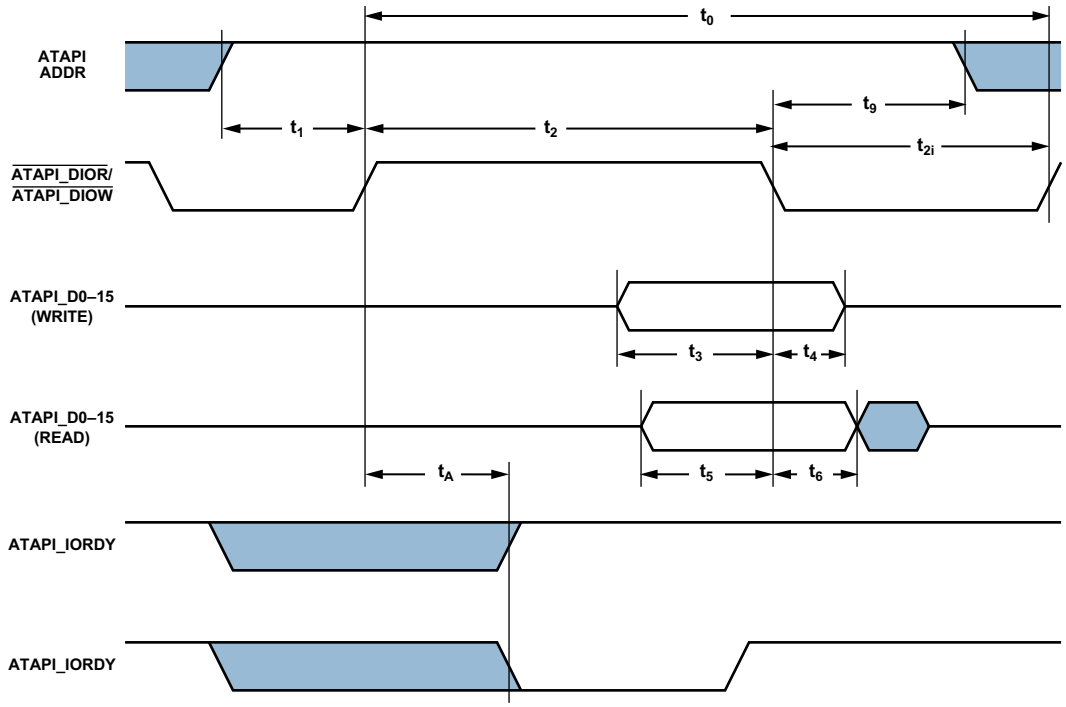


Figure 48. REG and PIO Data Transfer Timing

USB On-The-Go-Dual-Role Device Controller Timing

Table 62 describes the USB On-The-Go Dual-Role Device Controller timing requirements.

Table 62. USB On-The-Go Dual-Role Device Controller Timing Requirements

Parameter		Min	Max	Unit
Timing Requirements				
f_{USB}	USB_XI frequency	9	33.3	MHz
FS_{USB}	USB_XI Clock Frequency Stability	–50	+50	ppm

JTAG Test And Emulation Port Timing

Table 63 and Figure 61 describe JTAG port operations.

Table 63. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High	4		ns
t_{HTAP}	TDI, TMS Hold After TCK High	4		ns
t_{SSYS}	System Inputs Setup Before TCK High[1]	4		ns
t_{HSYS}	System Inputs Hold After TCK High[1]	11		ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse-Width[2] (measured in TCK cycles)	4		t_{TCK}
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	16.5	ns

[1] System inputs = PA15–0, PB14–0, PC13–0, PD15–0, PE15–0, PF15–0, PG15–0, PH13–0, PI15–0, PJ13–0, DQ15–0, DQS1–0, D15–0, $\overline{\text{ATAPI\_PDIAG}}$, $\overline{\text{RESET}}$, $\overline{\text{NMI}}$, and BMODE3–0.

[2] 50 MHz Maximum.

[3] System outputs = PA15–0, PB14–0, PC13–0, PD15–0, PE15–0, PF15–0, PG15–0, PH13–0, PI15–0, PJ13–0, DQ15–0, DQS1–0, D15–0, DA12–0, DBA1–0, DQM1–0, DCLK0-1, $\overline{\text{DCLK0–1}}$, $\overline{\text{DCS1–0}}$, DCLKE, $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, $\overline{\text{DWE}}$, $\overline{\text{AMS3–0}}$, $\overline{\text{ABE1–0}}$, $\overline{\text{AOE}}$, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$, CLKOUT, A3–1, and MFS.

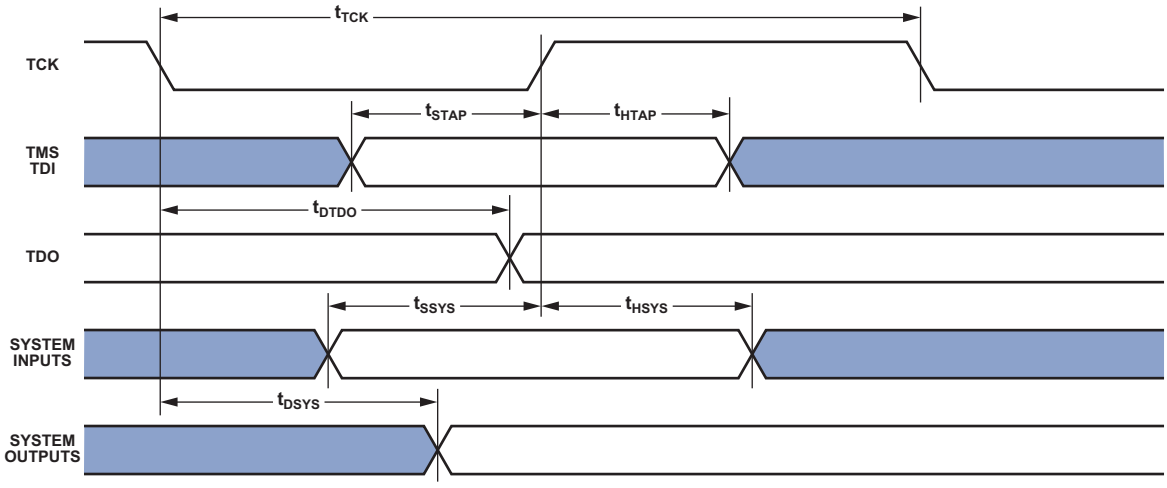


Figure 61. JTAG Port Timing

Table 66 lists the CSP_BGA package by ball number for the ADSP-BF549. Table 65 on Page 94 lists the CSP_BGA package by signal.

Table 66. 400-Ball CSP_BGA Ball Assignment (Numerical by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	GND	C1	MXO	E1	USB_DP	G1	PC5
A2	A2	C2	MXI	E2	USB_DM	G2	PC4
A3	PI0	C3	PH5	E3	GND	G3	USB_ID
A4	PI2	C4	PH9	E4	MLF_P	G4	V_{DDUSB}
A5	PI4	C5	PH11	E5	V_{DDEXT}	G5	V_{DDEXT}
A6	PI6	C6	PH13	E6	MFS	G6	V_{DDEXT}
A7	PI8	C7	PH10	E7	GND_{MP}	G7	V_{DDEXT}
A8	PI11	C8	PI9	E8	V_{DDMP}	G8	V_{DDINT}
A9	PI12	C9	PI13	E9	V_{DDEXT}	G9	GND
A10	$\overline{AMS0}$	C10	$\overline{AOE}$	E10	V_{DDEXT}	G10	GND
A11	CLKIN	C11	$\overline{NMI}$	E11	V_{DDEXT}	G11	GND
A12	XTAL	C12	$\overline{RESET}$	E12	V_{DDEXT}	G12	V_{DDINT}
A13	GND	C13	D1	E13	V_{DDRTC}	G13	V_{DDINT}
A14	RTXI	C14	D8	E14	D14	G14	V_{DDEXT}
A15	D4	C15	D9	E15	D13	G15	V_{DDDDR}
A16	D6	C16	$\overline{ABE1}$	E16	$\overline{DCLK0}$	G16	DA4
A17	D10	C17	$\overline{ABE0}$	E17	$\overline{DRAS}$	G17	DA1
A18	$VROUT_0$	C18	DCLK1	E18	$\overline{DWE}$	G18	DA3
A19	$VROUT_1$	C19	$\overline{DCS0}$	E19	DA9	G19	DA0
A20	GND	C20	DA7	E20	DA2	G20	DQM0
B1	USB_VREF	D1	GND	F1	USB_XI	H1	PC3
B2	A1	D2	USB_VBUS	F2	USB_XO	H2	PC0
B3	A3	D3	USB_RSET	F3	GND	H3	PC7
B4	PI1	D4	GND	F4	MLF_M	H4	PH7
B5	PI3	D5	PH8	F5	V_{DDUSB}	H5	V_{DDEXT}
B6	PI5	D6	PH6	F6	GND	H6	V_{DDEXT}
B7	PI7	D7	PH12	F7	V_{DDEXT}	H7	GND
B8	PI10	D8	PI14	F8	V_{DDEXT}	H8	GND
B9	PI15	D9	$\overline{AMS1}$	F9	V_{DDINT}	H9	GND
B10	$\overline{AMS2}$	D10	$\overline{AMS3}$	F10	V_{DDDDR}	H10	GND
B11	GND	D11	CLKBUF	F11	V_{DDDDR}	H11	GND
B12	$\overline{ARE}$	D12	$\overline{AWE}$	F12	V_{DDDDR}	H12	GND
B13	D2	D13	D0	F13	V_{DDEXT}	H13	V_{DDDDR}
B14	RTXO	D14	D11	F14	GND	H14	V_{DDDDR}
B15	D3	D15	D12	F15	V_{DDVR}	H15	V_{DDDDR}
B16	D5	D16	DCLK0	F16	$\overline{DCAS}$	H16	DBA1
B17	D7	D17	D15	F17	DA11	H17	DBA0
B18	DCLKE	D18	$\overline{DCLK1}$	F18	DA8	H18	DQS1
B19	$\overline{DCS1}$	D19	DA12	F19	DA5	H19	DQM1
B20	DA10	D20	DA6	F20	DQS0	H20	DQ11

Table 66. 400-Ball CSP_BGA Ball Assignment (Numerical by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
J1	PF1	L1	PF5	N1	PF14	R1	PD2
J2	PC2	L2	PF4	N2	PF15	R2	PD3
J3	PC1	L3	PF8	N3	PG3	R3	PD5
J4	PG0	L4	PF6	N4	PF13	R4	PD7
J5	PC6	L5	PG2	N5	V_{DDEXT}	R5	$\overline{EMU}$
J6	V_{DDINT}	L6	V_{DDINT}	N6	GND	R6	V_{DDEXT}
J7	GND	L7	GND	N7	GND	R7	V_{DDEXT}
J8	GND	L8	GND	N8	GND	R8	V_{DDEXT}
J9	GND	L9	GND	N9	GND	R9	GND
J10	GND	L10	GND	N10	GND	R10	V_{DDINT}
J11	GND	L11	GND	N11	GND	R11	V_{DDINT}
J12	GND	L12	GND	N12	GND	R12	V_{DDINT}
J13	V_{DDINT}	L13	GND	N13	GND	R13	GND
J14	V_{DDDDR}	L14	GND	N14	GND	R14	GND
J15	V_{DDDDR}	L15	V_{DDINT}	N15	V_{DDEXT}	R15	V_{DDEXT}
J16	DQ15	L16	CLKOUT	N16	PJ7	R16	GND
J17	DQ14	L17	DQ4	N17	PJ4	R17	PE7
J18	DQ13	L18	DQ0	N18	PJ1	R18	PG13
J19	DQ12	L19	DQ2	N19	PJ13	R19	PJ8
J20	DQ9	L20	DQ3	N20	DDR_VSSR	R20	PJ0
K1	PF3	M1	PF9	P1	PG4	T1	PD4
K2	PF2	M2	PF10	P2	PE11	T2	PD6
K3	PF0	M3	PF11	P3	PD0	T3	PD10
K4	PF7	M4	PF12	P4	PD1	T4	PD12
K5	PG1	M5	PE12	P5	PE13	T5	$\overline{TRST}$
K6	V_{DDEXT}	M6	GND	P6	V_{DDINT}	T6	PB2
K7	GND	M7	GND	P7	V_{DDINT}	T7	V_{DDEXT}
K8	GND	M8	GND	P8	GND	T8	V_{DDEXT}
K9	GND	M9	GND	P9	GND	T9	V_{DDEXT}
K10	GND	M10	GND	P10	GND	T10	V_{DDEXT}
K11	GND	M11	GND	P11	GND	T11	V_{DDEXT}
K12	GND	M12	GND	P12	GND	T12	V_{DDEXT}
K13	GND	M13	GND	P13	GND	T13	V_{DDEXT}
K14	V_{DDDDR}	M14	GND	P14	V_{DDINT}	T14	V_{DDEXT}
K15	V_{DDDDR}	M15	V_{DDEXT}	P15	V_{DDEXT}	T15	V_{DDEXT}
K16	DQ5	M16	PJ2	P16	PG12	T16	V_{DDEXT}
K17	DQ7	M17	PJ11	P17	PJ9	T17	PE1
K18	DQ10	M18	EXT_WAKE	P18	PJ6	T18	PE10
K19	DQ8	M19	DQ1	P19	$\overline{ATAPI\_PDIAG}$	T19	PJ10
K20	DQ6	M20	DDR_VREF	P20	PJ12	T20	PJ3

AUTOMOTIVE PRODUCTS

The ADSP-BF542, ADSP-BF544, and the ADSP-BF549 models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the product Specifications section of this data sheet carefully.

Only the automotive grade products shown in Table 68 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

Table 68. Automotive Products

Product Family[1, 2]	Temperature Range[3]	Speed Grade (Max)	Package Description	Package Option
ADBF542WBBCZ4xx	–40°C to +85°C	400 MHz	400-Ball CSP_BGA	BC-400-1
ADBF542WBBCZ5xx	–40°C to +85°C	533 MHz	400-Ball CSP_BGA	BC-400-1
ADBF544WBBCZ5xx	–40°C to +85°C	533 MHz	400-Ball CSP_BGA	BC-400-1
ADBF549WBBCZ5xx	–40°C to +85°C	533 MHz	400-Ball CSP_BGA	BC-400-1
ADBF549MWBBCZ5xx	–40°C to +85°C	533 MHz	400-Ball CSP_BGA	BC-400-1

[1] Z = RoHS compliant part.
[2] The use of xx designates silicon revision.
[3] Referenced temperature is ambient temperature.

ORDERING GUIDE

Model[1, 2, 3, 4]	Temperature Range[5, 6]	Speed Grade (Max)	Package Description	Package Option
ADSP-BF542BBCZ-4A	–40°C to +85°C	400 MHz	400-Ball CSP_BGA	BC-400-1
ADSP-BF542BBCZ-5A	–40°C to +85°C	533 MHz	400-Ball CSP_BGA	BC-400-1
ADSP-BF542MBBCZ-5M	–40°C to +85°C	533 MHz	400-Ball CSP_BGA	BC-400-1
ADSP-BF542KBCZ-6A	0°C to +70°C	600 MHz	400-Ball CSP_BGA	BC-400-1
ADSP-BF544BBCZ-4A	–40°C to +85°C	400 MHz	400-Ball CSP_BGA	BC-400-1
ADSP-BF544BBCZ-5A	–40°C to +85°C	533 MHz	400-Ball CSP_BGA	BC-400-1
ADSP-BF544MBBCZ-5M	–40°C to +85°C	533 MHz	400-Ball CSP_BGA	BC-400-1
ADSP-BF547BBCZ-5A	–40°C to +85°C	533 MHz	400-Ball CSP_BGA	BC-400-1
ADSP-BF547MBBCZ-5M	–40°C to +85°C	533 MHz	400-Ball CSP_BGA	BC-400-1
ADSP-BF547KBCZ-6A	0°C to +70°C	600 MHz	400-Ball CSP_BGA	BC-400-1
ADSP-BF547YBC-4A	–40°C to +105°C	400 MHz	400-Ball CSP_BGA	BC-400-1
ADSP-BF547YBCZ-4A	–40°C to +105°C	400 MHz	400-Ball CSP_BGA	BC-400-1
ADSP-BF548MBBCZ-5M	–40°C to +85°C	533 MHz	400-Ball CSP_BGA	BC-400-1
ADSP-BF548BBCZ-5A	–40°C to +85°C	533 MHz	400-Ball CSP_BGA	BC-400-1
ADSP-BF548BBCZ-5AA	–40°C to +85°C	533 MHz	400-Ball CSP_BGA	BC-400-1

[1] Each ADSP-BF54xM model contains a mobile DDR controller and does not support the use of standard DDR memory.
[2] Z = RoHS compliant part.
[3] The ADSP-BF549 is available for automotive use only. Please contact your local ADI product representative or authorized distributor for specific automotive product ordering information.
[4] AA = low Alpha Package.
[5] Referenced temperature is ambient temperature.
[6] Temperature range –40°C to +105°C is classified as extended temperature range.