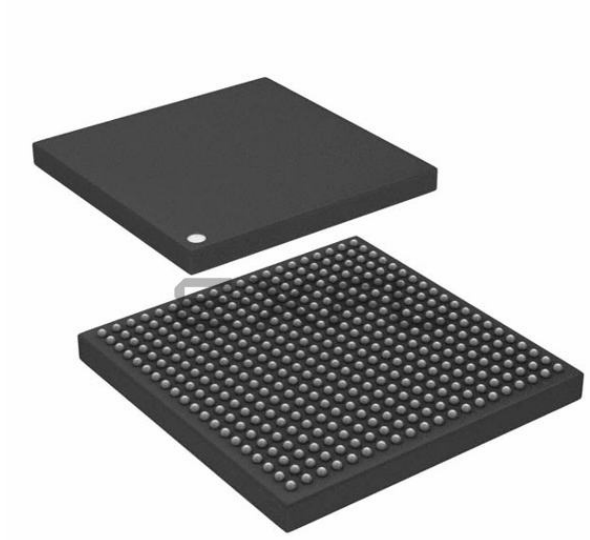

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	CAN, SPI, SSP, TWI, UART
Clock Rate	533MHz
Non-Volatile Memory	External
On-Chip RAM	196kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf544mbbcz-5m

MEMORY ARCHITECTURE

The ADSP-BF54x processors view memory as a single unified 4G byte address space, using 32-bit addresses. All resources, including internal memory, external memory, and I/O control registers, occupy separate sections of this common address space. The memory portions of this address space are arranged in a hierarchical structure to provide a good cost/performance balance of some very fast, low-latency on-chip memory as cache or SRAM, and larger, lower-cost and performance off-chip memory systems. See Figure 3 on Page 6.

The on-chip L1 memory system is the highest-performance memory available to the Blackfin processor. The off-chip memory system, accessed through the external bus interface unit (EBIU), provides expansion with flash memory, SRAM, and double-rate SDRAM (standard or mobile DDR), optionally accessing up to 768M bytes of physical memory.

Most of the ADSP-BF54x Blackfin processors also include an L2 SRAM memory array which provides up to 128K bytes of high speed SRAM, operating at one half the frequency of the core and with slightly longer latency than the L1 memory banks (for information on L2 memory in each processor, see Table 1). The L2 memory is a unified instruction and data memory and can hold any mixture of code and data required by the system design. The Blackfin cores share a dedicated low latency 64-bit data path port into the L2 SRAM memory.

The memory DMA controllers (DMAC1 and DMAC0) provide high-bandwidth data-movement capability. They can perform block transfers of code or data between the internal memory and the external memory spaces.

Internal (On-Chip) Memory

The ADSP-BF54x processors have several blocks of on-chip memory providing high bandwidth access to the core.

The first block is the L1 instruction memory, consisting of 64K bytes of SRAM, of which 16K bytes can be configured as a four-way set-associative cache or as SRAM. This memory is accessed at full processor speed.

The second on-chip memory block is the L1 data memory, consisting of 64K bytes of SRAM, of which 32K bytes can be configured as a two-way set-associative cache or as SRAM. This memory block is accessed at full processor speed.

The third memory block is a 4K byte scratchpad SRAM, which runs at the same speed as the L1 memories. It is only accessible as data SRAM and cannot be configured as cache memory.

The fourth memory block is the factory programmed L1 instruction ROM, operating at full processor speed. This ROM is not customer-configurable.

The fifth memory block is the L2 SRAM, providing up to 128K bytes of unified instruction and data memory, operating at one half the frequency of the core.

Finally, there is a 4K byte boot ROM connected as L3 memory. It operates at full SCLK rate.

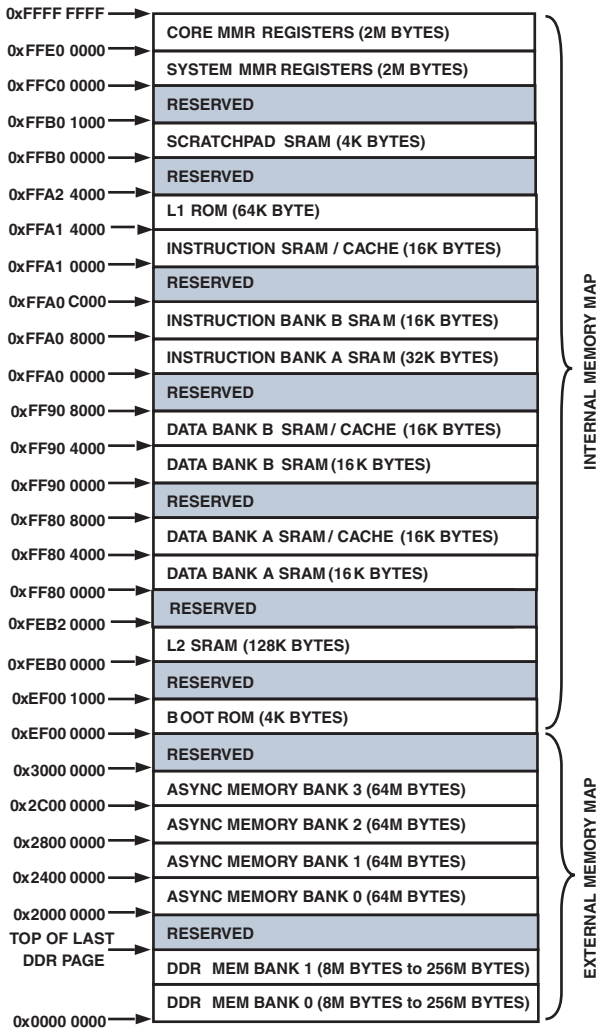

Figure 3. ADSP-BF547/ADSP-BF548/ADSP-BF549 Internal/External Memory Map[1]

[1] For ADSP-BF544 processors, L2 SRAM is 64K Bytes (0xFEB0000–0xFEB0FFFF). For ADSP-BF542 processors, there is no L2 SRAM.

External (Off-Chip) Memory

Through the external bus interface unit (EBIU), the ADSP-BF54x Blackfin processors provide glueless connectivity to external 16-bit wide memories, such as DDR and mobile DDR SDRAM, SRAM, NOR flash, NAND flash, and FIFO devices. To provide the best performance, the bus system of the DDR and mobile DDR interface is completely separate from the other parallel interfaces. Furthermore, the DDR controller supports either standard DDR memory or mobile DDR memory. See the Ordering Guide on Page 101 for details. Throughout this document, references to "DDR" are intended to cover both the standard and mobile DDR standards.

The timer units can be used in conjunction with the four UARTs and the CAN controllers to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timers can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to a count of external signals.

In addition to the general-purpose programmable timers, another timer is also provided by the processor core. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of periodic operating system interrupts.

UP/DOWN COUNTER AND THUMBWHEEL INTERFACE

A 32-bit up/down counter is provided that can sense the 2-bit quadrature or binary codes typically emitted by industrial drives or manual thumb wheels. The counter can also operate in general-purpose up/down count modes. Then count direction is either controlled by a level-sensitive input pin or by two edge detectors.

A third input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumb wheels. All three pins have a programmable debouncing circuit.

An internal signal forwarded to the timer unit enables one timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmable count values are exceeded.

SERIAL PORTS (SPORTS)

The ADSP-BF54x Blackfin processors incorporate up to four dual-channel synchronous serial ports (SPORT0, SPORT1, SPORT2, and SPORT3) for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation. Each SPORT has two sets of independent transmit and receive pins, enabling up to eight channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports. Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking. Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length. Each SPORT supports serial data words from 3 to 32 bits in length, transferred most-significant-bit first or least-significant-bit first.
- Framing. Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware. Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead. Each SPORT can receive and transmit multiple buffers of memory data automatically. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts. Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer or buffers through DMA.
- Multichannel capability. Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

SERIAL PERIPHERAL INTERFACE (SPI) PORTS

The ADSP-BF54x Blackfin processors have up to three SPI-compatible ports that allow the processor to communicate with multiple SPI-compatible devices.

Each SPI port uses three pins for transferring data: two data pins (master output slave input, SPIxMOSI, and master input-slave output, SPIxMISO) and a clock pin (serial clock, SPIxSCK). An SPI chip select input pin ($\overline{\text{SPIxSS}}$) lets other SPI devices select the processor, and three SPI chip select output pins per SPI port $\overline{\text{SPIxSELy}}$ let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI ports provide a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port's baud rate and clock phase/polarities are programmable, and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI's DMA controller can only service unidirectional accesses at any given time.

The SPI port's clock rate is calculated as

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

Where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port transmits and receives simultaneously by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORTS (UARTS)

The ADSP-BF54x Blackfin processors provide up to four full-duplex universal asynchronous receiver/transmitter (UART) ports. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port

The USB clock (USB_XI) is provided through a dedicated external crystal or crystal oscillator. See Table 62 for related timing requirements. If using a fundamental mode crystal to provide the USB clock, connect the crystal between USB_XI and USB_XO with a circuit similar to that shown in Figure 7. Use a parallel-resonant, fundamental mode, microprocessor-grade crystal. If a third-overtone crystal is used, follow the circuit guidelines outlined in Clock Signals on Page 17 for third-overtone crystals.

The USB On-the-Go dual-role device controller includes a Phase Locked Loop with programmable multipliers to generate the necessary internal clocking frequency for USB. The multiplier value should be programmed based on the USB_XI clock frequency to achieve the necessary 480 MHz internal clock for USB high speed operation. For example, for a USB_XI crystal frequency of 24 MHz, the USB_PLLOSC_CTRL register should be programmed with a multiplier value of 20 to generate a 480 MHz internal clock.

ATA/ATAPI-6 INTERFACE

The ATAPI interface connects to CD/DVD and HDD drives and is ATAPI-6 compliant. The controller implements the peripheral I/O mode, the multi-DMA mode, and the Ultra DMA mode. The DMA modes enable faster data transfer and reduced host management. The ATAPI controller supports PIO, multi-DMA, and ultra DMA ATAPI accesses. Key features include:

- Supports PIO modes 0, 1, 2, 3, 4
- Supports multiword DMA modes 0, 1, 2
- Supports ultra DMA modes 0, 1, 2, 3, 4, 5 (up to UDMA 100)
- Programmable timing for ATA interface unit
- Supports CompactFlash cards using true IDE mode

By default, the ATAPI_A0-2 address signals and the ATAPI_D0-15 data signals are shared on the asynchronous memory interface with the asynchronous memory and NAND flash controllers. The data and address signals can be remapped to GPIO ports F and G, respectively, by setting PORTF_MUX[1:0] to b#01.

KEYPAD INTERFACE

The keypad interface is a 16-pin interface module that is used to detect the key pressed in a 8 × 8 (maximum) keypad matrix. The size of the input keypad matrix is programmable. The interface is capable of filtering the bounce on the input pins, which is common in keypad applications. The width of the filtered bounce is programmable. The module is capable of generating an interrupt request to the core once it identifies that any key has been pressed.

The interface supports a press-release-press mode and infrastructure for a press-hold mode. The former mode identifies a press, release and press of a key as two consecutive presses of the same key, whereas the latter mode checks the input key's state in periodic intervals to determine the number of times the same key is meant to be pressed. It is possible to detect when multiple keys are pressed simultaneously and to provide limited key resolution capability when this happens.

SECURE DIGITAL (SD)/SDIO CONTROLLER

The SD/SDIO controller is a serial interface that stores data at a data rate of up to 10M bytes per second using a 4-bit data line.

The SD/SDIO controller supports the SD memory mode only. The interface supports all the power modes and performs error checking by CRC.

CODE SECURITY

An OTP/security system, consisting of a blend of hardware and software, provides customers with a flexible and rich set of code security features with Lockbox® secure technology. Key features include:

- OTP memory
- Unique chip ID
- Code authentication
- Secure mode of operation

The security scheme is based upon the concept of authentication of digital signatures using standards-based algorithms and provides a secure processing environment in which to execute code and protect assets. See Lockbox Secure Technology Disclaimer on Page 23.

MEDIA TRANSCEIVER MAC LAYER (MXVR)

The ADSP-BF549 Blackfin processors provide a media transceiver (MXVR) MAC layer, allowing the processor to be connected directly to a MOST® [1] network through an FOT. See Figure 5 on Page 15 for an example of a MXVR MOST connection.

The MXVR is fully compatible with industry-standard standalone MOST controller devices, supporting 22.579 Mbps or 24.576 Mbps data transfer. It offers faster lock times, greater jitter immunity, and a sophisticated DMA scheme for data transfers. The high speed internal interface to the core and L1 memory allows the full bandwidth of the network to be utilized. The MXVR can operate as either the network master or as a network slave.

The MXVR supports synchronous data, asynchronous packets, and control messages using dedicated DMA channels that operate autonomously from the processor core moving data to and from L1 and/or L2 memory. Synchronous data is transferred to or from the synchronous data physical channels on the MOST bus through eight programmable DMA channels. The synchronous data DMA channels can operate in various modes including modes that trigger DMA operation when data patterns are detected in the receive data stream. Furthermore, two DMA channels support asynchronous traffic, and two others support control message traffic.

[1] MOST is a registered trademark of Standard Microsystems, Corp.

Interrupts are generated when a user-defined amount of synchronous data has been sent or received by the processor or when asynchronous packets or control messages have been sent or received.

The MXVR peripheral can wake up the ADSP-BF549 Blackfin processor from sleep mode when a wakeup preamble is received over the network or based on any other MXVR interrupt event. Additionally, detection of network activity by the MXVR can be used to wake up the ADSP-BF549 Blackfin processor from the hibernate state. These features allow the ADSP-BF549 processor to operate in a low-power state when there is no network activity or when data is not currently being received or transmitted by the MXVR.

The MXVR clock is provided through a dedicated external crystal or crystal oscillator. The frequency of the external crystal or crystal oscillator can be 256 Fs, 384 Fs, 512 Fs, or 1024 Fs for Fs = 38 kHz, 44.1 kHz, or 48 kHz. If using a crystal to provide the MXVR clock, use a parallel-resonant, fundamental mode, microprocessor-grade crystal.

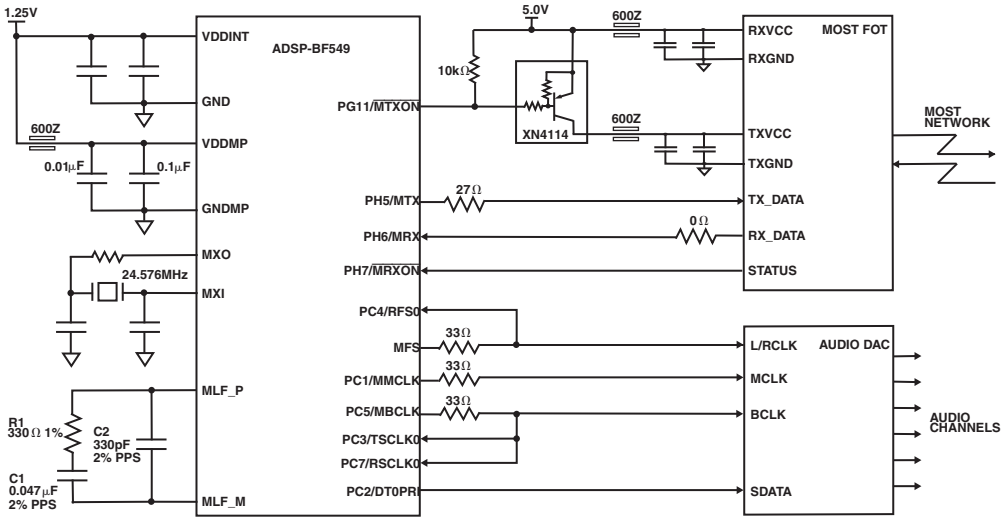

Figure 5. MXVR MOST Connection

DYNAMIC POWER MANAGEMENT

The ADSP-BF54x Blackfin processors provide five operating modes, each with a different performance/power profile. In addition, dynamic power management provides the control functions to dynamically alter the processor core supply voltage, further reducing power dissipation. Control of clocking to each of the ADSP-BF54x Blackfin processors' peripherals also reduces power consumption. See Table 4 for a summary of the power settings for each mode.

Full-On Operating Mode—Maximum Performance

In the full-on mode, the PLL is enabled and is not bypassed, providing the capability to run at the maximum operational frequency. This is the power-up default execution state in which maximum performance can be achieved. The processor core and all enabled peripherals run at full speed.

Active Operating Mode—Moderate Power Savings

In the active mode, the PLL is enabled but bypassed. Because the PLL is bypassed, the processor's core clock (CCLK) and system clock (SCLK) run at the input clock (CLKIN) frequency. DMA access is available to appropriately configured L1 memories.

In the active mode, it is possible to disable the control input to the PLL by setting the PLL_OFF bit in the PLL control register. This register can be accessed with a user-callable routine in the on-chip ROM called bfrom_SysControl(). For more information, see the "Dynamic Power Management" chapter in the *ADSP-BF54x Blackfin Processor Hardware Reference*. If disabled, the PLL must be re-enabled before transitioning to the full-on or sleep modes.

Table 4. Power Settings

Mode/State	PLL	PLL Bypassed	Core Clock (CCLK)	System Clock (SCLK)	Core Power
Full On	Enabled	No	Enabled	Enabled	On
Active	Enabled/ Disabled	Yes	Enabled	Enabled	On
Sleep	Enabled	-	Disabled	Enabled	On
Deep Sleep	Disabled	-	Disabled	Disabled	On
Hibernate	Disabled	-	Disabled	Disabled	Off

Table 6. Example System Clock Ratios

Signal Name SSEL3–0	Divider Ratio VCO/SCLK	Example Frequency Ratios (MHz)	
		VCO	SCLK
0010	2:1	200	100
0110	6:1	300	50
1010	10:1	500	50

Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be dynamically changed without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV) using the bfrom_SysControl() function in the on-chip ROM.

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 7. The default ratio is 1. This programmable core clock capability is useful for fast core frequency modifications.

The maximum CCLK frequency not only depends on the part's speed grade, it also depends on the applied V_{DDINT} voltage. See Table 12 on Page 35 for details.

Table 7. Core Clock Ratios

Signal Name CSEL1–0	Divider Ratio VCO/CCLK	Example Frequency Ratios (MHz)	
		VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	500	125
11	8:1	200	25

BOOTING MODES

The ADSP-BF54x Blackfin processors have many mechanisms (listed in Table 8) for automatically loading internal and external memory after a reset. The boot mode is specified by four BMODE input pins dedicated to this purpose. There are two categories of boot modes: master and slave. In master boot modes, the processor actively loads data from parallel or serial memories. In slave boot modes, the processor receives data from an external host device.

Table 8. Booting Modes

BMODE3–0	Description
0000	Idle-no boot
0001	Boot from 8- or 16-bit external flash memory
0010	Boot from 16-bit asynchronous FIFO
0011	Boot from serial SPI memory (EEPROM or flash)
0100	Boot from SPI host device
0101	Boot from serial TWI memory (EEPROM or flash)
0110	Boot from TWI host
0111	Boot from UART host

Table 8. Booting Modes (Continued)

BMODE3–0	Description
1000	Reserved
1001	Reserved
1010	Boot from DDR SDRAM/Mobile DDR SDRAM
1011	Boot from OTP memory
1100	Reserved
1101	Boot from 8- or 16-bit NAND flash memory via NFC
1110	Boot from 16-bit host DMA
1111	Boot from 8-bit host DMA

The boot modes listed in Table 8 provide a number of mechanisms for automatically loading the processor's internal and external memories after a reset. By default, all boot modes use the slowest allowed configuration settings. Default settings can be altered via the initialization code feature at boot time or by proper OTP programming at pre-boot time. Some boot modes require a boot host wait (HWAIT) signal, which is a GPIO output signal that is driven and toggled by the boot kernel at boot time. If pulled high through an external pull-up resistor, the HWAIT signal behaves active high and will be driven low when the processor is ready for data. Conversely, when pulled low, HWAIT is driven high when the processor is ready for data. When the boot sequence completes, the HWAIT pin can be used for other purposes. By default, HWAIT functionality is on GPIO port B (PB11). However, if PB11 is otherwise utilized in the system, an alternate boot host wait (HWAITA) signal can be enabled on GPIO port H (PH7) by programming the OTP_ALTERNATE_HWAIT bit in the PBS00L OTP memory page.

The BMODE pins of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the following modes:

- Idle-no boot mode (BMODE = 0x0)—In this mode, the processor goes into the idle state. The idle boot mode helps to recover from illegal operating modes, in case the OTP memory is misconfigured.
- Boot from 8- or 16-bit external flash memory—(BMODE = 0x1)—In this mode, the boot kernel loads the first block header from address 0x2000 0000 and, depending on instructions contained in the header, the boot kernel performs an 8- or 16-bit boot or starts program execution at the address provided by the header. By default, all configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).

  The ARDY pin is not enabled by default. It can, however, be enabled by OTP programming. Similarly, all interface behavior and timings can be customized through OTP programming. This includes activation of burst-mode or page-mode operation. In this mode, all asynchronous interface signals are enabled at the port muxing level.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *“Analog Devices JTAG Emulation Technical Reference”* (EE-68) on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

MXVR BOARD LAYOUT GUIDELINES

The MXVR Loop Filter RC network is connected between the MLF_P and MLF_M pins in the following manner:

Capacitors:

- C1: 0.047 µF (PPS type, 2% tolerance recommended)
- C2: 330 pF (PPS type, 2% tolerance recommended)

Resistor:

- R1: 330 Ω (1% tolerance)

The RC network should be located physically close to the MLF_P and MLF_M pins on the board.

The RC network should be shielded using GND_{MP} traces.

Avoid routing other switching signals near the RC network to avoid crosstalk.

MXI driven with external clock oscillator IC:

- MXI should be driven with the clock output of a clock oscillator IC running at a frequency of 49.152 MHz or 45.1584 MHz.
- MXO should be left unconnected.
- Avoid routing other switching signals near the oscillator and clock output trace to avoid crosstalk. When not possible, shield traces with ground.

MXI/MXO with external crystal:

- The crystal must be a fundamental mode crystal running at a frequency of 49.152 MHz or 45.1584 MHz.
- The crystal and load capacitors should be placed physically close to the MXI and MXO pins on the board.
- Board trace capacitance on each lead should not be more than 3 pF.
- Trace capacitance plus load capacitance should equal the load capacitance specification for the crystal.
- Avoid routing other switching signals near the crystal and components to avoid crosstalk. When not possible, shield traces and components with ground.

V_{DDMP}/GND_{MP}—MXVR PLL power domain:

- Route V_{DDMP} and GND_{MP} with wide traces or as isolated power planes.
- Drive V_{DDMP} to same level as V_{DDINT}.
- Place a ferrite bead between the V_{DDINT} power plane and the V_{DDMP} pin for noise isolation.
- Locally bypass V_{DDMP} with 0.1 µF and 0.01 µF decoupling capacitors to GND_{MP}.
- Avoid routing switching signals near to V_{DDMP} and GND_{MP} traces to avoid crosstalk.

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
DDR Memory Interface			
DA0–12	O	DDR Address Bus	D
DBA0–1	O	DDR Bank Active Strobe	D
DQ0–15	I/O	DDR Data Bus	D
DQS0–1	I/O	DDR Data Strobe	D
DQM0–1	O	DDR Data Mask for Reads and Writes	D
DCLK0–1	O	DDR Output Clock	D
$\overline{\text{DCLK0–1}}$	O	DDR Complementary Output Clock	D
$\overline{\text{DCS0–1}}$	O	DDR Chip Selects	D
DCLKE[9]	O	DDR Clock Enable (Requires a pull-down if hibernate with DDR self-refresh is used.)	D
$\overline{\text{DRAS}}$	O	DDR Row Address Strobe	D
$\overline{\text{DCAS}}$	O	DDR Column Address Strobe	D
$\overline{\text{DWE}}$	O	DDR Write Enable	D
DDR_VREF	I	DDR Voltage Reference	
DDR_VSSR	I	DDR Voltage Reference Shield (Must be connected to GND.)	
Asynchronous Memory Interface			
A1-3	O	Address Bus for Async and ATAPI Addresses	A
D0-15/ND_D0-15/ATAPI_D0-15	I/O	Data Bus for Async, NAND and ATAPI Accesses	A
$\overline{\text{AMS0–3}}$	O	Bank Selects (Pull high with a resistor when used as chip select. Require pull-ups if hibernate is used.)	A
$\overline{\text{ABE0}}$ / *ND_CLE*	O	Byte Enables: Data Masks for Asynchronous Access / *NAND Command Latch Enable*	A
$\overline{\text{ABE1}}$ / *ND_ALE*	O	Byte Enables: Data Masks for Asynchronous Access / *NAND Address Latch Enable*	A
$\overline{\text{AOE}}$ / *NR_ADV*	O	Output Enable / *NOR Address Data Valid*	A
$\overline{\text{ARE}}$	O	Read Enable / *NOR Output Enable*	A
$\overline{\text{AWE}}$	O	Write Enable	A
ATAPI Controller Pins			
$\overline{\text{ATAPI\_PDIAG}}$	I	Determines if an 80-pin cable is connected to the host. (Pull high or low when unused.)	
High Speed USB OTG Pins			
USB_DP	I/O	USB D+ Pin (Pull low when unused.)	
USB_DM	I/O	USB D– Pin (Pull low when unused.)	
USB_XI	C	Clock XTAL Input (Pull high or low when unused.)	
USB_XO	C	Clock XTAL Output (Leave unconnected when unused.)	
USB_ID[10]	I	USB OTG ID Pin (Pull high when unused.)	

[13]See the *ADSP-BF54x Blackfin Processor Hardware Reference Manual* for definition of sleep, deep sleep, and hibernate operating modes.
[14]Includes current on V_{DDEXT}, V_{DDUSB}, V_{DDVR}, and V_{DDDR} supplies. Clock inputs are tied high or low.
[15]Guaranteed maximum specifications.
[16]Unit for V_{DDINT} is V (volts). Unit for f_{SCLK} is MHz. Example: 1.2 V, 133 MHz would be 0.77 × 1.2 × 133 = 122.9 mA added to $I_{DDDEEPSLEEP}$.
[17]See Table 18 for the list of I_{DDINT} power vectors covered.

Total power dissipation has two components:

- Static, including leakage current
- Dynamic, due to transistor switching characteristics

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. Electrical Characteristics on Page 36 shows the current dissipation for internal circuitry (V_{DDINT}). $I_{DDDEEPSLEEP}$ specifies static power dissipation as a function of voltage (V_{DDINT}) and temperature (see Table 16 and Table 17), and I_{DDINT} specifies the total power specification for the listed test conditions, including the dynamic component as a function of voltage (V_{DDINT}) and frequency (Table 19).

There are two parts to the dynamic component. The first part is due to transistor switching in the core clock (CCLK) domain. This part is subject to an activity scaling factor (ASF) which represents application code running on the processor core and L1/L2 memories (Table 18). The ASF is combined with the CCLK frequency and V_{DDINT} dependent data in Table 19 to calculate this part. The second part is due to transistor switching in the system clock (SCLK) domain, which is included in the I_{DDINT} specification equation.

Table 16. Static Current—Low Power Process (mA)[1]

	Voltage (V_{DDINT})[2]												
T_J (°C)[2]	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.38 V	1.40 V	1.43 V
–40	11.9	13.5	15.5	17.7	20.3	23.3	26.8	30.6	35.0	39.9	43.2	45.5	49.5
0	20.1	22.3	24.7	27.8	31.1	34.9	39.3	44.2	49.6	55.7	59.8	62.5	67.2
25	31.2	34.2	37.5	41.3	45.6	50.3	55.7	61.7	68.2	75.4	80.3	83.6	88.6
45	47.0	51.0	55.5	60.6	66.0	72.0	78.8	86.1	94.2	102.9	108.9	112.8	118.2
55	58.6	63.1	68.3	74.1	80.3	87.1	94.9	103.0	112.0	122.0	128.4	132.8	140.0
70	80.7	86.6	93.0	100.2	108.1	116.7	125.9	136.0	146.8	158.7	166.4	171.6	179.5
85	107.0	114.3	122.5	131.5	141.2	151.7	163.1	175.3	188.5	202.7	211.8	218.0	226.7
100	153.9	163.0	173.3	184.8	197.0	210.0	224.1	239.0	255.1	272.4	283.4	290.8	300.6
105	171.7	181.5	192.7	205.1	218.3	232.4	247.5	263.6	280.9	299.3	308.7	314.9	325.7
115	210.1	221.4	234.2	248.6	263.7	279.9	297.3	311.0	331.1	352.5	366.3	N/A	N/A
125	257.9	270.9	285.9	302.5	314.6	334.0	354.3	375.7	399.2	423.8	439.6	N/A	N/A

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ for 400 MHz speed-grade devices.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 34.

Table 17. Static Current—Automotive 400 MHz and All 533 MHz/600 MHz Speed Grade Devices (mA)[1]

	Voltage (V_{DDINT})[2]												
T_J (°C)[2]	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.38 V	1.40 V	1.43 V
–40	19.7	22.1	24.8	27.9	31.4	35.4	39.9	45.0	50.6	57.0	61.2	64.0	70.4
0	45.2	49.9	55.2	61.3	67.9	75.3	83.5	92.6	102.6	113.6	121.0	125.8	135.0
25	80.0	87.5	96.2	105.8	116.4	127.9	140.4	154.1	169.2	185.4	196.1	203.3	218.0
45	124.2	134.8	147.1	160.7	175.3	191.2	208.6	227.3	247.6	269.6	284.0	293.6	312.0
55	154.6	167.2	181.7	197.7	214.9	233.8	254.2	276.1	299.7	325.9	343.1	354.6	374.0
70	209.8	225.6	243.9	264.1	285.8	309.4	334.8	363.5	394.3	427.7	449.4	463.9	489.0
85	281.8	301.3	323.5	350.2	378.5	408.9	442.1	477.9	516.5	557.5	584.2	602.0	629.0
100	366.5	390.5	419.4	452.1	486.9	524.4	564.8	608.2	654.8	704.7	737.0	758.5	793.0
105	403.8	428.3	459.5	494.3	531.7	571.9	614.9	661.5	711.1	763.9	798.5	821.6	864.0

[1] Values are guaranteed maximum $I_{DDDEEPSLEEP}$ for automotive 400 MHz and all 533 MHz and 600 MHz speed grade devices.
[2] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 34.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 20 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Table 21 details the maximum duty cycle for input transient voltage.

Table 20. Absolute Maximum Ratings

Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.43 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +3.8 V
Input Voltage[1, 2, 3]	–0.5 V to +3.6 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
I_{OH}/I_{OL} Current per Single Pin[4]	40 mA (max)
I_{OH}/I_{OL} Current per Pin Group[4]	80 mA (max)
Storage Temperature Range	–65°C to +150°C
Junction Temperature Underbias	+125°C

[1] Applies to all bidirectional and input only pins except PB1-0, PE15-14, PG15–11, and PH7-6, where the absolute maximum input voltage range is –0.5 V to +5.5 V.

[2] Pins USB_DP, USB_DM, and USB_VBUS are 5 V-tolerant when VDDUSB is powered according to the operating conditions table. If VDDUSB supply voltage does not meet the specification in the operating conditions table, these pins could suffer long-term damage when driven to +5 V. If this condition is seen in the application, it can be corrected with additional circuitry to use the external host to power only the V_{DDUSB} pins. Contact factory for application detail and reliability information.

[3] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2 V.

[4] For more information, see description preceding Table 22.

Table 21. Maximum Duty Cycle for Input[1] Transient Voltage

V_{IN} Max (V)[2]	V_{IN} Min (V)	Maximum Duty Cycle
3.63	–0.33	100%
3.80	–0.50	48%
3.90	–0.60	30%
4.00	–0.70	20%
4.10	–0.80	10%
4.20	–0.90	8%
4.30	–1.00	5%

[1] Does not apply to CLKIN. Absolute maximum for pins PB1-0, PE15-14, PG15-11, and PH7-6 is +5.5V.

[2] Only one of the listed options can apply to a particular design.

The Absolute Maximum Ratings table specifies the maximum total source/sink (I_{OH}/I_{OL}) current for a group of pins. Permanent damage can occur if this value is exceeded. To understand this specification, if pins PA4, PA3, PA2, PA1 and PA0 from group 1 in the Total Current Pin Groups table were sourcing or sinking 2 mA each, the total current for those pins would be 10 mA. This would allow up to 70 mA total that could be sourced or sunk by the remaining pins in the group without damaging the device. For a list of all groups and their pins, see the Total Current Pin Groups table. Note that the V_{OL} and V_{OH} specifications have separate per-pin maximum current requirements, see the Electrical Characteristics table.

Table 22. Total Current Pin Groups

Group	Pins in Group
1	PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PA8, PA9, PA10, PA11
2	PA12, PA13, PA14, PA15, PB8, PB9, PB10, PB11, PB12, PB13, PB14
3	PB0, PB1, PB2, PB3, PB4, PB5, PB6, PB7, BMODE0, BMODE1, BMODE2, BMODE3
4	TCK, TDI, TDO, TMS, $\overline{\text{TRST}}$, PD14, $\overline{\text{EMU}}$
5	PD8, PD9, PD10, PD11, PD12, PD13, PD15
6	PD0, PD1, PD2, PD3, PD4, PD5, PD6, PD7
7	PE11, PE12, PE13, PF12, PF13, PF14, PF15, PG3, PG4
8	PF4, PF5, PF6, PF7, PF8, PF9, PF10, PF11
9	PF0, PF1, PF2, PF3, PG0, PG1, PG2
10	PC0, PC1, PC2, PC3, PC4, PC5, PC6, PC7
11	PH5, PH6, PH7
12	A1, A2, A3
13	PH8, PH9, PH10, PH11, PH12, PH13
14	PI0, PI1, PI2, PI3, PI4, PI5, PI6, PI7
15	PI8, PI9, PI10, PI11, PI12, PI13, PI14, PI15
16	$\overline{\text{AMS0}}$, $\overline{\text{AMS1}}$, $\overline{\text{AMS2}}$, $\overline{\text{AMS3}}$, $\overline{\text{AOE}}$, CLKBUF, $\overline{\text{NMI}}$
17	CLKIN, XTAL, $\overline{\text{RESET}}$, RTXI, RTXO, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$
18	D0, D1, D2, D3, D4, D5, D6, D7
19	D8, D9, D10, D11, D12
20	D13, D14, D15, $\overline{\text{ABE0}}$, $\overline{\text{ABE1}}$
21	EXT_WAKE, CLKOUT, PJ11, PJ12, PJ13
22	PJ0, PJ1, PJ2, PJ3, PJ4, PJ5, PJ6, PJ7, $\overline{\text{ATAPI\_PDIAG}}$
23	PJ8, PJ9, PJ10, PE7, PG12, PG13
24	PE0, PE1, PE2, PE4, PE5, PE6, PE8, PE9, PE10, PH3, PH4
25	PH0, PH2, PE14, PE15, PG5, PG6, PG7, PG8, PG9, PG10, PG11
26	PC8, PC9, PC10, PC11, PC12, PC13, PE3, PG14, PG15, PH1

Asynchronous Memory Write Cycle Timing

Table 29 and Table 30 on Page 47 and Figure 15 and Figure 16 on Page 47 describe asynchronous memory write cycle operations for synchronous and for asynchronous ARDY.

Table 29. Asynchronous Memory Write Cycle Timing with Synchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{SARDY}	ARDY Setup Before the Falling Edge of CLKOUT	5.0		ns
t_{HARDY}	ARDY Hold After the Falling Edge of CLKOUT	0.0		ns
Switching Characteristics				
t_{DDAT}	DATA15–0 Disable After CLKOUT		6.0	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT	0.0		ns
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT[1]	0.3		ns

[1] Output pins include $\overline{AMS3–0}$, $\overline{ABE1–0}$, ADDR19–1, and $\overline{AWE}$.

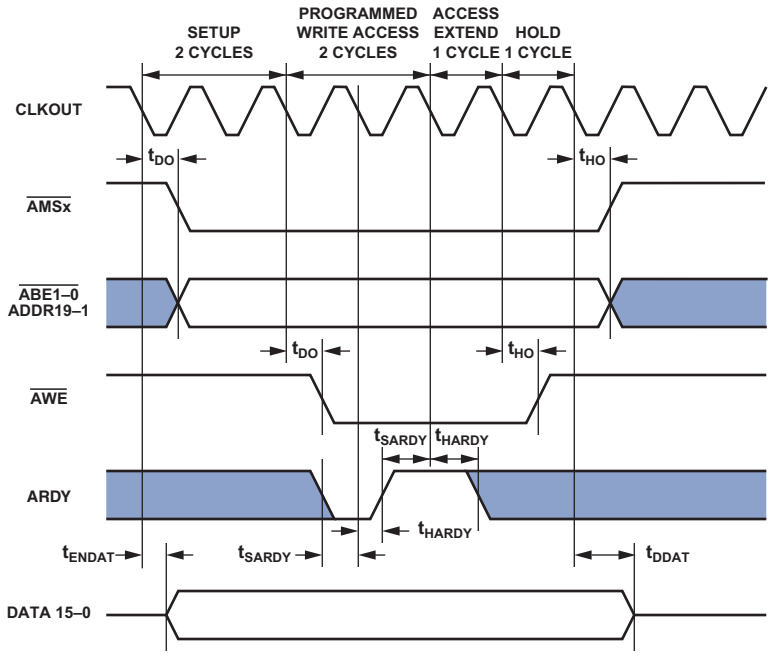

Figure 15. Asynchronous Memory Write Cycle Timing with Synchronous ARDY

Table 35. External Port Bus Request and Grant Cycle Timing with Asynchronous $\overline{BR}$

Parameter		Min	Max	Unit
Timing Requirement				
t_{WBR}	$\overline{BR}$ Pulsewidth	$2 \times t_{SCLK}$		ns
Switching Characteristics				
t_{SD}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}/\overline{AWE}$ Disable		5.0	ns
t_{SE}	CLKOUT Low to $\overline{AMSx}$, Address, and $\overline{ARE}/\overline{AWE}$ Enable		5.0	ns
t_{DBG}	CLKOUT Low to $\overline{BG}$ Asserted Output Delay		4.0	ns
t_{EBG}	CLKOUT Low to $\overline{BG}$ Deasserted Output Hold		4.0	ns
t_{DBH}	CLKOUT Low to $\overline{BGH}$ Asserted Output Delay		3.6	ns
t_{EBH}	CLKOUT Low to $\overline{BGH}$ Deasserted Output Hold		3.6	ns

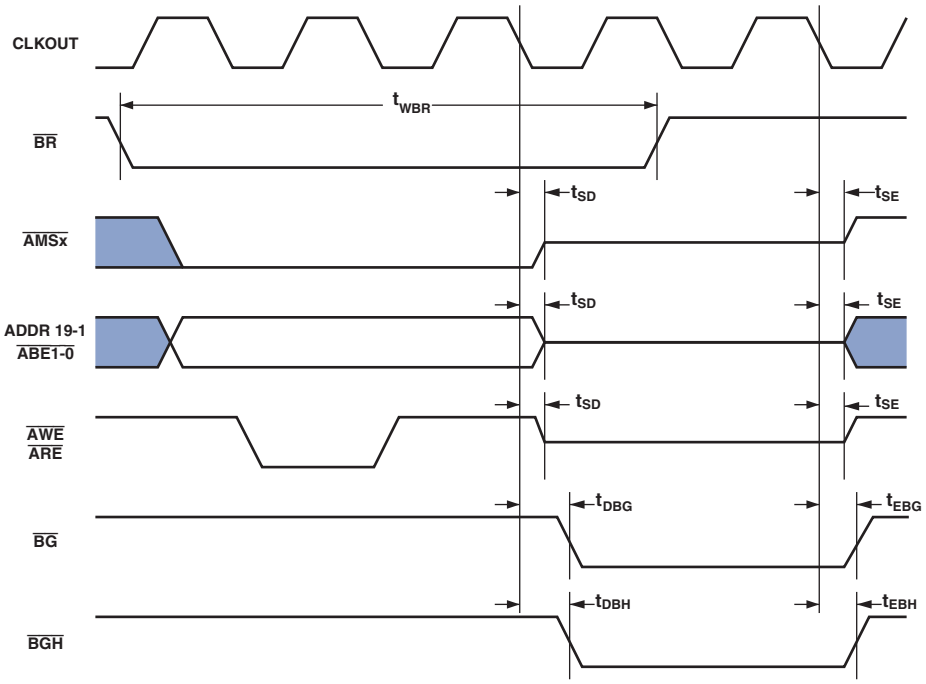

Figure 22. External Port Bus Request and Grant Cycle Timing with Asynchronous $\overline{BR}$

Enhanced Parallel Peripheral Interface Timing

Table 39 and Figure 32 on Page 60, Figure 30 on Page 59, Figure 33 on Page 60, and Figure 31 on Page 59 describe enhanced parallel peripheral interface timing operations.

Table 39. Enhanced Parallel Peripheral Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCLKW}	PPIx_CLK Width	6.0		ns
t_{PCLK}	PPIx_CLK Period	13.3		ns
Timing Requirements—GP Input and Frame Capture Modes				
t_{SFSPE}	External Frame Sync Setup Before PPIx_CLK	0.9		ns
t_{HFSPE}	External Frame Sync Hold After PPIx_CLK	1.9		ns
t_{SDRPE}	Receive Data Setup Before PPIx_CLK	1.6		ns
t_{HDRPE}	Receive Data Hold After PPIx_CLK	1.5		ns
Switching Characteristics—GP Output and Frame Capture Modes				
t_{DFSPE}	Internal Frame Sync Delay After PPIx_CLK		10.5	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPIx_CLK	2.4		ns
t_{DDTPE}	Transmit Data Delay After PPIx_CLK		9.9	ns
t_{HDTPE}	Transmit Data Hold After PPIx_CLK	2.4		ns

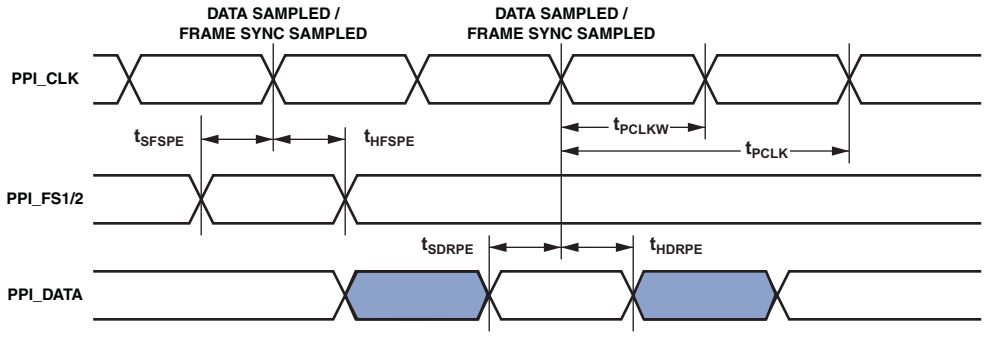

Figure 30. EPPI GP Rx Mode with External Frame Sync Timing

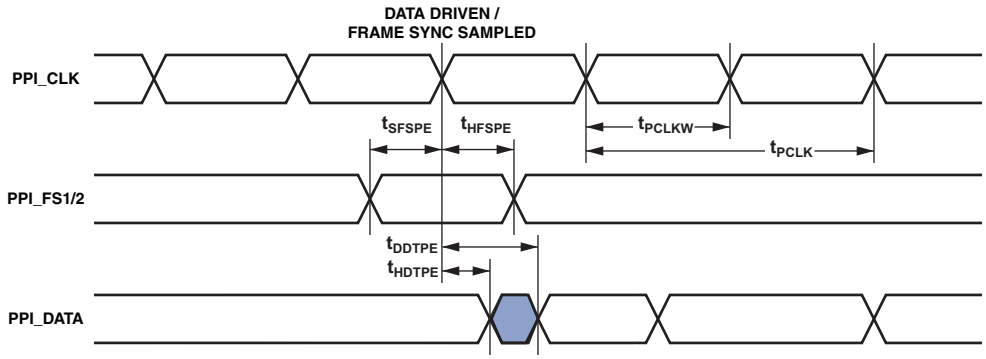

Figure 31. EPPI GP Tx Mode with External Frame Sync Timing

Up/Down Counter/Rotary Encoder Timing

Table 49 and Figure 43 describe up/down counter/rotary encoder timing.

Table 49. Up/Down Counter/Rotary Encoder Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{WCOUNT}	CUD/CDG/CZM Input Pulse Width	t_{SCLK} + 1		ns
t_{CIS}	CUD/CDG/CZM Input Setup Time Before CLKOUT High[1]	7.2		ns
t_{CIH}	CUD/CDG/CZM Input Hold Time After CLKOUT High[1]	0.0		ns

[1] Either a valid setup and hold time or a valid pulse width is sufficient. There is no need to resynchronize counter inputs.

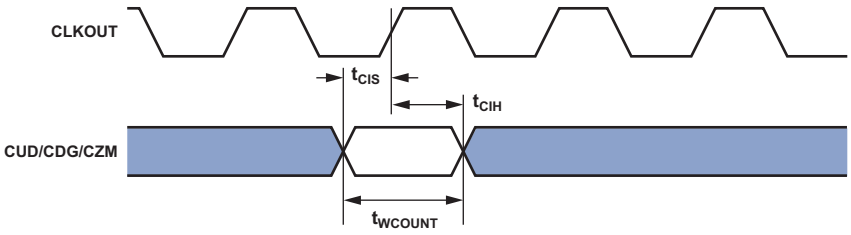

Figure 43. Up/Down Counter/Rotary Encoder Timing

Table 51. SD/SDIO Controller Timing (High Speed Mode)

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	SD_Dx and SD_CMD Input Setup Time	7.2		ns
t_{IH}	SD_Dx and SD_CMD Input Hold Time	2		ns
Switching Characteristics				
f_{PP}	SD_CLK Frequency During Data Transfer Mode[1]	0	40	MHz
t_{WL}	SD_CLK Low Time	9.5		ns
t_{WH}	SD_CLK High Time	9.5		ns
t_{TLH}	SD_CLK Rise Time		3	ns
t_{THL}	SD_CLK Fall Time		3	ns
t_{ODLY}	SD_Dx and SD_CMD Output Delay Time During Data Transfer Mode		2	ns
t_{OH}	SD_Dx and SD_CMD Output Hold Time	2.5		ns

[1] $t_{PP}=1/f_{PP}$.

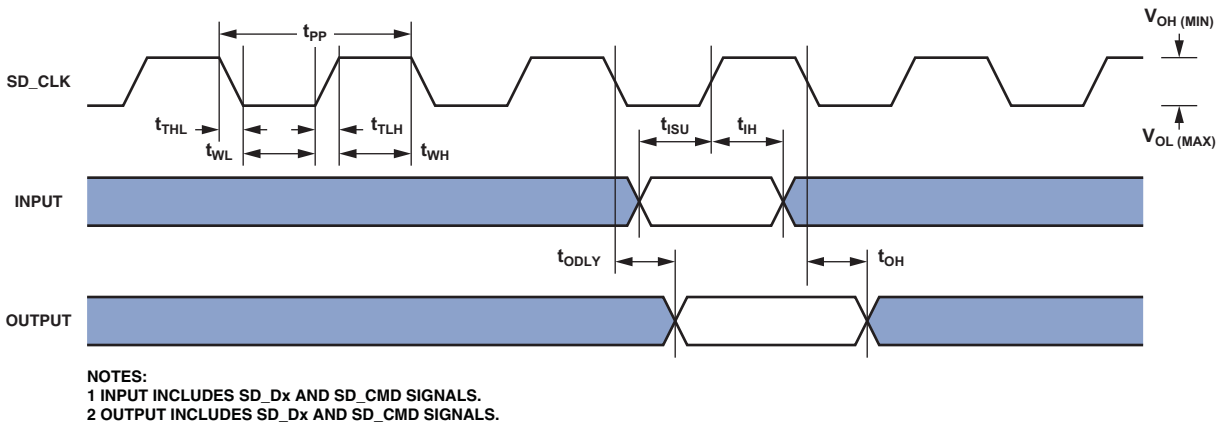

Figure 45. SD/SDIO Controller Timing (High Speed Mode)

ATAPI Multiword DMA Transfer Timing

Table 59 and Figure 49 through Figure 52 describe the ATAPI multiword DMA transfer timing. The material in these figures is adapted from ATAPI-6 (INCITS 361-2002[R2007] and is used with permission of the American National Standards Institute (ANSI) on behalf of the Information Technology Industry Council ("ITIC"). Copies of ATAPI-6 (INCITS 361-2002 [R2007] can be purchased from ANSI.

Table 59. ATAPI Multiword DMA Transfer Timing

ATAPI Parameter/Description		ATAPI_MULTI_TIM_x Timing Register Setting[1]	Timing Equation
t_0	Cycle time	TD, TK	$(TD + TK) \times t_{SCLK}$
t_D	$\overline{ATAPI\_DIOR}$/$\overline{ATAPI\_DIOW}$ asserted Pulse Width	TD	$TD \times t_{SCLK}$
t_F	$\overline{ATAPI\_DIOR}$ data hold	N/A	0
$t_{G(write)}$	$\overline{ATAPI\_DIOW}$ data setup	TD	$TD \times t_{SCLK} - (t_{SK1} + t_{SK2} + t_{SK4})$
$t_{G(read)}$	$\overline{ATAPI\_DIOR}$ data setup	TD	$t_{OD} + t_{SUD} + 2 \times t_{BD} + t_{CDD} + t_{CDC}$
t_H	$\overline{ATAPI\_DIOW}$ data hold	TK	$TK \times t_{SCLK} - (t_{SK1} + t_{SK2} + t_{SK4})$
t_I	$\overline{ATAPI\_DMACK}$ to $\overline{ATAPI\_DIOR}$/$\overline{ATAPI\_DIOW}$ setup	TM	$TM \times t_{SCLK} - (t_{SK1} + t_{SK2} + t_{SK4})$
t_J	$\overline{ATAPI\_DIOR}$/$\overline{ATAPI\_DIOW}$ to $\overline{ATAPI\_DMACK}$ hold	TK, TEOC_MDMA	$(TK + TEOC\_MDMA) \times t_{SCLK} - (t_{SK1} + t_{SK2} + t_{SK4})$
t_{KR}	$\overline{ATAPI\_DIOR}$ negated pulse width	TKR	$TKR \times t_{SCLK}$
t_{KW}	$\overline{ATAPI\_DIOW}$ negated pulse width	TKW	$TKW \times t_{SCLK}$
t_{LR}	$\overline{ATAPI\_DIOR}$ to $\overline{ATAPI\_DMARQ}$ delay	N/A	$(TD + TK) \times t_{SCLK} - (t_{OD} + 2 \times t_{BD} + 2 \times t_{CDC})$
t_M	$\overline{ATAPI\_CS0\text{-}1}$ valid to $\overline{ATAPI\_DIOR}$/$\overline{ATAPI\_DIOW}$	TM	$TM \times t_{SCLK} - (t_{SK1} + t_{SK2} + t_{SK4})$
t_N	$\overline{ATAPI\_CS0\text{-}1}$ hold	TK, TEOC_MDMA	$(TK + TEOC\_MDMA) \times t_{SCLK} - (t_{SK1} + t_{SK2} + t_{SK4})$

[1] ATAPI timing register setting should be programmed with a value that guarantees parameter compliance with the ATA ANSI specification for an ATA device mode of operation.

ATAPI Ultra DMA Data-In Transfer Timing

Table 60 and Figure 53 through Figure 56 describe the ATAPI ultra DMA data-in data transfer timing. The material in these figures is adapted from ATAPI-6 (INCITS 361-2002[R2007] and is used with permission of the American National Standards Institute (ANSI) on behalf of the Information Technology Industry Council ("ITIC"). Copies of ATAPI-6 (INCITS 361-2002[R2007] can be purchased from ANSI.

Table 60. ATAPI Ultra DMA Data-In Transfer Timing

ATAPI Parameter		ATAPI_ULTRA_TIM_x Timing Register Setting[1]	Timing Equation
t_{DS}	Data setup time at host	N/A	$T_{SK3} + t_{SUDU}$
t_{DH}	Data hold time at host	N/A	$T_{SK3} + t_{HDU}$
t_{CVS}	CRC word valid setup time at host	TDVS	$TDVS \times t_{SCLK} - (t_{SK1} + t_{SK2})$
t_{CVH}	CRC word valid hold time at host	TACK	$TACK \times t_{SCLK} - (t_{SK1} + t_{SK2})$
t_{LI}	Limited interlock time	N/A	$2 \times t_{BD} + 2 \times t_{SCLK} + t_{OD}$
t_{MLI}	Interlock time with minimum	TZAH, TCVS	$(TZAH + TCVS) \times t_{SCLK} - (4 \times t_{BD} + 4 \times t_{SCLK} + 2 \times t_{OD})$
t_{AZ}	Maximum time allowed for output drivers to release	N/A	0
t_{ZAH}	Minimum delay time required for output	TZAH	$2 \times t_{SCLK} + TZAH \times t_{SCLK} + t_{SCLK}$
t_{ENV}[2]	$\overline{ATAPI\_DMACK}$ to $\overline{ATAPI\_DIOR}/\overline{DIOW}$	TENV	$(TENV \times t_{SCLK}) +/- (t_{SK1} + t_{SK2})$
t_{RP}	$\overline{ATAPI\_DMACK}$ to $\overline{ATAPI\_DIOR}/\overline{DIOW}$	TRP	$TRP \times t_{SCLK} - (t_{SK1} + t_{SK2} + t_{SK4})$
t_{ACK}	Setup and hold times for $\overline{ATAPI\_DMACK}$	TACK	$TACK \times t_{SCLK} - (t_{SK1} + t_{SK2})$

[1] ATAPI Timing Register Setting should be programmed with a value that guarantees parameter compliance with the ATA ANSI specification for ATA device mode of operation.
[2] This timing equation can be used to calculate both the minimum and maximum t_{ENV}.

OUTPUT DRIVE CURRENTS

Figure 62 through Figure 71 show typical current-voltage characteristics for the output drivers of the ADSP-BF54x Blackfin processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

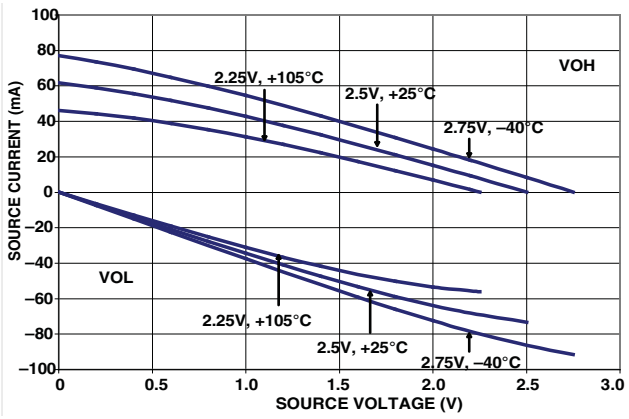

Figure 62. Drive Current A (Low V_{DDEXT})

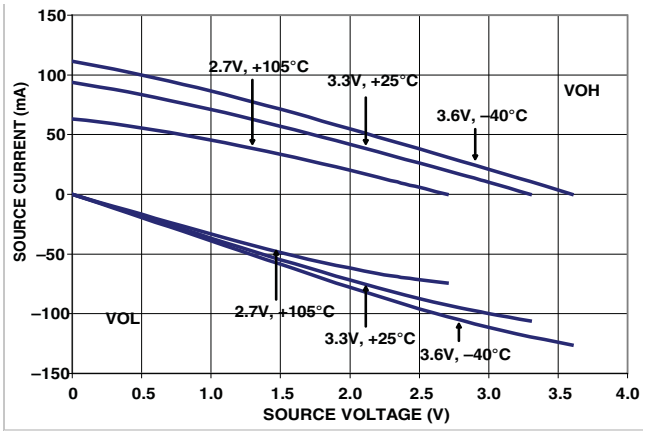

Figure 63. Drive Current A (High V_{DDEXT})

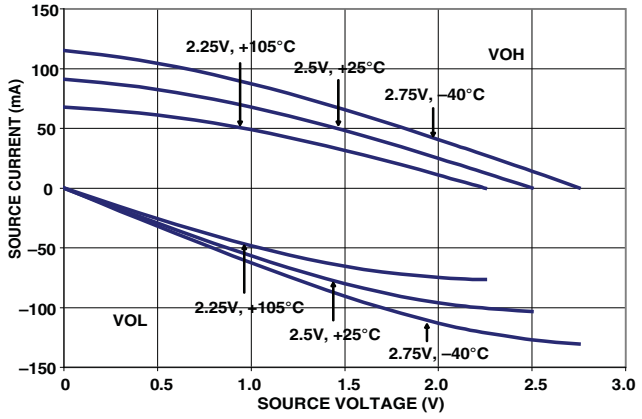

Figure 64. Drive Current B (Low V_{DDEXT})

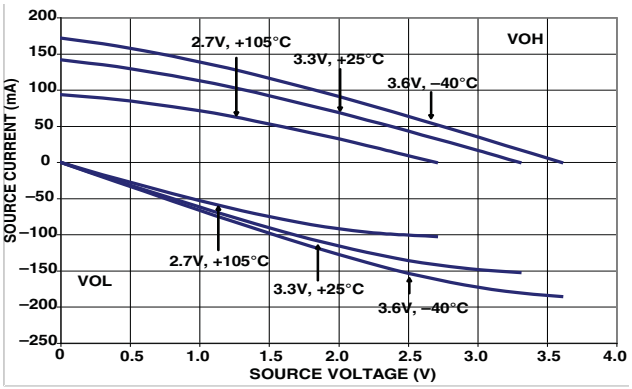

Figure 65. Drive Current B (High V_{DDEXT})

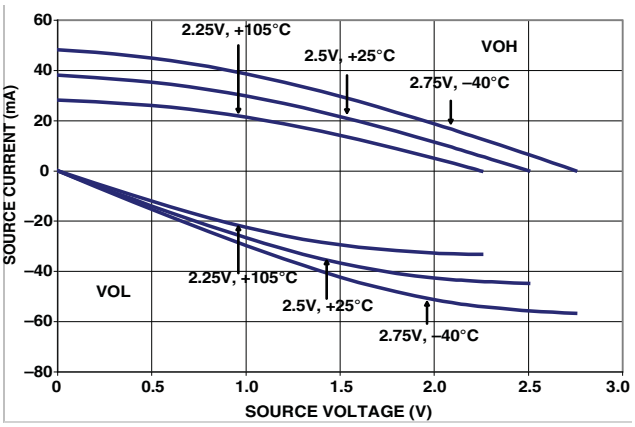

Figure 66. Drive Current C (Low V_{DDEXT})

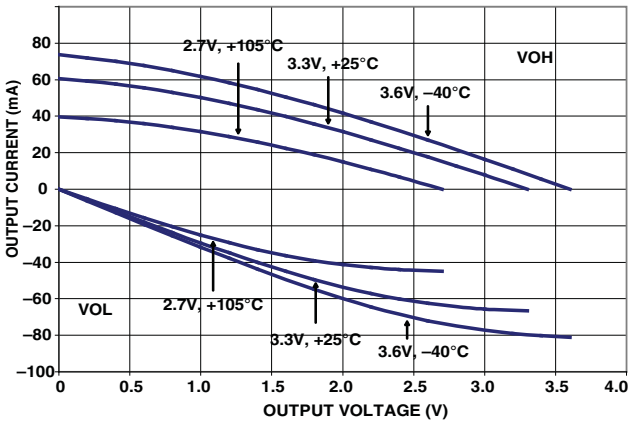

Figure 67. Drive Current C (High V_{DDEXT})

Table 65. 400-Ball CSP_BGA Ball Assignment (Alphabetical by Signal) (Continued)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
TCK	V3	V_{DDDDR}	J14	V_{DDEXT}	N5	V_{DDINT}	G13
TDI	V5	V_{DDDDR}	J15	V_{DDEXT}	N15	V_{DDINT}	J6
TDO	V4	V_{DDDDR}	K14	V_{DDEXT}	P15	V_{DDINT}	J13
TMS	U5	V_{DDDDR}	K15	V_{DDEXT}	R6	V_{DDINT}	L6
$\overline{TRST}$	T5	V_{DDEXT}	E5	V_{DDEXT}	R7	V_{DDINT}	L15
USB_DM	E2	V_{DDEXT}	E9	V_{DDEXT}	R8	V_{DDINT}	P6
USB_DP	E1	V_{DDEXT}	E10	V_{DDEXT}	R15	V_{DDINT}	P7
USB_ID	G3	V_{DDEXT}	E11	V_{DDEXT}	T7	V_{DDINT}	P14
USB_RSET	D3	V_{DDEXT}	E12	V_{DDEXT}	T8	V_{DDINT}	R10
USB_VBUS	D2	V_{DDEXT}	F7	V_{DDEXT}	T9	V_{DDINT}	R11
USB_VREF	B1	V_{DDEXT}	F8	V_{DDEXT}	T10	V_{DDINT}	R12
USB_XI	F1	V_{DDEXT}	F13	V_{DDEXT}	T11	V_{DDINT}	U9
USB_XO	F2	V_{DDEXT}	G5	V_{DDEXT}	T12	V_{DDMP}	E8
V_{DDDDR}	F10	V_{DDEXT}	G6	V_{DDEXT}	T13	V_{DDRTC}	E13
V_{DDDDR}	F11	V_{DDEXT}	G7	V_{DDEXT}	T14	V_{DDUSB}	F5
V_{DDDDR}	F12	V_{DDEXT}	G14	V_{DDEXT}	T15	V_{DDUSB}	G4
V_{DDDDR}	G15	V_{DDEXT}	H5	V_{DDEXT}	T16	V_{DDVR}	F15
V_{DDDDR}	H13	V_{DDEXT}	H6	V_{DDINT}	F9	VR_{OUT0}	A18
V_{DDDDR}	H14	V_{DDEXT}	K6	V_{DDINT}	G8	VR_{OUT1}	A19
V_{DDDDR}	H15	V_{DDEXT}	M15	V_{DDINT}	G12	XTAL	A12

Table 66. 400-Ball CSP_BGA Ball Assignment (Numerical by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
J1	PF1	L1	PF5	N1	PF14	R1	PD2
J2	PC2	L2	PF4	N2	PF15	R2	PD3
J3	PC1	L3	PF8	N3	PG3	R3	PD5
J4	PG0	L4	PF6	N4	PF13	R4	PD7
J5	PC6	L5	PG2	N5	V_{DDEXT}	R5	$\overline{EMU}$
J6	V_{DDINT}	L6	V_{DDINT}	N6	GND	R6	V_{DDEXT}
J7	GND	L7	GND	N7	GND	R7	V_{DDEXT}
J8	GND	L8	GND	N8	GND	R8	V_{DDEXT}
J9	GND	L9	GND	N9	GND	R9	GND
J10	GND	L10	GND	N10	GND	R10	V_{DDINT}
J11	GND	L11	GND	N11	GND	R11	V_{DDINT}
J12	GND	L12	GND	N12	GND	R12	V_{DDINT}
J13	V_{DDINT}	L13	GND	N13	GND	R13	GND
J14	V_{DDDDR}	L14	GND	N14	GND	R14	GND
J15	V_{DDDDR}	L15	V_{DDINT}	N15	V_{DDEXT}	R15	V_{DDEXT}
J16	DQ15	L16	CLKOUT	N16	PJ7	R16	GND
J17	DQ14	L17	DQ4	N17	PJ4	R17	PE7
J18	DQ13	L18	DQ0	N18	PJ1	R18	PG13
J19	DQ12	L19	DQ2	N19	PJ13	R19	PJ8
J20	DQ9	L20	DQ3	N20	DDR_VSSR	R20	PJ0
K1	PF3	M1	PF9	P1	PG4	T1	PD4
K2	PF2	M2	PF10	P2	PE11	T2	PD6
K3	PF0	M3	PF11	P3	PD0	T3	PD10
K4	PF7	M4	PF12	P4	PD1	T4	PD12
K5	PG1	M5	PE12	P5	PE13	T5	$\overline{TRST}$
K6	V_{DDEXT}	M6	GND	P6	V_{DDINT}	T6	PB2
K7	GND	M7	GND	P7	V_{DDINT}	T7	V_{DDEXT}
K8	GND	M8	GND	P8	GND	T8	V_{DDEXT}
K9	GND	M9	GND	P9	GND	T9	V_{DDEXT}
K10	GND	M10	GND	P10	GND	T10	V_{DDEXT}
K11	GND	M11	GND	P11	GND	T11	V_{DDEXT}
K12	GND	M12	GND	P12	GND	T12	V_{DDEXT}
K13	GND	M13	GND	P13	GND	T13	V_{DDEXT}
K14	V_{DDDDR}	M14	GND	P14	V_{DDINT}	T14	V_{DDEXT}
K15	V_{DDDDR}	M15	V_{DDEXT}	P15	V_{DDEXT}	T15	V_{DDEXT}
K16	DQ5	M16	PJ2	P16	PG12	T16	V_{DDEXT}
K17	DQ7	M17	PJ11	P17	PJ9	T17	PE1
K18	DQ10	M18	EXT_WAKE	P18	PJ6	T18	PE10
K19	DQ8	M19	DQ1	P19	$\overline{ATAPI\_PDIAG}$	T19	PJ10
K20	DQ6	M20	DDR_VREF	P20	PJ12	T20	PJ3

Table 66. 400-Ball CSP_BGA Ball Assignment (Numerical by Ball Number) (Continued)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
U1	PD8	V1	PD11	W1	BMODE0	Y1	GND
U2	PD9	V2	PD13	W2	BMODE1	Y2	PB1
U3	PD15	V3	TCK	W3	BMODE2	Y3	PB5
U4	PD14	V4	TDO	W4	BMODE3	Y4	PB4
U5	TMS	V5	TDI	W5	PB0	Y5	PB14
U6	PB3	V6	GND	W6	PB6	Y6	PB12
U7	PB10	V7	PB7	W7	PB11	Y7	PA14
U8	GND	V8	PB9	W8	PB8	Y8	PA12
U9	V_{DDINT}	V9	PB13	W9	PA15	Y9	PA10
U10	PA8	V10	PA11	W10	PA13	Y10	PA9
U11	PA7	V11	PA5	W11	PA4	Y11	PA6
U12	PA0	V12	PA1	W12	PA2	Y12	PA3
U13	PC10	V13	PC9	W13	PG15	Y13	PG14
U14	PH1	V14	PE3	W14	PC11	Y14	PC8
U15	PG11	V15	PG5	W15	PC13	Y15	PC12
U16	PE14	V16	PG8	W16	PG7	Y16	PE4
U17	PH4	V17	PH2	W17	PE15	Y17	PG6
U18	PE2	V18	PH3	W18	PH0	Y18	PG10
U19	PE9	V19	PE0	W19	PE6	Y19	PG9
U20	PJ5	V20	PE8	W20	PE5	Y20	GND

Figure 87 shows the top view of the BGA ball configuration.

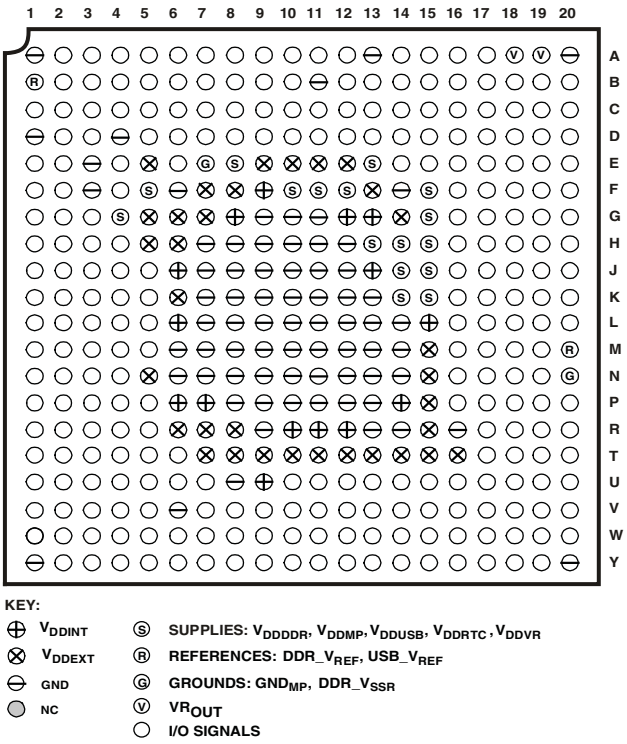

Figure 87. 400-Ball CSP_BGA Configuration (Top View)