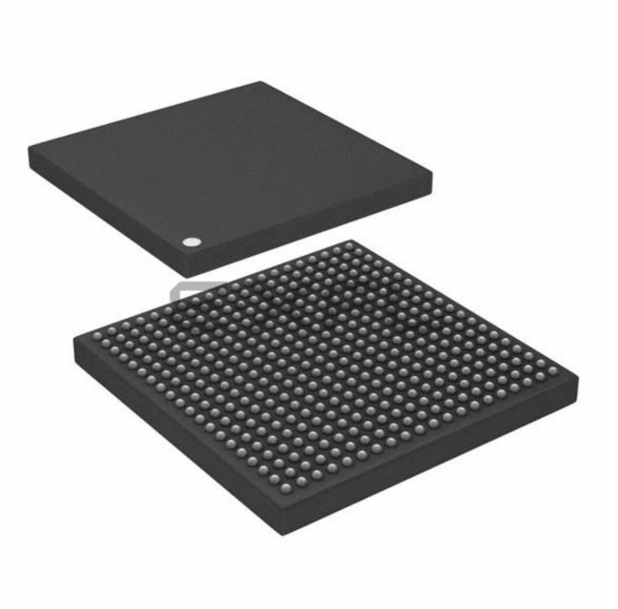
Analog Devices Inc. - ADSP-BF547MBBCZ-5M Datasheet



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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	SPI, SSP, TWI, UART, USB
Clock Rate	533MHz
Non-Volatile Memory	External
On-Chip RAM	260kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf547mbbcz-5m

The timer units can be used in conjunction with the four UARTs and the CAN controllers to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels.

The timers can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to a count of external signals.

In addition to the general-purpose programmable timers, another timer is also provided by the processor core. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generation of periodic operating system interrupts.

UP/DOWN COUNTER AND THUMBWHEEL INTERFACE

A 32-bit up/down counter is provided that can sense the 2-bit quadrature or binary codes typically emitted by industrial drives or manual thumb wheels. The counter can also operate in general-purpose up/down count modes. Then count direction is either controlled by a level-sensitive input pin or by two edge detectors.

A third input can provide flexible zero marker support and can alternatively be used to input the push-button signal of thumb wheels. All three pins have a programmable debouncing circuit.

An internal signal forwarded to the timer unit enables one timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmable count values are exceeded.

SERIAL PORTS (SPORTS)

The ADSP-BF54x Blackfin processors incorporate up to four dual-channel synchronous serial ports (SPORT0, SPORT1, SPORT2, and SPORT3) for serial and multiprocessor communications. The SPORTs support the following features:

- I^2S capable operation.
- Bidirectional operation. Each SPORT has two sets of independent transmit and receive pins, enabling up to eight channels of I^2S stereo audio.
- Buffered (8-deep) transmit and receive ports. Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking. Each transmit and receive port can either use an external serial clock or generate its own, in frequencies ranging from (f_{SCLK}/131,070) Hz to (f_{SCLK}/2) Hz.
- Word length. Each SPORT supports serial data words from 3 to 32 bits in length, transferred most-significant-bit first or least-significant-bit first.
- Framing. Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Companding in hardware. Each SPORT can perform A-law or μ-law companding according to ITU recommendation G.711. Companding can be selected on the transmit and/or receive channel of the SPORT without additional latencies.
- DMA operations with single-cycle overhead. Each SPORT can receive and transmit multiple buffers of memory data automatically. The processor can link or chain sequences of DMA transfers between a SPORT and memory.
- Interrupts. Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer or buffers through DMA.
- Multichannel capability. Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

SERIAL PERIPHERAL INTERFACE (SPI) PORTS

The ADSP-BF54x Blackfin processors have up to three SPI-compatible ports that allow the processor to communicate with multiple SPI-compatible devices.

Each SPI port uses three pins for transferring data: two data pins (master output slave input, SPIxMOSI, and master input-slave output, SPIxMISO) and a clock pin (serial clock, SPIxSCK). An SPI chip select input pin ($\overline{\text{SPIxSS}}$) lets other SPI devices select the processor, and three SPI chip select output pins per SPI port $\overline{\text{SPIxSELy}}$ let the processor select other SPI devices. The SPI select pins are reconfigured general-purpose I/O pins. Using these pins, the SPI ports provide a full-duplex, synchronous serial interface, which supports both master/slave modes and multimaster environments.

The SPI port's baud rate and clock phase/polarities are programmable, and it has an integrated DMA controller, configurable to support transmit or receive data streams. The SPI's DMA controller can only service unidirectional accesses at any given time.

The SPI port's clock rate is calculated as

$$SPI\ Clock\ Rate = \frac{f_{SCLK}}{2 \times SPI\_BAUD}$$

Where the 16-bit SPI_BAUD register contains a value of 2 to 65,535.

During transfers, the SPI port transmits and receives simultaneously by serially shifting data in and out on its two serial data lines. The serial clock line synchronizes the shifting and sampling of data on the two serial data lines.

UART PORTS (UARTS)

The ADSP-BF54x Blackfin processors provide up to four full-duplex universal asynchronous receiver/transmitter (UART) ports. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. A UART port

Sleep Operating Mode—High Dynamic Power Savings

The sleep mode reduces dynamic power dissipation by disabling the clock to the processor core (CCLK). The PLL and system clock (SCLK), however, continue to operate in this mode. Typically an external event or RTC activity will wake up the processor. In the sleep mode, assertion of a wakeup event enabled in the SIC_IWRx register causes the processor to sense the value of the BYPASS bit in the PLL control register (PLL_CTL). If BYPASS is disabled, the processor transitions to the full on mode. If BYPASS is enabled, the processor transitions to the active mode.

In the sleep mode, system DMA access to L1 memory is not supported.

Deep Sleep Operating Mode—Maximum Dynamic Power Savings

The deep sleep mode maximizes dynamic power savings by disabling the clocks to the processor core (CCLK) and to all synchronous peripherals (SCLK). Asynchronous peripherals, such as the RTC, may still be running but will not be able to access internal resources or external memory. This powered-down mode can only be exited by assertion of the reset interrupt ($\overline{\text{RESET}}$) or by an asynchronous interrupt generated by the RTC. In deep sleep mode, an asynchronous RTC interrupt causes the processor to transition to the active mode. Assertion of $\overline{\text{RESET}}$ while in deep sleep mode causes the processor to transition to the full on mode.

Hibernate State—Maximum Static Power Savings

The hibernate state maximizes static power savings by disabling the voltage and clocks to the processor core (CCLK) and to all the synchronous peripherals (SCLK). The internal voltage regulator for the processor can be shut off by using the bfrom_SysControl() function in the on-chip ROM. This sets the internal power supply voltage (V_{DDINT}) to 0 V to provide the greatest power savings mode. Any critical information stored internally (memory contents, register contents, and so on) must be written to a non-volatile storage device prior to removing power if the processor state is to be preserved.

Since V_{DDEXT} is still supplied in this mode, all of the external pins three-state, unless otherwise specified. This allows other devices that may be connected to the processor to have power still applied without drawing unwanted current.

The internal supply regulator can be woken up by CAN, by the MXVR, by the keypad, by the up/down counter, by the USB, and by some GPIO pins. It can also be woken up by a real-time clock wakeup event or by asserting the $\overline{\text{RESET}}$ pin. Waking up from hibernate state initiates the hardware reset sequence.

With the exception of the VR_CTL and the RTC registers, all internal registers and memories lose their content in hibernate state. State variables may be held in external SRAM or DDR memory.

Power Domains

As shown in Table 5, the ADSP-BF54x Blackfin processors support different power domains. The use of multiple power domains maximizes flexibility while maintaining compliance with industry standards and conventions. By isolating the internal logic of the ADSP-BF54x Blackfin processors into its own power domain separate from the RTC and other I/O, the processors can take advantage of dynamic power management without affecting the RTC or other I/O devices. There are no sequencing requirements for the various power domains.

Table 5. Power Domains

Power Domain	VDD Range
All internal logic, except RTC, DDR, and USB	V_{DDINT}
RTC internal logic and crystal I/O	V_{DDRTC}
DDR external memory supply	V_{DDDDR}
USB internal logic and crystal I/O	V_{DDUSB}
Internal voltage regulator	V_{DDVR}
MXVR PLL and logic	V_{DDMP}
All other I/O	V_{DDEXT}

VOLTAGE REGULATION

The ADSP-BF54x Blackfin processors provide an on-chip voltage regulator that can generate processor core voltage levels from an external supply (see specifications in Operating Conditions on Page 34). Figure 6 on Page 17 shows the typical external components required to complete the power management system. The regulator controls the internal logic voltage levels and is programmable with the voltage regulator control register (VR_CTL) in increments of 50 mV. This register can be accessed using the bfrom_SysControl() function in the on-chip ROM. To reduce standby power consumption, the internal voltage regulator can be programmed to remove power to the processor core while keeping I/O power supplied. While in hibernate state, V_{DDEXT}, V_{DDRTC}, V_{DDDDR}, V_{DDUSB}, and V_{DDVR} can still be applied, eliminating the need for external buffers. The voltage regulator can be activated from this power-down state by assertion of the $\overline{\text{RESET}}$ pin, which then initiates a boot sequence. The regulator can also be disabled and bypassed at the user's discretion. For all 600 MHz speed grade models and all automotive grade models, the internal voltage regulator must not be used and V_{DDVR} must be tied to V_{DDEXT}. For additional information regarding design of the voltage regulator circuit, see *Switching Regulator Design Considerations for the ADSP-BF533 Blackfin Processors (EE-228)*.

Table 6. Example System Clock Ratios

Signal Name	Divider Ratio	Example Frequency Ratios (MHz)	
SSEL3–0	VCO/SCLK	VCO	SCLK
0010	2:1	200	100
0110	6:1	300	50
1010	10:1	500	50

Note that the divisor ratio must be chosen to limit the system clock frequency to its maximum of f_{SCLK}. The SSEL value can be dynamically changed without any PLL lock latencies by writing the appropriate values to the PLL divisor register (PLL_DIV) using the bfrom_SysControl() function in the on-chip ROM.

The core clock (CCLK) frequency can also be dynamically changed by means of the CSEL1–0 bits of the PLL_DIV register. Supported CCLK divider ratios are 1, 2, 4, and 8, as shown in Table 7. The default ratio is 1. This programmable core clock capability is useful for fast core frequency modifications.

The maximum CCLK frequency not only depends on the part's speed grade, it also depends on the applied V_{DDINT} voltage. See Table 12 on Page 35 for details.

Table 7. Core Clock Ratios

Signal Name	Divider Ratio	Example Frequency Ratios (MHz)	
CSEL1–0	VCO/CCLK	VCO	CCLK
00	1:1	300	300
01	2:1	300	150
10	4:1	500	125
11	8:1	200	25

BOOTING MODES

The ADSP-BF54x Blackfin processors have many mechanisms (listed in Table 8) for automatically loading internal and external memory after a reset. The boot mode is specified by four BMODE input pins dedicated to this purpose. There are two categories of boot modes: master and slave. In master boot modes, the processor actively loads data from parallel or serial memories. In slave boot modes, the processor receives data from an external host device.

Table 8. Booting Modes

BMODE3–0	Description
0000	Idle-no boot
0001	Boot from 8- or 16-bit external flash memory
0010	Boot from 16-bit asynchronous FIFO
0011	Boot from serial SPI memory (EEPROM or flash)
0100	Boot from SPI host device
0101	Boot from serial TWI memory (EEPROM or flash)
0110	Boot from TWI host
0111	Boot from UART host
1000	Reserved
1001	Reserved
1010	Boot from DDR SDRAM/Mobile DDR SDRAM
1011	Boot from OTP memory
1100	Reserved
1101	Boot from 8- or 16-bit NAND flash memory via NFC
1110	Boot from 16-bit host DMA
1111	Boot from 8-bit host DMA

The boot modes listed in Table 8 provide a number of mechanisms for automatically loading the processor's internal and external memories after a reset. By default, all boot modes use the slowest allowed configuration settings. Default settings can be altered via the initialization code feature at boot time or by proper OTP programming at pre-boot time. Some boot modes require a boot host wait (HWAIT) signal, which is a GPIO output signal that is driven and toggled by the boot kernel at boot time. If pulled high through an external pull-up resistor, the HWAIT signal behaves active high and will be driven low when the processor is ready for data. Conversely, when pulled low, HWAIT is driven high when the processor is ready for data. When the boot sequence completes, the HWAIT pin can be used for other purposes. By default, HWAIT functionality is on GPIO port B (PB11). However, if PB11 is otherwise utilized in the system, an alternate boot host wait (HWAITA) signal can be enabled on GPIO port H (PH7) by programming the OTP_ALTERNATE_HWAIT bit in the PBS00L OTP memory page.

The BMODE pins of the reset configuration register, sampled during power-on resets and software-initiated resets, implement the following modes:

- Idle-no boot mode (BMODE = 0x0)—In this mode, the processor goes into the idle state. The idle boot mode helps to recover from illegal operating modes, in case the OTP memory is misconfigured.
- Boot from 8- or 16-bit external flash memory—(BMODE = 0x1)—In this mode, the boot kernel loads the first block header from address 0x2000 0000 and, depending on instructions contained in the header, the boot kernel performs an 8- or 16-bit boot or starts program execution at the address provided by the header. By default, all configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).

  The ARDY pin is not enabled by default. It can, however, be enabled by OTP programming. Similarly, all interface behavior and timings can be customized through OTP programming. This includes activation of burst-mode or page-mode operation. In this mode, all asynchronous interface signals are enabled at the port muxing level.

For large page NAND flash devices, the 4-byte electronic signature is read in order to configure the kernel for booting. This allows support for multiple large page devices. The fourth byte of the electronic signature must comply with the specifications in Table 9.

Any configuration from Table 9 that also complies with the command set listed below is directly supported by the boot kernel. There are no restrictions on the page size or block size as imposed by the small-page boot kernel.

Table 9. Byte 4 Electronic Signature Specification

Page Size (excluding spare area)	D1:D0	00	1K bytes
		01	2K bytes
		10	4K bytes
		11	8K bytes
Spare Area Size	D2	0	8 bytes/512 bytes
		1	16 bytes/512 bytes
Block Size (excluding spare area)	D5:4	00	64K bytes
		01	128K bytes
		10	256K bytes
		11	512K bytes
Bus Width	D6	0	x8
		1	x16
Not Used for Configuration	D3, D7		

Large page devices must support the following command set:

Reset: 0xFF
Read Electronic Signature: 0x90
Read: 0x00, 0x30 (confirm command)

Large page devices must not support or react to NAND flash command 0x50. This is a small page NAND flash command used for device auto detection.

By default, the boot kernel will always issue five address cycles; therefore, if a large page device requires only four cycles, the device must be capable of ignoring the additional address cycle.

16-bit NAND flash memory devices must only support the issuing of command and address cycles via the lower eight bits of the data bus. Devices that use the full 16-bit bus for command and address cycles are not supported.

- Boot from OTP memory (BMODE = 0xB)—This provides a standalone booting method. The boot stream is loaded from on-chip OTP memory. By default, the boot stream is expected to start from OTP page 0x40 and can occupy all public OTP memory up to page 0xDF (2560 bytes). Since the start page is programmable, the maximum size of the boot stream can be extended to 3072 bytes.
- Boot from 16-bit host DMA (BMODE = 0xE)—In this mode, the host DMA port is configured in 16-bit acknowledge mode with little endian data format. Unlike other modes, the host is responsible for interpreting the boot stream. It writes data blocks individually into the host DMA port. Before configuring the DMA settings for each block, the host may either poll the ALLOW_CONFIG bit in HOST_STATUS or wait to be interrupted by the HWAIT signal. When using HWAIT, the host must still check ALLOW_CONFIG at least once before beginning to configure the host DMA port. After completing the configuration, the host is required to poll the READY bit in HOST_STATUS before beginning to transfer data. When the host sends an HIRQ control command, the boot kernel issues a CALL instruction to address 0xFFA0 0000. It is the host's responsibility to ensure valid code has been placed at this address. The routine at address 0xFFA0 0000 can be a simple initialization routine to configure internal resources, such as the SDRAM controller, which then returns using an RTS instruction. The routine may also be the final application, which will never return to the boot kernel.
- Boot from 8-bit host DMA (BMODE = 0xF)—In this mode, the host DMA port is configured in 8-bit interrupt mode with little endian data format. Unlike other modes, the host is responsible for interpreting the boot stream. It writes data blocks individually to the host DMA port. Before configuring the DMA settings for each block, the host may either poll the ALLOW_CONFIG bit in HOST_STATUS or wait to be interrupted by the HWAIT signal. When using HWAIT, the host must still check ALLOW_CONFIG at least once before beginning to configure the host DMA port. The host will receive an interrupt from the HOST_ACK signal every time it is allowed to send the next FIFO depth's worth (sixteen 32-bit words) of information. When the host sends an HIRQ control command, the boot kernel issues a CALL instruction to address 0xFFA0 0000. It is the host's responsibility to ensure valid code has been placed at this address. The routine at address 0xFFA0 0000 can be a simple initialization routine to configure internal resources, such as the SDRAM controller, which then returns using an RTS instruction. The routine may also be the final application, which will never return to the boot kernel.

For each of the boot modes, a 16-byte header is first read from an external memory device. The header specifies the number of bytes to be transferred and the memory destination address. Multiple memory blocks may be loaded by any boot sequence. Once all blocks are loaded, program execution commences from the address stored in the EVT1 register.

Prior to booting, the pre-boot routine interrogates the OTP memory. Individual boot modes can be customized or disabled based on OTP programming. External hardware, especially booting hosts, may monitor the HWAIT signal to determine when the pre-boot has finished and the boot kernel starts the boot process. However, the HWAIT signal does not toggle in NAND boot mode. By programming OTP memory, the user can instruct the preboot routine to also customize the PLL, voltage regulator, DDR controller, and/or asynchronous memory interface controller.

The boot kernel differentiates between a regular hardware reset and a wakeup-from-hibernate event to speed up booting in the later case. Bits 6-4 in the system reset configuration (SYSCR) register can be used to bypass the pre-boot routine and/or boot kernel in case of a software reset. They can also be used to simulate a wakeup-from-hibernate boot in the software reset case.

The boot process can be further customized by "initialization code." This is a piece of code that is loaded and executed prior to the regular application boot. Typically, this is used to configure the DDR controller or to speed up booting by managing PLL, clock frequencies, wait states, and/or serial bit rates.

The boot ROM also features C-callable function entries that can be called by the user application at run time. This enables second-stage boot or booting management schemes to be implemented with ease.

INSTRUCTION SET DESCRIPTION

The Blackfin processor family assembly language instruction set employs an algebraic syntax designed for ease of coding and readability. The instructions have been specifically tuned to provide a flexible, densely encoded instruction set that compiles to a very small final memory size. The instruction set also provides fully featured multifunction instructions that allow the programmer to use many of the processor core resources in a single instruction. Coupled with many features more often seen on microcontrollers, this instruction set is very efficient when compiling C and C++ source code. In addition, the architecture supports both user (algorithm/application code) and supervisor (O/S kernel, device drivers, debuggers, ISRs) modes of operation, allowing multiple levels of access to core processor resources.

The assembly language, which takes advantage of the processor's unique architecture, offers the following advantages:

- Seamlessly integrated DSP/MCU features are optimized for both 8-bit and 16-bit operations.
- A multi-issue load/store modified-Harvard architecture, which supports two 16-bit MAC or four 8-bit ALU + two load/store + two pointer updates per cycle.
- All registers, I/O, and memory are mapped into a unified 4G byte memory space, providing a simplified programming model.
- Microcontroller features, such as arbitrary bit and bit-field manipulation, insertion, and extraction; integer operations on 8-, 16-, and 32-bit data-types; and separate user and supervisor stack pointers.
- Code density enhancements, which include intermixing of 16- and 32-bit instructions (no mode switching, no code segregation). Frequently used instructions are encoded in 16 bits.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 20 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Table 21 details the maximum duty cycle for input transient voltage.

Table 20. Absolute Maximum Ratings

Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +1.43 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +3.8 V
Input Voltage[1, 2, 3]	–0.5 V to +3.6 V
Output Voltage Swing	–0.5 V to V_{DDEXT}+0.5 V
I_{OH}/I_{OL} Current per Single Pin[4]	40 mA (max)
I_{OH}/I_{OL} Current per Pin Group[4]	80 mA (max)
Storage Temperature Range	–65°C to +150°C
Junction Temperature Underbias	+125°C

[1] Applies to all bidirectional and input only pins except PB1-0, PE15-14, PG15–11, and PH7-6, where the absolute maximum input voltage range is –0.5 V to +5.5 V.

[2] Pins USB_DP, USB_DM, and USB_VBUS are 5 V-tolerant when VDDUSB is powered according to the operating conditions table. If VDDUSB supply voltage does not meet the specification in the operating conditions table, these pins could suffer long-term damage when driven to +5 V. If this condition is seen in the application, it can be corrected with additional circuitry to use the external host to power only the V_{DDUSB} pins. Contact factory for application detail and reliability information.

[3] Applies only when V_{DDEXT} is within specifications. When V_{DDEXT} is outside specifications, the range is V_{DDEXT} ± 0.2 V.

[4] For more information, see description preceding Table 22.

Table 21. Maximum Duty Cycle for Input[1] Transient Voltage

V_{IN} Max (V)[2]	V_{IN} Min (V)	Maximum Duty Cycle
3.63	–0.33	100%
3.80	–0.50	48%
3.90	–0.60	30%
4.00	–0.70	20%
4.10	–0.80	10%
4.20	–0.90	8%
4.30	–1.00	5%

[1] Does not apply to CLKIN. Absolute maximum for pins PB1-0, PE15-14, PG15-11, and PH7-6 is +5.5V.

[2] Only one of the listed options can apply to a particular design.

The Absolute Maximum Ratings table specifies the maximum total source/sink (I_{OH}/I_{OL}) current for a group of pins. Permanent damage can occur if this value is exceeded. To understand this specification, if pins PA4, PA3, PA2, PA1 and PA0 from group 1 in the Total Current Pin Groups table were sourcing or sinking 2 mA each, the total current for those pins would be 10 mA. This would allow up to 70 mA total that could be sourced or sunk by the remaining pins in the group without damaging the device. For a list of all groups and their pins, see the Total Current Pin Groups table. Note that the V_{OL} and V_{OH} specifications have separate per-pin maximum current requirements, see the Electrical Characteristics table.

Table 22. Total Current Pin Groups

Group	Pins in Group
1	PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PA8, PA9, PA10, PA11
2	PA12, PA13, PA14, PA15, PB8, PB9, PB10, PB11, PB12, PB13, PB14
3	PB0, PB1, PB2, PB3, PB4, PB5, PB6, PB7, BMODE0, BMODE1, BMODE2, BMODE3
4	TCK, TDI, TDO, TMS, $\overline{\text{TRST}}$, PD14, $\overline{\text{EMU}}$
5	PD8, PD9, PD10, PD11, PD12, PD13, PD15
6	PD0, PD1, PD2, PD3, PD4, PD5, PD6, PD7
7	PE11, PE12, PE13, PF12, PF13, PF14, PF15, PG3, PG4
8	PF4, PF5, PF6, PF7, PF8, PF9, PF10, PF11
9	PF0, PF1, PF2, PF3, PG0, PG1, PG2
10	PC0, PC1, PC2, PC3, PC4, PC5, PC6, PC7
11	PH5, PH6, PH7
12	A1, A2, A3
13	PH8, PH9, PH10, PH11, PH12, PH13
14	PI0, PI1, PI2, PI3, PI4, PI5, PI6, PI7
15	PI8, PI9, PI10, PI11, PI12, PI13, PI14, PI15
16	$\overline{\text{AMS0}}$, $\overline{\text{AMS1}}$, $\overline{\text{AMS2}}$, $\overline{\text{AMS3}}$, $\overline{\text{AOE}}$, CLKBUF, $\overline{\text{NMI}}$
17	CLKIN, XTAL, $\overline{\text{RESET}}$, RTXI, RTXO, $\overline{\text{ARE}}$, $\overline{\text{AWE}}$
18	D0, D1, D2, D3, D4, D5, D6, D7
19	D8, D9, D10, D11, D12
20	D13, D14, D15, $\overline{\text{ABE0}}$, $\overline{\text{ABE1}}$
21	EXT_WAKE, CLKOUT, PJ11, PJ12, PJ13
22	PJ0, PJ1, PJ2, PJ3, PJ4, PJ5, PJ6, PJ7, $\overline{\text{ATAPI\_PDIAG}}$
23	PJ8, PJ9, PJ10, PE7, PG12, PG13
24	PE0, PE1, PE2, PE4, PE5, PE6, PE8, PE9, PE10, PH3, PH4
25	PH0, PH2, PE14, PE15, PG5, PG6, PG7, PG8, PG9, PG10, PG11
26	PC8, PC9, PC10, PC11, PC12, PC13, PE3, PG14, PG15, PH1

Table 25. Clock Out Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{SCLK}	CLKOUT Period[1, 2]	7.5		ns
t_{SCLKH}	CLKOUT Width High	2.5		ns
t_{SCLKL}	CLKOUT Width Low	2.5		ns

[1] The t_{SCLK} value is the inverse of the f_{SCLK} specification. Reduced supply voltages affect the best-case value of 7.5 ns listed here.
[2] The t_{SCLK} value does not account for the effects of jitter.

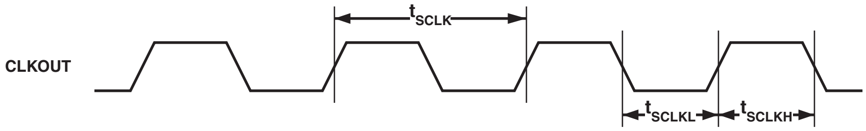


Figure 11. CLKOUT Interface Timing

Table 26. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirement				
$t_{RST\_IN\_PWR}$	$\overline{\text{RESET}}$ Deasserted After the V_{DDINT}, V_{DDEXT}, V_{DDDDR}, V_{DDUSB}, V_{DDRTC}, V_{DDVR}, V_{DDMP}, and CLKIN Pins Are Stable and Within Specification	3500 × t_{CKIN}		ns

In Figure 12, $V_{DD\_SUPPLIES}$ is V_{DDINT}, V_{DDEXT}, V_{DDDDR}, V_{DDUSB}, V_{DDRTC}, V_{DDVR}, and V_{DDMP}.

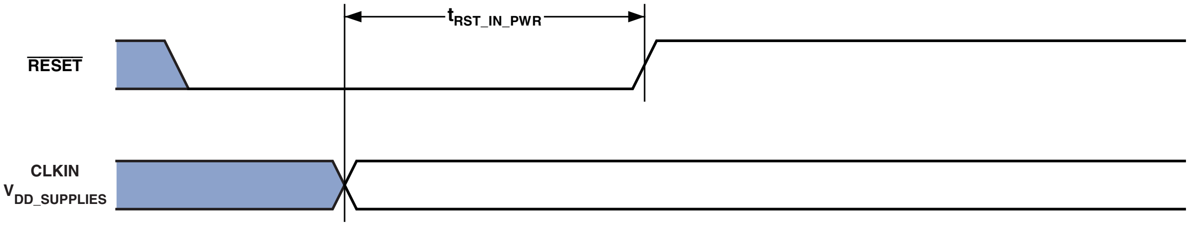


Figure 12. Power-Up Reset Timing

Asynchronous Memory Write Cycle Timing

Table 29 and Table 30 on Page 47 and Figure 15 and Figure 16 on Page 47 describe asynchronous memory write cycle operations for synchronous and for asynchronous ARDY.

Table 29. Asynchronous Memory Write Cycle Timing with Synchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{SARDY}	ARDY Setup Before the Falling Edge of CLKOUT	5.0		ns
t_{HARDY}	ARDY Hold After the Falling Edge of CLKOUT	0.0		ns
Switching Characteristics				
t_{DDAT}	DATA15–0 Disable After CLKOUT		6.0	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT	0.0		ns
t_{DO}	Output Delay After CLKOUT[1]		6.0	ns
t_{HO}	Output Hold After CLKOUT[1]	0.3		ns

[1] Output pins include $\overline{\text{AMS3–0}}$, $\overline{\text{ABE1–0}}$, ADDR19–1, and $\overline{\text{AWE}}$.

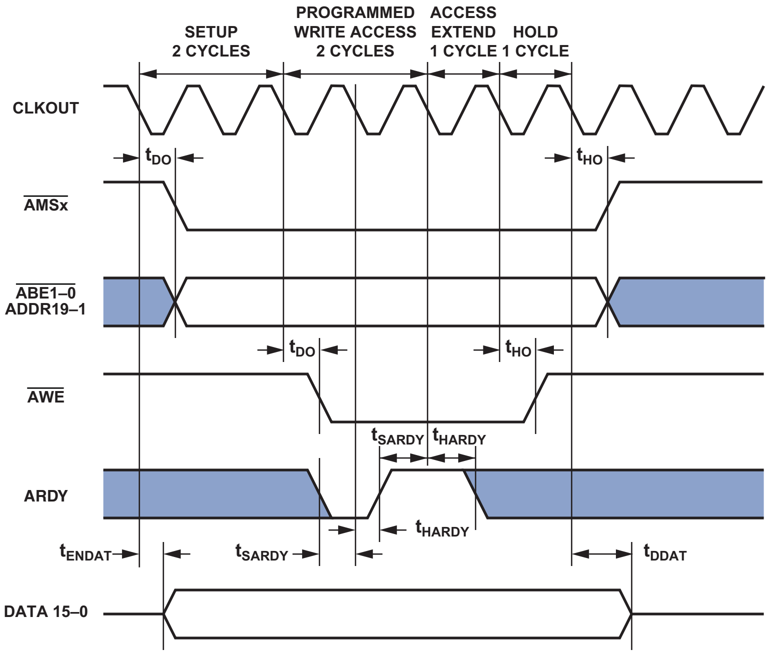


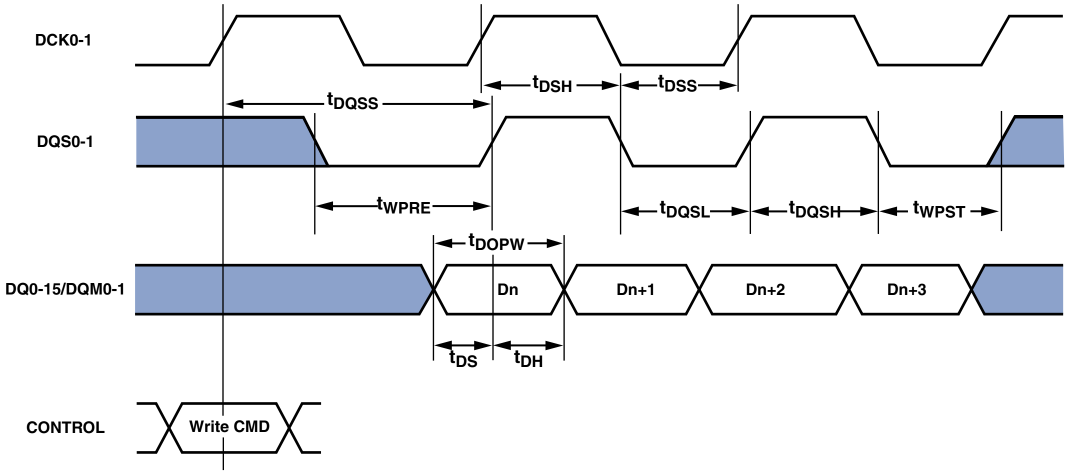
Figure 15. Asynchronous Memory Write Cycle Timing with Synchronous ARDY

DDR SDRAM/Mobile DDR SDRAM Write Cycle Timing

Table 33 and Figure 20 describe DDR SDRAM/mobile DDR SDRAM write cycle timing.

Table 33. DDR SDRAM/Mobile DDR SDRAM Write Cycle Timing

		DDR SDRAM		Mobile DDR SDRAM		
Parameter		**Min**	**Max**	**Min**	**Max**	**Unit**
Switching Characteristics						
t_{DQSS}	Write CMD to First DQS0-1	0.75	1.25	0.75	1.25	t_{CK}
t_{DS}	DQ0-15/DQM0-1 Setup to DQS0-1	0.90		0.90		ns
t_{DH}	DQ0-15/DQM0-1 Hold to DQS0-1	0.90		0.90		ns
t_{DSS}	DQS0-1 Falling to DCK0-1 Rising (DQS0-1 Setup)	0.20		0.20		t_{CK}
t_{DSH}	DQS0-1 Falling from DCK0-1 Rising (DQS0-1 Hold)	0.20		0.20		t_{CK}
t_{DQSH}	DQS0-1 High Pulse Width	0.35		0.40	0.60	t_{CK}
t_{DQSL}	DQS0-1 Low Pulse Width	0.35		0.40	0.60	t_{CK}
t_{WPRE}	DQS0-1 Write Preamble	0.25		0.25		t_{CK}
t_{WPST}	DQS0-1 Write Postamble	0.40	0.60	0.40	0.60	t_{CK}
t_{DOPW}	DQ0-15 and DQM0-1 Output Pulse Width (for Each)	1.75		1.75		ns



NOTE: CONTROL = $\overline{DCS0-1}$, DCLKE, $\overline{DRAS}$, $\overline{DCAS}$, AND $\overline{DWE}$.

Figure 20. DDR SDRAM /Mobile DDR SDRAM Controller Write Cycle Timing

External Port Bus Request and Grant Cycle Timing

Table 34 and Table 35 on Page 52 and Figure 21 and Figure 22 on Page 52 describe external port bus request and grant cycle operations for synchronous and for asynchronous $\overline{\text{BR}}$.

Table 34. External Port Bus Request and Grant Cycle Timing with Synchronous $\overline{\text{BR}}$

Parameter		Min	Max	Unit
Timing Requirements				
t_{BS}	$\overline{\text{BR}}$ Asserted to CLKOUT Low Setup	5.0		ns
t_{BH}	CLKOUT Low to $\overline{\text{BR}}$ Deasserted Hold Time	0.0		ns
Switching Characteristics				
t_{SD}	CLKOUT Low to $\overline{\text{AMSx}}$, Address, and $\overline{\text{ARE}}$/$\overline{\text{AWE}}$ Disable		5.0	ns
t_{SE}	CLKOUT Low to $\overline{\text{AMSx}}$, Address, and $\overline{\text{ARE}}$/$\overline{\text{AWE}}$ Enable		5.0	ns
t_{DBG}	CLKOUT Low to $\overline{\text{BG}}$ Asserted Output Delay		4.0	ns
t_{EBG}	CLKOUT Low to $\overline{\text{BG}}$ Deasserted Output Hold		4.0	ns
t_{DBH}	CLKOUT Low to $\overline{\text{BGH}}$ Asserted Output Delay		3.6	ns
t_{EBH}	CLKOUT Low to $\overline{\text{BGH}}$ Deasserted Output Hold		3.6	ns

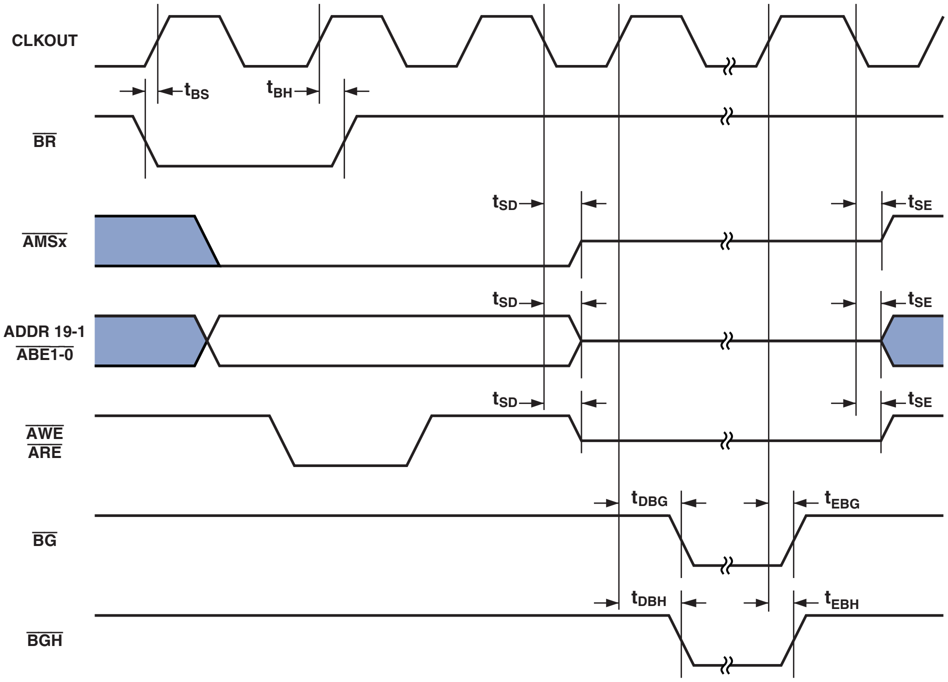


Figure 21. External Port Bus Request and Grant Cycle Timing with Synchronous $\overline{\text{BR}}$

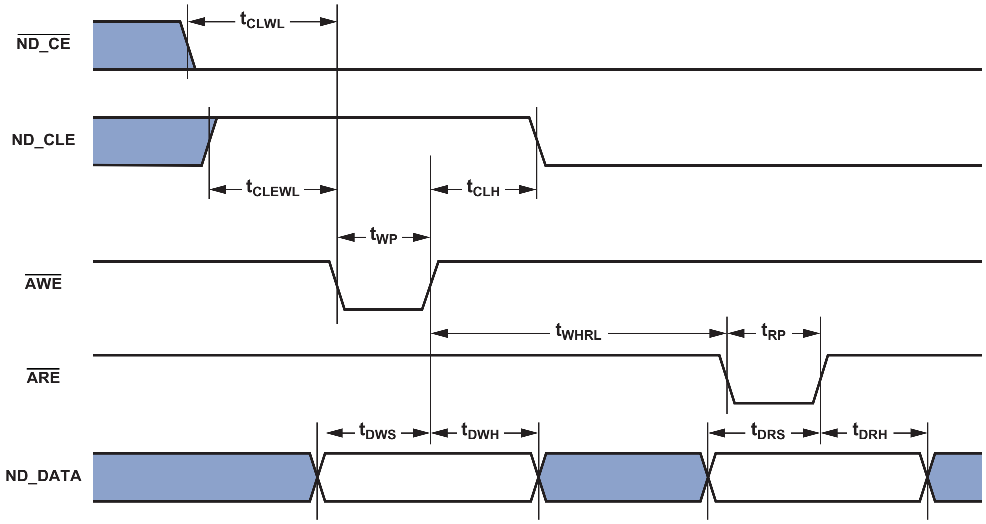


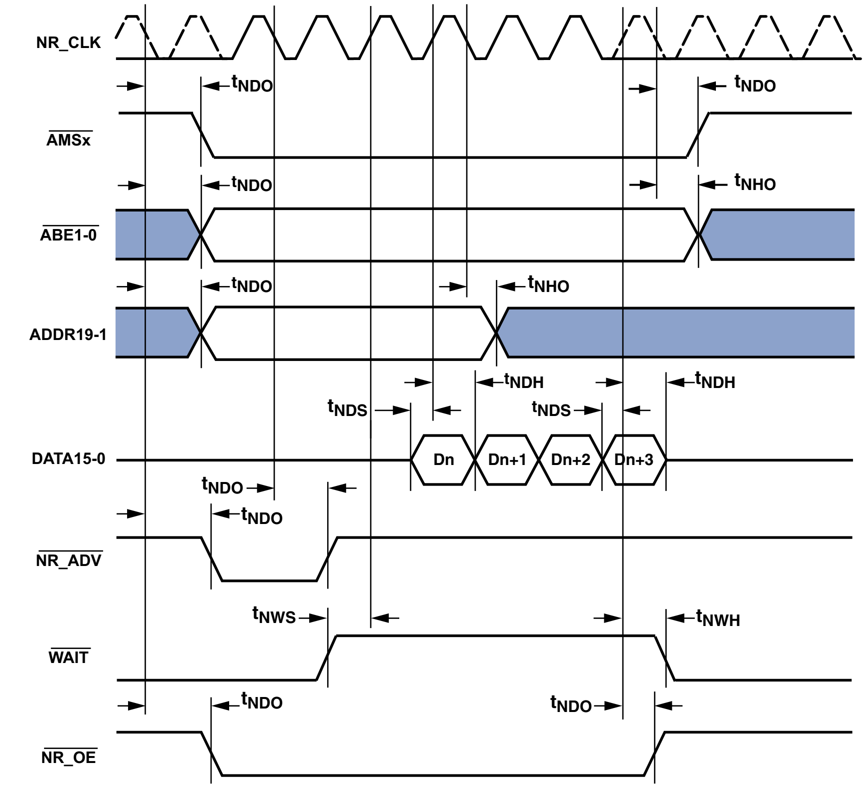
Figure 27. NAND Flash Controller Interface Timing—Write Followed by Read Operation

Synchronous Burst AC Timing

Table 37 and Figure 28 on Page 57 describe Synchronous Burst AC operations.

Table 37. Synchronous Burst AC Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{NDS}	DATA15-0 Setup Before NR_CLK	4.0		ns
t_{NDH}	DATA15-0 Hold After NR_CLK	2.0		ns
t_{NWS}	WAIT Setup Before NR_CLK	8.0		ns
t_{NWH}	WAIT Hold After NR_CLK	0.0		ns
Switching Characteristics				
t_{NDO}	$\overline{\text{AMSx}}$, $\overline{\text{ABE1-0}}$, ADDR19-1, $\overline{\text{NR\_ADV}}$, $\overline{\text{NR\_OE}}$ Output Delay After NR_CLK	6.0		ns
t_{NHO}	$\overline{\text{ABE1-0}}$, ADDR19-1 Output Hold After NR_CLK	–3.0		ns



NOTE: NR_CLK dotted line represents a free running version of NR_CLK that is not visible on the NR_CLK pin.

Figure 28. Synchronous Burst AC Interface Timing

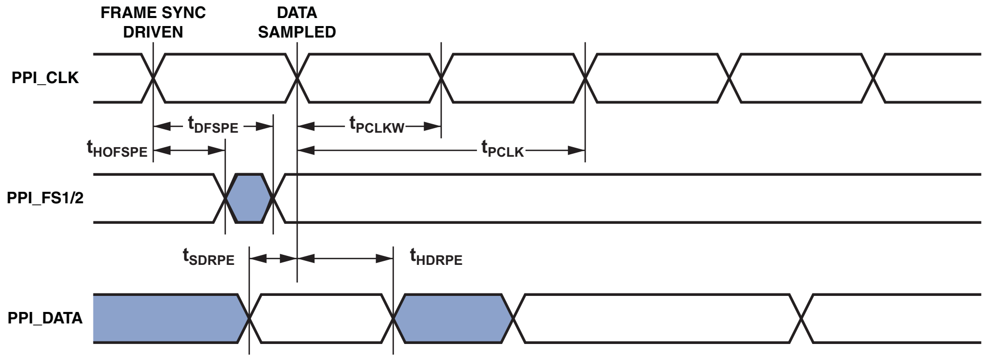


Figure 32. EPPI GP Rx Mode with Internal Frame Sync Timing

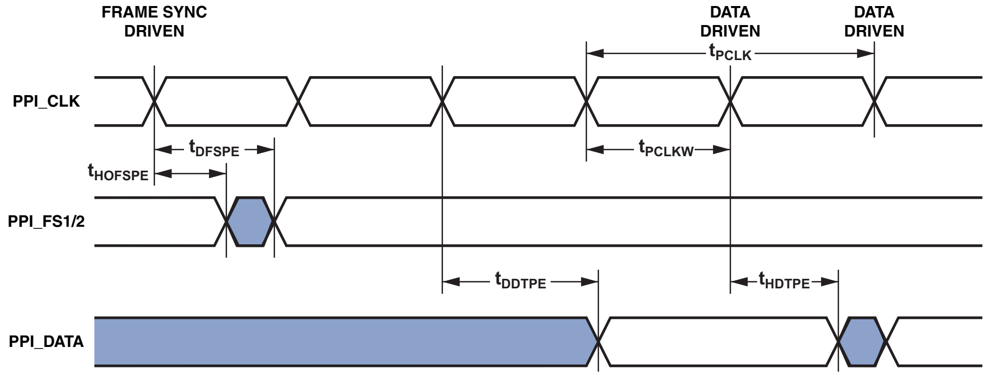


Figure 33. EPPI GP Tx Mode with Internal Frame Sync Timing

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 45 and Figure 39 describe SPI port slave operations.

Table 45. Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SPICHS}	SPIxSCK High Period	$2t_{SCLK} - 1.5$		ns
t_{SPICLS}	SPIxSCK Low Period	$2t_{SCLK} - 1.5$		ns
t_{SPICLK}	SPIxSCK Period	$4t_{SCLK}$		ns
t_{HDS}	Last SPIxSCK Edge to $\overline{\text{SPIxSS}}$ Not Asserted	$2t_{SCLK} - 1.5$		ns
t_{SPITDS}	Sequential Transfer Delay	$2t_{SCLK} - 1.5$		ns
t_{SDSCI}	$\overline{\text{SPIxSS}}$ Assertion to First SPIxSCK Edge	$2t_{SCLK} - 1.5$		ns
t_{SSPID}	Data Input Valid to SPIxSCK Edge (Data Input Setup)	1.6		ns
t_{HSPID}	SPIxSCK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{\text{SPIxSS}}$ Assertion to Data Out Active	0	8	ns
t_{DSDHI}	$\overline{\text{SPIxSS}}$ Deassertion to Data High Impedance	0	8	ns
t_{DDSPID}	SPIxSCK Edge to Data Out Valid (Data Out Delay)		10	ns
t_{HDSPID}	SPIxSCK Edge to Data Out Invalid (Data Out Hold)	0		ns

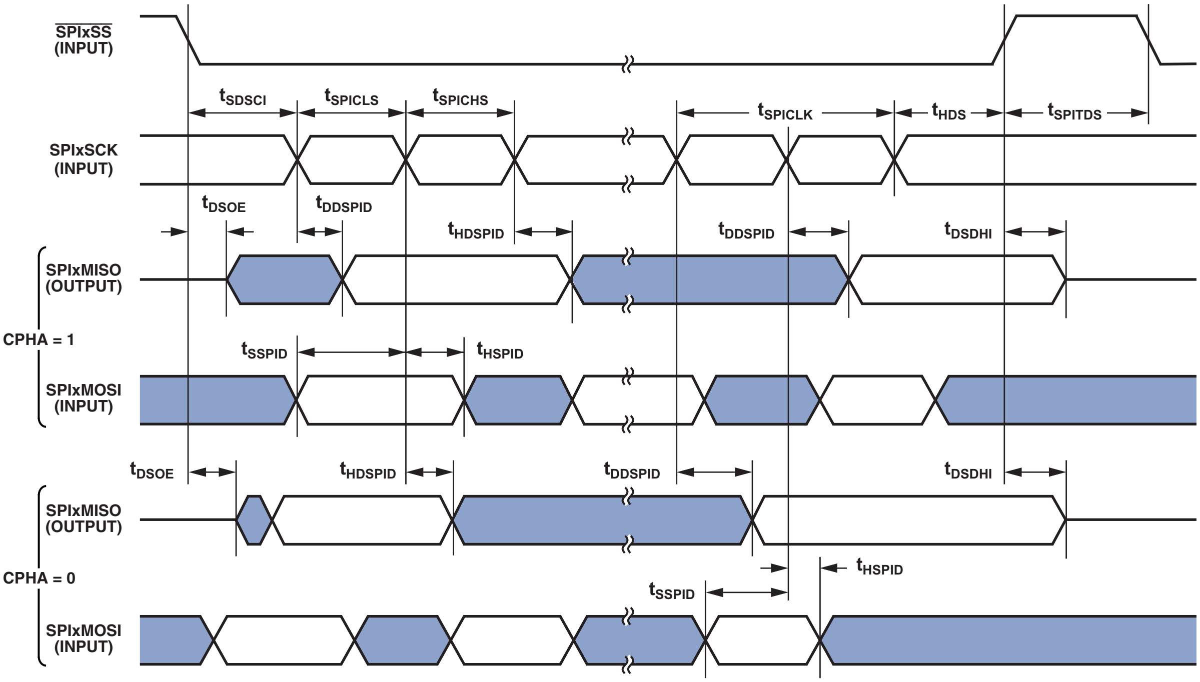


Figure 39. Serial Peripheral Interface (SPI) Port—Slave Timing

ATA/ATAPI-6 Interface Timing

The following tables and figures specify ATAPI timing parameters. For detailed parameter descriptions, refer to the ATAPI specification (ANSI INCITS 361-2002). Table 58 to Table 61 include ATAPI timing parameter equations. System designers should use these equations along with the parameters provided in Table 56 and Table 57. ATAPI timing control registers should be programmed such that ANSI INCITS 361-2002 specifications are met for the desired transfer type and mode.

Table 56. ATA/ATAPI-6 Timing Parameters

Parameter		Min	Max	Unit
t_{SK1}	Difference in output delay after CLKOUT for ATAPI output pins[1]		6	ns
t_{OD}	Output delay after CLKOUT for outputs[1]		12	ns
t_{SUD}	ATAPI_D0-15 or ATAPI_D0-15A Setup Before CLKOUT	6		ns
t_{SUI}	ATAPI_IORDY Setup Before CLKOUT	6		ns
t_{SUDU}	ATAPI_D0-15 or ATAPI_D0-15A Setup Before ATAPI_IORDY (UDMA-in only)	2		ns
t_{HDU}	ATAPI_D0-15 or ATAPI_D0-15A Hold After ATAPI_IORDY (UDMA-in only)	2.6		ns

[1] ATAPI output pins include ATAPI_CS0, ATAPI_CS1, A1-3, ATAPI_DIOR, ATAPI_DIOW, ATAPI_DMACK, ATAPI_D0-15, ATAPI_A0-2A, and ATAPI_D0-15A.

Table 57. ATA/ATAPI-6 System Timing Parameters

Parameter		Source
t_{SK2}	Maximum difference in board propagation delay between any 2 ATAPI output pins[1]	System Design
t_{BD}	Maximum board propagation delay.	System Design
t_{SK3}	Maximum difference in board propagation delay during a read between ATAPI_IORDY and ATAPI_D0-15/ATAPI_D0-15A.	System Design
t_{SK4}	Maximum difference in ATAPI cable propagation delay between output pin group A and output pin group B[2]	ATAPI Cable Specification
t_{CDD}	ATAPI cable propagation delay for ATAPI_D0-15 and ATAPI_D0-15A signals.	ATAPI Cable Specification
t_{CDC}	ATAPI cable propagation delay for ATAPI_DIOR, ATAPI_DIOW, ATAPI_IORDY, and ATAPI_DMACK signals.	ATAPI Cable Specification

[1] ATAPI output pins include ATAPI_CS0, ATAPI_CS1, A1-3, ATAPI_DIOR, ATAPI_DIOW, ATAPI_DMACK, ATAPI_D0-15, ATAPI_A0-2A, and ATAPI_D0-15A.

[2] Output pin group A includes ATAPI_DIOR, ATAPI_DIOW, and ATAPI_DMACK. Output pin group B includes ATAPI_CS0, ATAPI_CS1, A1-3, ATAPI_D0-15, ATAPI_A0-2A, and ATAPI_D0-15A.

ATAPI Multiword DMA Transfer Timing

Table 59 and Figure 49 through Figure 52 describe the ATAPI multiword DMA transfer timing. The material in these figures is adapted from ATAPI-6 (INCITS 361-2002[R2007] and is used with permission of the American National Standards Institute (ANSI) on behalf of the Information Technology Industry Council ("ITIC"). Copies of ATAPI-6 (INCITS 361-2002 [R2007] can be purchased from ANSI.

Table 59. ATAPI Multiword DMA Transfer Timing

ATAPI Parameter/Description		ATAPI_MULTI_TIM_x Timing Register Setting[1]	Timing Equation
t_0	Cycle time	TD, TK	$(\text{TD} + \text{TK}) \times t_{\text{SCLK}}$
t_D	$\overline{\text{ATAPI\_DIOR}}$/$\overline{\text{ATAPI\_DIOW}}$ asserted Pulse Width	TD	$\text{TD} \times t_{\text{SCLK}}$
t_F	$\overline{\text{ATAPI\_DIOR}}$ data hold	N/A	0
$t_{G(\text{write})}$	$\overline{\text{ATAPI\_DIOW}}$ data setup	TD	$\text{TD} \times t_{\text{SCLK}} - (t_{\text{SK1}} + t_{\text{SK2}} + t_{\text{SK4}})$
$t_{G(\text{read})}$	$\overline{\text{ATAPI\_DIOR}}$ data setup	TD	$t_{\text{OD}} + t_{\text{SUD}} + 2 \times t_{\text{BD}} + t_{\text{CDD}} + t_{\text{CDC}}$
t_H	$\overline{\text{ATAPI\_DIOW}}$ data hold	TK	$\text{TK} \times t_{\text{SCLK}} - (t_{\text{SK1}} + t_{\text{SK2}} + t_{\text{SK4}})$
t_I	$\overline{\text{ATAPI\_DMACK}}$ to $\overline{\text{ATAPI\_DIOR}}$/$\overline{\text{ATAPI\_DIOW}}$ setup	TM	$\text{TM} \times t_{\text{SCLK}} - (t_{\text{SK1}} + t_{\text{SK2}} + t_{\text{SK4}})$
t_J	$\overline{\text{ATAPI\_DIOR}}$/$\overline{\text{ATAPI\_DIOW}}$ to $\overline{\text{ATAPI\_DMACK}}$ hold	TK, TEOC_MDMA	$(\text{TK} + \text{TEOC\_MDMA}) \times t_{\text{SCLK}} - (t_{\text{SK1}} + t_{\text{SK2}} + t_{\text{SK4}})$
t_{KR}	$\overline{\text{ATAPI\_DIOR}}$ negated pulse width	TKR	$\text{TKR} \times t_{\text{SCLK}}$
t_{KW}	$\overline{\text{ATAPI\_DIOW}}$ negated pulse width	TKW	$\text{TKW} \times t_{\text{SCLK}}$
t_{LR}	$\overline{\text{ATAPI\_DIOR}}$ to $\overline{\text{ATAPI\_DMARQ}}$ delay	N/A	$(\text{TD} + \text{TK}) \times t_{\text{SCLK}} - (t_{\text{OD}} + 2 \times t_{\text{BD}} + 2 \times t_{\text{CDC}})$
t_M	$\overline{\text{ATAPI\_CS0-1}}$ valid to $\overline{\text{ATAPI\_DIOR}}$/$\overline{\text{ATAPI\_DIOW}}$	TM	$\text{TM} \times t_{\text{SCLK}} - (t_{\text{SK1}} + t_{\text{SK2}} + t_{\text{SK4}})$
t_N	$\overline{\text{ATAPI\_CS0-1}}$ hold	TK, TEOC_MDMA	$(\text{TK} + \text{TEOC\_MDMA}) \times t_{\text{SCLK}} - (t_{\text{SK1}} + t_{\text{SK2}} + t_{\text{SK4}})$

[1] ATAPI timing register setting should be programmed with a value that guarantees parameter compliance with the ATA ANSI specification for an ATA device mode of operation.

In Figure 57 and Figure 58 an alternate ATAPI_D0–15 port bus is ATAPI_D0–15A.

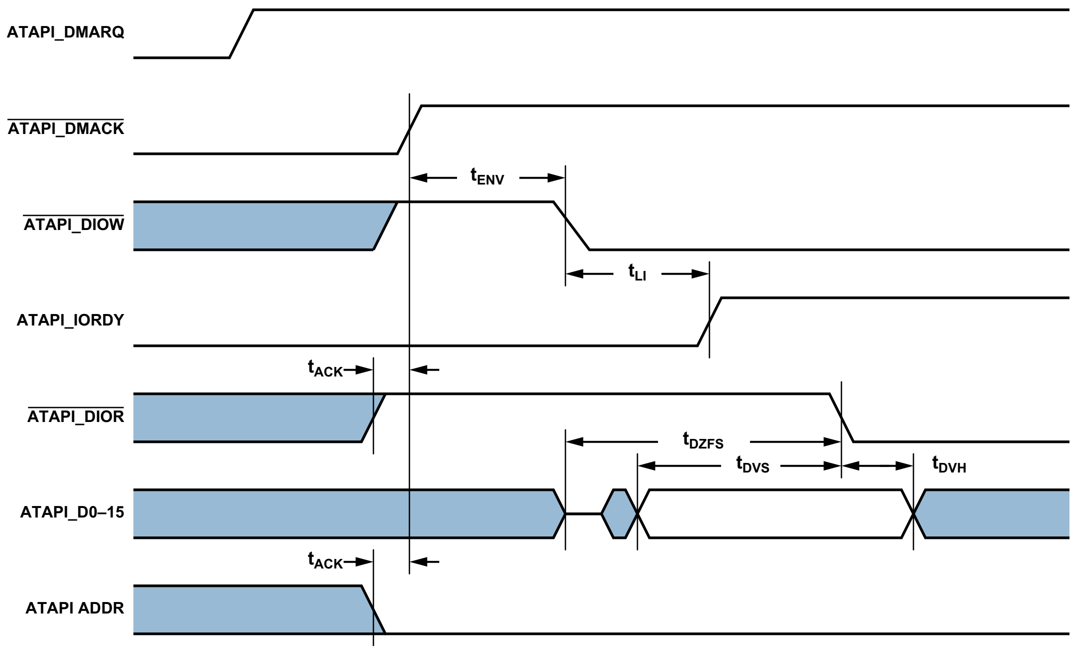


Figure 57. Initiating an Ultra DMA Data-Out Burst

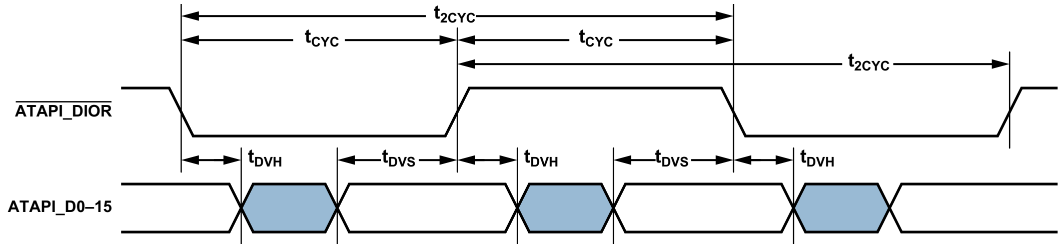


Figure 58. Sustained Ultra DMA Data-Out Burst

OUTPUT DRIVE CURRENTS

Figure 62 through Figure 71 show typical current-voltage characteristics for the output drivers of the ADSP-BF54x Blackfin processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

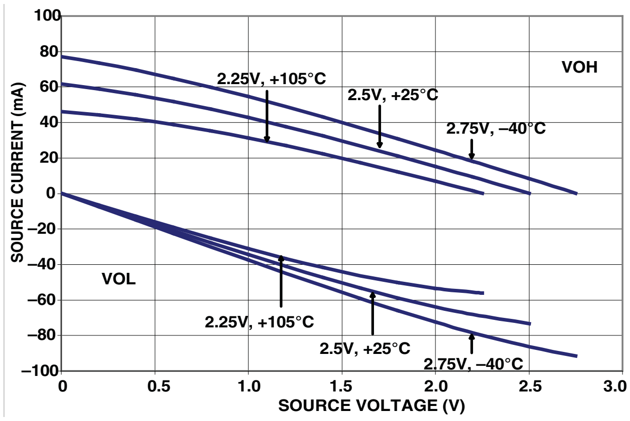


Figure 62. Drive Current A (Low V_{DDEXT})

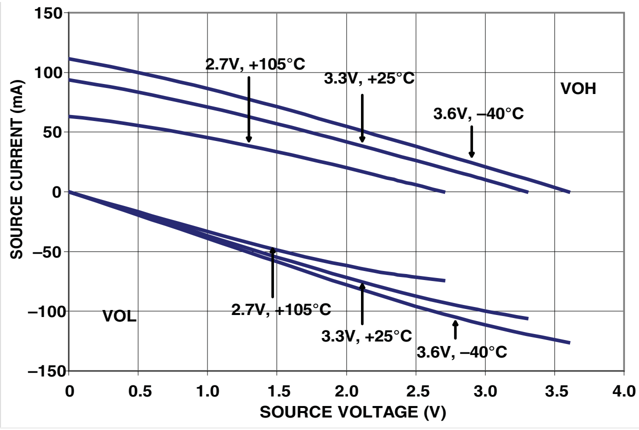


Figure 63. Drive Current A (High V_{DDEXT})

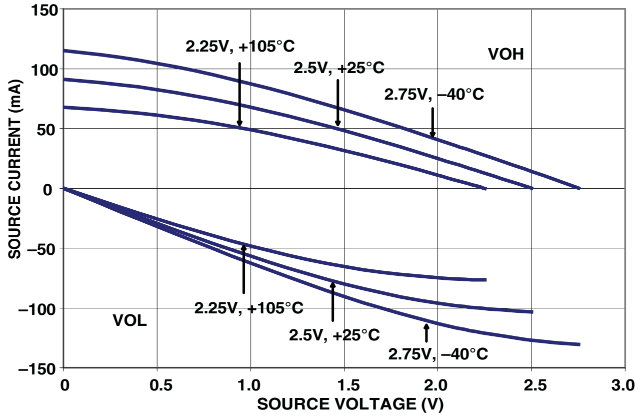


Figure 64. Drive Current B (Low V_{DDEXT})

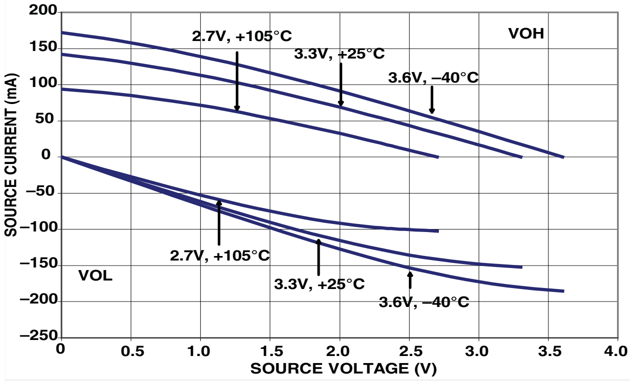


Figure 65. Drive Current B (High V_{DDEXT})

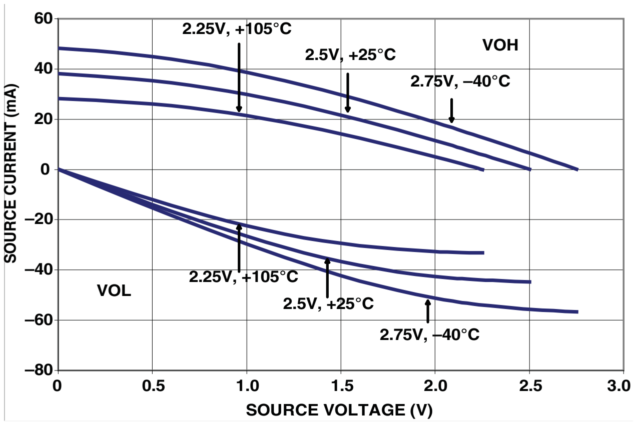


Figure 66. Drive Current C (Low V_{DDEXT})

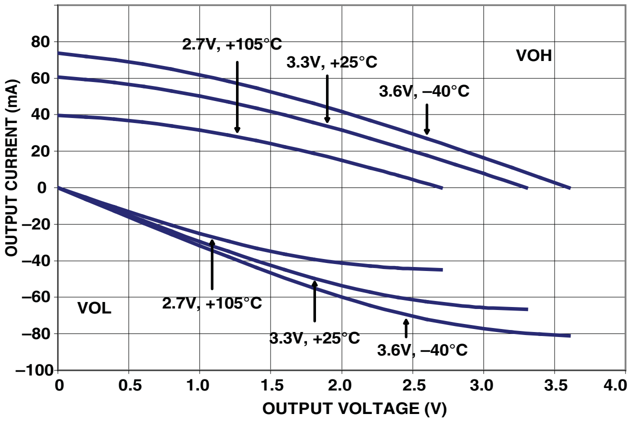


Figure 67. Drive Current C (High V_{DDEXT})

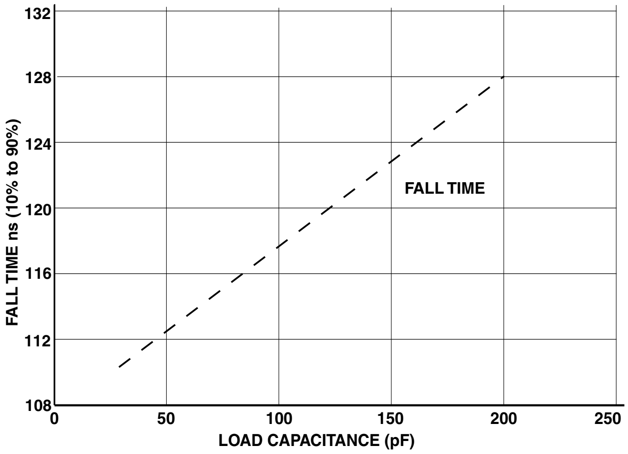


Figure 85. Typical Fall Time (10% to 90%) vs. Load Capacitance for Driver E at V_{DDEXT} = 2.7 V

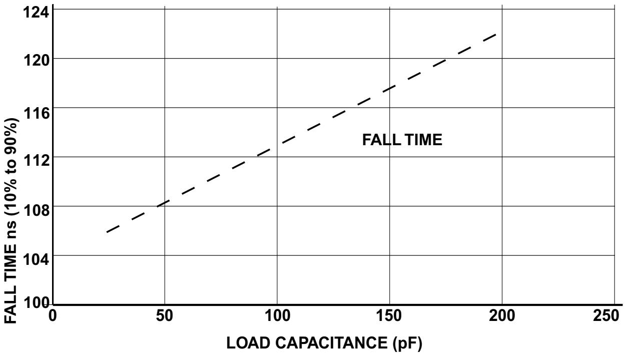


Figure 86. Typical Fall Time (10% to 90%) vs. Load Capacitance for Driver E at V_{DDEXT} = 3.65 V

THERMAL CHARACTERISTICS

To determine the junction temperature on the application printed circuit board use

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J =junction temperature (°C)

T_{CASE} = case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = from Table 64

P_D = power dissipation. (See Table 17 on Page 38 for a method to calculate P_D.)

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature (°C)

Table 64 lists values for θ_{JC} and θ_{JB} parameters. These values are provided for package comparison and printed circuit board design considerations. Airflow measurements in Table 64 comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC testboard.

Table 64. Thermal Characteristics, 400-Ball CSP_BGA

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s air flow	18.4	°C/W
	1 linear m/s air flow	15.8	°C/W
	2 linear m/s air flow	15.0	°C/W
θ_{JB}		9.75	°C/W
θ_{JC}		6.37	°C/W
ψ_{JT}	0 linear m/s air flow	0.27	°C/W
	1 linear m/s air flow	0.60	°C/W
	2 linear m/s air flow	0.66	°C/W

Table 65. 400-Ball CSP_BGA Ball Assignment (Alphabetical by Signal) (Continued)

Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.
TCK	V3	V_{DDDDR}	J14	V_{DDEXT}	N5	V_{DDINT}	G13
TDI	V5	V_{DDDDR}	J15	V_{DDEXT}	N15	V_{DDINT}	J6
TDO	V4	V_{DDDDR}	K14	V_{DDEXT}	P15	V_{DDINT}	J13
TMS	U5	V_{DDDDR}	K15	V_{DDEXT}	R6	V_{DDINT}	L6
$\overline{\text{TRST}}$	T5	V_{DDEXT}	E5	V_{DDEXT}	R7	V_{DDINT}	L15
USB_DM	E2	V_{DDEXT}	E9	V_{DDEXT}	R8	V_{DDINT}	P6
USB_DP	E1	V_{DDEXT}	E10	V_{DDEXT}	R15	V_{DDINT}	P7
USB_ID	G3	V_{DDEXT}	E11	V_{DDEXT}	T7	V_{DDINT}	P14
USB_RSET	D3	V_{DDEXT}	E12	V_{DDEXT}	T8	V_{DDINT}	R10
USB_VBUS	D2	V_{DDEXT}	F7	V_{DDEXT}	T9	V_{DDINT}	R11
USB_VREF	B1	V_{DDEXT}	F8	V_{DDEXT}	T10	V_{DDINT}	R12
USB_XI	F1	V_{DDEXT}	F13	V_{DDEXT}	T11	V_{DDINT}	U9
USB_XO	F2	V_{DDEXT}	G5	V_{DDEXT}	T12	V_{DDMP}	E8
V_{DDDDR}	F10	V_{DDEXT}	G6	V_{DDEXT}	T13	V_{DDRTC}	E13
V_{DDDDR}	F11	V_{DDEXT}	G7	V_{DDEXT}	T14	V_{DDUSB}	F5
V_{DDDDR}	F12	V_{DDEXT}	G14	V_{DDEXT}	T15	V_{DDUSB}	G4
V_{DDDDR}	G15	V_{DDEXT}	H5	V_{DDEXT}	T16	V_{DDVR}	F15
V_{DDDDR}	H13	V_{DDEXT}	H6	V_{DDINT}	F9	VR_{OUT0}	A18
V_{DDDDR}	H14	V_{DDEXT}	K6	V_{DDINT}	G8	VR_{OUT1}	A19
V_{DDDDR}	H15	V_{DDEXT}	M15	V_{DDINT}	G12	XTAL	A12