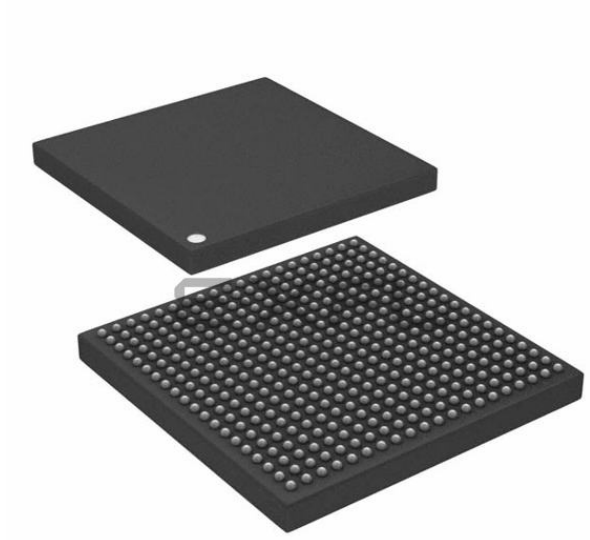

Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, SSP, TWI, UART, USB
Clock Rate	400MHz
Non-Volatile Memory	External
On-Chip RAM	260kB
Voltage - I/O	2.50V, 3.30V
Voltage - Core	1.25V
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	400-LFBGA, CSPBGA
Supplier Device Package	400-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-bf547ybc-4a

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REVISION HISTORY

03/14—Rev. D to Rev. E

Updated Development Tools 21

Corrected SPI2 pin count in Port B configuration in Pin Multiplexing 24

Corrected typographical error of parameter name in External DMA Request Timing 58

Added note to Table 42 in Serial Ports—Enable and Three-State 63

Corrected t_{WL} and t_{WH} minimum specifications from t_{SCLK} +1 to $1 \times t_{SCLK}$ in Timer Cycle Timing 69

Added/changed package dimensions to Figure 88 in Outline Dimensions 100

Added low Alpha Package model to Ordering Guide 101

The DDR memory controller can gluelessly manage up to two banks of double-rate synchronous dynamic memory (DDR and mobile DDR SDRAM). The 16-bit interface operates at the SCLK frequency, enabling a maximum throughput of 532M bytes/s. The DDR and mobile DDR controller is augmented with a queuing mechanism that performs efficient bursts into the DDR and mobile DDR. The controller is an industry standard DDR and mobile DDR SDRAM controller with each bank supporting from 64M bit to 512M bit device sizes and 4-, 8-, or 16-bit widths. The controller supports up to 256M bytes per external bank. With 2 external banks, the controller supports up to 512M bytes total. Each bank is independently programmable and is contiguous with adjacent banks regardless of the sizes of the different banks or their placement.

Traditional 16-bit asynchronous memories, such as SRAM, EPROM, and flash devices, can be connected to one of the four 64M byte asynchronous memory banks, represented by four memory select strobes. Alternatively, these strobes can function as bank-specific read or write strobes preventing further glue logic when connecting to asynchronous FIFO devices. See the Ordering Guide on Page 101 for a list of specific products that provide support for DDR memory.

In addition, the external bus can connect to advanced flash device technologies, such as:

- Page-mode NOR flash devices
- Synchronous burst-mode NOR flash devices
- NAND flash devices

Customers should consult the Ordering Guide when selecting a specific ADSP-BF54x component for the intended application. Products that provide support for mobile DDR memory are noted in the ordering guide footnotes.

NAND Flash Controller (NFC)

The ADSP-BF54x Blackfin processors provide a NAND Flash Controller (NFC) as part of the external bus interface. NAND flash devices provide high-density, low-cost memory. However, NAND flash devices also have long random access times, invalid blocks, and lower reliability over device lifetimes. Because of this, NAND flash is often used for read-only code storage. In this case, all DSP code can be stored in NAND flash and then transferred to a faster memory (such as DDR or SRAM) before execution. Another common use of NAND flash is for storage of multimedia files or other large data segments. In this case, a software file system may be used to manage reading and writing of the NAND flash device. The file system selects memory segments for storage with the goal of avoiding bad blocks and equally distributing memory accesses across all address locations. Hardware features of the NFC include:

- Support for page program, page read, and block erase of NAND flash devices, with accesses aligned to page boundaries.
- Error checking and correction (ECC) hardware that facilitates error detection and correction.
- A single 8-bit or 16-bit external bus interface for commands, addresses, and data.
- Support for SLC (single level cell) NAND flash devices unlimited in size, with page sizes of 256 bytes and 512 bytes. Larger page sizes can be supported in software.
- The ability to release external bus interface pins during long accesses.
- Support for internal bus requests of 16 bits or 32 bits.
- A DMA engine to transfer data between internal memory and a NAND flash device.

One-Time-Programmable Memory

The ADSP-BF54x Blackfin processors have 64K bits of one-time-programmable (OTP) non-volatile memory that can be programmed by the developer only one time. It includes the array and logic to support read access and programming. Additionally, its pages can be write protected.

OTP enables developers to store both public and private data on-chip. In addition to storing public and private key data for applications requiring security, it also allows developers to store completely user-definable data such as a customer ID, product ID, or a MAC address. By using this feature, generic parts can be shipped, which are then programmed and protected by the developer within this non-volatile memory. The OTP memory can be accessed through an API provided by the on-chip ROM.

I/O Memory Space

The ADSP-BF54x Blackfin processors do not define a separate I/O space. All resources are mapped through the flat 32-bit address space. On-chip I/O devices have their control registers mapped into memory-mapped registers (MMRs) at addresses near the top of the 4G byte address space. These are separated into two smaller blocks, one containing the control MMRs for all core functions and the other containing the registers needed for setup and control of the on-chip peripherals outside of the core. The MMRs are accessible only in supervisor mode and appear as reserved space to on-chip peripherals.

Booting

The ADSP-BF54x Blackfin processors contain a small on-chip boot kernel, which configures the appropriate peripheral for booting. If the ADSP-BF54x Blackfin processors are configured to boot from boot ROM memory space, the processor starts executing from the on-chip boot ROM. For more information, see Booting Modes on Page 18.

Event Handling

The event controller on the ADSP-BF54x Blackfin processors handles all asynchronous and synchronous events to the processors. The ADSP-BF54x Blackfin processors provide event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing of a higher-priority event takes precedence over servicing of a lower-priority event.

The controller provides support for five different types of events:

- Emulation. An emulation event causes the processor to enter emulation mode, allowing command and control of the processor via the JTAG interface.
- Reset. This event resets the processor.
- Non-maskable interrupt (NMI). The NMI event can be generated by the software watchdog timer or by the $\overline{\text{NMI}}$ input signal to the processor. The NMI event is frequently used as a power-down indicator to initiate an orderly shut-down of the system.
- Exceptions. Events that occur synchronously to program flow (that is, the exception is taken before the instruction is allowed to complete). Conditions such as data alignment violations and undefined instructions cause exceptions.
- Interrupts. Events that occur asynchronously to program flow. They are caused by input pins, timers, and other peripherals, as well as by an explicit software instruction.

Each event type has an associated register to hold the return address and an associated return-from-event instruction. When an event is triggered, the state of the processor is saved on the supervisor stack.

The ADSP-BF54x Blackfin processor event controller consists of two stages, the core event controller (CEC) and the system interrupt controller (SIC). The core event controller works with the system interrupt controller to prioritize and control all system events. Conceptually, interrupts from the peripherals enter into the SIC and are then routed directly into the general-purpose interrupts of the CEC.

Core Event Controller (CEC)

The CEC supports nine general-purpose interrupts (IVG15–7), in addition to the dedicated interrupt and exception events. Of these general-purpose interrupts, the two lowest-priority interrupts (IVG15–14) are recommended to be reserved for software interrupt handlers, leaving seven prioritized interrupt inputs to support the peripherals of the ADSP-BF54x Blackfin processors. Table 3 describes the inputs to the CEC, identifies their names in the event vector table (EVT), and lists their priorities.

System Interrupt Controller (SIC)

The system interrupt controller provides the mapping and routing of events from the many peripheral interrupt sources to the prioritized general-purpose interrupt inputs of the CEC. Although the ADSP-BF54x Blackfin processors provide a default mapping, the user can alter the mappings and priorities of interrupt events by writing the appropriate values into the interrupt assignment registers (SIC_IARx). The *ADSP-BF54x Hardware Reference Manual*, "System Interrupts" chapter describes the inputs into the SIC and the default mappings into the CEC.

Table 3. Core Event Controller (CEC)

Priority (0 is Highest)	Event Class	EVT Entry
0	Emulation/Test Control	EMU
1	Reset	RST
2	Nonmaskable Interrupt	NMI
3	Exception	EVX
4	Reserved	—
5	Hardware Error	IVHW
6	Core Timer	IVTMR
7	General Interrupt 7	IVG7
8	General Interrupt 8	IVG8
9	General Interrupt 9	IVG9
10	General Interrupt 10	IVG10
11	General Interrupt 11	IVG11
12	General Interrupt 12	IVG12
13	General Interrupt 13	IVG13
14	General Interrupt 14	IVG14
15	General Interrupt 15	IVG15

Event Control

The ADSP-BF54x Blackfin processors provide the user with a very flexible mechanism to control the processing of events. In the CEC, three registers are used to coordinate and control events. Each register is 16 bits wide:

- CEC interrupt latch register (ILAT). The ILAT register indicates when events have been latched. The appropriate bit is set when the processor has latched the event and cleared when the event has been accepted into the system. This register is updated automatically by the controller, but it may be written only when its corresponding IMASK bit is cleared.
- CEC interrupt mask register (IMASK). The IMASK register controls the masking and unmasking of individual events. When a bit is set in the IMASK register, that event is unmasked and is processed by the CEC when asserted. A cleared bit in the IMASK register masks the event, preventing the processor from servicing the event even though the event may be latched in the ILAT register. This register may be read or written while in supervisor mode. Note that general-purpose interrupts can be globally enabled and disabled with the STI and CLI instructions, respectively.
- CEC interrupt pending register (IPEND). The IPEND register keeps track of all nested events. A set bit in the IPEND register indicates that the event is currently active or nested at some level. This register is updated automatically by the controller but may be read while in supervisor mode.

The SIC allows further control of event processing by providing three 32-bit interrupt control and status registers. Each register contains a bit corresponding to each of the peripheral interrupt events shown in the *ADSP-BF54x Hardware Reference Manual*, "System Interrupts" chapter.

The USB clock (USB_XI) is provided through a dedicated external crystal or crystal oscillator. See Table 62 for related timing requirements. If using a fundamental mode crystal to provide the USB clock, connect the crystal between USB_XI and USB_XO with a circuit similar to that shown in Figure 7. Use a parallel-resonant, fundamental mode, microprocessor-grade crystal. If a third-overtone crystal is used, follow the circuit guidelines outlined in Clock Signals on Page 17 for third-overtone crystals.

The USB On-the-Go dual-role device controller includes a Phase Locked Loop with programmable multipliers to generate the necessary internal clocking frequency for USB. The multiplier value should be programmed based on the USB_XI clock frequency to achieve the necessary 480 MHz internal clock for USB high speed operation. For example, for a USB_XI crystal frequency of 24 MHz, the USB_PLLOSC_CTRL register should be programmed with a multiplier value of 20 to generate a 480 MHz internal clock.

ATA/ATAPI-6 INTERFACE

The ATAPI interface connects to CD/DVD and HDD drives and is ATAPI-6 compliant. The controller implements the peripheral I/O mode, the multi-DMA mode, and the Ultra DMA mode. The DMA modes enable faster data transfer and reduced host management. The ATAPI controller supports PIO, multi-DMA, and ultra DMA ATAPI accesses. Key features include:

- Supports PIO modes 0, 1, 2, 3, 4
- Supports multiword DMA modes 0, 1, 2
- Supports ultra DMA modes 0, 1, 2, 3, 4, 5 (up to UDMA 100)
- Programmable timing for ATA interface unit
- Supports CompactFlash cards using true IDE mode

By default, the ATAPI_A0-2 address signals and the ATAPI_D0-15 data signals are shared on the asynchronous memory interface with the asynchronous memory and NAND flash controllers. The data and address signals can be remapped to GPIO ports F and G, respectively, by setting PORTF_MUX[1:0] to b#01.

KEYPAD INTERFACE

The keypad interface is a 16-pin interface module that is used to detect the key pressed in a 8 × 8 (maximum) keypad matrix. The size of the input keypad matrix is programmable. The interface is capable of filtering the bounce on the input pins, which is common in keypad applications. The width of the filtered bounce is programmable. The module is capable of generating an interrupt request to the core once it identifies that any key has been pressed.

The interface supports a press-release-press mode and infrastructure for a press-hold mode. The former mode identifies a press, release and press of a key as two consecutive presses of the same key, whereas the latter mode checks the input key's state in periodic intervals to determine the number of times the same key is meant to be pressed. It is possible to detect when multiple keys are pressed simultaneously and to provide limited key resolution capability when this happens.

SECURE DIGITAL (SD)/SDIO CONTROLLER

The SD/SDIO controller is a serial interface that stores data at a data rate of up to 10M bytes per second using a 4-bit data line.

The SD/SDIO controller supports the SD memory mode only. The interface supports all the power modes and performs error checking by CRC.

CODE SECURITY

An OTP/security system, consisting of a blend of hardware and software, provides customers with a flexible and rich set of code security features with Lockbox® secure technology. Key features include:

- OTP memory
- Unique chip ID
- Code authentication
- Secure mode of operation

The security scheme is based upon the concept of authentication of digital signatures using standards-based algorithms and provides a secure processing environment in which to execute code and protect assets. See Lockbox Secure Technology Disclaimer on Page 23.

MEDIA TRANSCEIVER MAC LAYER (MXVR)

The ADSP-BF549 Blackfin processors provide a media transceiver (MXVR) MAC layer, allowing the processor to be connected directly to a MOST® [1] network through an FOT. See Figure 5 on Page 15 for an example of a MXVR MOST connection.

The MXVR is fully compatible with industry-standard standalone MOST controller devices, supporting 22.579 Mbps or 24.576 Mbps data transfer. It offers faster lock times, greater jitter immunity, and a sophisticated DMA scheme for data transfers. The high speed internal interface to the core and L1 memory allows the full bandwidth of the network to be utilized. The MXVR can operate as either the network master or as a network slave.

The MXVR supports synchronous data, asynchronous packets, and control messages using dedicated DMA channels that operate autonomously from the processor core moving data to and from L1 and/or L2 memory. Synchronous data is transferred to or from the synchronous data physical channels on the MOST bus through eight programmable DMA channels. The synchronous data DMA channels can operate in various modes including modes that trigger DMA operation when data patterns are detected in the receive data stream. Furthermore, two DMA channels support asynchronous traffic, and two others support control message traffic.

[1] MOST is a registered trademark of Standard Microsystems, Corp.

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
Port C: GPIO/*SPORT0/SD Controller/MXVR (MOST)*			
PC0/*TFS0*	I/O	GPIO/*SPORT0 Transmit Frame Sync*	C
PC1/*DT0SEC/MMCLK*	I/O	GPIO/*SPORT0 Transmit Data Secondary/MXVR Master Clock*	C
PC2/*DT0PRI*	I/O	GPIO/*SPORT0 Transmit Data Primary*	C
PC3/*TSCLK0*	I/O	GPIO/*SPORT0 Transmit Serial Clock*	A
PC4/*RFS0*	I/O	GPIO/*SPORT0 Receive Frame Sync*	C
PC5/*DR0SEC/MBCLK*	I/O	GPIO/*SPORT0 Receive Data Secondary/MXVR Bit Clock*	C
PC6/*DR0PRI*	I/O	GPIO/*SPORT0 Receive Data Primary*	C
PC7/*RSCLK0*	I/O	GPIO/*SPORT0 Receive Serial Clock*	C
PC8/*SD_D0*	I/O	GPIO/*SD Data Bus*	A
PC9/*SD_D1*	I/O	GPIO/*SD Data Bus*	A
PC10/*SD_D2*	I/O	GPIO/*SD Data Bus*	A
PC11/*SD_D3*	I/O	GPIO/*SD Data Bus*	A
PC12/*SD_CLK*	I/O	GPIO/*SD Clock Output*	A
PC13/*SD_CMD*	I/O	GPIO/*SD Command*	A
Port D: GPIO/*PPI0–2/SPORT 1/Keypad/Host DMA*			
PD0/*PPI1_D0/HOST_D8/ TFS1/PPI0_D18*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Transmit Frame Sync/PPI0 Data*	C
PD1/*PPI1_D1/HOST_D9/ DT1SEC/PPI0_D19*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Transmit Data Secondary/PPI0 Data*	C
PD2/*PPI1_D2/HOST_D10/ DT1PRI/PPI0_D20*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Transmit Data Primary/PPI0 Data*	C
PD3/*PPI1_D3/HOST_D11/ TSCLK1/PPI0_D21*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Transmit Serial Clock/PPI0 Data*	A
PD4/*PPI1_D4/HOST_D12/RFS1/PPI0_D22*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Receive Frame Sync/PPI0 Data*	C
PD5/*PPI1_D5/HOST_D13/DR1SEC/PPI0_D23*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Receive Data Secondary/PPI0 Data*	C
PD6/*PPI1_D6/HOST_D14/DR1PRI*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Receive Data Primary*	C
PD7/*PPI1_D7/HOST_D15/RSCLK1*	I/O	GPIO/*PPI1 Data/Host DMA/SPORT1 Receive Serial Clock*	A
PD8/*PPI1_D8/HOST_D0/ PPI2_D0/KEY_ROW0*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Row Input*	A
PD9/*PPI1_D9/HOST_D1/PPI2_D1/KEY_ROW1*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Row Input*	A
PD10/*PPI1_D10/HOST_D2/PPI2_D2/KEY_ROW2*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Row Input*	A
PD11/*PPI1_D11/HOST_D3/PPI2_D3/KEY_ROW3*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Row Input*	A
PD12/*PPI1_D12/HOST_D4/PPI2_D4/KEY_COL0*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Column Output*	A
PD13/*PPI1_D13/HOST_D5/PPI2_D5/KEY_COL1*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Column Output*	A
PD14/*PPI1_D14/HOST_D6/PPI2_D6/KEY_COL2*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Column Output*	A
PD15/*PPI1_D15/HOST_D7/PPI2_D7/KEY_COL3*	I/O	GPIO/*PPI1 Data/Host DMA/PPI2 Data/Keypad Column Output*	A

Table 11. Pin Descriptions (Continued)

Pin Name	I/O[1]	Function (First/Second/Third/Fourth)	Driver Type[2]
Port E: GPIO/*SPI0/UART0-1/PPI1/TWI0/Keypad*			
PE0/*SPI0SCK*/*KEY_COL7*[3]	I/O	GPIO/*SPI0 Clock*/*Keypad Column Output*	A
PE1/*SPI0MISO*/*KEY_ROW6*[3]	I/O	GPIO/*SPI0 Master In Slave Out*/*Keypad Row Input*	C
PE2/*SPI0MOSI*/*KEY_COL6*	I/O	GPIO/*SPI0 Master Out Slave In*/*Keypad Column Output*	C
PE3/$\overline{SPI0SS}$/*KEY_ROW5*	I/O	GPIO/*SPI0 Slave Select Input*/*Keypad Row Input*	A
PE4/$\overline{SPI0SEL1}$/*KEY_COL*[3]	I/O	GPIO/*SPI0 Slave Select Enable 1*/*Keypad Column Output*	A
PE5/$\overline{SPI0SEL2}$/*KEY_ROW4*	I/O	GPIO/*SPI0 Slave Select Enable 2*/*Keypad Row Input*	A
PE6/$\overline{SPI0SEL3}$/*KEY_COL4*	I/O	GPIO/*SPI0 Slave Select Enable 3*/*Keypad Column Output*	A
PE7/*UART0TX*/*KEY_ROW7*	I/O	GPIO/*UART0 Transmit*/*Keypad Row Input*	A
PE8/*UART0RX*/*TACI0*	I/O	GPIO/*UART0 Receive*/*Alternate Capture Input 0*	A
PE9/$\overline{UART1RTS}$	I/O	GPIO/*UART1 Request to Send*	A
PE10/$\overline{UART1CTS}$	I/O	GPIO/*UART1 Clear to Send*	A
PE11/*PPI1_CLK*	I/O	GPIO/*PPI1 Clock*	A
PE12/*PPI1_FS1*	I/O	GPIO/*PPI1 Frame Sync 1*	A
PE13/*PPI1_FS2*	I/O	GPIO/*PPI1 Frame Sync 2*	A
PE14/*SCL0*	I/O	GPIO/*TWI0 Serial Clock* (Open-drain output: requires a pull-up resistor.)	E
PE15/*SDA0*	I/O	GPIO/*TWI0 Serial Data* (Open-drain output: requires a pull-up resistor.)	E
Port F: *GPIO/PPI0/Alternate ATAPI Data*			
PF0/*PPI0_D0/ATAPI_D0A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A
PF1/*PPI0_D1/ATAPI_D1A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A
PF2/*PPI0_D2/ATAPI_D2A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A
PF3/*PPI0_D3/ATAPI_D3A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A
PF4/*PPI0_D4/ATAPI_D4A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A
PF5/*PPI0_D5/ATAPI_D5A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A
PF6/*PPI0_D6/ATAPI_D6A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A
PF7/*PPI0_D7/ATAPI_D7A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A
PF8/*PPI0_D8/ATAPI_D8A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A
PF9/*PPI0_D9/ATAPI_D9A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A
PF10/*PPI0_D10/ATAPI_D10A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A
PF11/*PPI0_D11/ATAPI_D11A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A
PF12/*PPI0_D12/ATAPI_D12A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A
PF13/*PPI0_D13/ATAPI_D13A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A
PF14/*PPI0_D14/ATAPI_D14A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A
PF15/*PPI0_D15/ATAPI_D15A*	I/O	GPIO/*PPI0 Data/Alternate ATAPI Data*	A

Table 18. Activity Scaling Factors[1]

I_{DDINT} Power Vector	Activity Scaling Factor (ASF)
$I_{DD-PEAK}$	1.29
$I_{DD-HIGH}$	1.24
I_{DD-TYP}	1.00
I_{DD-APP}	0.87
I_{DD-NOP}	0.74
$I_{DD-IDLE}$	0.47

[1] See *Estimating Power for ADSP-BF534/BF536/BF537 Blackfin Processors (EE-297)*. The power vector information also applies to the ADSP-BF542/ADSP-BF544/ADSP-BF547/ADSP-BF548/ADSP-BF549 processors.

Table 19. Dynamic Current in CCLK Domain (mA, with ASF = 1.0)[1]

	Voltage (V_{DDINT})[2]												
f_{CCLK} (MHz)[2]	0.90 V	0.95 V	1.00 V	1.05 V	1.10 V	1.15 V	1.20 V	1.25 V	1.30 V	1.35 V	1.38 V	1.40 V	1.43 V
100	29.7	31.6	33.9	35.7	37.9	40.5	42.9	45.5	48.2	50.8	52.0	53.5	54.6
200	55.3	58.9	62.5	66.0	70.0	74.0	78.3	82.5	86.7	91.3	93.3	95.6	97.6
300	80.8	85.8	91.0	96.0	101.3	107.0	112.8	118.7	124.6	130.9	133.8	137.0	140.0
400	N/A	112.2	119.4	125.5	132.4	139.6	146.9	154.6	162.3	170.0	173.8	177.8	181.6
500	N/A	N/A	N/A	N/A	N/A	171.9	180.6	189.9	199.1	205.7	210.3	213.0	217.6
533	N/A	N/A	N/A	N/A	N/A	N/A	191.9	201.6	211.5	218.0	222.8	225.7	230.5
600	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	233.1	241.4	246.7	252.7	258.1

[1] The values are not guaranteed as stand-alone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 36.
[2] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 34.

Table 30. Asynchronous Memory Write Cycle Timing with Asynchronous ARDY

Parameter		Min	Max	Unit
Timing Requirements				
t_{DANW}	ARDY Negated Delay from $\overline{AMSx}$ Asserted[1]		(S + WA – 2) × t_{SCLK}	ns
t_{HAA}	ARDY Asserted Hold After $\overline{AWE}$ Negated	0.0		ns
Switching Characteristics				
t_{DDAT}	DATA15–0 Disable After CLKOUT		6.0	ns
t_{ENDAT}	DATA15–0 Enable After CLKOUT	0.0		ns
t_{DO}	Output Delay After CLKOUT[2]		6.0	ns
t_{HO}	Output Hold After CLKOUT[2]	0.3		ns

[1] S = number of programmed setup cycles, WA = number of programmed write access cycles.
[2] Output pins include $\overline{AMS3–0}$, $\overline{ABE1–0}$, ADDR19–1, $\overline{AOE}$, and $\overline{AWE}$.

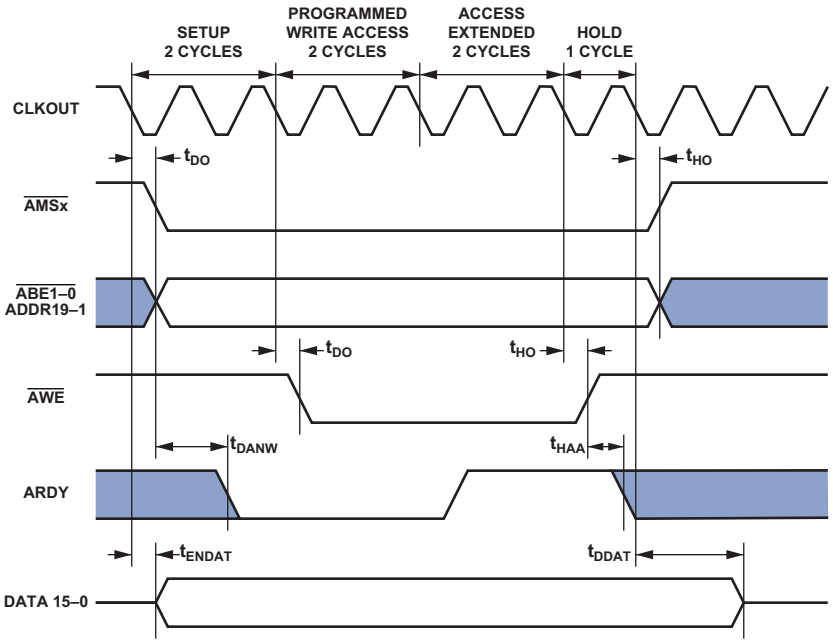

Figure 16. Asynchronous Memory Write Cycle Timing with Asynchronous ARDY

DDR SDRAM/Mobile DDR SDRAM Write Cycle Timing

Table 33 and Figure 20 describe DDR SDRAM/mobile DDR SDRAM write cycle timing.

Table 33. DDR SDRAM/Mobile DDR SDRAM Write Cycle Timing

Parameter		DDR SDRAM Min	DDR SDRAM Max	Mobile DDR SDRAM Min	Mobile DDR SDRAM Max	Unit
Switching Characteristics						
t_{DQSS}	Write CMD to First DQS0-1	0.75	1.25	0.75	1.25	t_{CK}
t_{DS}	DQ0-15/DQM0-1 Setup to DQS0-1	0.90		0.90		ns
t_{DH}	DQ0-15/DQM0-1 Hold to DQS0-1	0.90		0.90		ns
t_{DSS}	DQS0-1 Falling to DCK0-1 Rising (DQS0-1 Setup)	0.20		0.20		t_{CK}
t_{DSH}	DQS0-1 Falling from DCK0-1 Rising (DQS0-1 Hold)	0.20		0.20		t_{CK}
t_{DQSH}	DQS0-1 High Pulse Width	0.35		0.40	0.60	t_{CK}
t_{DQSL}	DQS0-1 Low Pulse Width	0.35		0.40	0.60	t_{CK}
t_{WPRE}	DQS0-1 Write Preamble	0.25		0.25		t_{CK}
t_{WPST}	DQS0-1 Write Postamble	0.40	0.60	0.40	0.60	t_{CK}
t_{DOPW}	DQ0-15 and DQM0-1 Output Pulse Width (for Each)	1.75		1.75		ns

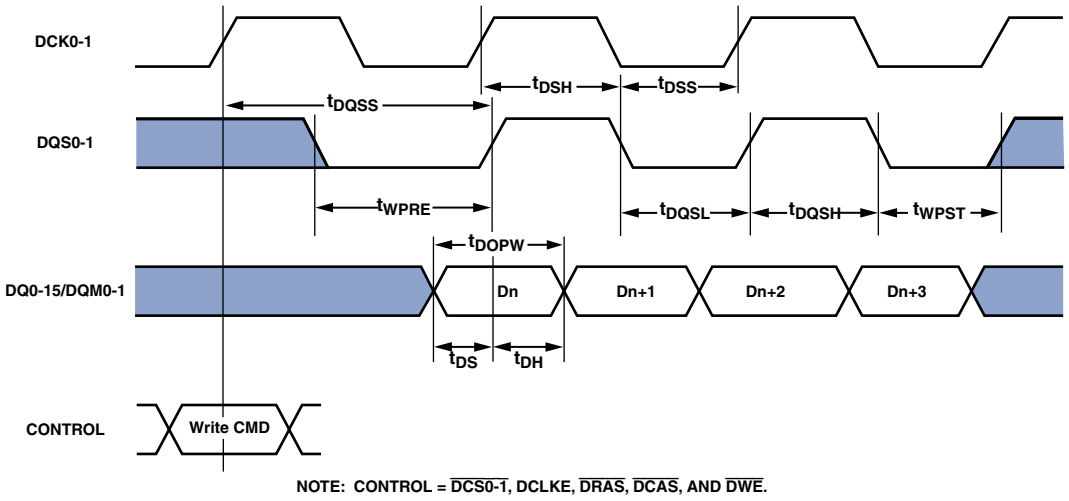

Figure 20. DDR SDRAM /Mobile DDR SDRAM Controller Write Cycle Timing

NAND Flash Controller Interface Timing

Table 36 and Figure 23 on Page 54 through Figure 27 on Page 56 describe NAND flash controller interface operations. In the figures, ND_DATA is ND_D0–D15.

Table 36. NAND Flash Controller Interface Timing

Parameter		Min	Max	Unit
Write Cycle				
Switching Characteristics				
t_{CWL}	$\overline{ND\_CE}$ Setup Time to $\overline{AWE}$ Low	$1.0 \times t_{SCLK} - 4$		ns
t_{CH}	$\overline{ND\_CE}$ Hold Time from $\overline{AWE}$ High	$3.0 \times t_{SCLK} - 4$		ns
t_{CLEWL}	ND_CLE Setup Time High to $\overline{AWE}$ Low	0.0		ns
t_{CLH}	ND_CLE Hold Time from $\overline{AWE}$ High	$2.5 \times t_{SCLK} - 4$		ns
t_{ALEWL}	ND_ALE Setup Time Low to $\overline{AWE}$ Low	0.0		ns
t_{ALH}	ND_ALE Hold Time from $\overline{AWE}$ High	$2.5 \times t_{SCLK} - 4$		ns
t_{WP}[1]	$\overline{AWE}$ Low to $\overline{AWE}$ High	$(WR\_DLY + 1.0) \times t_{SCLK} - 4$		ns
t_{WHWL}	$\overline{AWE}$ High to $\overline{AWE}$ Low	$4.0 \times t_{SCLK} - 4$		ns
t_{WC}[1]	$\overline{AWE}$ Low to $\overline{AWE}$ Low	$(WR\_DLY + 5.0) \times t_{SCLK} - 4$		ns
t_{DWS}[1]	Data Setup Time for a Write Access	$(WR\_DLY + 1.5) \times t_{SCLK} - 4$		ns
t_{DWH}	Data Hold Time for a Write Access	$2.5 \times t_{SCLK} - 4$		ns
Read Cycle				
Switching Characteristics				
t_{CRL}	$\overline{ND\_CE}$ Setup Time to $\overline{ARE}$ Low	$1.0 \times t_{SCLK} - 4$		ns
t_{CRH}	$\overline{ND\_CE}$ Hold Time from $\overline{ARE}$ High	$3.0 \times t_{SCLK} - 4$		ns
t_{RP}[1]	$\overline{ARE}$ Low to $\overline{ARE}$ High	$(RD\_DLY + 1.0) \times t_{SCLK} - 4$		ns
t_{RHRL}	$\overline{ARE}$ High to $\overline{ARE}$ Low	$4.0 \times t_{SCLK} - 4$		ns
t_{RC}[1]	$\overline{ARE}$ Low to $\overline{ARE}$ Low	$(RD\_DLY + 5.0) \times t_{SCLK} - 4$		ns
Timing Requirements				
t_{DRS}	Data Setup Time for a Read Transaction	8.0		ns
t_{DRH}	Data Hold Time for a Read Transaction	0.0		ns
Write Followed by Read				
Switching Characteristic				
t_{WHRL}	$\overline{AWE}$ High to $\overline{ARE}$ Low	$5.0 \times t_{SCLK} - 4$		ns

[1] WR_DLY and RD_DLY are defined in the NFC_CTL register.

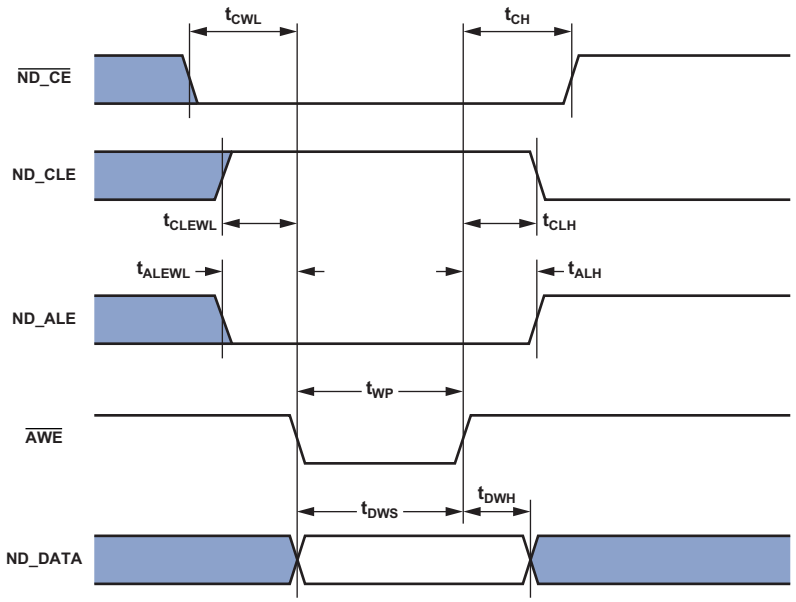

Figure 23. NAND Flash Controller Interface Timing—Command Write Cycle

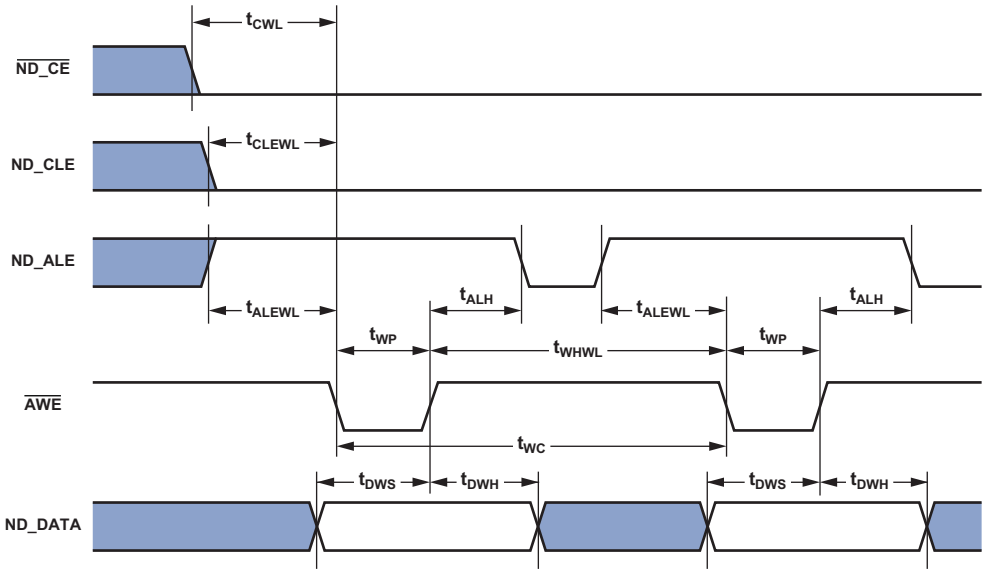

Figure 24. NAND Flash Controller Interface Timing—Address Write Cycle

Enhanced Parallel Peripheral Interface Timing

Table 39 and Figure 32 on Page 60, Figure 30 on Page 59, Figure 33 on Page 60, and Figure 31 on Page 59 describe enhanced parallel peripheral interface timing operations.

Table 39. Enhanced Parallel Peripheral Interface Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCLKW}	PPIx_CLK Width	6.0		ns
t_{PCLK}	PPIx_CLK Period	13.3		ns
Timing Requirements—GP Input and Frame Capture Modes				
t_{SFSPE}	External Frame Sync Setup Before PPIx_CLK	0.9		ns
t_{HFSPE}	External Frame Sync Hold After PPIx_CLK	1.9		ns
t_{SDRPE}	Receive Data Setup Before PPIx_CLK	1.6		ns
t_{HDRPE}	Receive Data Hold After PPIx_CLK	1.5		ns
Switching Characteristics—GP Output and Frame Capture Modes				
t_{DFSPE}	Internal Frame Sync Delay After PPIx_CLK		10.5	ns
t_{HOFSPE}	Internal Frame Sync Hold After PPIx_CLK	2.4		ns
t_{DDTPE}	Transmit Data Delay After PPIx_CLK		9.9	ns
t_{HDTPE}	Transmit Data Hold After PPIx_CLK	2.4		ns

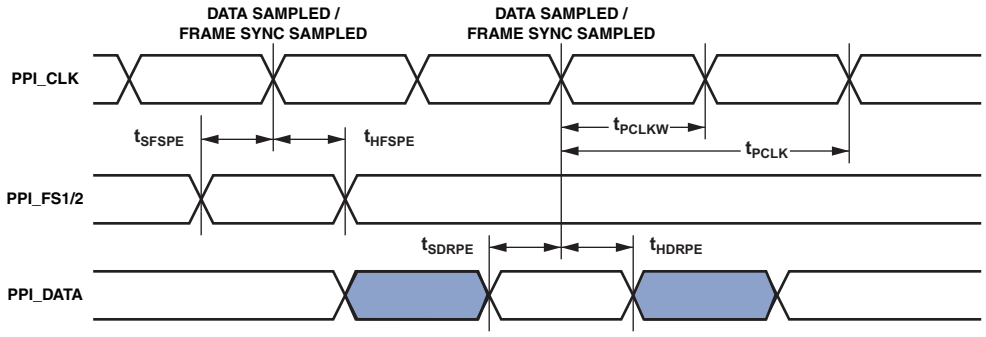

Figure 30. EPPI GP Rx Mode with External Frame Sync Timing

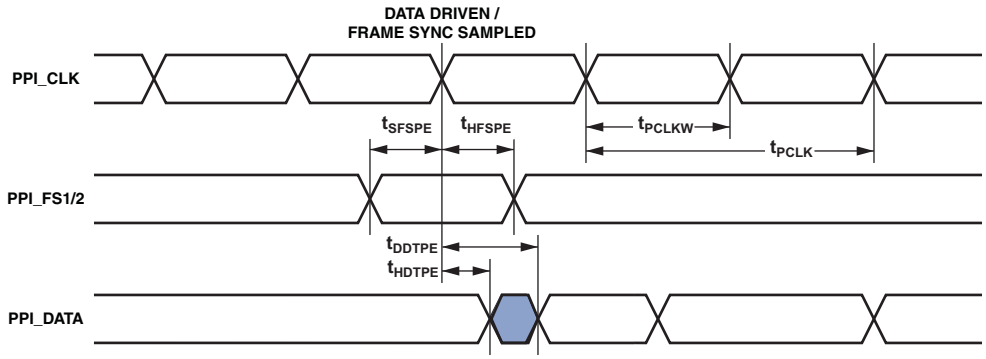

Figure 31. EPPI GP Tx Mode with External Frame Sync Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The UART ports have a maximum baud rate of SCLK/16. There is some latency between the generation of internal UART interrupts and the external data operations. These latencies are negligible at the data transmission rates for the UART. For more information, see the *ADSP-BF54x Blackfin Processor Hardware Reference*.

General-Purpose Port Timing

Table 46 and Figure 40 describe general-purpose port operations.

Table 46. General-Purpose Port Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	t_{SCLK} + 1		ns
Switching Characteristic				
t_{GPOD}	General-Purpose Port Pin Output Delay from CLKOUT Low	–0.3	+6	ns

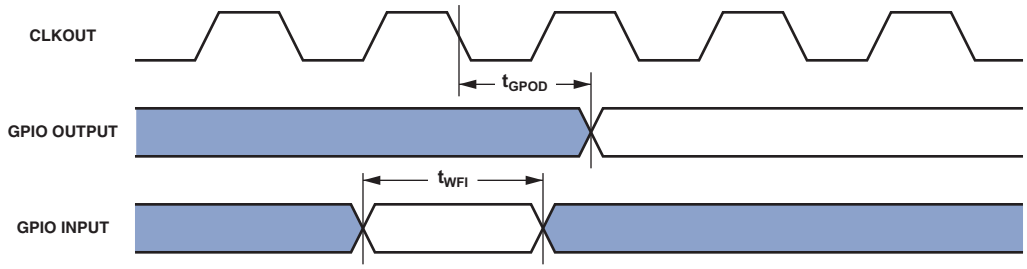

Figure 40. General-Purpose Port Timing

Table 51. SD/SDIO Controller Timing (High Speed Mode)

Parameter		Min	Max	Unit
Timing Requirements				
t_{ISU}	SD_Dx and SD_CMD Input Setup Time	7.2		ns
t_{IH}	SD_Dx and SD_CMD Input Hold Time	2		ns
Switching Characteristics				
f_{PP}	SD_CLK Frequency During Data Transfer Mode[1]	0	40	MHz
t_{WL}	SD_CLK Low Time	9.5		ns
t_{WH}	SD_CLK High Time	9.5		ns
t_{TLH}	SD_CLK Rise Time		3	ns
t_{THL}	SD_CLK Fall Time		3	ns
t_{ODLY}	SD_Dx and SD_CMD Output Delay Time During Data Transfer Mode		2	ns
t_{OH}	SD_Dx and SD_CMD Output Hold Time	2.5		ns

[1] $t_{PP}=1/f_{PP}$.

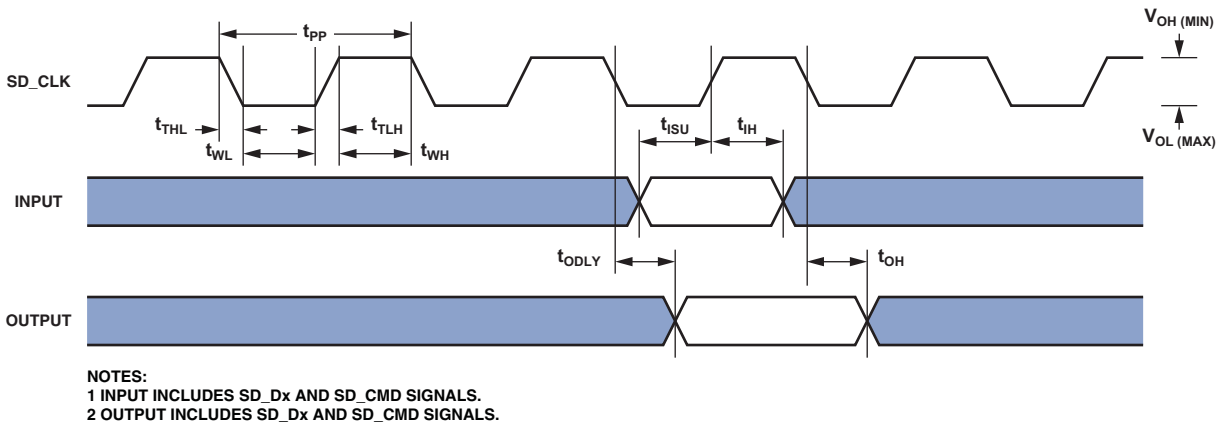

Figure 45. SD/SDIO Controller Timing (High Speed Mode)

MXVR Timing

Table 52 and Table 53 describe the MXVR timing requirements.
Figure 5 illustrates the MOST connection.

Table 52. MXVR Timing—MXI Center Frequency Requirements

Parameter		Fs = 38 kHz	Fs = 44.1 kHz	Fs = 48 kHz	Unit
f_{MXI_256}	MXI Center Frequency (256 Fs)	9.728	11.2896	12.288	MHz
f_{MXI_384}	MXI Center Frequency (384 Fs)	14.592	16.9344	18.432	MHz
f_{MXI_512}	MXI Center Frequency (512 Fs)	19.456	22.5792	24.576	MHz
f_{MXI_1024}	MXI Center Frequency (1024 Fs)	38.912	45.1584	49.152	MHz

Table 53. MXVR Timing— MXI Clock Requirements

Parameter		Min	Max	Unit
Timing Requirements				
FS_{MXI}	MXI Clock Frequency Stability	–50	+50	ppm
FT_{MXI}	MXI Frequency Tolerance Over Temperature	–300	+300	ppm
DC_{MXI}	MXI Clock Duty Cycle	+40	+60	%

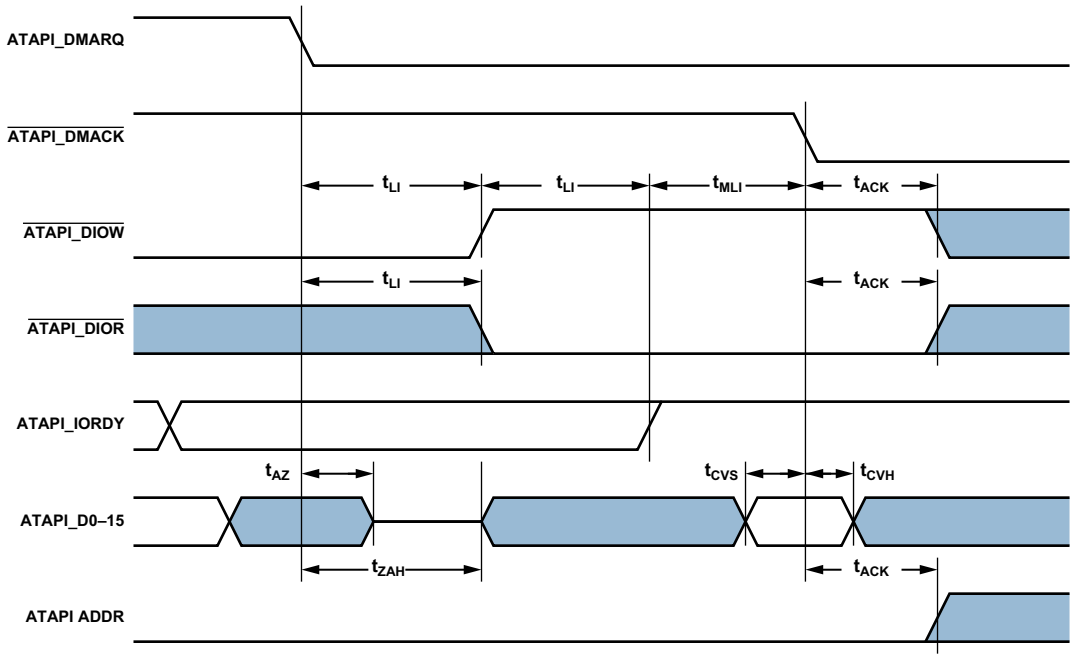

Figure 55. Device Terminating an Ultra DMA Data-In Burst

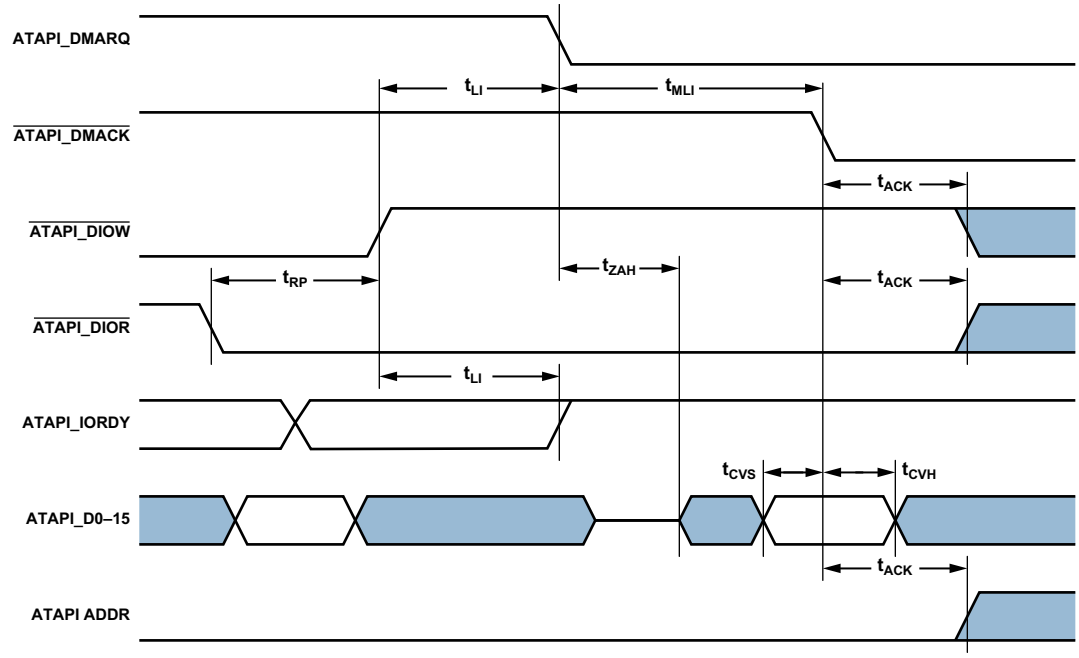

Figure 56. Host Terminating an Ultra DMA Data-In Burst

TYPICAL RISE AND FALL TIMES

Figure 75 through Figure 86 on Page 93 show how output rise time varies with capacitance. The delay and hold specifications given should be derated by a factor derived from these figures. The graphs in these figures may not be linear outside the ranges shown.

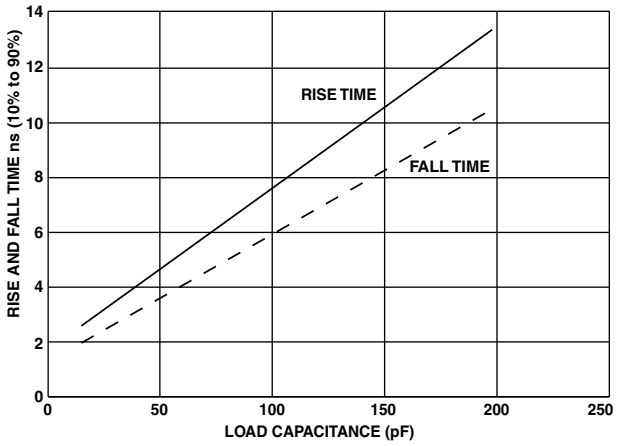

Figure 75. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 2.25 V

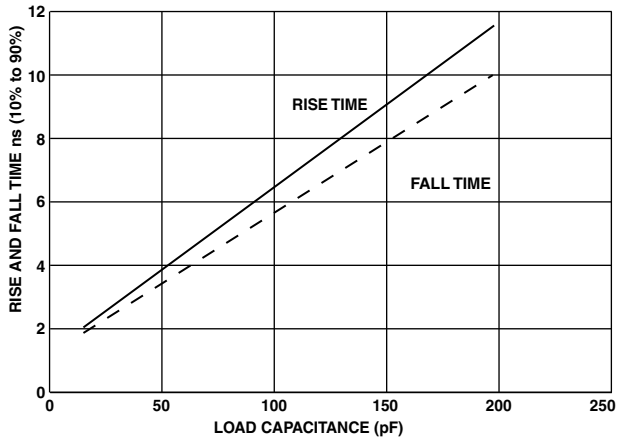

Figure 76. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver A at V_{DDEXT} = 3.65 V

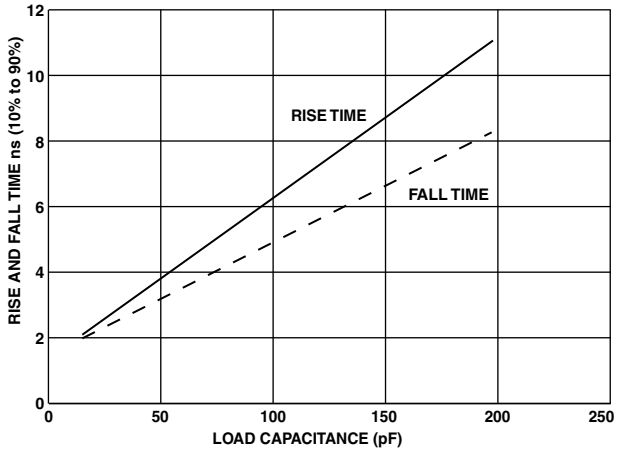

Figure 77. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 2.25 V

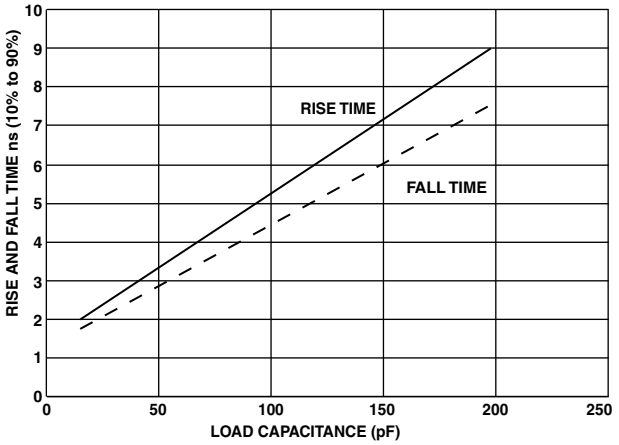

Figure 78. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver B at V_{DDEXT} = 3.65 V

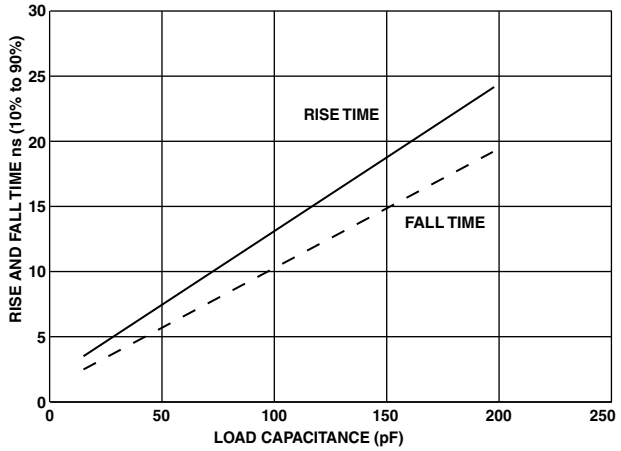

Figure 79. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 2.25 V

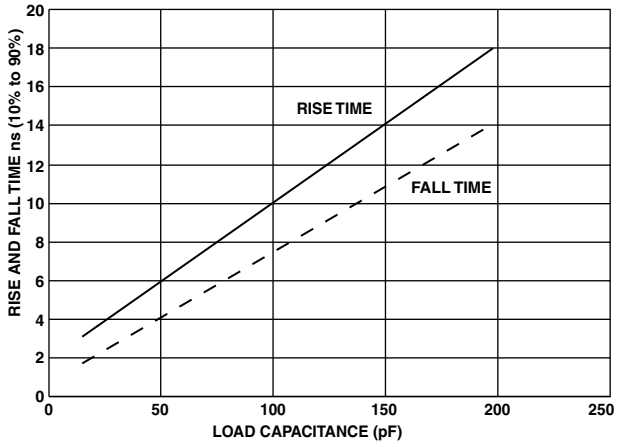

Figure 80. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver C at V_{DDEXT} = 3.65 V

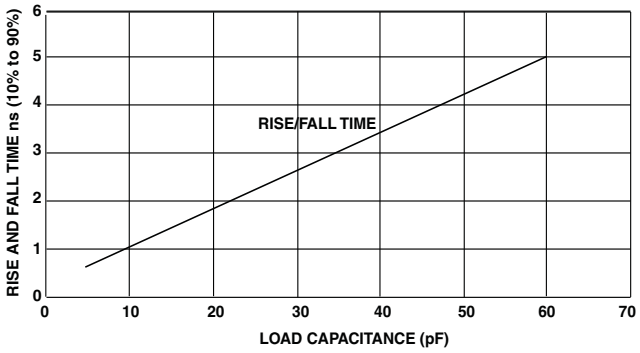

Figure 81. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D DDR SDRAM at V_{DDDDR} = 2.5 V

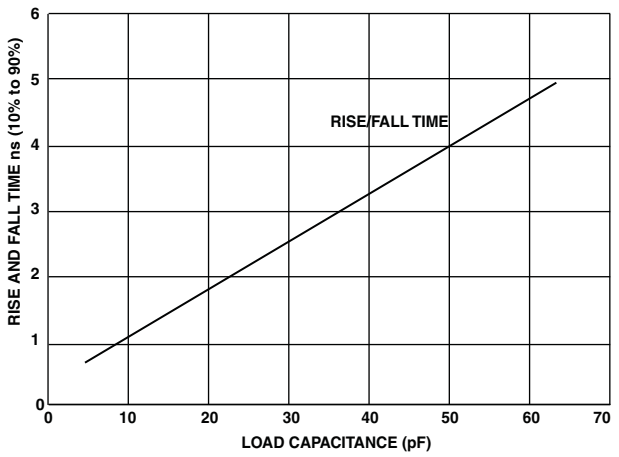

Figure 82. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D DDR SDRAM at V_{DDDDR} = 2.7 V

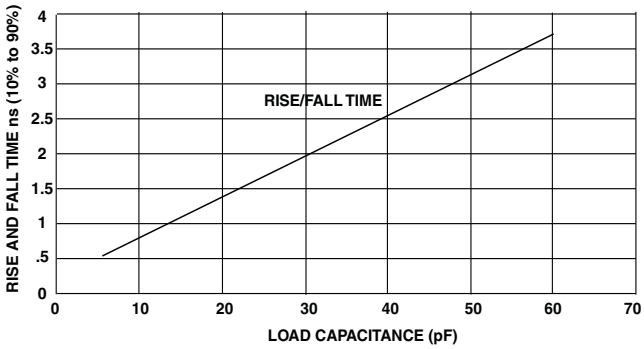

Figure 83. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D Mobile DDR SDRAM at V_{DDDDR} = 1.8 V

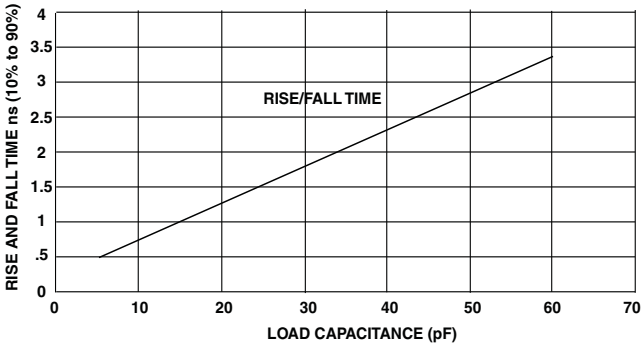

Figure 84. Typical Rise and Fall Times (10% to 90%) vs. Load Capacitance for Driver D Mobile DDR SDRAM at V_{DDDDR} = 1.95 V

OUTLINE DIMENSIONS

Dimensions for the 17 mm × 17 mm CSP_BGA package in Figure 88 are shown in millimeters.

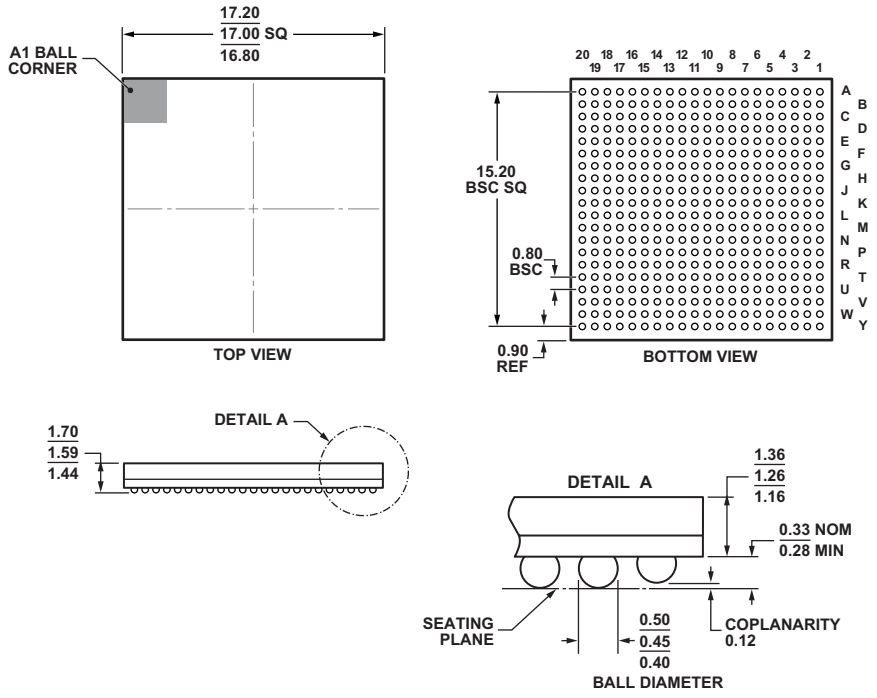

Figure 88. 400-Ball, 17 mm × 17 mm CSP_BGA (Chip Scale Package Ball Grid Array) (BC-400-1)

SURFACE-MOUNT DESIGN

Table 67 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Table 67. BGA Data for Use with Surface-Mount Design

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
400-Ball CSP_BGA (Chip Scale Package Ball Grid Array) BC-400-1	Solder Mask Defined	0.40 mm Diameter	0.50 mm Diameter